16-/14-/12-Bit Dual Rail-to-Rail DACs with I²C Interface

FEATURES

- **Smallest Pin-Compatible Dual DACs:**
  LTC2607: 16 Bits
  LTC2617: 14 Bits
  LTC2627: 12 Bits
- **Guaranteed Monotonic Over Temperature**
- **27 Selectable Addresses**
- 400kHz I²C Interface
- Wide 2.7V to 5.5V Supply Range
- Low Power Operation: 260µA per DAC at 3V
- Power Down to 1µA, Max
- High Rail-to-Rail Output Drive (±15mA, Min)
- Ultralow Crosstalk (30µV)
- Double-Buffered Data Latches
- Asynchronous DAC Update Pin
- LTC2607/LTC2617/LTC2627: Power-On Reset to Zero Scale
- LTC2607-1/LTC2617-1/LTC2627-1: Power-On Reset to Mid-Scale
- Tiny (3mm × 4mm) 12-Lead DFN Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

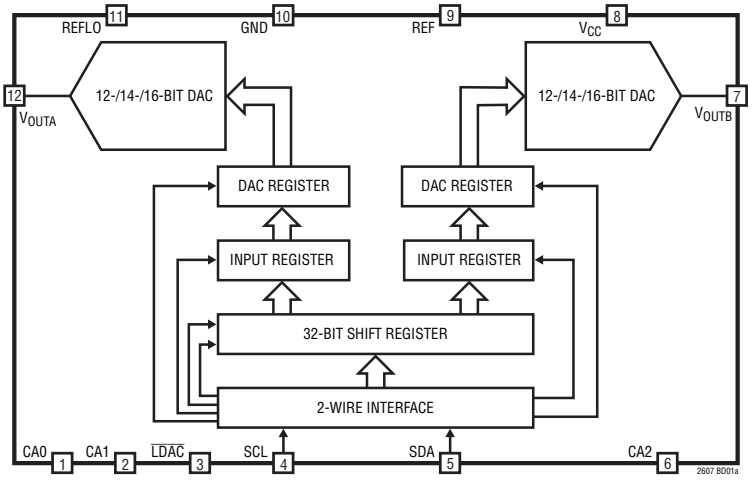
The LTC®2607/LTC2617/LTC2627 are dual 16-, 14- and 12-bit, 2.7V to 5.5V rail-to-rail voltage output DACs in a 12-lead DFN package. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish new board-density benchmarks for 16- and 14-bit DACs and advance performance standards for output drive and load regulation in single-supply, voltage-output DACs.

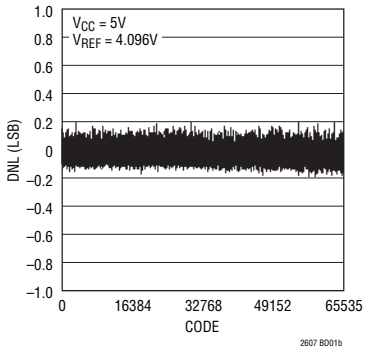
The parts use a 2-wire, I²C compatible serial interface. The LTC2607/LTC2617/LTC2627 operate in both the standard mode (clock rate of 100kHz) and the fast mode (clock rate of 400kHz). An asynchronous DAC update pin ($\overline{LDAC}$) is also included.

The LTC2607/LTC2617/LTC2627 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale; and after power-up, they stay at zero scale until a valid write and update take place. The power-on reset circuit resets the LTC2607-1/LTC2617-1/LTC2627-1 to mid-scale. The voltage outputs stay at mid-scale until a valid write and update takes place.

BLOCK DIAGRAM



Differential Nonlinearity (LTC2607)

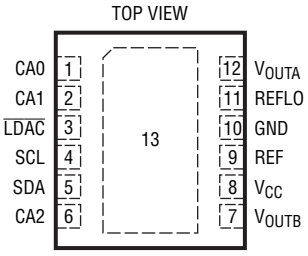


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Any Pin to GND ..... –0.3V to 6V
Any Pin to V_{CC} ..... –6V to 0.3V
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)..... 300°C
Operating Temperature Range:
LTC2607C/LTC2617C/LTC2627C
LTC2607C-1/LTC2617C-1/LTC2627C-1 .... 0°C to 70°C
LTC2607I/LTC2617I/LTC2627I
LTC2607I-1/LTC2617I-1/LTC2627I-1 .... –40°C to 85°C

PIN CONFIGURATION



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2607CDE#PBF	LTC2607CDE#TRPBF	2607	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2607IDE#PBF	LTC2607IDE#TRPBF	2607	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2607CDE-1#PBF	LTC2607CDE-1#TRPBF	26071	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2607IDE-1#PBF	LTC2607IDE-1#TRPBF	26071	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2617CDE#PBF	LTC2617CDE#TRPBF	2617	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2617IDE#PBF	LTC2617IDE#TRPBF	2617	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2617CDE-1#PBF	LTC2617CDE-1#TRPBF	26171	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2617IDE-1#PBF	LTC2617IDE-1#TRPBF	26171	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2627CDE#PBF	LTC2627CDE#TRPBF	2627	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2627IDE#PBF	LTC2627IDE#TRPBF	2627	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2627CDE-1#PBF	LTC2627CDE-1#TRPBF	26271	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2627IDE-1#PBF	LTC2627IDE-1#TRPBF	26271	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), REFLO = 0V, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2627/LTC2627-1 MIN	LTC2627/LTC2627-1 TYP	LTC2627/LTC2627-1 MAX	LTC2617/LTC2617-1 MIN	LTC2617/LTC2617-1 TYP	LTC2617/LTC2617-1 MAX	LTC2607/LTC2607-1 MIN	LTC2607/LTC2607-1 TYP	LTC2607/LTC2607-1 MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	(Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	(Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	(Note 2)	●		±1.5	±4		±5	±16		±19	±64	LSB
	Load Regulation	V_{REF} = V_{CC} = 5V, Mid-Scale											
		I_{OUT} = 0mA to 15mA Sourcing	●		0.02	0.125		0.1	0.5		0.35	2	LSB/mA
		I_{OUT} = 0mA to 15mA Sinking	●		0.03	0.125		0.1	0.5		0.42	2	LSB/mA
		V_{REF} = V_{CC} = 2.7V, Mid-Scale											
		I_{OUT} = 0mA to 7.5mA Sourcing	●		0.04	0.25		0.2	1		0.7	4	LSB/mA
		I_{OUT} = 0mA to 7.5mA Sinking	●		0.05	0.25		0.2	1		0.8	4	LSB/mA
ZSE	Zero-Scale Error	Code = 0	●		1	9		1	9		1	9	mV
V_{OS}	Offset Error	(Note 6)	●		±1	±9		±1	±9		±1	±9	mV
	V_{OS} Temperature Coefficient				±7			±7			±7		µV/°C
GE	Gain Error		●		±0.15	±0.7		±0.15	±0.7		±0.15	±0.7	%FSR
	Gain Temperature Coefficient				±4			±4			±4		ppm/°C

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), REFLO = 0V, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSR	Power Supply Rejection	V_{CC} ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{REF} = V_{CC} = 5V, Mid-Scale;					
		–15mA ≤ I_{OUT} ≤ 15mA	●		0.032	0.15	Ω
		V_{REF} = V_{CC} = 2.7V, Mid-Scale;					
		–7.5mA ≤ I_{OUT} ≤ 7.5mA	●		0.035	0.15	Ω
	DC Crosstalk (Note 4)	Due to Full Scale Output Change (Note 5)			±4		µV
		Due to Load Current Change			±3		µV/mA
		Due to Powering Down (Per Channel)			±30		µV
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.5V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	15	36	60	mA
		Code: Full Scale; Forcing Output to GND	●	15	37	60	mA
		V_{CC} = 2.7V, V_{REF} = 2.7V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	7.5	22	50	mA
		Code: Full Scale; Forcing Output to GND	●	7.5	30	50	mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	44	64	80	kΩ
	Capacitance				30		pF
I_{REF}	Reference Current, Power Down Mode	DAC Powered Down	●		0.001	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), REFLO = 0V, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) DAC Powered Down (Note 3) V_{CC} = 5V DAC Powered Down (Note 3) V_{CC} = 3V	● ● ● ●		0.66 0.52 0.4 0.10	1.3 1 1 1	mA mA µA µA
Digital I/O (Note 11)							
V_{IL}	Low Level Input Voltage (SDA and SCL)		●			$0.3V_{CC}$	V
V_{IH}	High Level Input Voltage (SDA and SCL)		●	$0.7V_{CC}$			V
$V_{IL(\overline{LDAC})}$	Low Level Input Voltage ($\overline{LDAC}$)	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 5.5V	● ●			0.8 0.6	V V
$V_{IH(\overline{LDAC})}$	High Level Input Voltage ($\overline{LDAC}$)	V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
$V_{IL(CAn)}$	Low Level Input Voltage on CA*n* (*n* = 0, 1, 2)	See Test Circuit 1	●			$0.15V_{CC}$	V
$V_{IH(CAn)}$	High Level Input Voltage on CAn (*n* = 0, 1, 2)	See Test Circuit 1	●	$0.85V_{CC}$			V
R_{INH}	Resistance from CA*n* (*n* = 0, 1, 2) to V_{CC} to Set CA*n* = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA*n* (*n* = 0, 1, 2) to GND to Set CA*n* = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA*n* (*n* = 0, 1, 2) to V_{CC} or GND to Set CA*n* = Float	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	$V_O = V_{IH(MIN)}$ to $V_O = V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 9)	●	$20 + 0.1C_B$		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	$0.1V_{CC} \le V_{IN} \le 0.9V_{CC}$	●			1	µA
C_{IN}	I/O Pin Capacitance	Note 12	●			10	pF
C_B	Capacitive Load for Each Bus Line		●			400	pF
C_{CAX}	External Capacitive Load on Address Pins CAn (*n* = 0, 1, 2)		●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), REFLO = 0V, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC2627/LTC2627-1			LTC2617/LTC2617-1			LTC2607/LTC2607-1			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
AC Performance												
t_S	Settling Time (Note 7)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		7			7 9			7 9 10		µs µs µs
	Settling Time for 1LSB Step (Note 8)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		2.7			2.7 4.8			2.7 4.8 5.2		µs µs µs
	Voltage Output Slew Rate			0.8			0.8			0.8		V/µs
	Capacitive Load Driving			1000			1000			1000		pF
	Glitch Impulse	At Mid-Scale Transition		12			12			12		nV • s
	Multiplying Bandwidth			180			180			180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz		120 100			120 100			120 100		nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz		15			15			15		μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1) (Notes 10, 11)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 2.7V to 5.5V							
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time of Both SDA and SCL Signals	(Note 9)	●	20 + 0.1C_B		300	ns
t_f	Fall Time of Both SDA and SCL Signals	(Note 9)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs
t_1	Falling Edge of 9th Clock of the 3rd Input Byte to $\overline{LDAC}$ High or Low Transition		●	400			ns
t_2	$\overline{LDAC}$ Low Pulse Width		●	20			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Linearity and monotonicity are defined from code k_L to code 2N – 1, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256 and linearity is defined from code 256 to code 65,535.

Note 3: SDA, SCL and $\overline{LDAC}$ at 0V or V_{CC}, CA0, CA1 and CA2 Floating.

Note 4: DC crosstalk is measured with V_{CC} = 5V and V_{REF} = 4.096V, with the measured DAC at mid-scale, unless otherwise noted.

Note 5: R_L = 2kΩ to GND or V_{CC}.

Note 6: Inferred from measurement at code k_L (Note 2) and at full scale.

Note 7: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2k in parallel with 200pF to GND.

Note 8: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped ±1LSB between half scale and half scale – 1. Load is 2k in parallel with 200pF to GND.

Note 9: C_B = capacitance of one bus line in pF.

Note 10: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

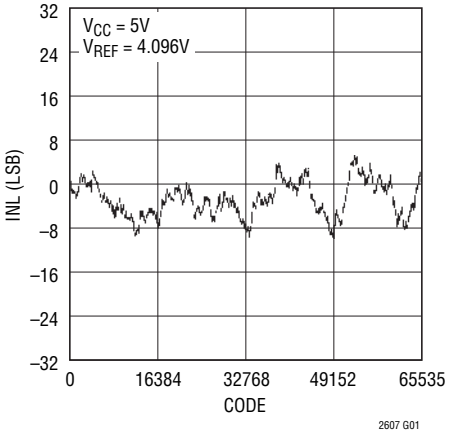
Note 11: These specifications apply to LTC2607/LTC2607-1, LTC2617/LTC2617-1, LTC2627/LTC2627-1.

Note 12: Guaranteed by design and not production tested.

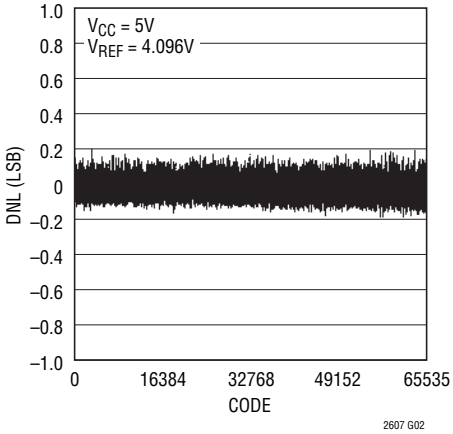
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2607

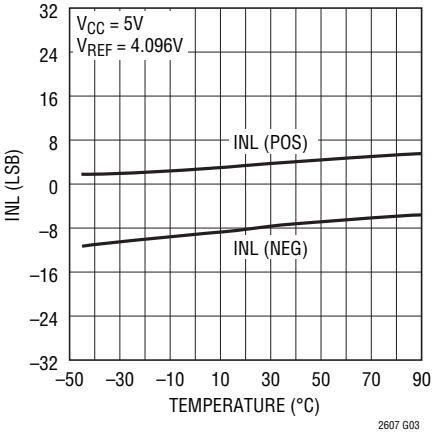
Integral Nonlinearity (INL)



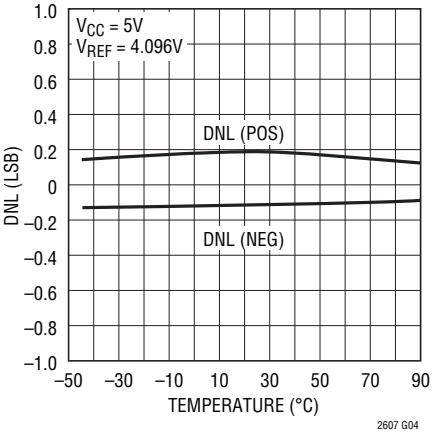
Differential Nonlinearity (DNL)



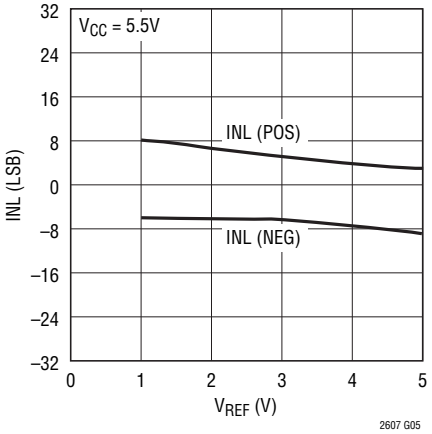
INL vs Temperature



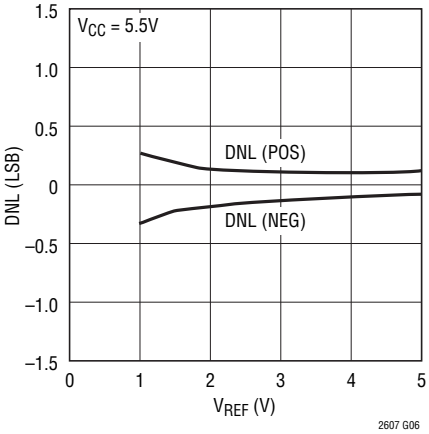
DNL vs Temperature



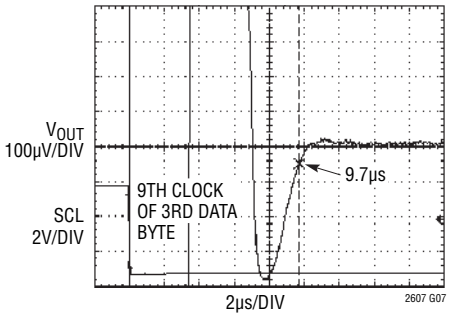
INL vs V_{REF}



DNL vs V_{REF}

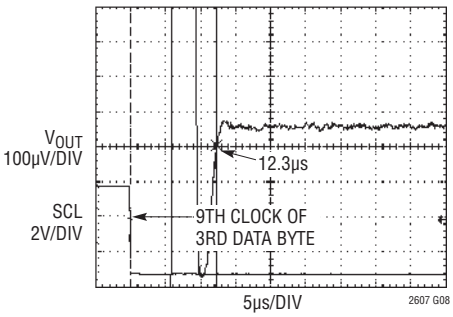


Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

Settling of Full-Scale Step

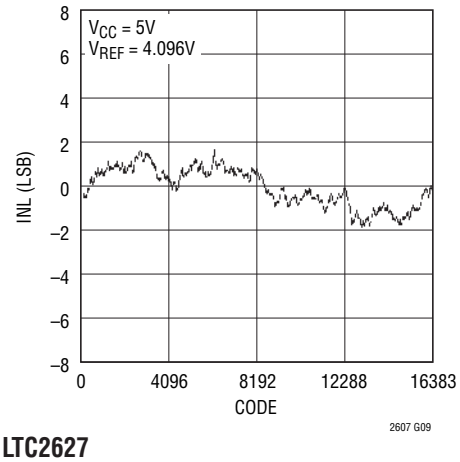


SETTLING TO ±1LSB
V_{CC} = 5V, V_{REF} = 4.096V
CODE 512 TO 65535 STEP
AVERAGE OF 2048 EVENTS

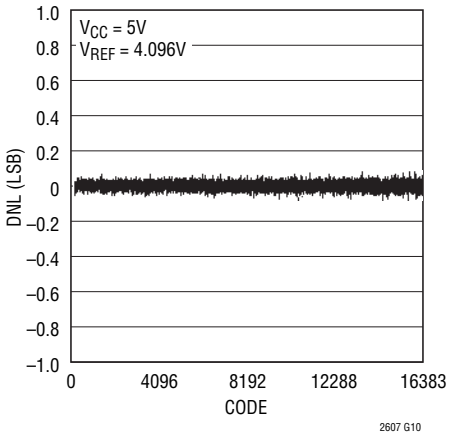
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2617

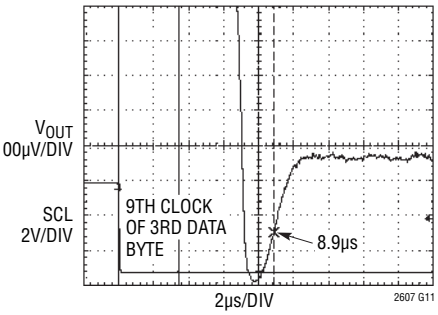
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



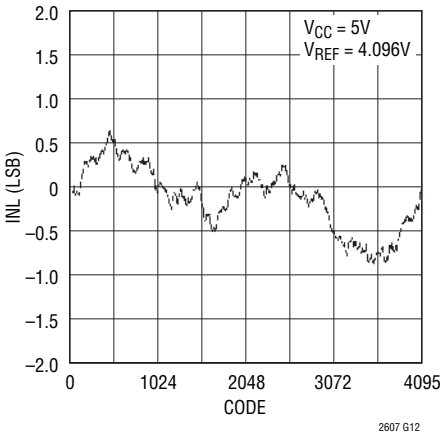
Settling to ±1LSB



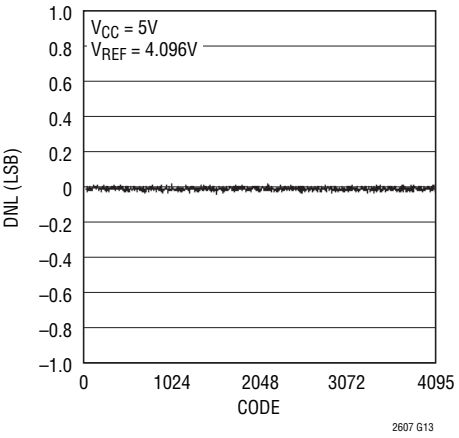
VCC = 5V, VREF = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
RL = 2k, CL = 200pF
AVERAGE OF 2048 EVENTS

LTC2627

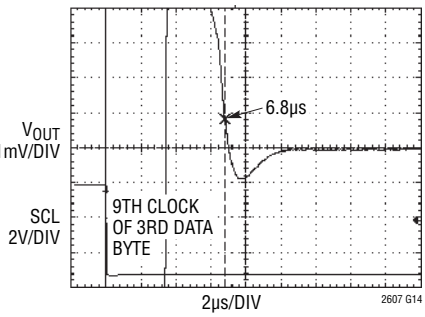
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



Settling to ±1LSB

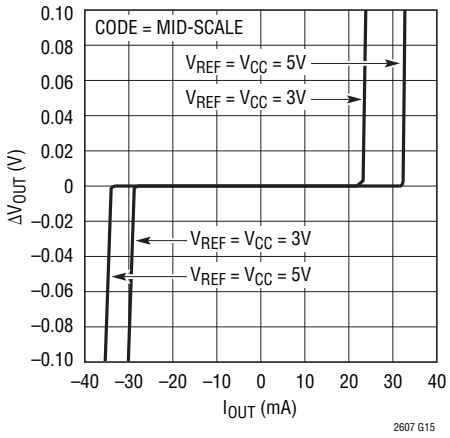


VCC = 5V, VREF = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
RL = 2k, CL = 200pF
AVERAGE OF 2048 EVENTS

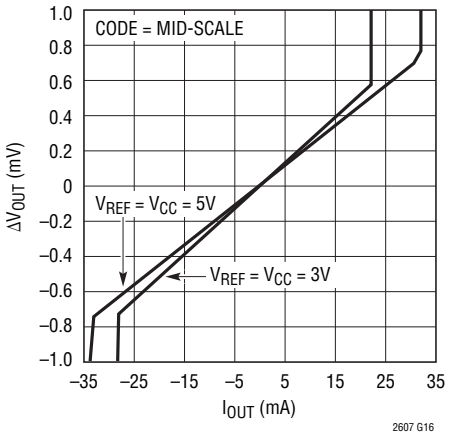
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2607/LTC2617/LTC2627

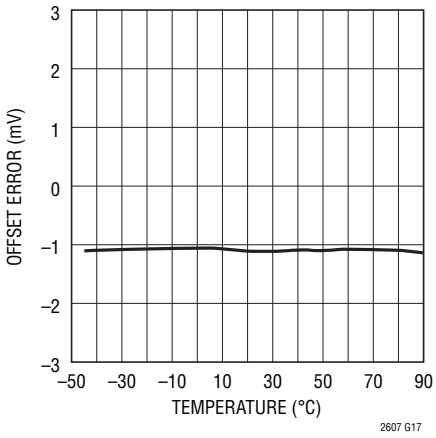
Current Limiting



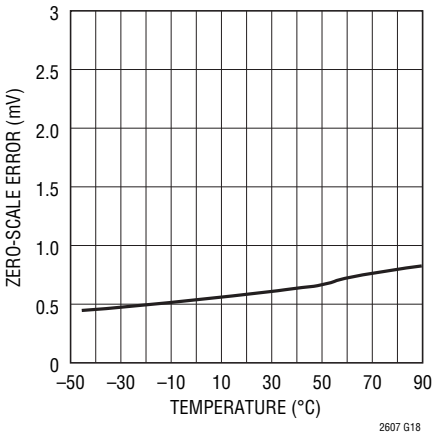
Load Regulation



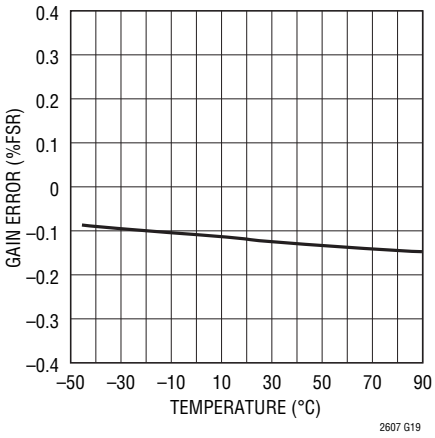
Offset Error vs Temperature



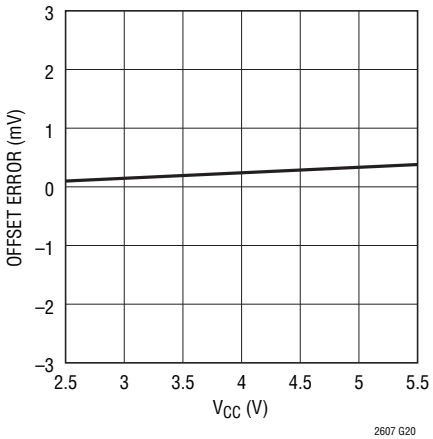
Zero-Scale Error vs Temperature



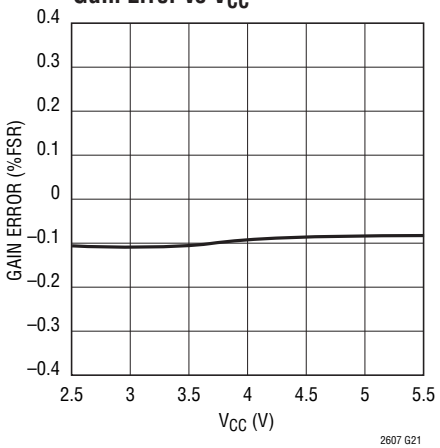
Gain Error vs Temperature



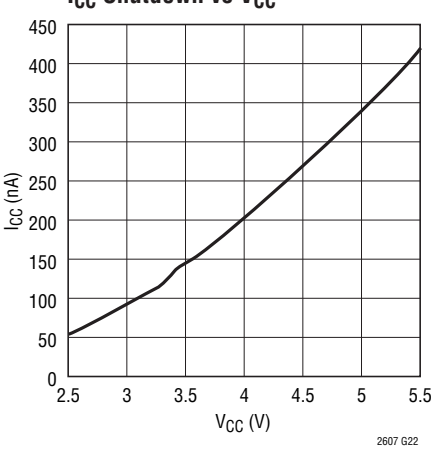
Offset Error vs V_{CC}



Gain Error vs V_{CC}



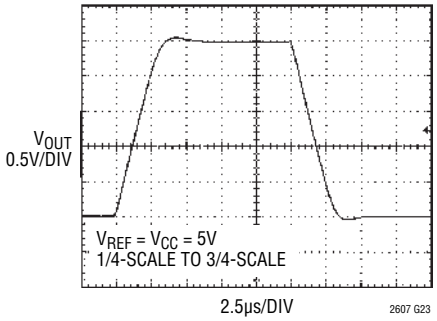
I_{CC} Shutdown vs V_{CC}



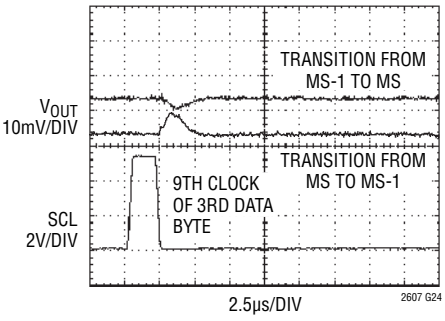
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2607/LTC2617/LTC2627

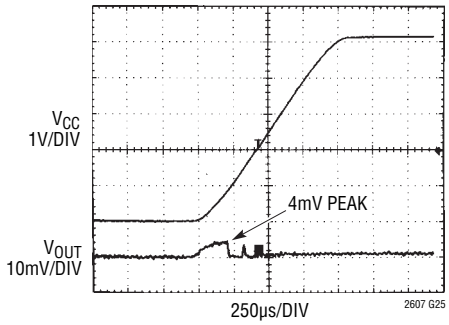
Large-Signal Response



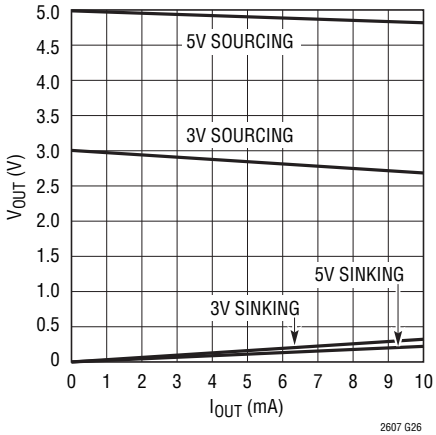
Mid-Scale Glitch Impulse



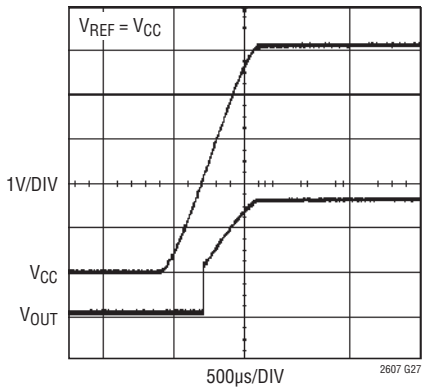
Power-On Reset to Zeroscale



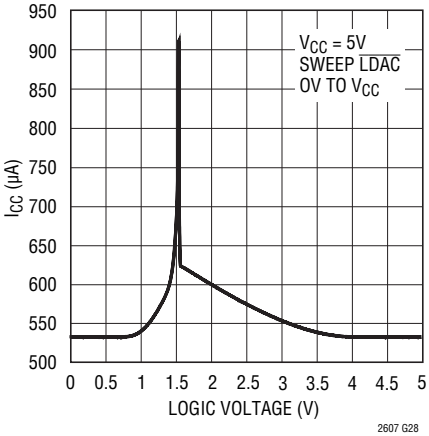
Headroom at Rails vs Output Current



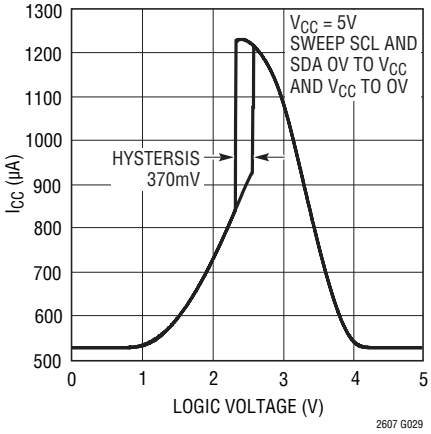
Power-On Reset to Midscale



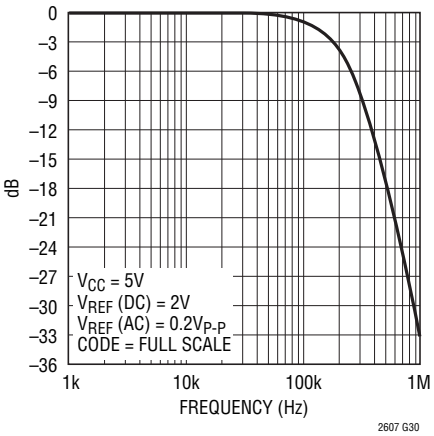
Supply Current vs Logic Voltage



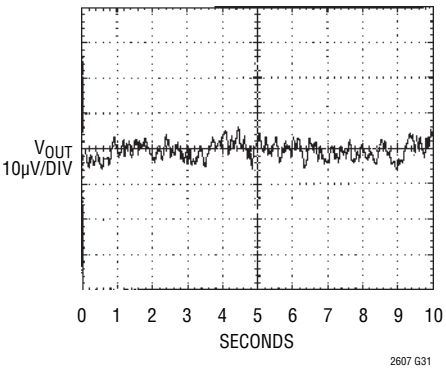
Supply Current vs Logic Voltage



Multiplying Bandwidth



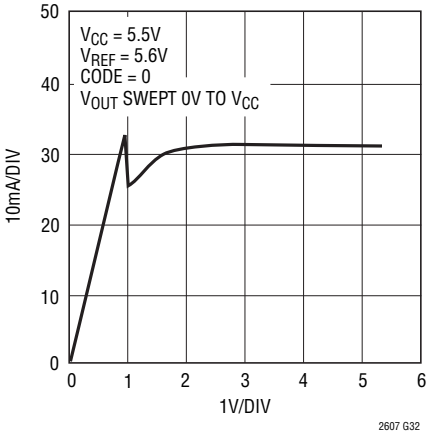
Output Voltage Noise, 0.1Hz to 10Hz



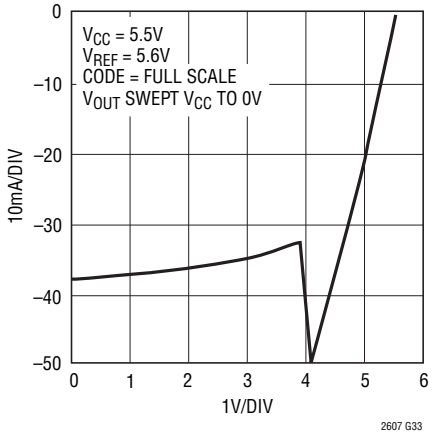
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2607/LTC2617/LTC2627

Short-Circuit Output Current vs V_{OUT} (Sinking)



Short-Circuit Output Current vs V_{OUT} (Sourcing)



PIN FUNCTIONS

CA0 (Pin 1): Chip Address Bit 0. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 1).

CA1 (Pin 2): Chip Address Bit 1. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 1).

$\overline{\text{LDAC}}$ (Pin 3): Asynchronous DAC Update. A falling edge of this input after four bytes have been written into the part immediately updates the DAC register with the contents of the input register. A low on this input without a complete 32-bit (four bytes including the slave address) data write transfer to the part wakes up sleeping DACs without updating the DAC output. Software power-down is disabled when $\overline{\text{LDAC}}$ is low. $\overline{\text{LDAC}}$ is disabled when tied high.

SCL (Pin 4): Serial Clock Input Pin. Data is shifted into the SDA pin at the rising edges of the clock. This high impedance pin requires a pull-up resistor or current source to V_{CC}.

SDA (Pin 5): Serial Data Bidirectional Pin. Data is shifted into the SDA pin and acknowledged by the SDA pin. This pin is high impedance while data is shifted in and an open-drain N-channel output during acknowledgment. Requires a pull-up resistor or current source to V_{CC}.

CA2 (Pin 6): Chip Address Bit 2. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 1).

V_{OUTB} (Pin 7): DAC Analog Voltage Output. The output range is V_{REFLO} to V_{REF}.

V_{CC} (Pin 8): Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$.

REF (Pin 9): Reference Voltage Input. The input range is $V_{REFLO} \le V_{REF} \le V_{CC}$.

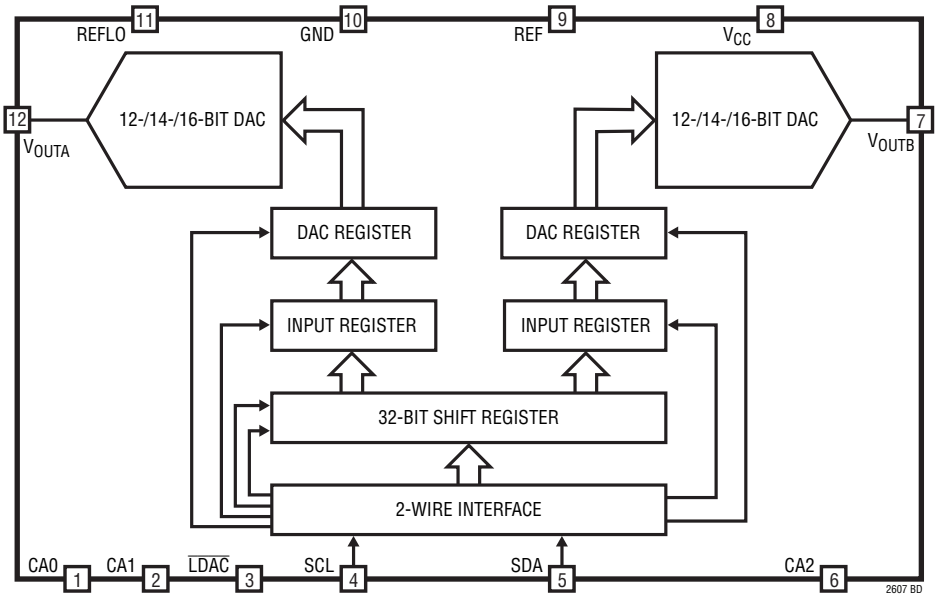
GND (Pin 10): Analog Ground.

REFLO (Pin 11): Reference Low. The voltage at this pin sets the zero scale (ZS) voltage of all DACs. The V_{REFLO} pin can be used at voltages up to 1V for V_{CC} = 5V, or 100mV for V_{CC} = 3V.

V_{OUTA} (Pin 12): DAC Analog Voltage Output. The output range is V_{REFLO} to V_{REF}.

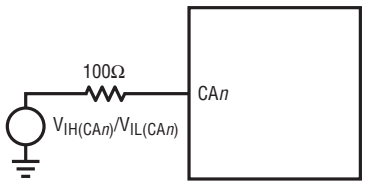
Exposed Pad (Pin 13): Ground. Must be soldered to PCB ground.

BLOCK DIAGRAM

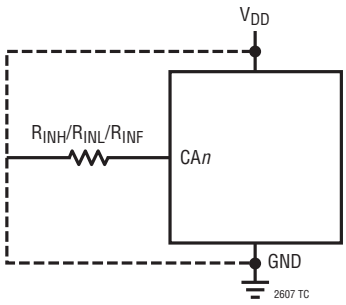


TEST CIRCUITS

Test Circuit 1



Test Circuit 2



TIMING DIAGRAMS

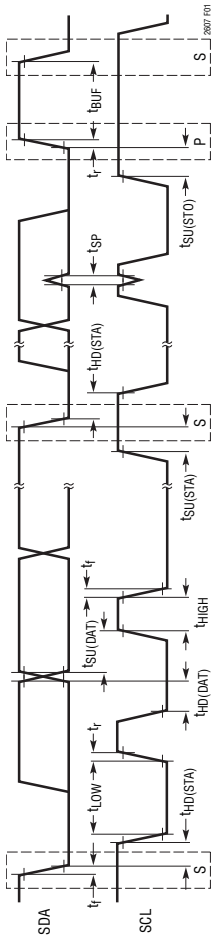


Figure 1

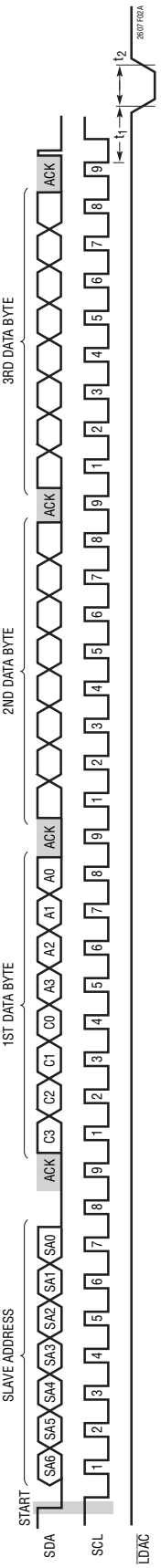


Figure 2a

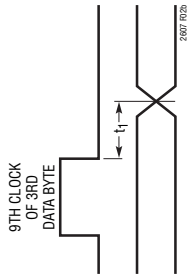


Figure 2b

OPERATION

Power-On Reset

The LTC2607/LTC2617/LTC2627 clear the outputs to zero scale when power is first applied, making system initialization consistent and repeatable. The LTC2607-1/LTC2617-1/LTC2627-1 set the voltage outputs to midscale when power is first applied.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2607/LTC2617/LTC2627 contain circuitry to reduce the power-on glitch; furthermore, the glitch amplitude can be made arbitrarily small by reducing the ramp rate of the power supply. For example, if the power supply is ramped to 5V in 1ms, the analog outputs rise less than 10mV above ground (typ) during power-on. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pin 9) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 8) is in transition.

Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)\left(V_{REF} - V_{REFLO}\right) + V_{REFLO}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is the voltage at REF (Pin 6).

Serial Digital Interface

The LTC2607/LTC2617/LTC2627 communicate with a host using the standard 2-wire I^2C interface. The Timing Diagrams (Figures 1 and 2) show the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The value of these pull-up resistors is dependent on the power supply and can be obtained from the I^2C specifications. For an I^2C bus operating in the fast mode, an active pull-up will be necessary if the bus capacitance is greater than 200pF. The V_{CC} power should not be removed from the LTC2607/LTC2617/LTC2627 when the I^2C bus is active to avoid loading the I^2C bus lines through the internal ESD protection diodes.

The LTC2607/LTC2617/LTC2627 are receive-only (slave) devices. The master can write to the LTC2607/LTC2617/LTC2627. The LTC2607/LTC2617/LTC2627 do not respond to a read from the master.

The START (S) and STOP (P) Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high.

When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave-receiver must pull down the SDA bus line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse. The LTC2607/LTC2617/LTC2627 respond to a write by a master in this manner. The LTC2607/LTC2617/LTC2627 do not acknowledge a read (retains SDA HIGH during the period of the Acknowledge clock pulse).

Chip Address

The state of CA0, CA1 and CA2 decides the slave address of the part. The pins CA0, CA1 and CA2 can be each set to any one of three states: V_{CC}, GND or float. This results

OPERATION

in 27 selectable addresses for the part. The slave address assignments are shown in Table 1.

Table 1. Slave Address Map

CA2	CA1	CA0	SA6	SA5	SA4	SA3	SA2	SA1	SA0
GND	GND	GND	0	0	1	0	0	0	0
GND	GND	FLOAT	0	0	1	0	0	0	1
GND	GND	V_{CC}	0	0	1	0	0	1	0
GND	FLOAT	GND	0	0	1	0	0	1	1
GND	FLOAT	FLOAT	0	1	0	0	0	0	0
GND	FLOAT	V_{CC}	0	1	0	0	0	0	1
GND	V_{CC}	GND	0	1	0	0	0	1	0
GND	V_{CC}	FLOAT	0	1	0	0	0	1	1
GND	V_{CC}	V_{CC}	0	1	1	0	0	0	0
FLOAT	GND	GND	0	1	1	0	0	0	1
FLOAT	GND	FLOAT	0	1	1	0	0	1	0
FLOAT	GND	V_{CC}	0	1	1	0	0	1	1
FLOAT	FLOAT	GND	1	0	0	0	0	0	0
FLOAT	FLOAT	FLOAT	1	0	0	0	0	0	1
FLOAT	FLOAT	V_{CC}	1	0	0	0	0	1	0
FLOAT	V_{CC}	GND	1	0	0	0	0	1	1
FLOAT	V_{CC}	FLOAT	1	0	1	0	0	0	0
FLOAT	V_{CC}	V_{CC}	1	0	1	0	0	0	1
V_{CC}	GND	GND	1	0	1	0	0	1	0
V_{CC}	GND	FLOAT	1	0	1	0	0	1	1
V_{CC}	GND	V_{CC}	1	1	0	0	0	0	0
V_{CC}	FLOAT	GND	1	1	0	0	0	0	1
V_{CC}	FLOAT	FLOAT	1	1	0	0	0	1	0
V_{CC}	FLOAT	V_{CC}	1	1	0	0	0	1	1
V_{CC}	V_{CC}	GND	1	1	1	0	0	0	0
V_{CC}	V_{CC}	FLOAT	1	1	1	0	0	0	1
V_{CC}	V_{CC}	V_{CC}	1	1	1	0	0	1	0
GLOBAL ADDRESS			1	1	1	0	0	1	1

In addition to the address selected by the address pins, the parts also respond to a global address. This address allows a common write to all LTC2607, LTC2617 and LTC2627 parts to be accomplished with one 3-byte write transaction on the I^2C bus. The global address is a 7-bit on-chip hardwired address and is not selectable by CA0, CA1 and CA2.

The addresses corresponding to the states of CA0, CA1 and CA2 and the global address are shown in Table 1. The maximum capacitive load allowed on the address pins (CA0, CA1 and CA2) is 10pF, as these pins are driven during address detection to determine if they are floating.

Write Word Protocol

The master initiates communication with the LTC2607/LTC2617/LTC2627 with a START condition and a 7-bit slave address followed by the Write bit (W) = 0. The LTC2607/LTC2617/LTC2627 acknowledges by pulling the SDA pin low at the 9th clock if the 7-bit slave address matches the address of the parts (set by CA0, CA1 and CA2) or the global address. The master then transmits three bytes of data. The LTC2607/LTC2617/LTC2627 acknowledges each byte of data by pulling the SDA line low at the 9th clock of each data byte transmission. After receiving three complete bytes of data, the LTC2607/LTC2617/LTC2627 executes the command specified in the 24-bit input word.

If more than three data bytes are transmitted after a valid 7-bit slave address, the LTC2607/LTC2617/LTC2627 do not acknowledge the extra bytes of data (SDA is high during the 9th clock).

The format of the three data bytes is shown in Figure 3. The first byte of the input word consists of the 4-bit command word C3-C0, and 4-bit DAC address A3-A0. The next two bytes consist of the 16-bit data word. The 16-bit data word consists of the 16-, 14- or 12-bit input code, MSB to LSB, followed by 0, 2 or 4 don't care bits (LTC2607, LTC2617 and LTC2627 respectively). A typical LTC2607 write transaction is shown in Figure 4.

The command (C3-C0) and address (A3-A0) assignments are shown in Table 2. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the selected DAC, n. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 16-, 14- or 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

OPERATION

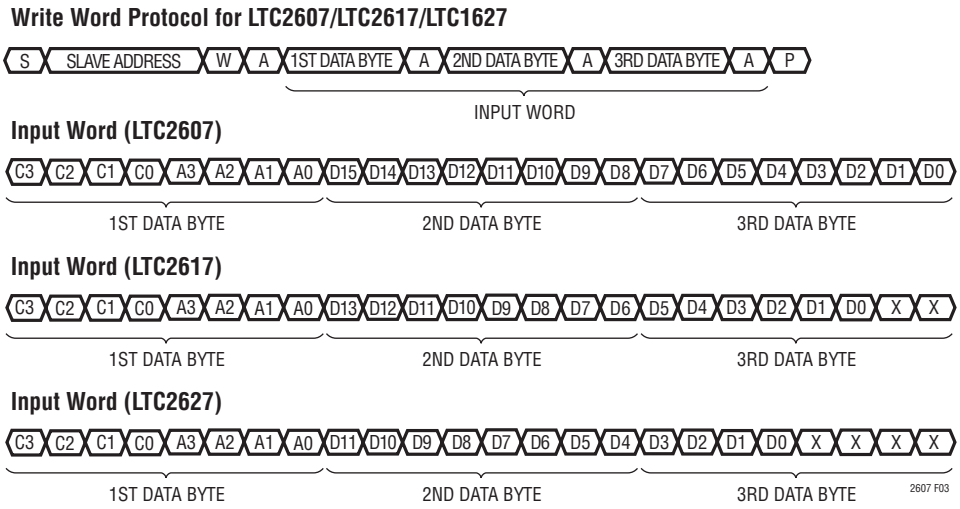


Figure 3

Table 2

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register
0	0	0	1	Update (Power Up) DAC Register
0	0	1	1	Write to and Update (Power Up)
0	1	0	0	Power Down
1	1	1	1	No Operation
ADDRESS*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
1	1	1	1	All DACs

*Command and address codes not shown are reserved and should not be used.

Power-Down Mode

For power-constrained applications, the power-down mode can be used to reduce the supply current whenever one or both of the DAC outputs are not needed. When in power-down, the buffer amplifiers, bias circuits and reference input are disabled and draw essentially zero current. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to V_{REFLO} through 90k resistors. Input-register and DAC-register contents are not disturbed during power-down.

Either or both DAC channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address. The 16-bit data word is ignored. The supply and reference currents are reduced by approximately 50% for each DAC powered down; the effective resistance at REF (Pin 9) rises accordingly, becoming a high-impedance input (typically > 1GΩ) when both DACs are powered down.

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 2 or performing an asychronous update ($\overline{LDAC}$) as described in the next section. The selected DAC is powered up as its voltage output is updated. When a DAC in powered-down state is powered up and updated, normal settling is delayed. If one of the two DACs is in a powered- down state prior to the update command, the power up delay is 5µs. If on the other hand, both DACs are powered down, the main bias generation circuit has been automatically shut down in addition to the DAC amplifiers and reference input and so the power up delay time is

12µs (for V_{CC} = 5V) or 30µs (for V_{CC} = 3V)

Asynchronous DAC Update Using $\overline{LDAC}$

In addition to the update commands shown in Table 2, the $\overline{LDAC}$ pin asynchronously updates the DAC registers with the contents of the input registers. Asynchronous update is disabled when the input word is being clocked into the part.

OPERATION

If a complete input word has been written to the part, a low on the $\overline{LDAC}$ pin causes the DAC registers to be updated with the contents of the input registers.

If the input word is being written to the part, a low going pulse on the $\overline{LDAC}$ pin before the completion of three bytes of data powers up the DACs but does not cause the outputs to be updated. If $\overline{LDAC}$ remains low after a complete input word has been written to the part, then $\overline{LDAC}$ is recognized, the command specified in the 24-bit word just transferred is executed and the DAC outputs updated.

The DACs are powered up when $\overline{LDAC}$ is taken low, independent of any activity on the I^2C bus.

If $\overline{LDAC}$ is low at the falling edge of the 9th clock of the 3rd byte of data, it inhibits any software power-down command that was specified in the input word. $\overline{LDAC}$ is disabled when tied high.

Voltage Output

Both of the two rail-to-rail amplifiers have guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifiers' ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.035Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 30Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 30Ω • 1mA = 30mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation performance is achieved in part by separating the signal and power grounds as REFLO and GND pins, respectively.

The PC Board should have separate areas for the analog and digital sections of the circuit. This keeps the digital signals away from the sensitive analog signals and facilitates the use of separate digital and analog ground planes that have minimal interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin functions as a return path for power supply currents in the device and should be connected to analog ground. Resistance from the GND pin to the analog power supply return should be as low as possible. Resistance here will add directly to the channel resistance of the output device when sinking load current. When a zero scale DAC output voltage of zero is required, the REFLO pin should be connected to system star ground. Any shared trace resistance between REFLO and GND pins is undesirable since it adds to the effective DC output impedance (typically 0.035Ω) of the part.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the device cannot go below ground, it may limit for the lowest codes as shown in Figure 5b. Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 5c. No full-scale limiting will occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

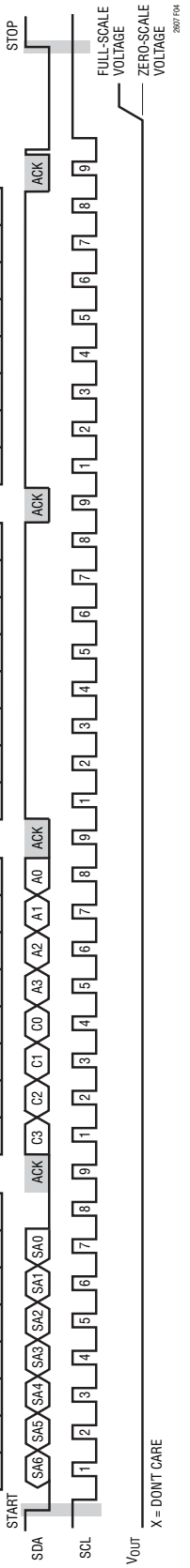


Figure 4. Typical LTC2607 Input Waveform—Programming DAC Output for Full Scale

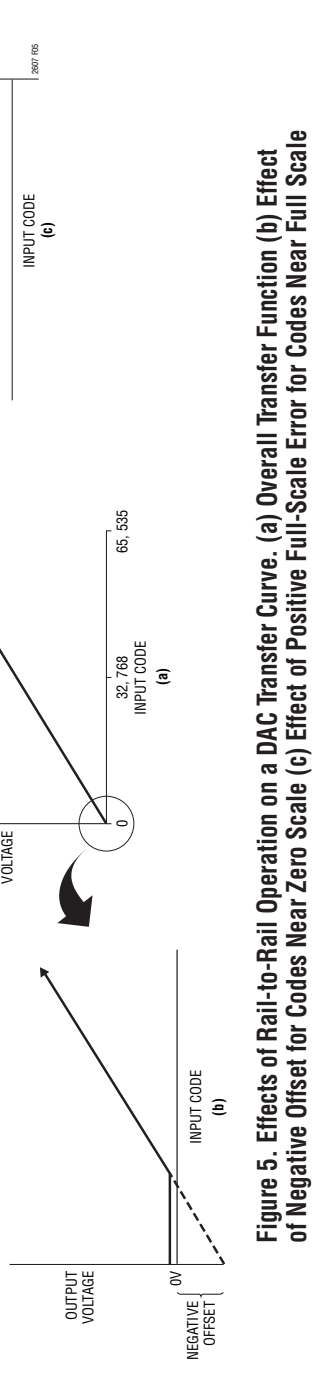
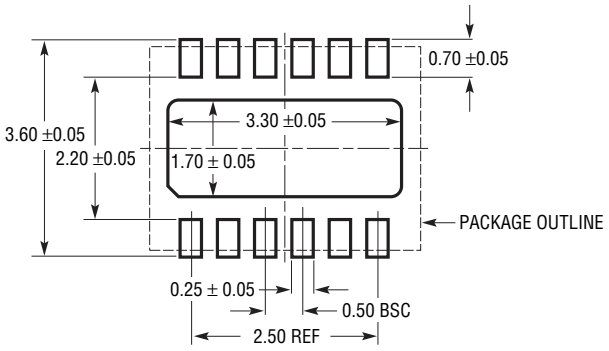


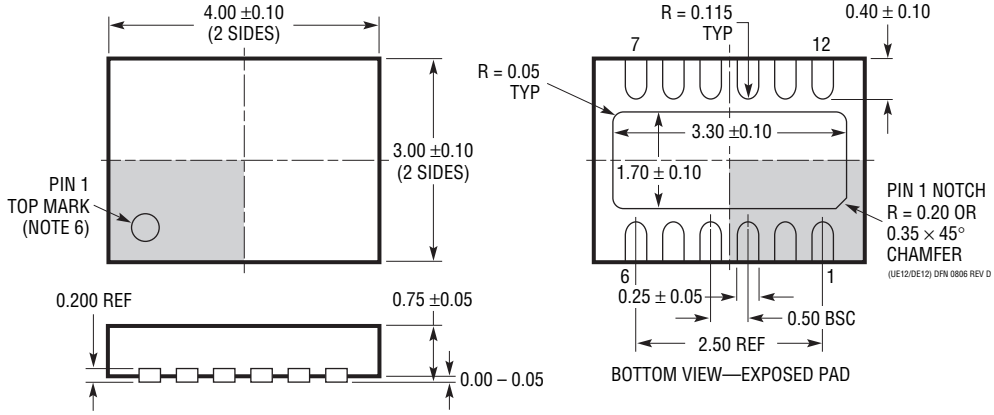
Figure 5. Effects of Rail-to-Rail Operation on a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/10	Revised Features	1
		Added Pin Configuration and Updated Order Information	2
		Added Text to Serial Digital Interface Section	13