16-Bit ΔΣ ADC with Easy Drive Input Current Cancellation

FEATURES

- **Easy Drive™ Technology Enables Rail-to-Rail Inputs with Zero Differential Input Current**
- **Directly Digitizes High Impedance Sensors with Full Accuracy**
- **600nV RMS Noise, Independent of V_{REF}**
- **Operates with a Reference as Low as 100mV with 16-Bit Resolution**
- **GND to V_{CC} Input/Reference Common Mode Range**
- Simultaneous 50Hz/60Hz Rejection Mode
- 2ppm INL, No Missing Codes
- 1ppm Offset and 15ppm Total Unadjusted Error
- No Latency: Digital Filter Settles in a Single Cycle
- Single Supply 2.7V to 5.5V Operation
- Internal Oscillator
- Available in a Tiny (3mm × 3mm) 10-Lead DFN Package

APPLICATIONS

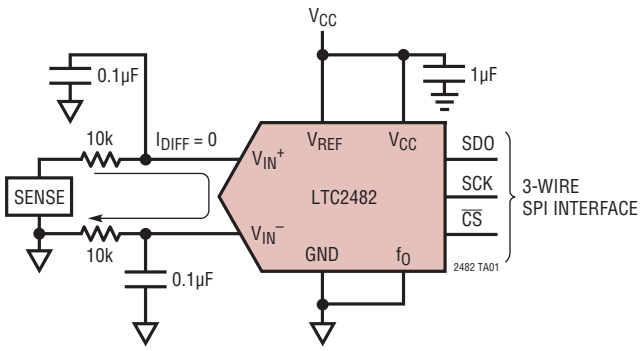
- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Strain Gauge Transducers
- Instrumentation
- Industrial Process Control
- DVMs and Meters

DESCRIPTION

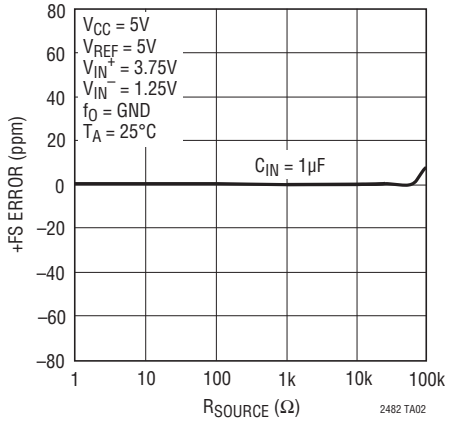
The LTC®2482 combines a 16-bit plus sign No Latency ΔΣ™ analog-to-digital converter with patented Easy Drive technology. The patented sampling scheme eliminates dynamic input current errors and the shortcomings of on-chip buffering through automatic cancellation of differential input current. This allows large external source impedances and input signals with rail-to-rail input range to be directly digitized while maintaining exceptional DC accuracy.

The LTC2482 allows a wide common mode input range (0V to V_{CC}) independent of the reference voltage. The reference can be as low as 100mV or can be tied directly to V_{CC}. The noise level is 600nV RMS independent of V_{REF}. This allows direct digitization of low level signals with 16-bit accuracy. The LTC2482 includes an on-chip trimmed oscillator, eliminating the need for external crystals or oscillators and provides 87dB rejection of 50Hz and 60Hz line frequency noise. Absolute accuracy and low drift are automatically maintained through continuous, transparent, offset and full-scale calibration.

TYPICAL APPLICATION



+FS Error vs R_{SOURCE} at IN^+ and IN^-

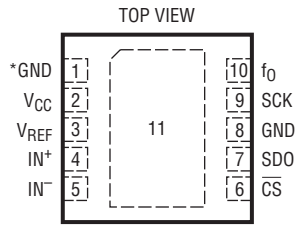


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 6V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2482C ..... 0°C to 70°C
LTC2482I ..... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 160°C/W
EXPOSED PAD (PIN #) IS GND, MUST BE SOLDERED TO PCB
*PIN 1 MAY BE DRIVEN WITH A DIGITAL SIGNAL IN ORDER TO REMAIN PIN COMPATIBLE WITH THE LTC2480/LTC2482

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2482CDD#PBF	LTC2482CDD#TRPBF	LBSQ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2482IDD#PBF	LTC2482IDD#TRPBF	LBSQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (NORMAL SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1 ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)	●	16			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	●		2 1	20	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = $IN^–$ ≤ V_{CC} (Note 14)	●		0.5	5	µV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = $IN^–$ ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, $IN^–$ = 0.25V_{REF}	●			32	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, $IN^–$ = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, $IN^–$ = 0.25V_{REF}	●			32	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, $IN^–$ = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V 5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V			15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, GND ≤ $IN^–$ = IN^+ ≤ V_{CC} (Note 13)			0.6		μV_{RMS}

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common Mode Rejection DC	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^- = IN^+ ≤ V_{CC} (Note 5)	●	140			dB
Input Common Mode Rejection, 50Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^- = IN^+ ≤ V_{CC} (Note 5)	●	140			dB
Input Common Mode Rejection, 60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^- = IN^+ ≤ V_{CC} (Note 5)	●	140			dB
Input Normal Mode Rejection, 50Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^- = IN^+ ≤ V_{CC} (Notes 5, 7)	●	110	120		dB
Input Normal Mode Rejection, 60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^- = IN^+ ≤ V_{CC} (Notes 5, 8)	●	110	120		dB
Input Normal Mode Rejection, 50Hz/60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^- = IN^+ ≤ V_{CC} (Notes 5, 9)	●	87			dB
Reference Common Mode Rejection DC	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^- = IN^+ ≤ V_{CC} (Note 5)	●	120	140		dB
Power Supply Rejection DC	V_{REF} = 2.5V, IN^- = IN^+ = GND			120		dB
Power Supply Rejection, 50Hz ±2%	V_{REF} = 2.5V, IN^- = IN^+ = GND (Note 7)			120		dB
Power Supply Rejection, 60Hz ±2%	V_{REF} = 2.5V, IN^- = IN^+ = GND (Note 8)			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage			GND – 0.3V		V_{CC} + 0.3V	V
IN^-	Absolute/Common Mode IN^- Voltage			GND – 0.3V		V_{CC} + 0.3V	V
FS	Full Scale of the Differential Input (IN^+ – IN^-)		●	$0.5V_{REF}$			V
LSB	Least Significant Bit of the Output Code		●	$FS/2^{16}$			
V_{IN}	Input Differential Voltage Range (IN^+ – IN^-)		●	–FS		+FS	V
V_{REF}	Reference Voltage Range		●	0.1		V_{CC}	V
C_S (IN^+)	IN^+ Sampling Capacitance				11		pF
C_S (IN^-)	IN^- Sampling Capacitance				11		pF
C_S (V_{REF})	V_{REF} Sampling Capacitance				11		pF
I_{DC_LEAK} (IN^+)	IN^+ DC Leakage Current	Sleep Mode, IN^+ = GND	●	–10	1	10	nA
I_{DC_LEAK} (IN^-)	IN^- DC Leakage Current	Sleep Mode, IN^- = GND	●	–10	1	10	nA
I_{DC_LEAK} (V_{REF})	V_{REF} Leakage Current	Sleep Mode, V_{REF} = V_{CC}	●	–100	1	100	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage; $\overline{CS}$, f_O	2.7V ≤ V_{CC} ≤ 5.5V (Note 16)	●	V_{CC} – 0.5			V
V_{IL}	Low Level Input Voltage; $\overline{CS}$, f_O	2.7V ≤ V_{CC} ≤ 5.5V	●			0.5	V
V_{IH}	High Level Input Voltage, SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 10)	●	V_{CC} – 0.5			V
V_{IL}	Low Level Input Voltage, SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 10)	●			0.5	V
I_{IN}	Digital Input Current; $\overline{CS}$, f_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current, SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 10)	●	–10		10	µA
C_{IN}	Digital Input Capacitance; $\overline{CS}$, f_O				10		pF
C_{IN}	Digital Input Capacitance, SCK				10		pF
V_{OH}	High Level Output Voltage, SDO	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage, SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage, SCK	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage, SCK	I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage, SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Mode (Note 12) Sleep Mode (Note 12)	● ●		160 1	250 2	µA µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 15)	●	10		4000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time	Simultaneous 50Hz/60Hz External Oscillator	● ●	144.1	146.9 41036/f_{EOSC} (in kHz)	149.9	ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 10)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Note 10)	●	125			ns
t_{HESCK}	External SCK High Period	(Note 10)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	0.61	0.625 192/f_{EOSC} (in kHz)	0.64	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Note 10)	●		24/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO Low		●	0		200	ns
t_2	CS↑ to SDO Hi-Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCKØ	(Note 10)	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK≠	(Note 10)	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$↓		●			50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified:

$V_{REFCM} = V_{REF}/2$, FS = $0.5V_{REF}$

$V_{IN} = IN^+ – IN^–$, $V_{IN(CM)} = (IN^+ + IN^–)/2$

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz rejection (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as digital input and the driving clock is f_{ESCK}. In internal SCK mode, the SCK pin is used as digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

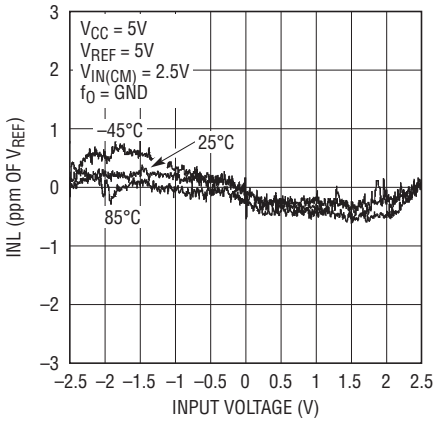
Note 14: Guaranteed by design and test correlation.

Note 15: Refer to Applications Information section for performance vs data rate graphs.

Note 16: For V_{CC} < 3V, V_{IH} is 2.5V for pin f_O.

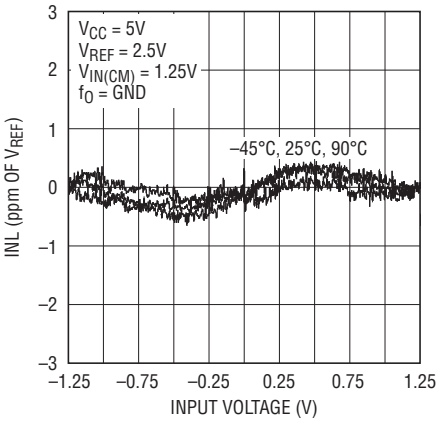
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 5V)



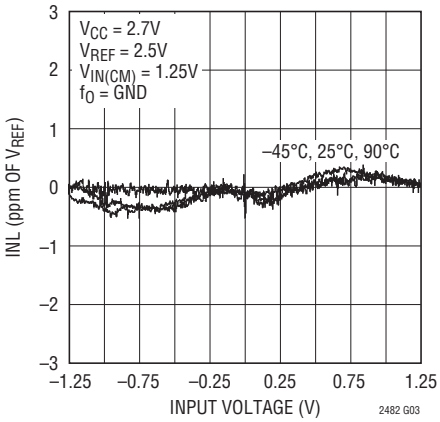
2482 G01

Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 2.5V)



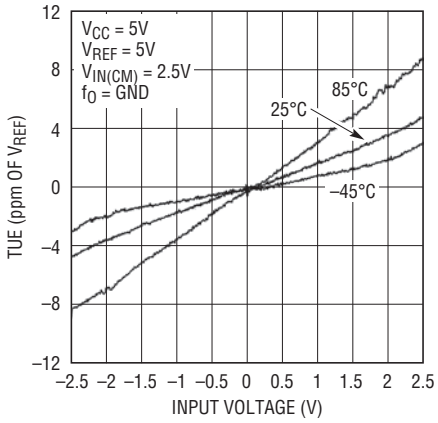
2482 G02

Integral Nonlinearity (V_{CC} = 2.7V, V_{REF} = 2.5V)



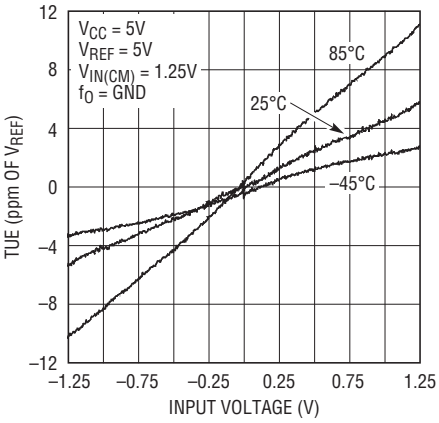
2482 G03

Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 5V)



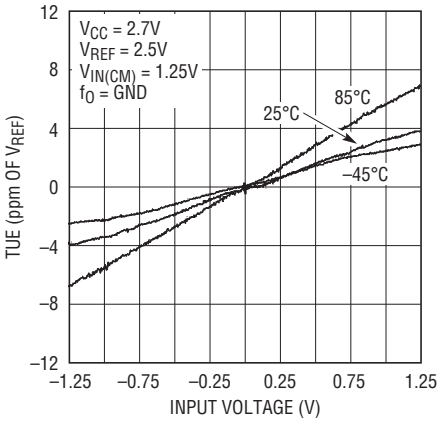
2482 G04

Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 2.5V)



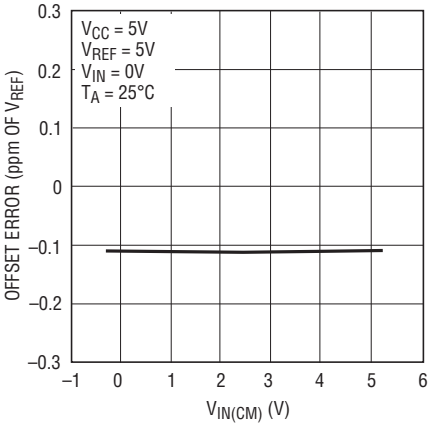
2482 G05

Total Unadjusted Error (V_{CC} = 2.7V, V_{REF} = 2.5V)



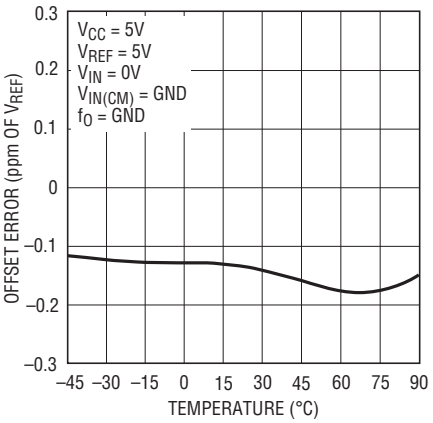
2482 G06

Offset Error vs $V_{IN(CM)}$



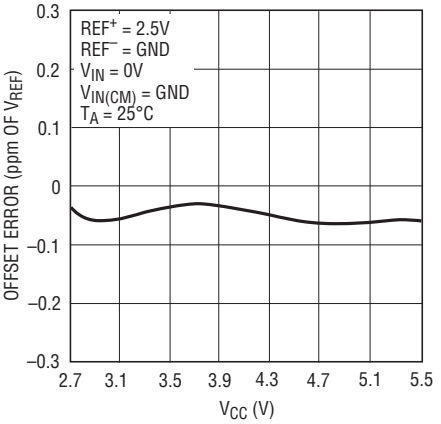
2482 G07

Offset Error vs Temperature



2482 G08

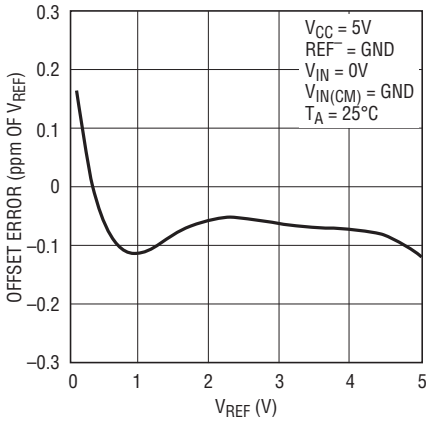
Offset Error vs V_{CC}



2482 G09

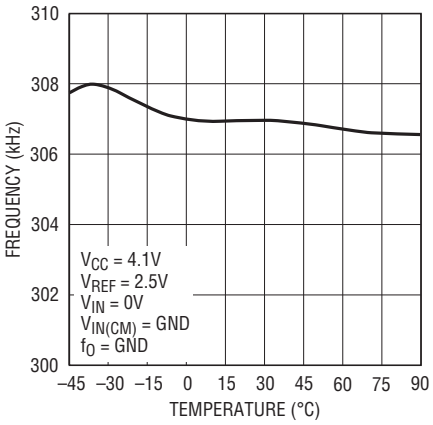
TYPICAL PERFORMANCE CHARACTERISTICS

Offset Error vs V_{REF}



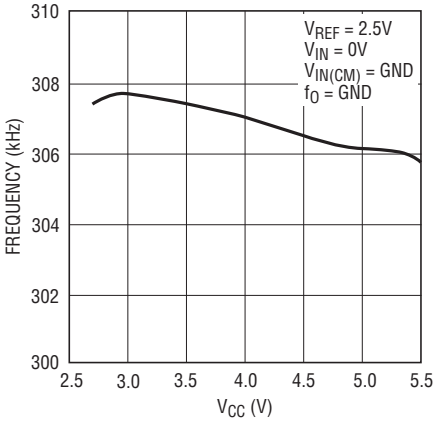
2482 G10

On-Chip Oscillator Frequency vs Temperature



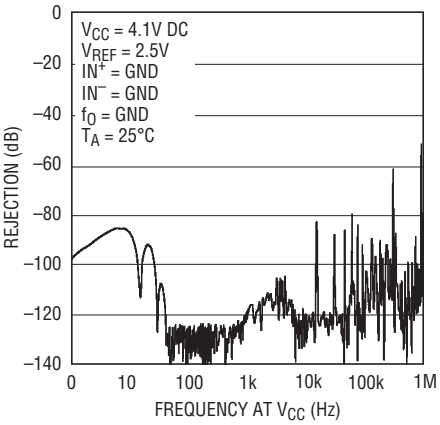
2482 G11

On-Chip Oscillator Frequency vs V_{CC}



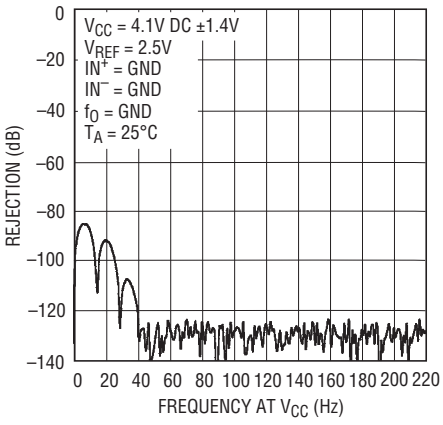
2482 G12

PSRR vs Frequency at V_{CC}



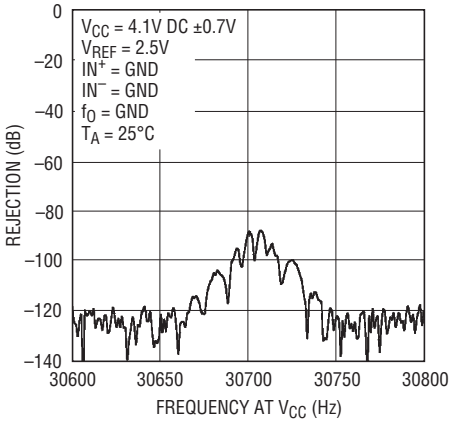
2482 G13

PSRR vs Frequency at V_{CC}



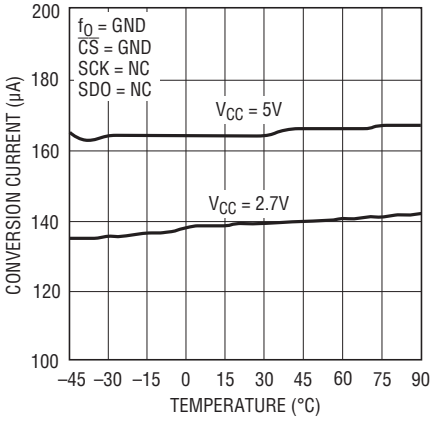
2482 G14

PSRR vs Frequency at V_{CC}



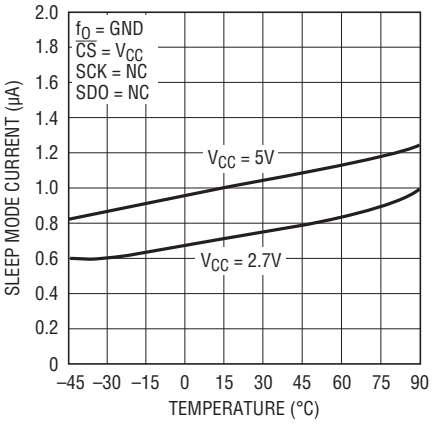
2482 G15

Conversion Current vs Temperature



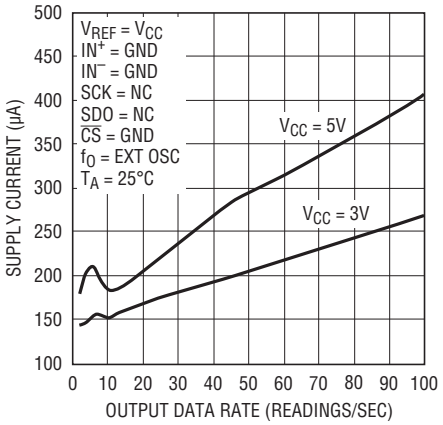
2482 G16

Sleep Mode Current vs Temperature



2482 G17

Conversion Current vs Data Output Rate



2482 G18

PIN FUNCTIONS

GND (Pin 1): Ground. This pin should be tied to ground; however, in order to remain pin compatible with the LTC2480/LTC2484, this pin may be driven high or low.

V_{CC} (Pin 2): Positive Supply Voltage. Bypass to GND (Pin 8) with a 1µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

V_{REF} (Pin 3): Positive Reference Input. The voltage on this pin can have any value between 0.1V and V_{CC}. The negative reference input is GND (Pin 8).

IN^+ (Pin 4), IN^- (Pin 5): Differential Analog Inputs. The voltage on these pins can have any value between GND – 0.3V and V_{CC} + 0.3V. Within these limits the converter bipolar input range ($V_{IN} = IN^+ – IN^-$) extends from –0.5 • V_{REF} to 0.5 • V_{REF}. Outside this input range the converter produces unique overrange and underrange output codes.

$\overline{CS}$ (Pin 6): Active Low Chip Select. A low on this pin enables the digital input/output and wakes up the ADC. Following each conversion the ADC automatically enters the sleep mode and remains in this low power state as long as $\overline{CS}$ is high. A low-to-high transition on $\overline{CS}$ during the data output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 7): Three-State Digital Output. During the data output period, this pin is used as the serial data output. When the chip select, $\overline{CS}$, is high ($\overline{CS} = V_{CC}$), the SDO pin is in a high impedance state. During the conversion and sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling $\overline{CS}$ low.

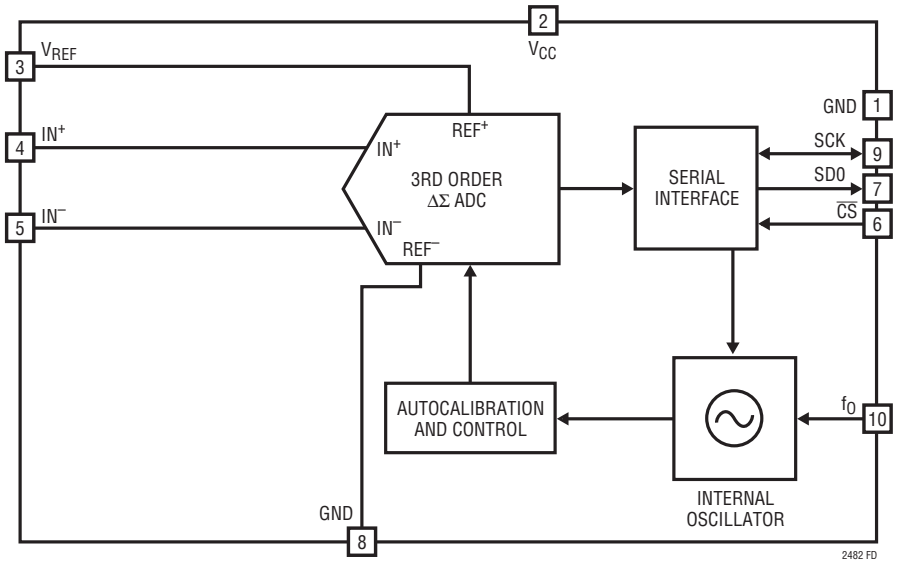
GND (Pin 8): Ground. Shared pin for analog ground, digital ground and reference ground. Should be connected directly to a ground plane through a minimum impedance.

SCK (Pin 9): Bidirectional Digital Clock Pin. In internal serial clock operation mode, SCK is used as the digital output for the internal serial interface clock during the data output period. In external serial clock operation mode, SCK is used as the digital input for the external serial interface clock during the data output period. A weak internal pull-up is automatically activated in internal serial clock operation mode. The serial clock operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of $\overline{CS}$.

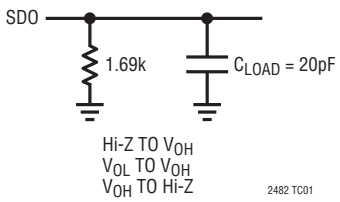
f_O (Pin 10): Frequency Control Pin. Digital input that controls the conversion clock. When f_O is connected to GND the converter uses its internal oscillator running at 307.2kHz. The conversion clock may also be overridden by driving the f_O pin with an external clock in order to change the output rate or the digital filter rejection null.

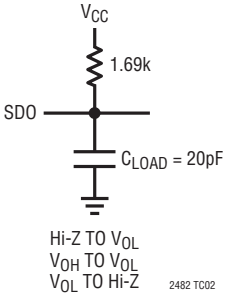
Exposed Pad (Pin 11): This pin is ground and should be soldered to the PCB, GND plane. For prototyping purposes this pin may remain floating.

FUNCTIONAL BLOCK DIAGRAM



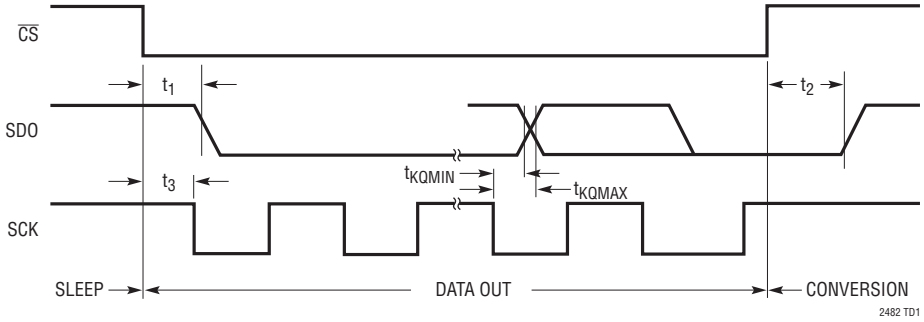
TEST CIRCUITS



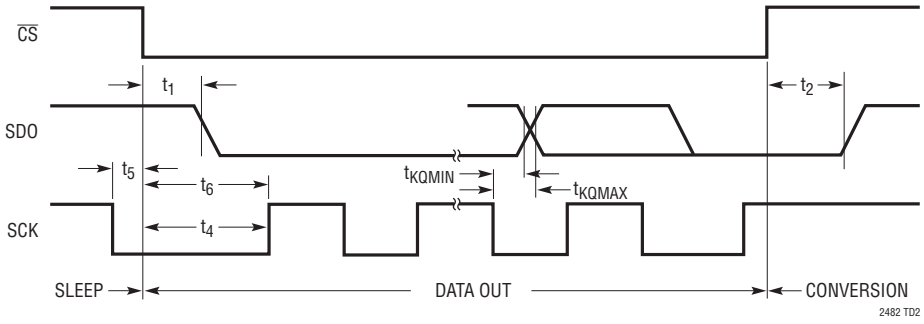


TIMING DIAGRAMS

Timing Diagram Using Internal SCK



Timing Diagram Using External SCK



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2482 is a low power, delta-sigma analog-to-digital converter with an easy-to-use 3-wire serial interface and automatic differential input current cancellation. Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 1). The 3-wire interface consists of serial data output (SDO), serial clock (SCK) and chip select ($\overline{CS}$).

Initially, the LTC2482 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced

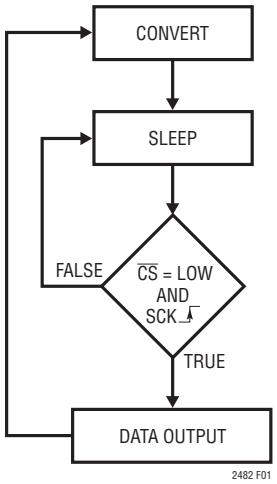


Figure 1. LTC2482 State Transition Diagram

APPLICATIONS INFORMATION

by two orders of magnitude. The part remains in the sleep state as long as $\overline{CS}$ is high. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{CS}$ is pulled low, the device exits the low power mode and enters the data output state. If $\overline{CS}$ is pulled high before the first rising edge of SCK, the device returns to the low power sleep mode and the conversion result is still held in the internal static shift register. If $\overline{CS}$ remains low after the first rising edge of SCK, the device begins outputting the conversion result. Taking $\overline{CS}$ high at this point will terminate the data output state and start a new conversion. The conversion result is shifted out of the device through the serial data output pin (SDO) on the falling edge of the serial clock (SCK) (see Figure 2).

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2482 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Easy Drive Input Current Cancellation

The LTC2482 combines a high precision delta-sigma ADC with an automatic differential input current cancellation front end. A proprietary front-end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2482 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Input Current Cancellation section). This unique architecture does not require on-chip buffers enabling input signals to swing all the way to ground and up to V_{CC}. Furthermore, the cancellation does not interfere with the transparent offset and full-scale autocalibration and the absolute accuracy (full scale + offset + linearity) is maintained with external RC networks.

Output Data Format

The LTC2482 serial output data stream is 24 bits long. The first 3 bits represent status information indicating the sign and conversion state. The next 17 bits are the conversion result, MSB first. The remaining 4 bits are always zero. Bit 21 and Bit 20 together are also used to indicate an underrange condition (the differential input voltage is below –FS) or an overrange condition (the differential input voltage is above +FS).

In applications where a processor generates 32 clock cycles, or to remain compatible with higher resolution converters, the LTC2482's digital interface will ignore extra clock edges seen during the next conversion period after the 24th and output "1" for the extra clock cycles. Furthermore, $\overline{CS}$ may be pulled high prior to outputting all 24 bits, aborting the data out transfer and initiating a new conversion.

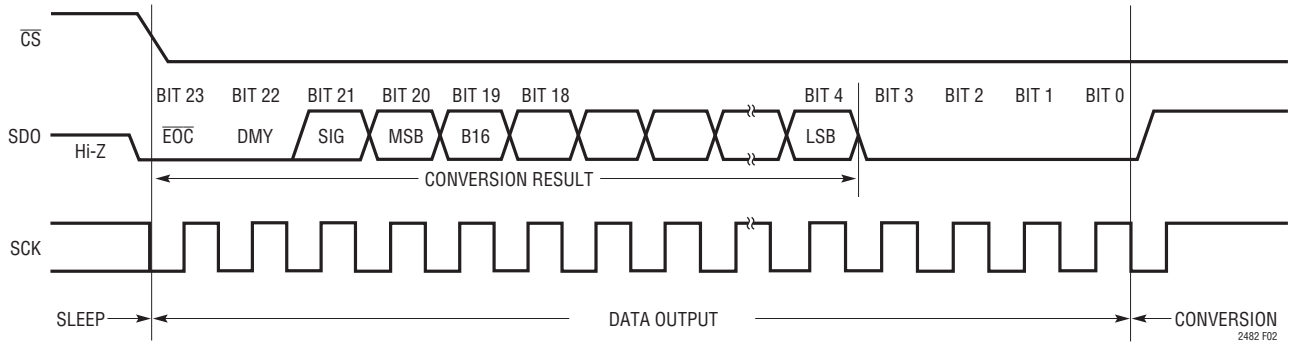


Figure 2. Output Data Timing

APPLICATIONS INFORMATION

Bit 23 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is low. This bit is high during the conversion and goes low when the conversion is complete.

Bit 22 (second output bit) is a dummy bit (DMY) and is always low.

Bit 21 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is high. If V_{IN} is <0, this bit is low.

Bit 20 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 21 also provides the underrange or overrange indication. If both Bit 21 and Bit 20 are high, the differential input voltage is above +FS. If both Bit 21 and Bit 20 are low, the differential input voltage is below –FS.

The function of these bits is summarized in Table 1.

Table 1. LTC2482 Status Bits

INPUT RANGE	BIT 23 $\overline{EOC}$	BIT 22 DMY	BIT 21 SIG	BIT 20 MSB
$V_{IN} \geq 0.5 \cdot V_{REF}$	0	0	1	1
$0V \leq V_{IN} < 0.5 \cdot V_{REF}$	0	0	1	0
$-0.5 \cdot V_{REF} \leq V_{IN} < 0V$	0	0	0	1
$V_{IN} < -0.5 \cdot V_{REF}$	0	0	0	0

Bits 20-4 are the 16-bit plus sign conversion result MSB first.

Bits 3-0 are always low and are included to maintain software compatibility with the LTC2480.

Data is shifted out of the SDO pin under control of the serial clock (SCK) (see Figure 2). Whenever $\overline{CS}$ is high, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven low. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled low. $\overline{EOC}$ changes in real time from high to low at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 23 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 22 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 23rd SCK and may be latched on the rising edge of the 24th SCK pulse. On the falling edge of the 24th SCK pulse, SDO goes high indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$ (Bit 23) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the IN^+ and IN^- pins is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value corresponding to –FS – 1LSB.

Table 2. LTC2482 Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 23 $\overline{EOC}$	BIT 22 DMY	BIT 21 SIG	BIT 20 MSB	BIT 19	BIT 18	BIT 17	…	BIT 4	BITS 3-0
V_{IN}* ≥ FS**	0	0	1	1	0	0	0	…	0	0
FS** – 1LSB	0	0	1	0	1	1	1	…	1	0
0.5 • FS**	0	0	1	0	1	0	0	…	0	0
0.5 • FS** – 1LSB	0	0	1	0	0	1	1	…	1	0
0	0	0	1	0	0	0	0	…	0	0
–1LSB	0	0	0	1	1	1	1	…	1	0
–0.5 • FS**	0	0	0	1	1	0	0	…	0	0
–0.5 • FS** – 1LSB	0	0	0	1	0	1	1	…	1	0
–FS**	0	0	0	1	0	0	0	…	0	0
V_{IN}* < –FS**	0	0	0	0	1	1	1	…	1	0

*The differential input voltage $V_{IN} = IN^+ – IN^-$. **The full-scale voltage FS = 0.5 • V_{REF}.

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Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a SINC or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz or 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2482 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators.

Frequency Rejection Selection (f_O)

The LTC2482 internal oscillator provides better than 87dB normal mode rejection at the line frequency and all its harmonics (up to the 255th) for the frequency range 48Hz to 62.4Hz.

When a fundamental rejection frequency different from 50Hz/60Hz is required, when more than 87dB rejection is needed for 50Hz/60Hz, or when the converter must be synchronized with an outside source, the LTC2482 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the f_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 10kHz to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2482 provides better than 110dB normal mode rejection in a frequency range of $f_{EOSC}/5120$ ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/5120$ is shown in Figure 3.

Whenever an external clock is not present at the f_O pin, the converter automatically activates its internal oscillator and enters the internal conversion clock mode. The LTC2482 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state and the achievable output data rate as a function of f_O.

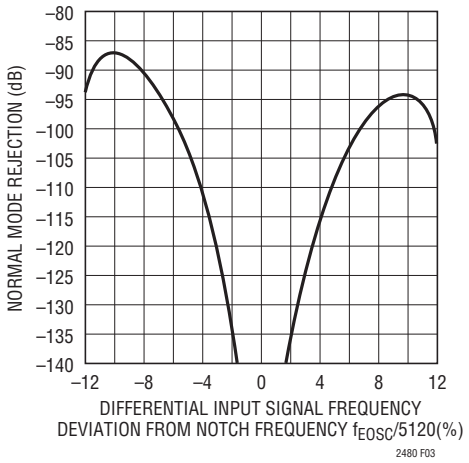

Figure 3. LTC2482 Normal Mode Rejection When Using an External Oscillator

Table 3. LTC2482 State Duration

STATE	OPERATING MODE		DURATION
CONVERT	Internal Oscillator	50Hz/60Hz Rejection	147ms, Output Data Rate ≤ 6.8 Readings/s
	External Oscillator	f_O = External Oscillator with Frequency f_{EOSC} kHz ($f_{EOSC}/5120$ Rejection)	$41036/f_{EOSC}$s, Output Data Rate ≤ $f_{EOSC}/41036$ Readings/s
SLEEP			As Long As $\overline{CS}$ = High, After a Conversion is Complete
DATA OUTPUT	Internal Serial Clock	f_O = Low/High (Internal Oscillator)	As Long As $\overline{CS}$ = Low But Not Longer Than 0.62ms (24 SCK Cycles)
		f_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = Low But Not Longer Than $192/f_{EOSC}$ms (24 SCK Cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = Low But Not Longer Than $24/f_{SCK}$ms (24 SCK Cycles)

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Ease of Use

The LTC2482 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

The LTC2482 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2482 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. Following the POR signal, the LTC2482 starts a normal conversion cycle and follows the succession of states described in Figure 1. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

The LTC2482 external reference voltage range is 0.1V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. Since the transition noise (600nV) is much less than the quantization noise (V_{REF}/217), a decrease in the reference voltage will increase the converter resolution. A reduced reference voltage will improve the converter performance when operated with an external conversion clock (external f_O signal) at substantially higher output data rates (see the Output Data Rate section).

The negative reference input to the converter is internally tied to GND. GND (Pin 8) should be connected to a ground plane through as short a trace as possible to minimize voltage drop. The LTC2482 has an average operational current of 160µA and for 1Ω parasitic resistance, the voltage drop of 160µV causes a gain error of 2LSB for V_{REF} = 5V.

Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the IN^+ and IN^- input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2482 converts bipolar differential input signal, $V_{IN} = IN^+ – IN^-$, from –FS to +FS where FS = 0.5 • V_{REF}. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes. Since the differential input current cancellation does not rely on an on-chip buffer, current cancellation as well as DC performance is maintained rail-to-rail.

Input signals applied to IN^+ and IN^- pins may extend by 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the IN^+ and IN^- pins without affecting the performance of the devices. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

APPLICATIONS INFORMATION

SERIAL INTERFACE TIMING MODES

The LTC2482's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle or continuous conversion. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (f_O = low or f_O = high) or an external oscillator connected to the f_O pin. Refer to Table 4 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 4.

The serial clock mode is selected on the falling edge of $\overline{CS}$. To select the external serial clock mode, the serial clock pin (SCK) must be low during each $\overline{CS}$ falling edge.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is high. At any time during the conversion cycle, $\overline{CS}$ may be pulled low in order to monitor the state of the converter. While $\overline{CS}$ is pulled low, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state, its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ is low. The output data is shifted out of the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 24th rising edge of SCK. On the 24th falling edge of SCK, the device begins a new conversion. SDO goes high ($\overline{EOC}$ = 1) indicating a conversion is in progress. In applications where the processor generates 32 clock cycles, or to remain compatible with higher resolution converters, the LTC2482's digital interface will ignore extra clock edges seen during the next conversion period after the 24th and outputs "1" for the extra clock cycles.

At the conclusion of the data cycle, $\overline{CS}$ may remain low and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven high setting SDO to Hi-Z. As described above, $\overline{CS}$ may be pulled low at any time in order to monitor the conversion status.

Typically, $\overline{CS}$ remains low during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ high anytime between the first rising edge and the 24th falling edge of SCK (see Figure 5). On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 24 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

Table 4. LTC2482 Interface Timing Modes

CONFIGURATION	SCK SOURCE	CONVERSION CYCLE CONTROL	DATA OUTPUT CONTROL	CONNECTION and WAVEFORMS
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 4, 5
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 6
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}\downarrow$	$\overline{CS}\downarrow$	Figures 7, 8
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 9

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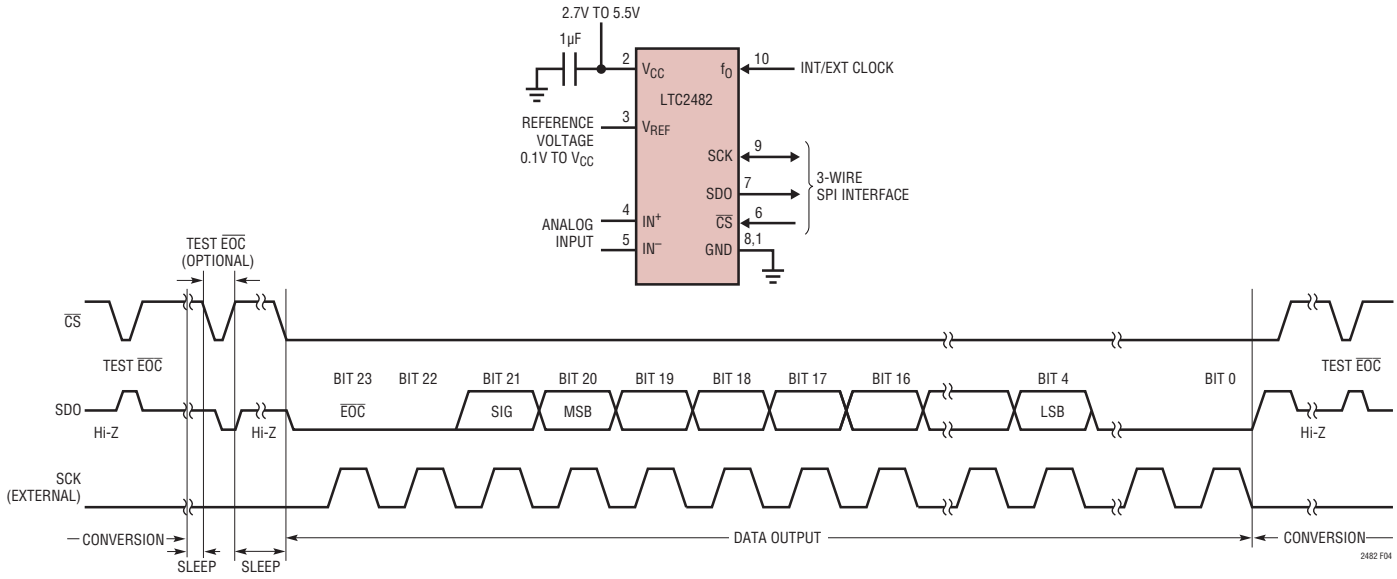

Figure 4. External Serial Clock, Single Cycle Operation

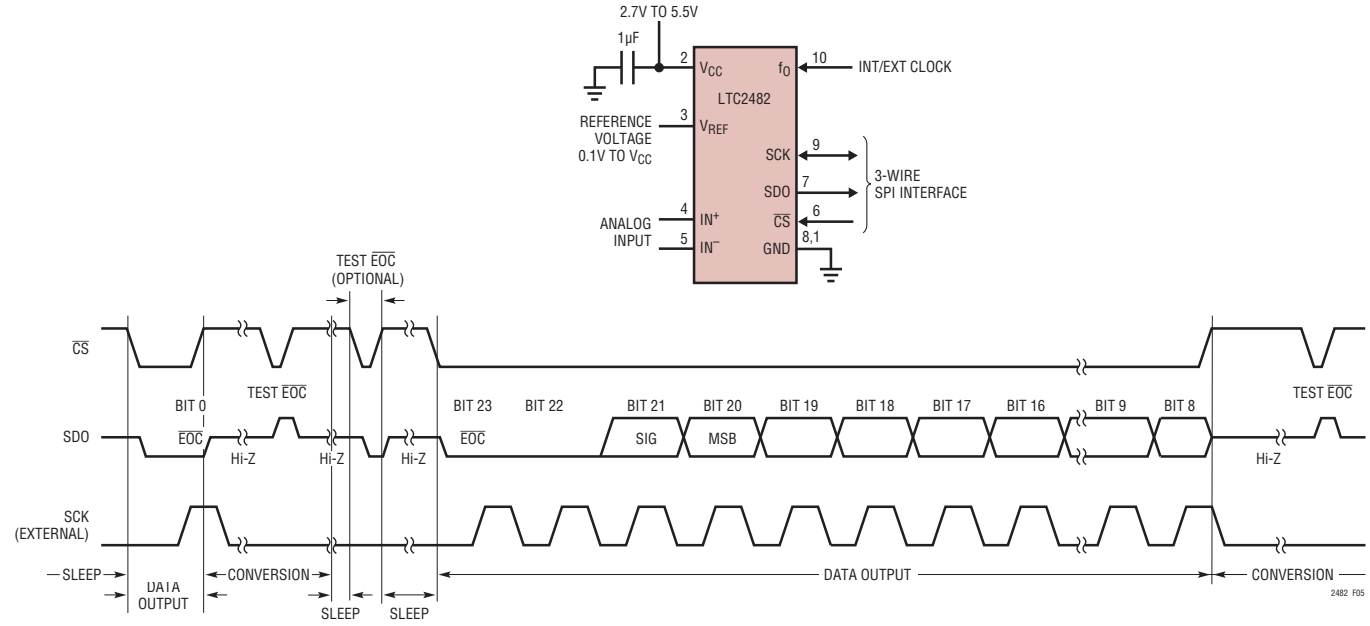

Figure 5. External Serial Clock, Reduced Data Output Length

APPLICATIONS INFORMATION

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal (see Figure 6). $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or transmission over an isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded typically 4ms after V_{CC} exceeds approximately 2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven low prior to the end of POR in order to enter the external serial clock timing mode.

Since $\overline{CS}$ is tied low, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion ends. On the falling edge of $\overline{EOC}$, the conversion result is loaded into an internal static shift register. The output data is shifted out of the SDO pin on each falling edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 24th falling edge of SCK, SDO goes high ($\overline{EOC}$ = 1) indicating a new conversion has begun. In applications where the processor generates 32 clock cycles, or to remain compatible with higher resolution converters, the LTC2482's digital interface will ignore extra clock edges seen during the next conversion period after the 24th and outputs "1" for the extra clock cycles.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle (see Figure 7).

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled high prior to the falling edge of $\overline{CS}$. The device will not enter the internal serial clock mode if SCK is driven low on the falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is high. At any time during the conversion cycle, $\overline{CS}$ may be pulled low in order to monitor the state of the converter. Once $\overline{CS}$ is pulled low, SCK goes low and $\overline{EOC}$ is output to the SDO pin. EOC = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

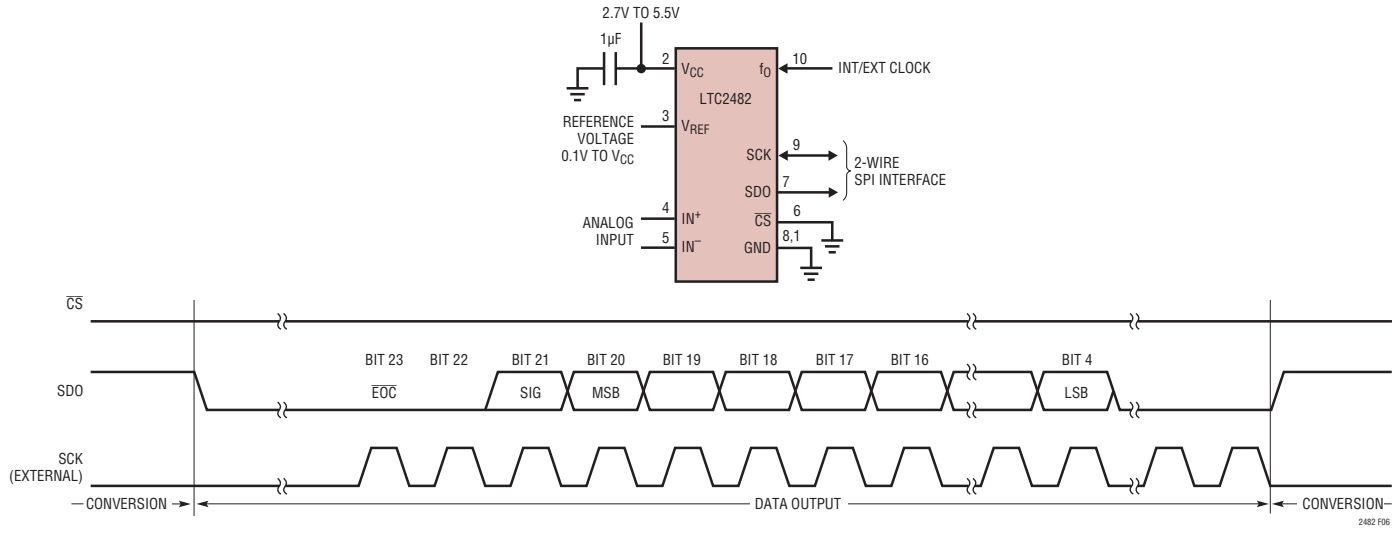

Figure 6. External Serial Clock, $\overline{CS}$ = 0 Operation

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When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the low power mode during the $\overline{EOC}$ test. In order to allow the device to return to the low power sleep state, $\overline{CS}$ must be pulled high before the first rising edge of SCK. In the internal SCK timing mode, SCK goes high and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes low (if $\overline{CS}$ is low during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 12µs if the device is using its internal oscillator. If f_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCtest}$ is $3.6/f_{EOSC}$ in seconds. If $\overline{CS}$ is pulled high before time $t_{EOCtest}$, the device returns to the sleep state and the conversion result is held in the internal static shift register.

If $\overline{CS}$ remains low longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data I/O cycle concludes after the 24th rising edge. The output data is shifted out of the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 24th rising edge of SCK. After the 24th rising edge, SDO goes high ($\overline{EOC}$ = 1), SCK stays high and a new conversion starts.

Typically, $\overline{CS}$ remains low during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ high anytime between the first and 24th rising edge of SCK (see Figure 8). On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 24 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ is pulled high while the converter is driving SCK low, the internal pull-up is not available to restore SCK to a logic high state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ high when SCK is low.

Whenever SCK is low, the LTC2482's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a low signal, the LTC2482's internal pull-up remains disabled. Hence, SCK remains low. On the next falling edge of $\overline{CS}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes high once the external driver goes Hi-Z. On the next $\overline{CS}$ falling edge, the device will remain in the internal SCK timing mode.

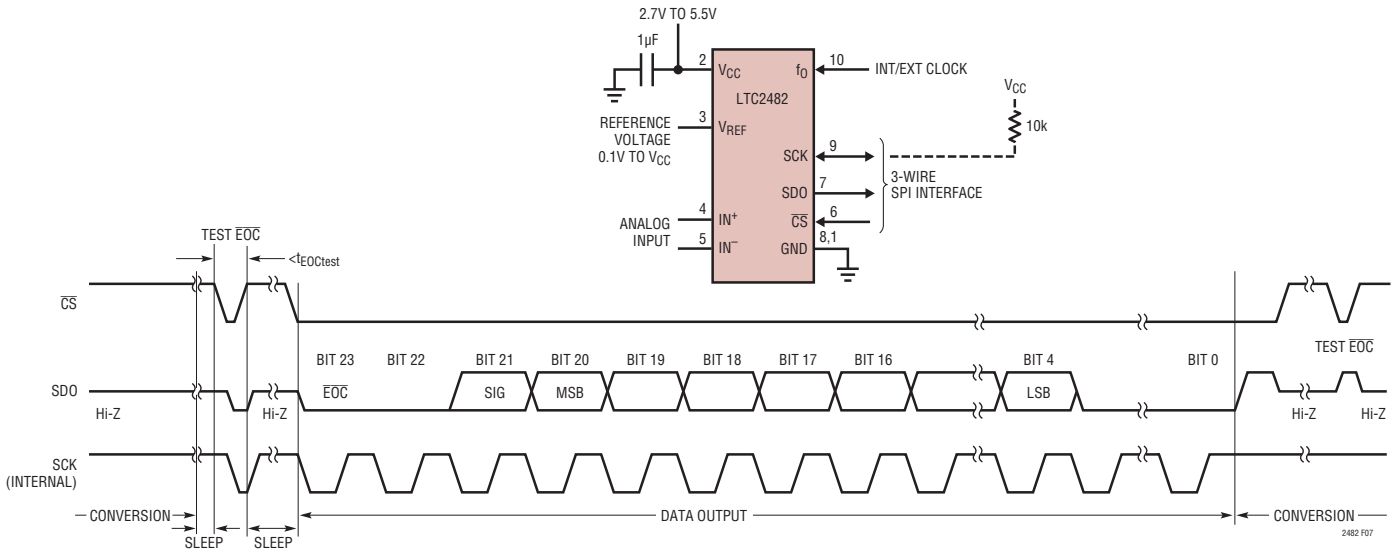

Figure 7. Internal Serial Clock, Single Cycle Operation

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A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed high-low-high in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go low. Once $\overline{CS}$ goes high (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a high level before $\overline{CS}$ goes low again. This is not a concern under normal conditions where $\overline{CS}$ remains low after detecting $\overline{EOC}$ = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire (output only) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal (see Figure 9). $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or transmission over an isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 1ms after V_{CC} exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven low (if SCK is loaded such that the internal pull-up cannot pull the pin high, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are high ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go low ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting data. The data input/output cycle begins on the first rising edge of SCK and ends after the 24th rising edge. The output data is shifted out of the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 24th rising edge of SCK. After the 24th rising edge, SDO goes high ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains high during the conversion.

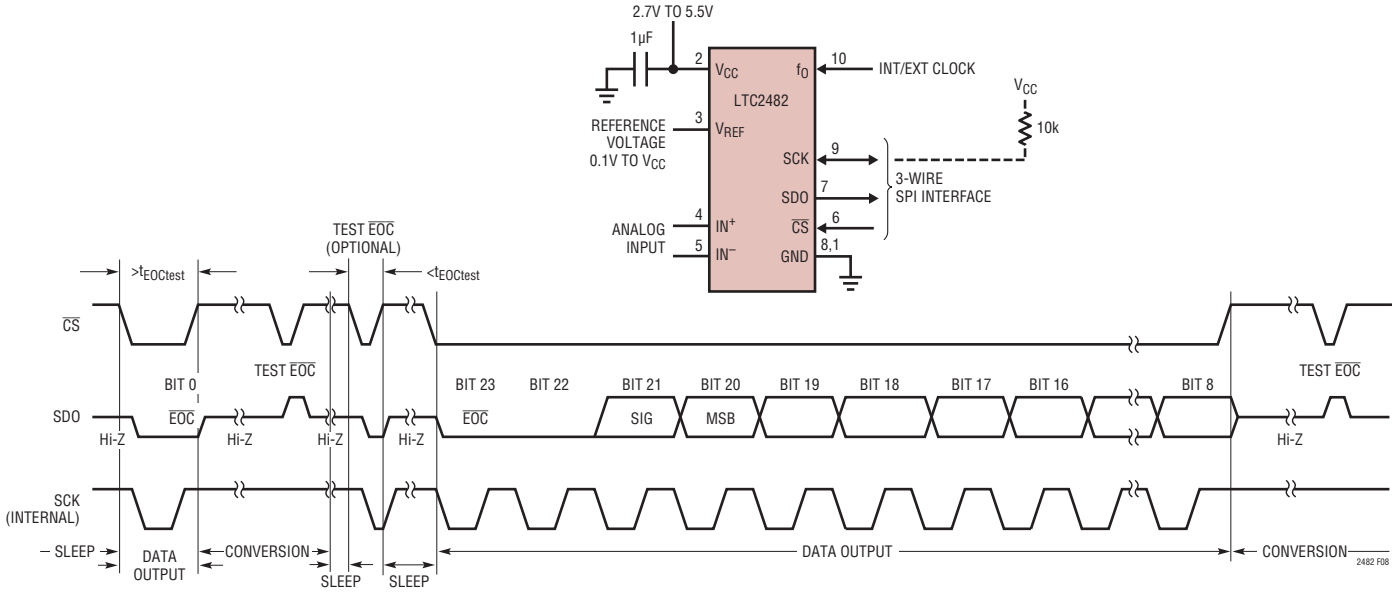

Figure 8. Internal Serial Clock, Reduce Data Output Length

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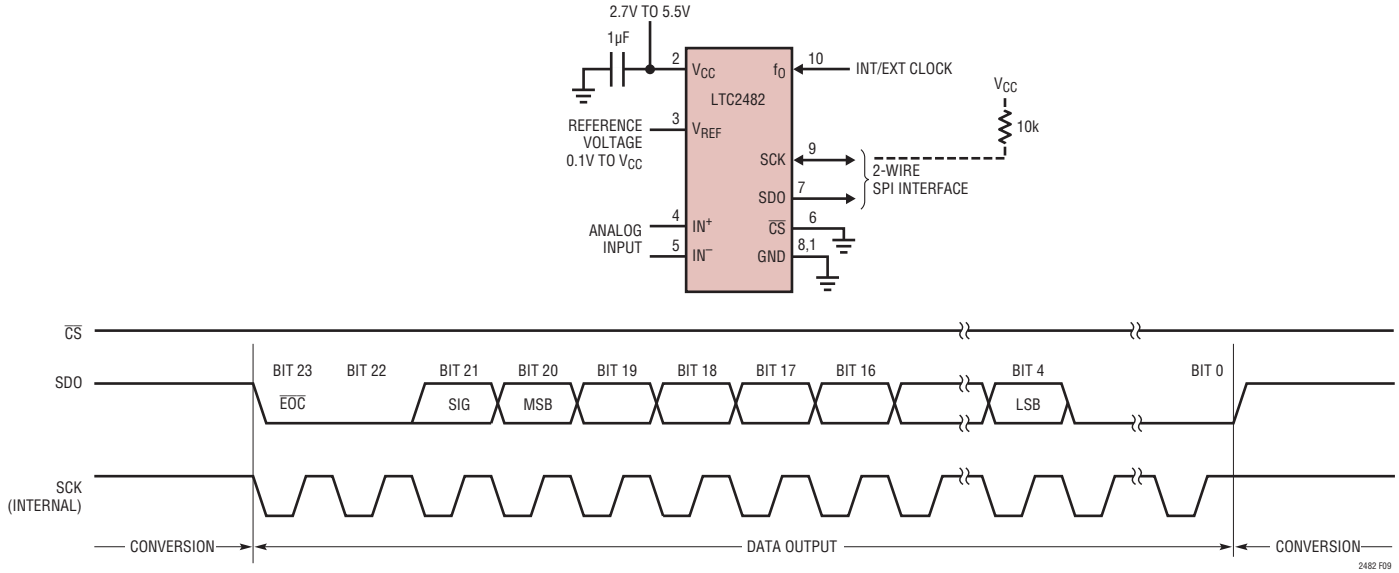

Figure 9. Internal Serial Clock, $\overline{CS}$ = 0 Continuous Operation

PRESERVING THE CONVERTER ACCURACY

The LTC2482 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, antialiasing circuits, line frequency perturbations and so on. Nevertheless, in order to preserve the extreme accuracy capability of this part, some simple precautions are required.

Digital Signal Levels

The LTC2482's digital interface is easy to use. Its digital inputs (f_O, $\overline{CS}$ and SCK in external SCK mode of operation) accept standard CMOS logic levels and the internal hysteresis receivers can tolerate edge transition times as slow as 100µs. However, some considerations are required to take advantage of the exceptional accuracy and low supply current of this converter.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

While a digital input signal is in the range 0.5V to (V_{CC} – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (f_O, $\overline{CS}$ and SCK in external SCK mode of operation) is within this range, the power supply current may increase even if the signal in question is at a valid logic level.

For micropower operation, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

During the conversion period, the undershoot and/or overshoot of a fast digital signal connected to the pins can severely disturb the analog to digital conversion process. Undershoot and overshoot occur because of the impedance mismatch of the circuit board trace at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to the LTC2482. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2482 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver output pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

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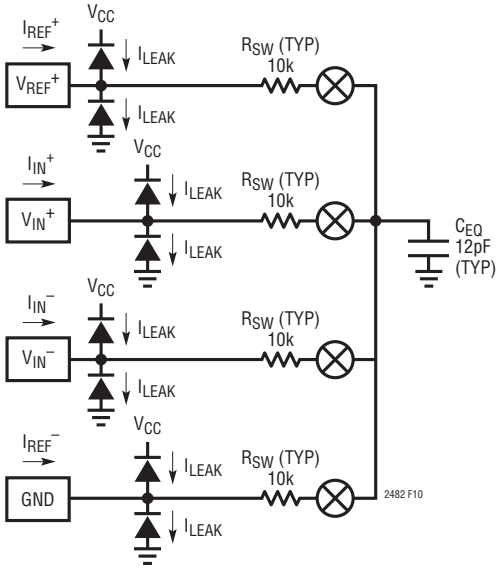
An alternate solution is to reduce the edge rate of the control signals. It should be noted that using very slow edges will increase the converter power supply current during the transition time. The differential input architecture reduces the converter's sensitivity to ground currents.

Particular attention must be given to the connection of the f_O signal when the LTC2482 is used with an external conversion clock. This clock is active during the conversion time and the normal mode rejection provided by the internal digital filter is not very high at this frequency. A normal mode signal of this frequency at the converter reference terminals can result in DC gain and INL errors. A normal mode signal of this frequency at the converter input terminals can result in a DC offset error. Such perturbations can occur due to asymmetric capacitive coupling between the f_O signal trace and the converter input and/or reference connection traces. An immediate solution is to maintain maximum possible separation between the f_O signal trace and the input/reference signals. When the f_O signal is parallel terminated near the converter, substantial AC current is flowing in the loop formed by the f_O connection trace, the termination and the ground return path. Thus, perturbation signals may be inductively coupled into the converter input and/or reference. In this situation, the user must reduce to a minimum the loop area for the f_O signal as well as the loop area for the differential input and reference connections. Even when f_O is not driven, other nearby signals pose similar EMI threats which will be minimized by following good layout practices.

Driving the Input and Reference

The input and reference pins of the LTC2482 converter are directly connected to a network of sampling capacitors. Depending upon the relation between the differential input voltage and the differential reference voltage, these capacitors are switching between these four pins transferring small amounts of charge in the process. A simplified equivalent circuit is shown in Figure 10.

For a simple approximation, the source impedance R_S driving an analog input pin (IN^+, IN^-, V_{REF}^+ or GND) can be considered to form, together with R_{SW} and C_{EQ} (see Figure 10), a first order passive network with a time constant $\tau = (R_S + R_{SW}) \bullet C_{EQ}$. The converter is able to sample the input signal with better than 1ppm accuracy if the sampling period is at least 14 times greater than the input circuit time constant τ. The sampling process on the four input analog pins is quasi-independent so each time constant should be considered by itself and, under worst-case circumstances, the errors may add.



SWITCHING FREQUENCY
f_{SW} = 123kHz INTERNAL OSCILLATOR
$f_{SW} = 0.4 \bullet f_{EOSC}$ EXTERNAL OSCILLATOR

$$I\left(IN^+\right)_{AVG} = I\left(IN^-\right)_{AVG} = \frac{V_{IN(CM)} - V_{REF(CM)}}{0.5 \bullet R_{EQ}}$$

$$I\left(REF^+\right)_{AVG} = \frac{1.5 \bullet V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}} - \frac{0.5 \bullet V_{REF} \bullet D_T}{R_{EQ}} \cong \frac{1.5V_{REF} + \left(V_{REF(CM)} - V_{IN(CM)}\right)}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

where:

$$V_{REFCM} = \left(\frac{V_{REF}^+}{2}\right)$$

$$V_{IN} = IN^+ - IN^-$$

$$V_{INCM} = \left(\frac{IN^+ + IN^-}{2}\right)$$

$R_{EQ} = 2.98M\Omega$ INTERNAL OSCILLATOR

$R_{EQ} = \left(0.915 \bullet 10^{12}\right) / f_{EOSC}$ EXTERNAL OSCILLATOR

D_T IS THE DENSITY OF A DIGITAL TRANSITION AT THE MODULATOR OUTPUT WHERE REF^- IS INTERNALLY TIED TO GND

Figure 10. LTC2482 Equivalent Analog Input Current

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When using the internal oscillator, the LTC2482's front-end switched-capacitor network is clocked at 123kHz corresponding to an 8.1µs sampling period. Thus, for settling errors of less than 1ppm, the driving source impedance should be chosen such that $\tau \leq 8.1\mu s/14 = 580ns$. When an external oscillator of frequency f_{EOSC} is used, the sampling period is $2.5/f_{EOSC}$ and, for a settling error of less than 1ppm, $\tau \leq 0.178/f_{EOSC}$.

Automatic Differential Input Current Cancellation

In applications where the sensor output impedance is low (up to 10kΩ with no external bypass capacitor or up to 500Ω with 0.001µF bypass), complete settling of the input occurs. In this case, no errors are introduced and direct digitization of the sensor is possible.

For many applications, the sensor output impedance combined with external bypass capacitors produces RC time constants much greater than the 580ns required for 1ppm accuracy. For example, a 10kΩ bridge driving a 0.1µF bypass capacitor has a time constant an order of magnitude greater than the required maximum. Historically, settling issues were solved using buffers. These buffers led to increased noise, reduced DC performance (offset/drift), limited input/output swing (cannot digitize signals near ground or V_{CC}), added system cost and increased power. The LTC2482 uses a proprietary switching algorithm that forces the average differential input current to zero independent of external settling errors. This allows accurate direct digitization of high impedance sensors without the need for buffers. Additional errors resulting from mismatched leakage currents must also be taken into account.

The switching algorithm forces the average input current on the positive input (I_{IN}^+) to be equal to the average input current on the negative input (I_{IN}^-). Over the complete conversion cycle, the average differential input current ($I_{IN}^+ - I_{IN}^-$) is zero. While the differential input current is zero, the common mode input current ($I_{IN}^+ + I_{IN}^-$)/2 is proportional to the difference between the common mode input voltage (V_{INCM}) and the common mode reference voltage (V_{REFCM}).

In applications where the input common mode voltage is equal to the reference common mode voltage, as in the case of a balance bridge type application, both the differential and common mode input current are zero. The accuracy of the converter is unaffected by settling errors. Mismatches in source impedances between IN^+ and IN^- also do not affect the accuracy.

In applications where the input common mode voltage is constant but different from the reference common mode voltage, the differential input current remains zero while the common mode input current is proportional to the difference between V_{INCM} and V_{REFCM}. For a reference common mode of 2.5V and an input common mode of 1.5V, the common mode input current is approximately 0.74µA. This common mode input current has no effect on the accuracy if the external source impedances tied to IN^+ and IN^- are matched. Mismatches in these source impedances lead to a fixed offset error but do not affect the linearity or full-scale reading. A 1% mismatch in 1k source resistances leads to a 1LSB shift (74µV) in offset voltage.

In applications where the common mode input voltage varies as a function of input signal level (single-ended input, RTDs, half bridges, current sensors, etc.), the common mode input current varies proportionally with input voltage. For the case of balanced input impedances, the common mode input current effects are rejected by the large CMRR of the LTC2482 leading to little degradation in accuracy. Mismatches in source impedances lead to gain errors proportional to the difference between the common mode input voltage and the common mode reference voltage. 1% mismatches in 1k source resistances lead to gain worst-case gain errors on the order of 1LSB (for 1V differences in reference and input common mode voltage). Table 5 summarizes the effects of mismatched source impedance and differences in reference/input common mode voltages.

Table 5. Suggested Input Configuration for LTC2482

	BALANCED INPUT RESISTANCES	UNBALANCED INPUT RESISTANCES
Constant $V_{IN(CM)} - V_{REF(CM)}$	C_{IN} > 1nF at Both IN^+ and IN^-. Can Take Large Source Resistance with Negligible Error	C_{IN} > 1nF at Both IN^+ and IN^-. Can Take Large Source Resistance. Unbalanced Resistance Results in an Offset Which Can be Calibrated
Varying $V_{IN(CM)} - V_{REF(CM)}$	C_{IN} > 1nF at Both IN^+ and IN^-. Can Take Large Source Resistance with Negligible Error	Minimize IN^+ and IN^- Capacitors and Avoid Large Source Impedance (<5k Recommended)

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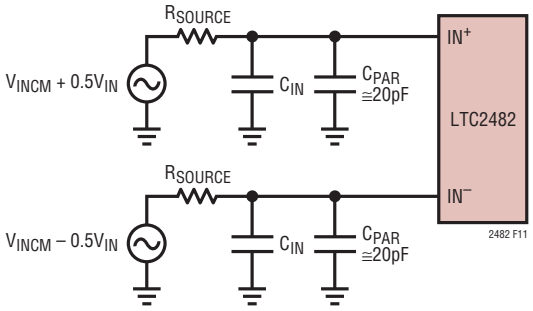

Figure 11. An RC Network at IN⁺ and IN⁻

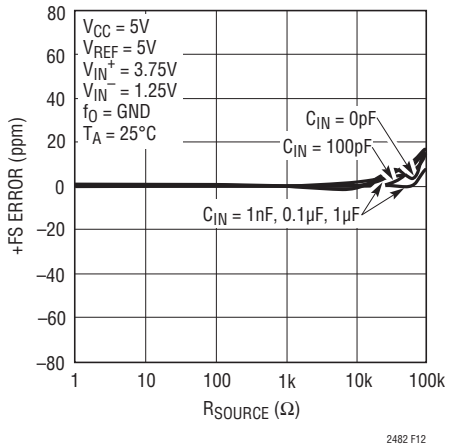

Figure 12. +FS Error vs R_{SOURCE} at IN⁺ and IN⁻

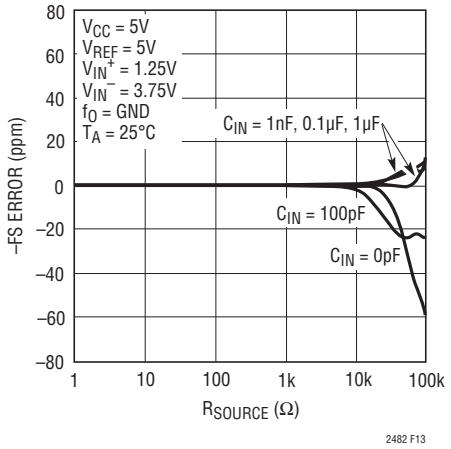

Figure 13. –FS Error vs R_{SOURCE} at IN⁺ and IN⁻

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by IN⁺ and IN⁻, the expected drift of the dynamic current and offset will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications, a one-time calibration operation may be sufficient.

In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA max), results in a small offset shift. A 1k source resistance will create a 1µV typical and 10µV maximum offset voltage.

Reference Current

In a similar fashion, the LTC2482 samples the differential reference pins V_{REF}^+ and GND transferring small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset, but it may degrade the gain and INL performance. The effect of this current can be analyzed in two distinct situations.

For relatively small values of the external reference capacitors (C_{REF} < 1nF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for C_{REF} will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

Larger values of reference capacitors (C_{REF} > 1nF) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge and the external source resistance will see a quasi constant reference differential impedance.

In the following discussion, it is assumed the input and reference common mode are the same. Using internal oscillator (50Hz/60Hz rejection), the differential reference

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resistance is 1.1MΩ and the resulting full-scale error is 0.46ppm for each ohm of source resistance driving the V_{REF} pin. When f_O is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential reference resistance is 0.33 • 1012/f_{EOSC} Ω and each ohm of source resistance driving the V_{REF} pin will result in 1.53 • 10–6 • f_{EOSC}ppm gain error. The typical +FS and –FS errors for various combinations of source resistance seen by the V_{REF} pin and external capacitance connected to that pin are shown in Figures 14-17.

In addition to this gain error, the converter INL performance is degraded by the reference source impedance. The INL is caused by the input dependent terms $–V_{IN2}/(V_{REF} • R_{EQ}) – (0.5 • V_{REF} • D_T)/R_{EQ}$ in the reference pin current as expressed in Figure 10. When using internal oscillator with 50Hz/60Hz rejection, every 100Ω of reference source resistance translates into about 0.61ppm additional INL error. When f_O is driven by an external oscillator with a frequency f_{EOSC}, every 100Ω of source resistance driving V_{REF} translates into about $1.99 • 10^{–6} • f_{EOSC}$ppm additional INL error. Figure 18 shows the typical INL error due to the source resistance driving the V_{REF} pin when large C_{REF} values are used. The user is advised to minimize the source impedance driving the V_{REF} pin.

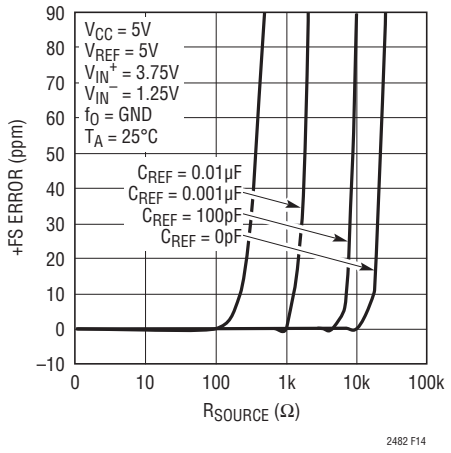

Figure 14. +FS Error vs R_{SOURCE} at V_{REF} (Small C_{REF})

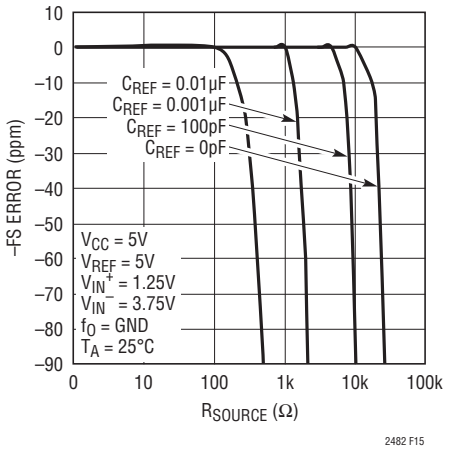

Figure 15. –FS Error vs R_{SOURCE} at V_{REF} (Small C_{REF})

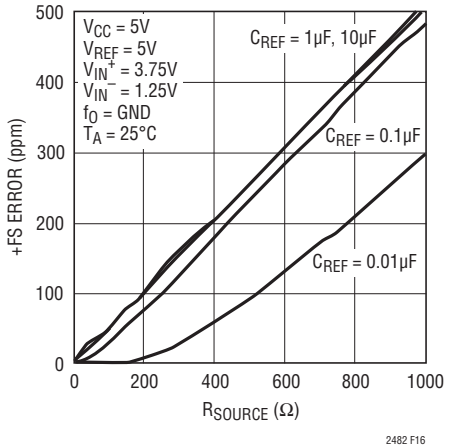

Figure 16. +FS Error vs R_{SOURCE} at V_{REF} (Large C_{REF})

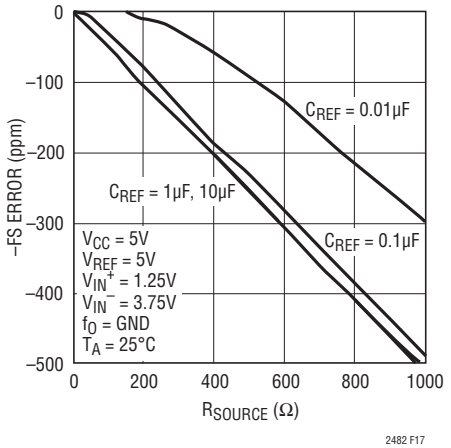

Figure 17. –FS Error vs R_{SOURCE} at V_{REF} (Large C_{REF})

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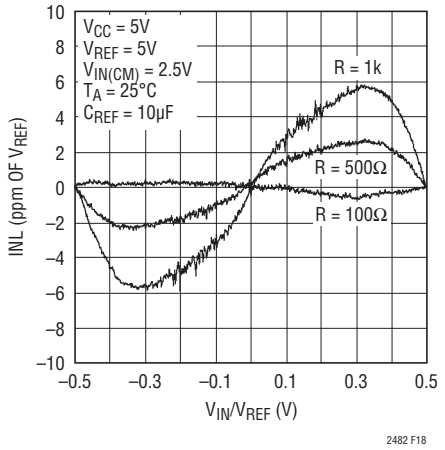

Figure 18. INL vs Differential Input Voltage and Reference Source Resistance for C_{REF} > 1µF

In applications where the reference and input common mode voltages are different, extra errors are introduced. For every 1V of the reference and input common mode voltage difference ($V_{REFCM} – V_{INCM}$) and a 5V reference, each Ohm of reference source resistance introduces an extra ($V_{REFCM} – V_{INCM}$)/($V_{REF} • R_{EQ}$) full-scale gain error which is 0.067ppm when using the internal oscillator (50Hz/60Hz rejection). If an external clock is used, the corresponding extra gain error is $0.22 • 10^{–6} • f_{EOSC}$ppm.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by V_{REF}^+ and GND, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

Output Data Rate

When using its internal oscillator, the LTC2482 produces 6.8ps with a notch frequency of 55Hz, for simultaneous 50Hz/60Hz rejection. The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock (f_O connected to an external oscillator), the LTC2482 output data rate can be increased as desired. The duration of the conversion phase is $41036/f_{EOSC}$.

An increase in f_{EOSC} over the nominal 307.2kHz will translate into a proportional increase in the maximum output data rate. The increase in output rate is nevertheless accompanied by three potential effects, which must be carefully considered.

First, a change in f_{EOSC} will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line frequency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2482's exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the IN^+ and $IN^–$ pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred through the input and the reference pins. If large external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of f_{EOSC}. If small external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the effect of the external source resistance upon the LTC2482 typical performance can be inferred from Figures 12, 13, 14 and 15 in which the horizontal axis is scaled by $307200/f_{EOSC}$.

Third, an increase in the frequency of the external oscillator above 1MHz (a more than 3× increase in the output data rate) will start to decrease the effectiveness of the internal autocalibration circuits. This will result in a progressive

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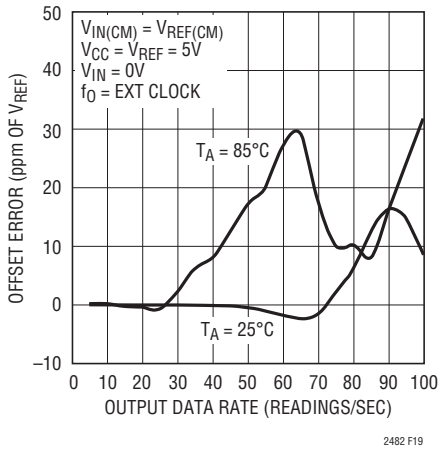

Figure 19. Offset Error vs Output Data Rate and Temperature

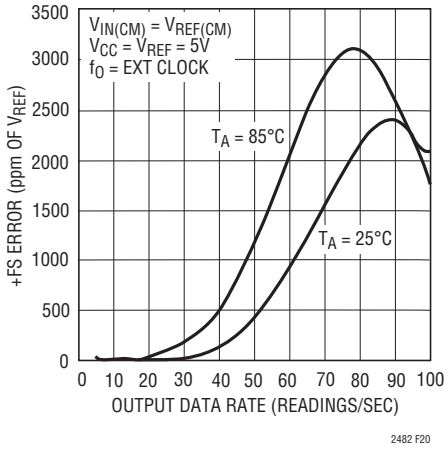

Figure 20. +FS Error vs Output Data Rate and Temperature

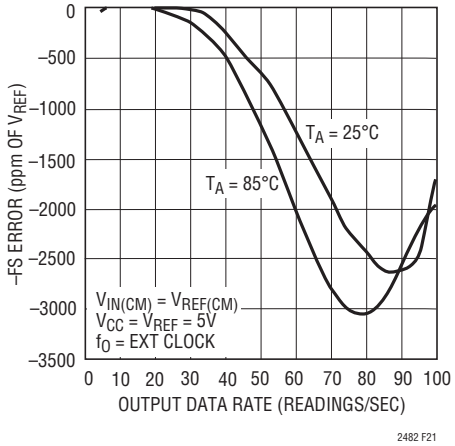

Figure 21. –FS Error vs Output Data Rate and Temperature

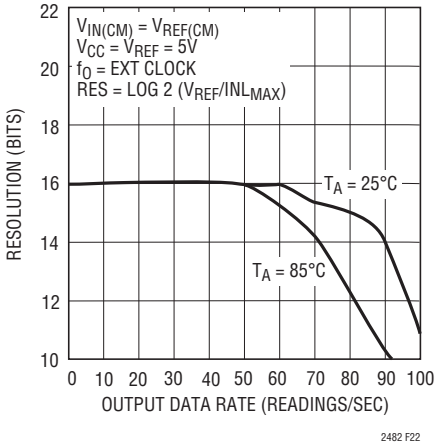

Figure 22. Resolution (INL_{MAX} ≤ 1LSB) vs Output Data Rate and Temperature

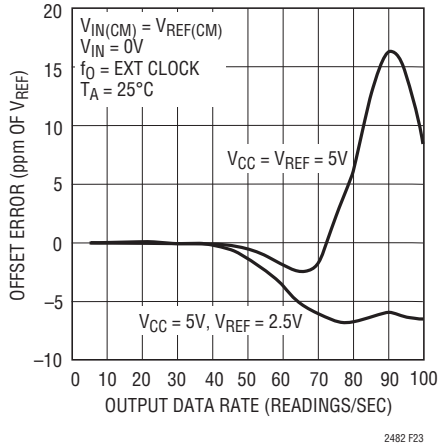

Figure 23. Offset Error vs Output Data Rate and Reference Voltage

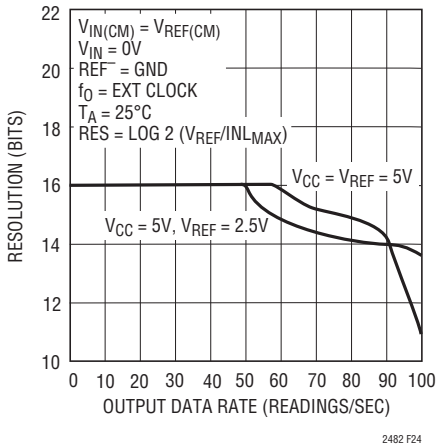

Figure 24. Resolution (INL_{MAX}) ≤ 2LSB vs Output Data Rate and Reference Voltage

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degradation in the converter accuracy and linearity. Typical measured performance curves for output data rates up to 100 readings per second are shown in Figures 19 to 24. In order to obtain the highest possible level of accuracy from this converter at output data rates above 20 readings per second, the user is advised to maximize the power supply voltage used and to limit the maximum ambient operating temperature. In certain circumstances, a reduction of the differential reference voltage may be beneficial.

Input Bandwidth

The combined effect of the internal SINC^4 digital filter and of the analog and digital autocalibration circuits determines the LTC2482 input bandwidth. When the internal oscillator is used the 3dB input bandwidth is 3.3Hz. If an external conversion clock generator of frequency f_{EOSC} is connected to the f_O pin, the 3dB input bandwidth is $10.7 \bullet 10^{-6} \bullet f_{EOSC}$.

Due to the complex filtering and calibration algorithms utilized, the converter input bandwidth is not modeled very accurately by a first order filter with the pole located at the 3dB frequency. When the internal oscillator is used, the shape of the LTC2482 input bandwidth is shown in Figure 25. When an external oscillator of frequency f_{EOSC} is used, the shape of the LTC2482 input bandwidth can be derived from Figure 25 in which the horizontal axis is scaled by $f_{EOSC}/307200$.

The conversion noise (600nV$_{RMS}$ typical for V_{REF} = 5V) can be modeled by a white noise source connected to a noise free converter. The noise spectral density is 47nV$\sqrt{Hz}$ for an infinite bandwidth source and 64nV$\sqrt{Hz}$ for a single 0.5MHz pole source. From these numbers, it is clear that particular attention must be given to the design of external amplification circuits. Such circuits face the simultaneous requirements of very low bandwidth (just a few Hz) in order to reduce the output referred noise and relatively high bandwidth (at least 500kHz) necessary to drive the input switched-capacitor network. A possible solution is a high gain, low bandwidth amplifier stage followed by a high bandwidth unity-gain buffer.

When external amplifiers are driving the LTC2482, the ADC input referred system noise calculation can be simplified by Figure 26. The noise of an amplifier driving the LTC2482 input pin can be modeled as a band limited white noise source. Its bandwidth can be approximated by the bandwidth of a single pole lowpass filter with a corner frequency f_i. The amplifier noise spectral density is n_i. From Figure 26, using f_i as the x-axis selector, we can find on the y-axis the noise equivalent bandwidth $freq_i$ of the input driving amplifier. This bandwidth includes the band limiting effects of the ADC internal calibration and filtering. The noise of the driving amplifier referred to the converter input and including all these effects can be calculated as $N = n_i \bullet \sqrt{freq_i}$. The total system noise

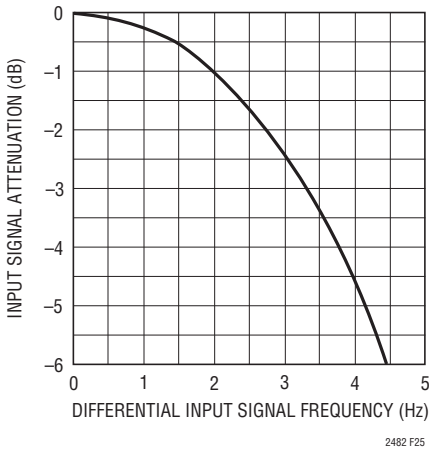

Figure 25. Input Signal Bandwidth Using the Internal Oscillator

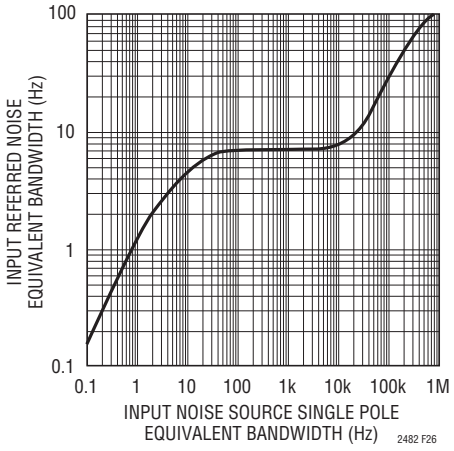

Figure 26. Input Referred Noise Equivalent Bandwidth of an Input Connected White Noise Source

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(referred to the LTC2482 input) can now be obtained by summing as square root of sum of squares the three ADC input referred noise sources: the LTC2482 internal noise, the noise of the IN+ driving amplifier and the noise of the IN– driving amplifier.

If the f_O pin is driven by an external oscillator of frequency f_{EOSC}, Figure 26 can still be used for noise calculation if the x-axis is scaled by $f_{EOSC}/307200$. For large values of the ratio $f_{EOSC}/307200$, the Figure 26 plot accuracy begins to decrease, but at the same time the LTC2482 noise floor rises and the noise contribution of the driving amplifiers lose significance.

Normal Mode Rejection and Antialiasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2482 significantly simplifies antialiasing filter requirements. Additionally, the input current cancellation feature of the LTC2482 allows external lowpass filtering without degrading the DC performance of the device.

The SINC^4 digital filter provides greater than 120dB normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency (f_S). The LTC2482's autocalibration circuits further simplify the antialiasing requirements by additional normal mode signal filtering both in the analog and digital domain. Independent of the operating mode, $f_S = 256 \cdot f_N = 2048 \cdot f_{OUTMAX}$ where f_N is the notch frequency and f_{OUTMAX} is the maximum output data rate. In the internal oscillator mode with 50Hz/60Hz rejection, f_S = 13960Hz. In the external oscillator mode, $f_S = f_{EOSC}/20$.

The regions of low rejection occurring at integer multiples of f_S have a very narrow bandwidth. Magnified details of the normal mode rejection curves are shown in Figure 27 (rejection near DC) and Figure 28 (rejection at $f_S = 256f_N$) where f_N represents the notch frequency. These curves have been derived for the external oscillator mode but they can be used in all operating modes by appropriately selecting the f_N value.

The user can expect to achieve this level of performance using the internal oscillator as it is demonstrated by Figure 29. Typical measured values of the normal mode rejection of the LTC2482 operating with an internal oscillator (50Hz/60Hz rejection) is shown in Figure 29.

As a result of these remarkable normal mode specifications, minimal (if any) antialias filtering is required in front of the LTC2482. If passive RC components are placed in front of the LTC2482, the input dynamic current should be considered (see Input Current section). In this case, the differential input current cancellation feature of the LTC2482 allows external RC networks without significant degradation in DC performance.

Traditional high order delta-sigma modulators, while providing very good linearity and resolution, suffer from potential instabilities at large input signal levels. The proprietary architecture used for the LTC2482 third

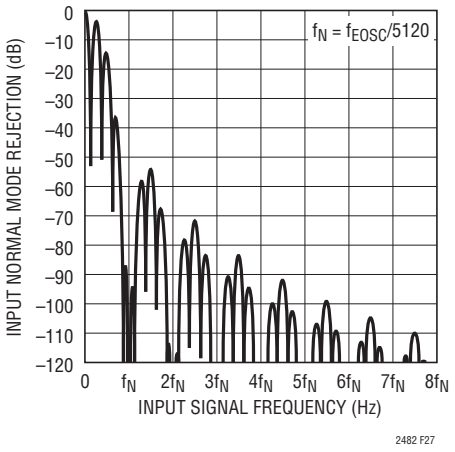

Figure 27. Input Normal Mode Rejection at DC

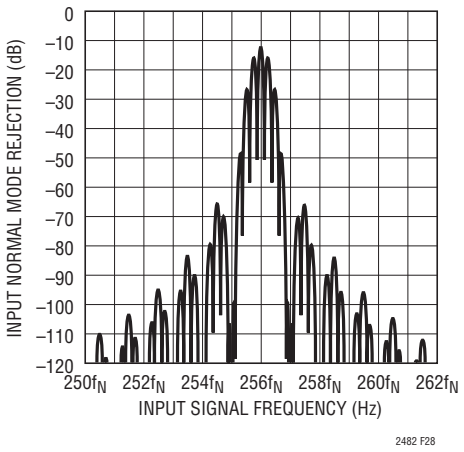

Figure 28. Input Normal Mode Rejection at $f_S = 256f_N$

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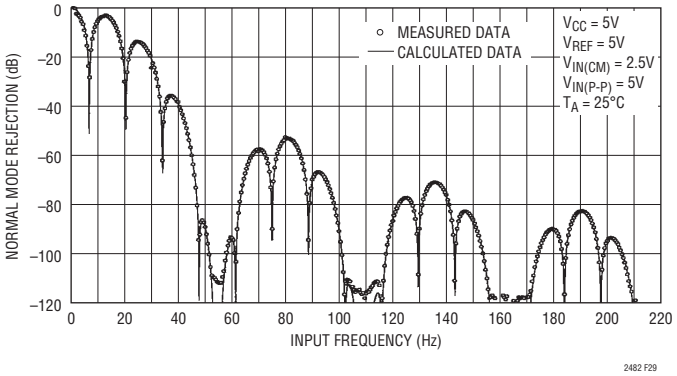


Figure 29. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full Scale

order modulator resolves this problem and guarantees a predictable stable behavior at input signal levels of up to 150% of full scale. In many industrial applications, it is not uncommon to have to measure microvolt level signals superimposed over volt level perturbations and the LTC2482 is eminently suited for such tasks. When the perturbation is differential, the specification of interest is the normal mode rejection for large input signal levels. With a reference voltage V_{REF} = 5V, the LTC2482 has a full-scale differential input range of 5V peak-to-peak.

Remote Sensing with Easy Drive Input Current Cancellation

One problem faced by designers of high performance data acquisition systems is achieving data sheet specified performance in a real world environment. One advantage delta sigma type ADCs offer over the alternatives is on-chip digital filtering (noise suppression). The disadvantage (solved by Easy Drive technology) is the drive requirements inherent in delta sigma ADC architectures. In order to demonstrate the full potential of the Easy Drive technology, a practical test case was characterized (see Figure 30).

Precise measurements of offset, noise and linearity were measured under extreme test conditions. A remote sensor was digitized through 100 meters of cable applied to an RC network with low accuracy 1% resistors. A remote sensor voltage was swept from 0 to 2.5 with less than 1LSB linearity error (see Figure 31). Noise levels of 650nV RMS and offsets below 5µV were measured (see Figure 32).

Fundamentally, an oversampled data converter (ΔΣ ADC) directly connected to a long cable and a low precision RC network leads to many problems greatly limiting the accuracy of the system. These include transmission line effects, noise and DC settling errors.

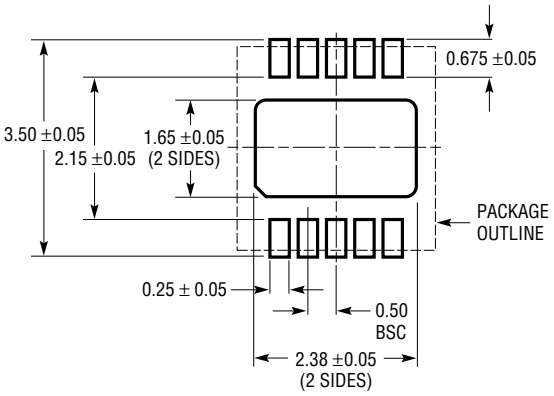
The sampling network of ΔΣ ADCs injects high frequency current spikes into the cable. The resulting voltage spikes are reflected through the long wire and result in excessive noise and reduced accuracy. This problem is solved by placing a bypass capacitor across the input to the ADC. This capacitor serves as a charge reservoir for the ADC's sampling network and reduces the voltage spikes by the ratio of internal sampling capacitor to external bypass capacitor. A 1µF bypass capacitor reduces the voltage spikes generated by the sampling network by a factor of 50,000 (1V spikes are reduced to 18µV) and is sufficient to achieve data sheet specified noise and accuracy.

The addition the large external bypass capacitor results in input settling errors. Typical 24-bit high resolution delta sigma ADCs sample at time intervals on the order of 10µs. In order to fully settle with a 1µF bypass capacitor, the source impedance must be lower than 1Ω. Source impedances greater than 1Ω result in offset and full-scale errors due to the accumulation of charge settling errors over the complete conversion cycle. Easy Drive technology automatically removes the differential component of this error. The remaining common mode error is reduced to a fixed offset as a function of the external resistor matching seen at the plus and minus input of the ADC. In this extreme case, 1k external resistors with 1% matching result in a 3.5µV offset while the linearity and noise are unaffected.

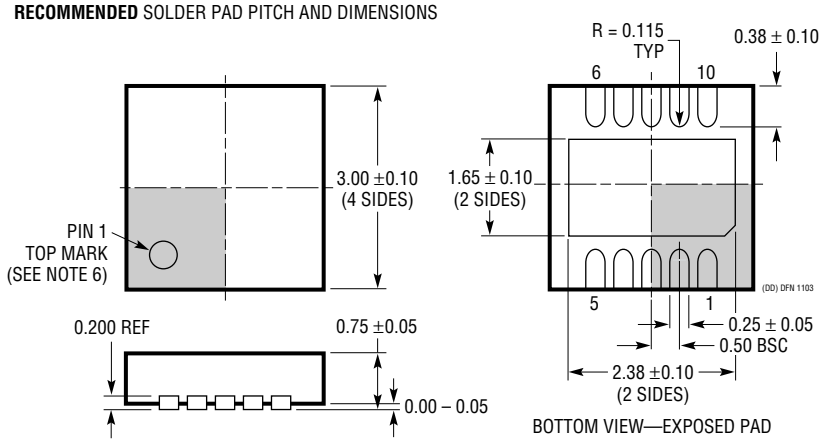
The signal path contains a 100 meter wire connected to a low voltage source in a very noisy environment. Line frequency noise is rejected by the on-chip digital filter and guaranteed by the high accuracy on-chip oscillator. High frequency noise is rejected by the external lowpass filter formed by the input bypass capacitor and external resistors.

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	7/10	Revised Typical Application drawing	1, 32
		Added Note 16	4, 5