Photoflash Chargers with Adjustable Input Current and IGBT Drivers

FEATURES

- **Adjustable Input Current**
- **Integrated IGBT Driver**
- **No Output Voltage Divider Needed**
- Uses Small Transformers: 5.8mm × 5.8mm × 3mm
- Fast Photoflash Charge Times
- Charges Any Size Photoflash Capacitor
- Supports Operation from Single Li-Ion Cell, Two AA Cells or any Supply from 1.5V Up to 16V
- Small 10-Lead (3mm × 2mm) DFN Package

Fast Charge Time

VERSION	INPUT CURRENT (mA)	NORMAL MODE CHARGE TIME (Sec)	REDUCED MODE CHARGE TIME (Sec)
LT3585-3	800/400	3.3	6.6
LT3585-0	550/275	4.6	9.2
LT3585-2	400/200	5.8	12.6
LT3585-1*	250/115	5.0	14.6

100µF capacitor, 320V, $V_{IN} = V_{BAT} = 3.6V$
*50µF capacitor, 320V, $V_{IN} = V_{BAT} = 3.6V$

APPLICATIONS

- Digital/Film Camera Flash
- PDA/Cell Phone Flash
- Emergency Strobe

DESCRIPTION

The LT®3585 series are highly integrated ICs designed to charge photoflash capacitors in digital and film cameras. A new control technique allows for the use of extremely small transformers. Each part contains an on-chip high voltage NPN power switch. Output voltage detection is completely contained within the part, eliminating the need for any discrete zener diodes or resistors. The output voltage can be adjusted by simply changing the turns ratio of the transformer.

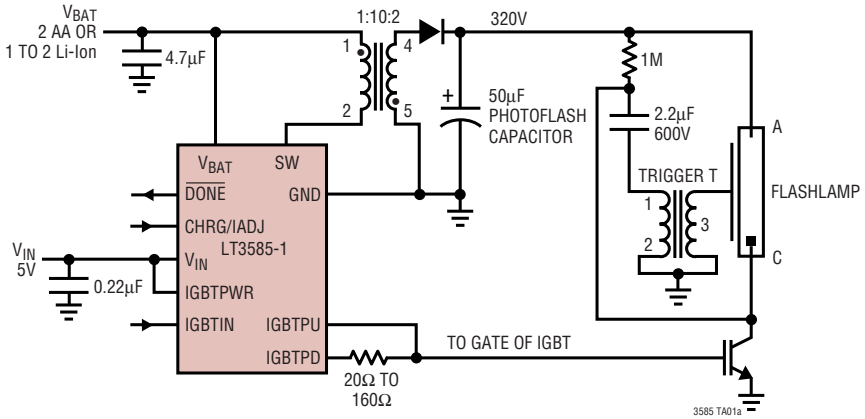
The CHRG/IADJ pin gives full control of the part to the user. Driving CHRG/IADJ low puts the part in low power shutdown. The CHRG/IADJ pin can also be used to reduce the input current of the charger, useful in extending battery life. The DONE pin indicates when the part has completed charging.

The LT3585 series of parts are housed in tiny 3mm × 2mm DFN packages.

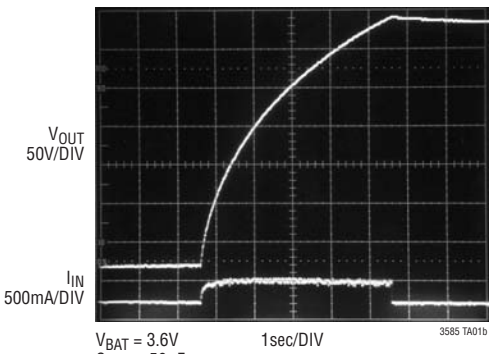
TYPICAL APPLICATION

LT3585-1 Photoflash Charger Uses High Efficiency 2mm Tall Transformers with Tunable IGBT Gate Drive

DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



LT3585-1 Charging Waveform Normal Input Current Mode

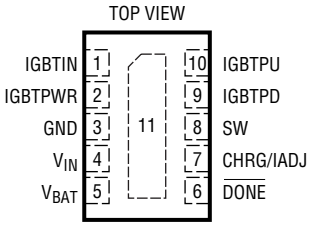


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 16V
V_{BATT} Voltage 16V
SW Voltage 60V
SW Pin Negative Current ..... –1A
CHRG/IADJ Voltage 10V
IGBTPWR Voltage 10V
IGBTIN Voltage 10V
IGBTPU Voltage 10V
IGBTPD Voltage 10V
$\overline{DONE}$ Voltage 10V
Current Into $\overline{DONE}$ Pin 0.2mA/–1mA
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) ... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DDB PART MARKING
LT3585EDDB-0	LCLK
LT3585EDDB-1	LCLJ
LT3585EDDB-2	LCLH
LT3585EDDB-3	LCFX

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{BAT} = V_{CHRG} = 3V unless otherwise noted (Note 2). Specifications are for the LT3585-0, LT3585-1, LT3585-2, LT3585-3 unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current	V_{CHRG} = 3V, Not Switching V_{CHRG} = 0V, In Shutdown			5 0	8 1	mA µA
V_{IN} Voltage Range		●	2.5		16	V
V_{BAT} Voltage Range		●	1.5		16	V
Switch Current Limit	LT3585-3 (Note 3) LT3585-0 (Note 3) LT3585-2 (Note 3) LT3585-1 (Note 3)		1.55 1.1 0.75 0.45	1.7 1.2 0.85 0.55	1.85 1.3 0.95 0.65	A A A A
Switch V_{CESAT}	LT3585-3, I_{SW} = 1.4A LT3585-0, I_{SW} = 1A LT3585-2, I_{SW} = 700mA LT3585-1, I_{SW} = 400mA			485 330 230 140		mV mV mV mV
V_{OUT} Comparator Trip Voltage	Measured as $V_{SW} – V_{BAT}$	 ●	31 30.5	31.5 31.5	32 32.5	V V
V_{OUT} Comparator Overdrive	300ns Pulse Width			200	400	mV
DCM Comparator Trip Voltage	Measured as $V_{SW} – V_{BAT}$		80	130	180	mV
CHRG/IADJ Pin Current	V_{CHRG} = 3V V_{CHRG} = 0V			45 0	70 0.1	µA µA
Switch Leakage Current	V_{BAT} = V_{SW} = 5V, In Shutdown	●		0.01	1	µA
CHRG/IADJ Minimum Enable Voltage		●	1.1			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{BAT} = V_{CHRG} = 3V unless otherwise noted (Note 2). Specifications are for the LT3585-0, LT3585-1, LT3585-2, LT3585-3 unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CHRG/IADJ Three-State Voltage for Reduced Input Current	CHRG/IADJ > 1.1V then Float		1.1	1.28	1.4	V
CHRG/IADJ Voltage Range for Normal Input Current		●	1.6		10	V
CHRG/IADJ Low Voltage		●			0.3	V
Delay Time for Reduced Input Current Mode	CHRG/IADJ Pin Three Stated: V_{BAT} = 4.2V, Fresh Li-Ion Cell V_{BAT} = 2.8V, Dead Li-Ion Cell V_{BAT} = 3V, Fresh 2 AA Cells V_{BAT} = 2V, Dead 2 AA Cells			 5.2 7.2 6.8 9.5		 µs µs µs µs
Minimum CHRG/IADJ Pin Low Time	High→Low→High			20		µs
$\overline{DONE}$ Output Signal High	100kΩ from V_{IN} to $\overline{DONE}$			3		V
$\overline{DONE}$ Output Signal Low	33µA into $\overline{DONE}$ Pin			120	200	mV
$\overline{DONE}$ Leakage Current	$V_{\overline{DONE}}$ = 3V, $\overline{DONE}$ NPN Off			1	100	nA
IGBTPWR Voltage Range		●	2.5		10	V
IGBT Input High Level		●	1.5			V
IGBT Input Low Level		●			0.5	V
IGBT Output Rise Time	IGBTPU Pin, C_{OUT} = 4000pF, IGBTPWR = 5V, IGBTIN = 0V→1.5V, 10%→90%			0.4		µs
IGBT Output Fall Time	IGBTPD Pin, C_{OUT} = 4000pF, IGBTPWR = 5V, IGBTIN = 1.5V→0V, 90%→10%			0.13		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Ratings are for DC levels only.

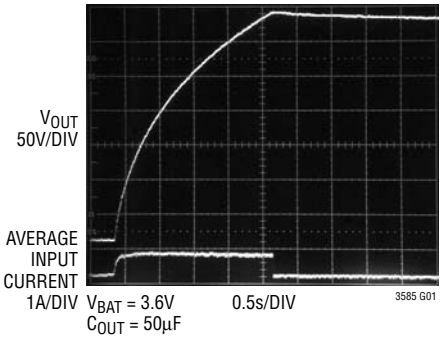
Note 2: The LT3585 series is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current limit is guaranteed by design and/or correlation to static test.

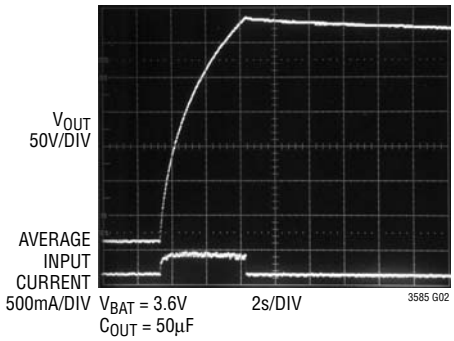
TYPICAL PERFORMANCE CHARACTERISTICS

LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

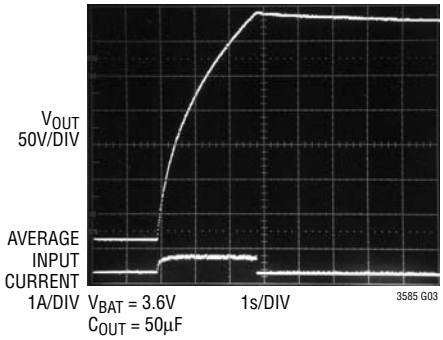
LT3585-0 Charging Waveform Normal Input Current Mode



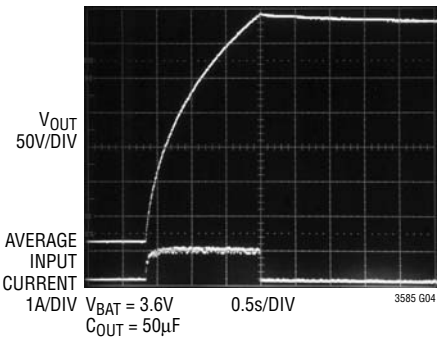
LT3585-1 Charging Waveform Normal Input Current Mode



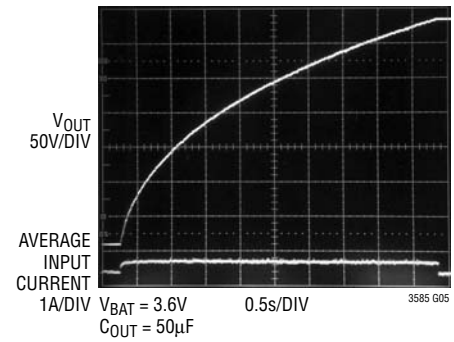
LT3585-2 Charging Waveform Normal Input Current Mode



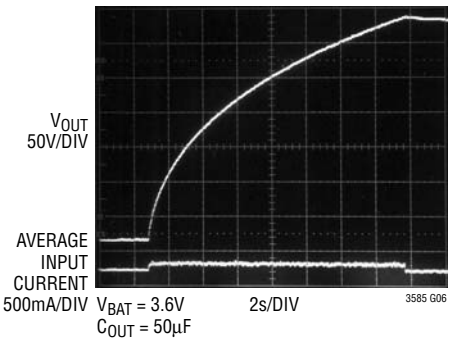
LT3585-3 Charging Waveform Normal Input Current Mode



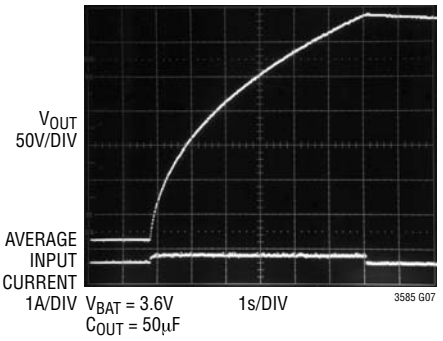
LT3585-0 Charging Waveform Reduced Input Current Mode



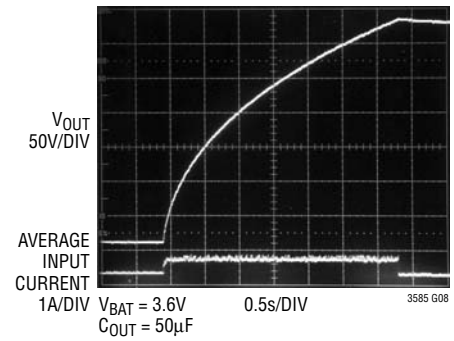
LT3585-1 Charging Waveform Reduced Input Current Mode



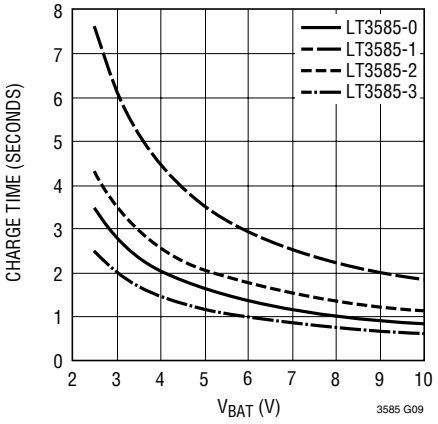
LT3585-2 Charging Waveform Reduced Input Current Mode



LT3585-3 Charging Waveform Reduced Input Current Mode



Charge Time* Normal Input Current Mode

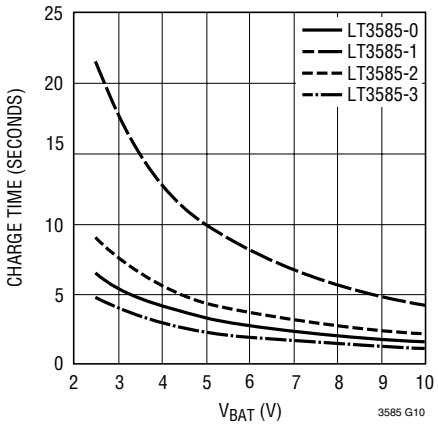


*USING RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)

TYPICAL PERFORMANCE CHARACTERISTICS

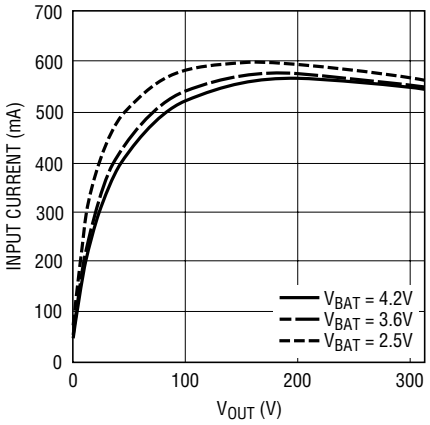
LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

Charge Time*
Reduced Input Current Mode

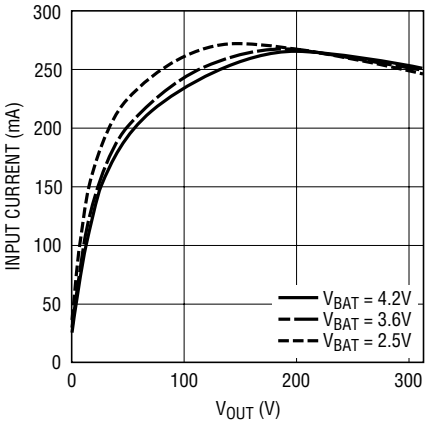


*USING RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)

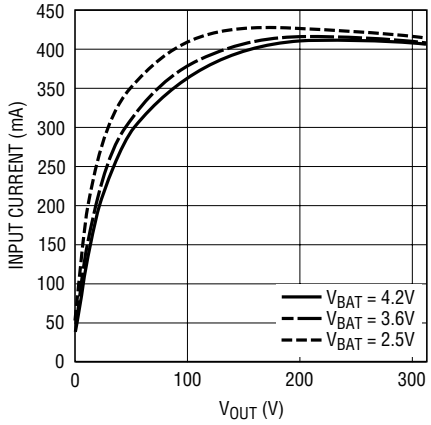
LT3585-0 Input Current
Normal Input Current Mode



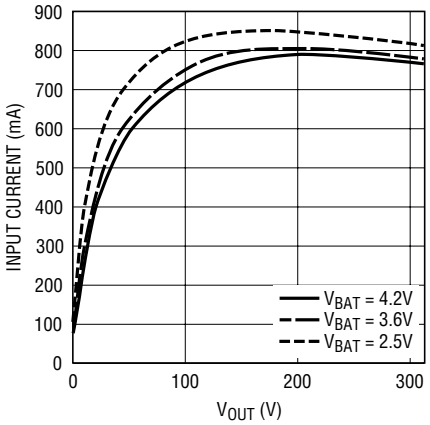
LT3585-1 Input Current
Normal Input Current Mode



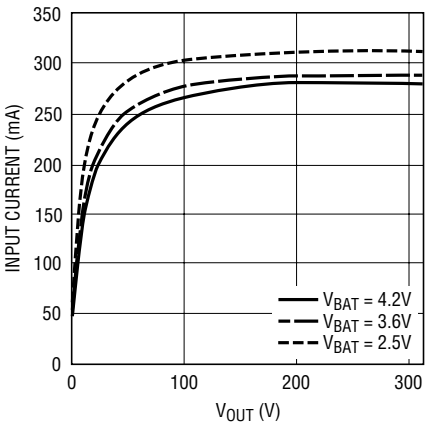
LT3585-2 Input Current
Normal Input Current Mode



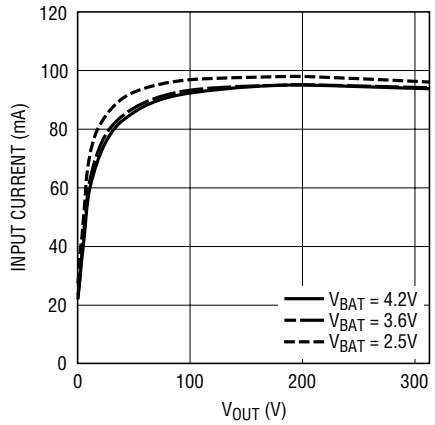
LT3585-3 Input Current
Normal Input Current Mode



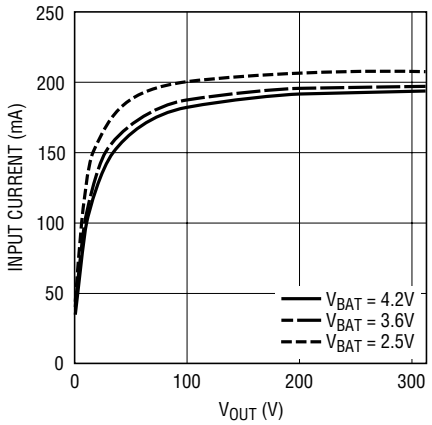
LT3585-0 Input Current
Reduced Input Current Mode



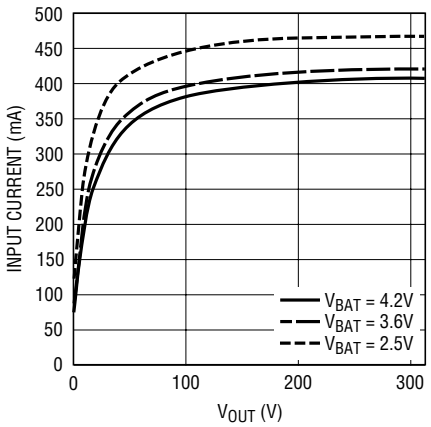
LT3585-1 Input Current
Reduced Input Current Mode



LT3585-2 Input Current
Reduced Input Current Mode



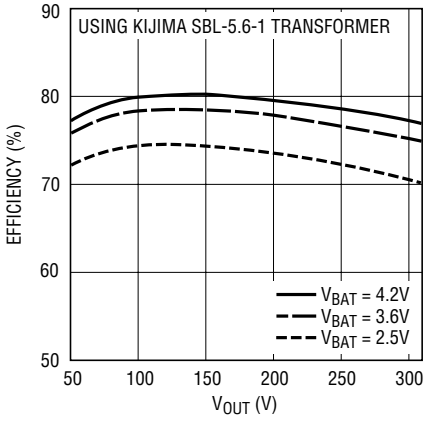
LT3585-3 Input Current
Reduced Input Current Mode



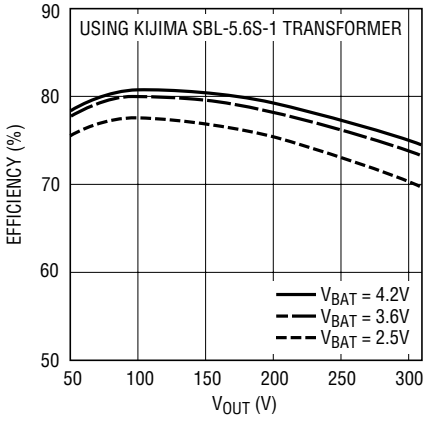
TYPICAL PERFORMANCE CHARACTERISTICS

LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

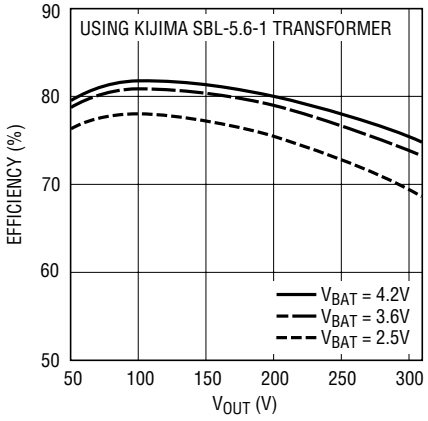
LT3585-0 Efficiency
Normal Input Current Mode



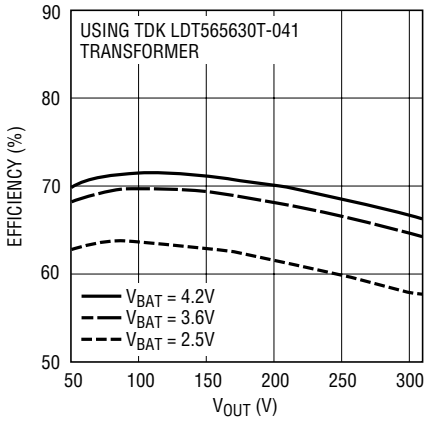
LT3585-1 Efficiency
Normal Input Current Mode



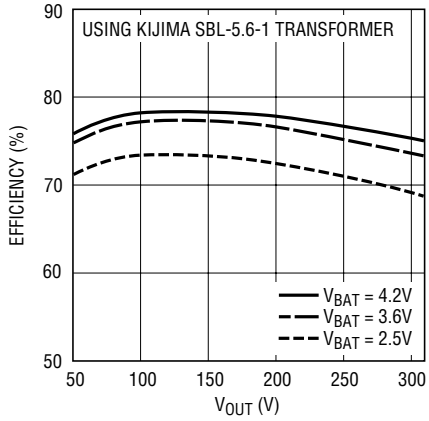
LT3585-2 Efficiency
Normal Input Current Mode



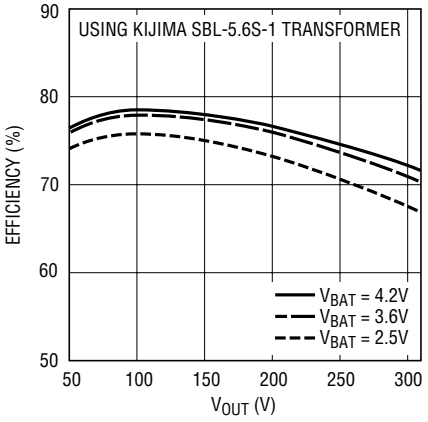
LT3585-3 Efficiency
Normal Input Current Mode



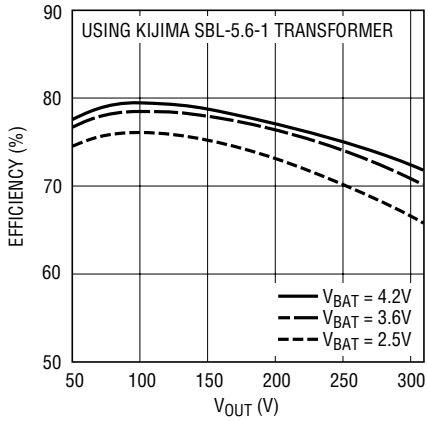
LT3585-0 Efficiency
Reduced Input Current Mode



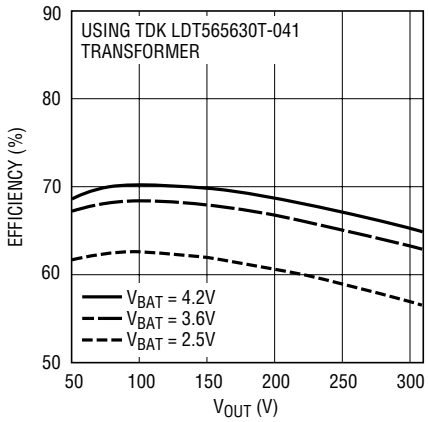
LT3585-1 Efficiency
Reduced Input Current Mode



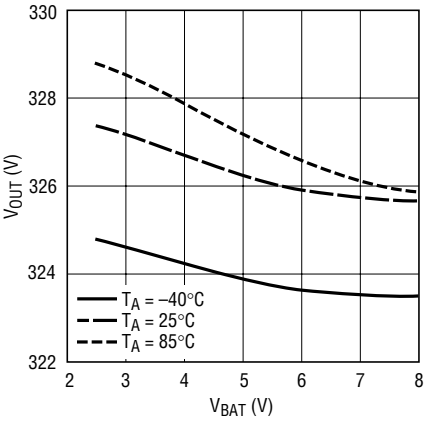
LT3585-2 Efficiency
Reduced Input Current Mode



LT3585-3 Efficiency
Reduced Input Current Mode



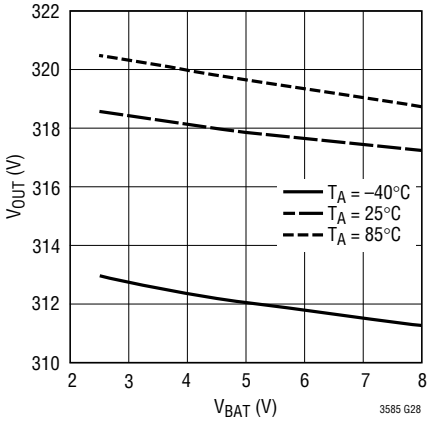
LT3585-0 Output Voltage



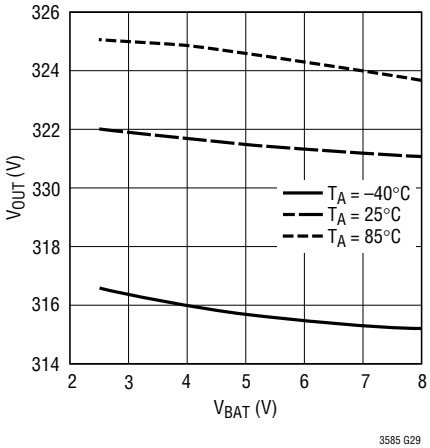
TYPICAL PERFORMANCE CHARACTERISTICS

LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

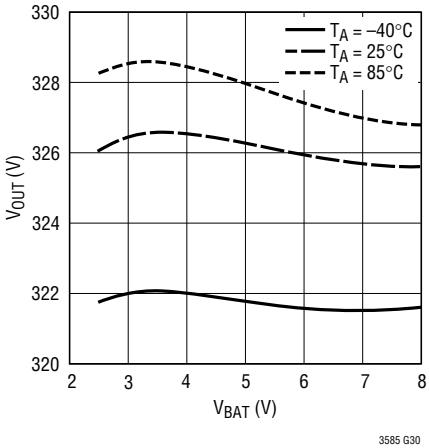
LT3585-1 Output Voltage



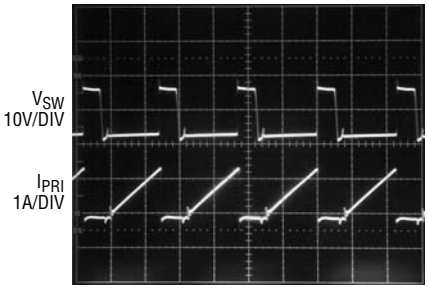
LT3585-2 Output Voltage



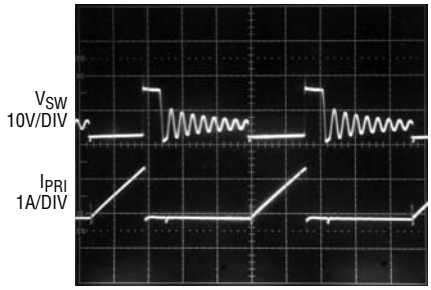
LT3585-3 Output Voltage



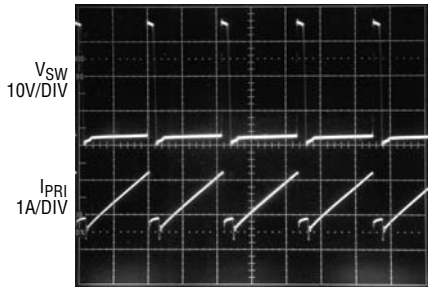
LT3585-0 Switch Waveform Normal Input Current Mode



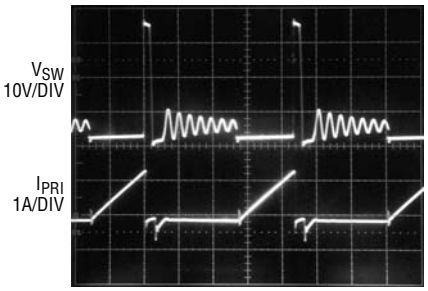
LT3585-0 Switch Waveform Reduced Input Current Mode



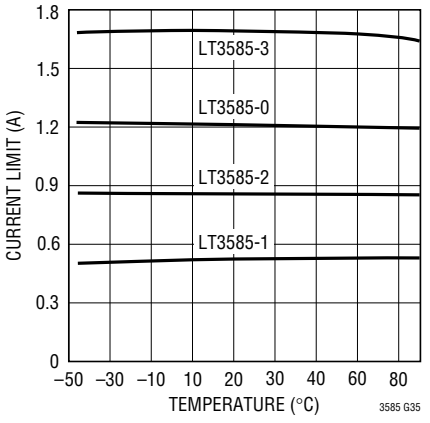
LT3585-0 Switch Waveform Normal Input Current Mode



LT3585-0 Switch Waveform Reduced Input Current Mode

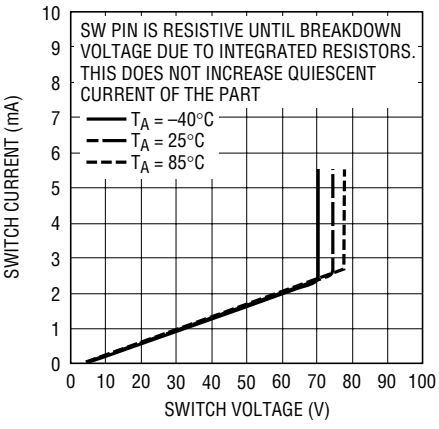


Switch DC Current Limit*



*DYNAMIC CURRENT LIMIT IS HIGHER THAN DC CURRENT LIMIT

LT3585-0/LT3585-1/LT3585-2/ LT3585-3 Switch Breakdown Voltage



PIN FUNCTIONS

IGBTIN (Pin 1): Logic Input for the IGBT Driver. When this pin is driven higher than 1.5V, the output goes high. When the pin is below 0.5V, the output will go low.

IGBTPWR (Pin 2): Supply Pin for the IGBT Driver. Must be locally bypassed with a good quality ceramic capacitor. The minimum operating voltage for the IGBT driver is 2.5V.

GND (Pin 3): Ground. Tie directly to local ground plane.

V_{IN} (Pin 4): Input Supply Pin. Must be locally bypassed with a good quality ceramic capacitor. The minimum operating voltage for V_{IN} is 2.5V.

V_{BAT} (Pin 5): Battery Supply Pin. Must be locally bypassed with a good quality ceramic capacitor. The minimum operating voltage for V_{BAT} is 1.5V.

$\overline{DONE}$ (Pin 6): Open NPN Collector Indication Pin. When target output voltage is reached, NPN turns on. This pin needs a proper pull-up resistor or current source.

CHRG/IADJ (Pin 7): Charge and Input Current Adjust Pin. A low (<0.3V) to high (>1.1V) transition on this pin puts the part into power delivery mode. Once the target output voltage is reached, the part will stop charging the output. Toggle this pin to start charging again. Ground to shut down. To enter into the input current reduction mode, the voltage on this pin should be driven high (>1.1V) and then floated. (For more information refer to the Operation section of this data sheet.) To enter normal mode, the voltage should be driven higher than 1.6V.

SW (Pin 8): Switch Pin. This is the collector of the internal NPN Power switch. Minimize the metal trace area connected to this pin to minimize EMI. Tie one side of the primary of the transformer to this pin. The target output voltage is set by the turns ratio of the transformer.

Choose turns ratio N by the following equation:

$$N = \frac{V_{OUT} + 2}{31.5}$$

where V_{OUT} is the desired output voltage.

IGBTPD (Pin 9): Pull-down Output for IGBT Gate. Connect this pin to the IGBT Gate. Add a series resistor to increase the turn-off time to protect the IGBT.

IGBTPU (Pin 10): Pull-up Output for IGBT Gate. Connect this pin to the gate of the IGBT.

Exposed Pad (Pin 11): Ground. Tie directly to local ground plane.

SIMPLIFIED BLOCK DIAGRAM

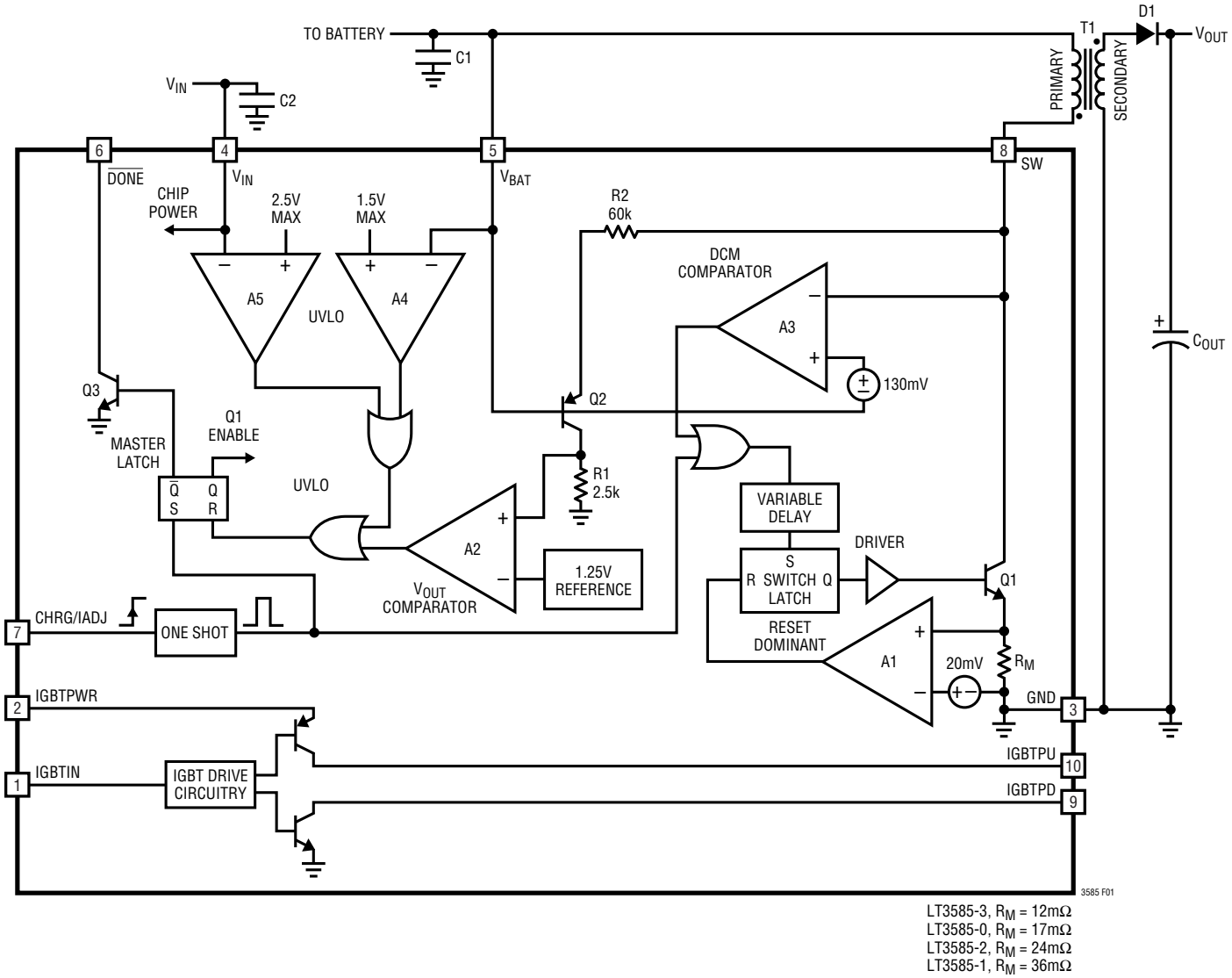


Figure 1

OPERATION

The LT3585 series of parts operate on the edge of discontinuous conduction mode. When CHRG/IADJ is driven higher than 1.1V, the master latch is set. This enables the part to deliver power to the photoflash capacitor. When the power switch, Q1, is turned on, current builds up in the primary of the transformer. When the desired current level is reached, the output of comparator A1 goes high, resetting the switch latch that controls the state of Q1, and the output of the DCM comparator goes low. Q1 now turns off and the flyback waveform on the SW node quickly rises to a level proportional to V_{OUT}. The secondary current flows through high voltage diode(s), D1, and into the photoflash capacitor. When the secondary current decays to zero, the voltage on the SW node collapses. When this voltage reaches 130mV higher than V_{BAT}, the output of A3 goes high. This sets the switch latch and the power switch, Q1, turns back on. This cycle repeats until the target V_{OUT} level is reached. When the target V_{OUT} is reached, the master latch resets and the $\overline{DONE}$ pin goes low.

The input current of an LT3585 series circuit can be reduced by changing the voltage of the CHRG/IADJ pin. When this pin is between 1.1V and 1.4V, a time delay is added between when A3 goes high and the switch latch is set, see Figure 2. If the part is enabled, and the CHRG/IADJ pin is floated, internal circuitry drives the voltage on the pin to 1.28V. This allows a single I/O port pin, which can be three-stated, to enable or disable the part as well as place the part into the input current reduction mode. This feature effectively reduces the average input current into the flyback transformer. The magnitude of the delay decreases with increasing V_{BAT}. This causes the reduced average input current to remain relatively flat with changes in V_{BAT}. When CHRG/IADJ is brought higher than 1.6V, no delay is added. The CHRG/IADJ pin functionality is shown in Figure 3.

Both V_{BAT} and V_{IN} have undervoltage lockout (UVLO). When one of these pins goes below its UVLO voltage, the $\overline{DONE}$ pin goes low. With an insufficient bypass capacitor on V_{BAT} or V_{IN}, the ripple on the pin is likely to activate UVLO and terminate the charge. The applications circuits in the data sheet suggest values adequate for most applications.

The LT3585 series also includes an integrated IGBT driver. There are two output pins, IGBTPU and IGBTPD. The IGBTPU pin is used to pull the gate of the IGBT up. This should be done quickly to guarantee proper Xenon lamp ignition. Tie this pin directly to the gate of the IGBT. The IGBTPD pin is pinned out separately to allow for greater flexibility in choosing a series resistor between the pin and the gate of the IGBT. This resistor can be used to slow down the turn off of the IGBT.

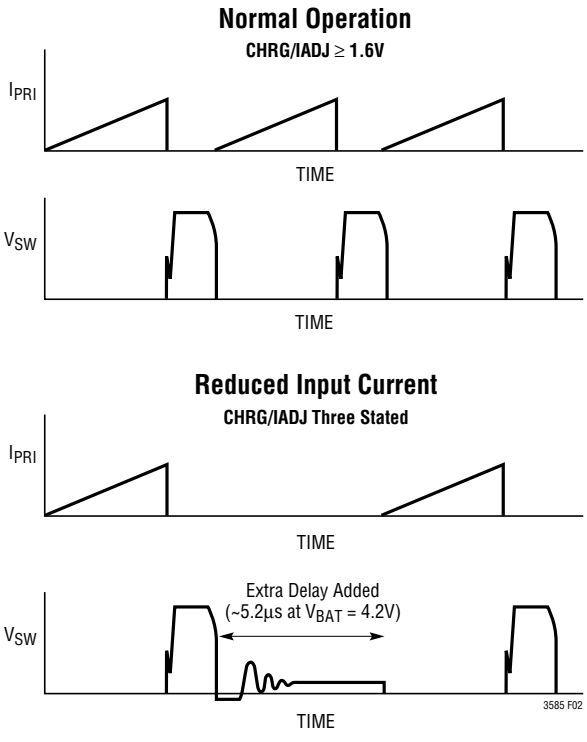


Figure 2. Normal and Reduced Input Current Waveforms

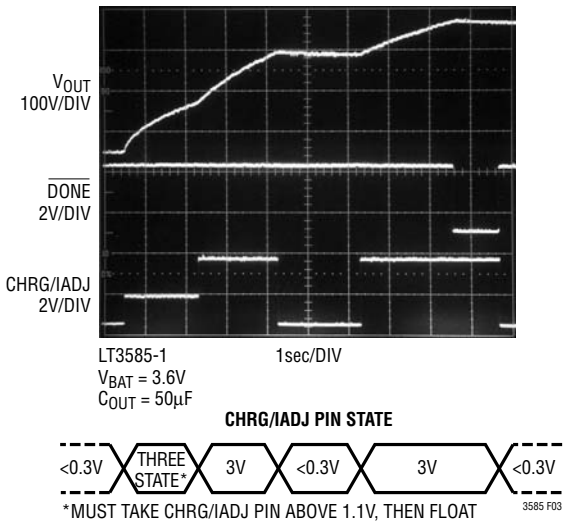


Figure 3. Basic Operation

APPLICATIONS INFORMATION

Choosing the Right Device (LT3585-0/LT3585-1/LT3585-2/LT3585-3)

The only difference between the four versions of the LT3585 series is the peak current level. For the fastest possible charge time, use the LT3585-3. The LT3585-1 has the lowest peak current capability, and is designed for applications that need a more limited drain on the batteries. Due to the lower peak current, the LT3585-1 can use a physically smaller transformer. The LT3585-0 and LT3585-2 have a current limit in between that of the LT3585-1 and the LT3585-3.

Transformer Design

The flyback transformer is a key element for any LT3585-0/LT3585-1/LT3585-2/LT3585-3 design. It must be designed carefully and checked that it does not cause excessive current or voltage on any pin of the part. The main parameters that need to be designed are shown in Table 1. The first transformer parameter that needs to be set is the turns ratio, N. The LT3585-0/LT3585-1/LT3585-2/LT3585-3 accomplish output voltage detection by monitoring the flyback waveform on the SW pin. When the SW voltage reaches 31.5V higher than the V_{BAT} voltage, the part halts power delivery. Thus, the choice of N sets the target output voltage and changes the amplitude gain of the reflected voltage from the output to the SW pin. Choose N according to the following equation:

$$N = \frac{V_{OUT} + 2}{31.5}$$

where V_{OUT} is the desired output voltage. The number 2 in the numerator is used to include the forward voltage drop across the output diode(s). Thus, for a 320V output, N should be 322/31.5 or 10.2. For a 300V output, choose N equal to 302/31.5 or 9.6. The next parameter that needs to be set is the primary inductance, L_{PRI}. Choose L_{PRI} according to the following formula:

$$L_{PRI} \geq \frac{V_{OUT} \bullet 200 \bullet 10^{-9}}{N \bullet I_{PK}}$$

where V_{OUT} is the desired output voltage. N is the transformer turns ratio. I_{PK} is 1.4 (LT3585-0), 0.7 (LT3585-1), 1 (LT3585-2) and 2 (LT3585-3). L_{PRI} needs to be equal or larger than this value to ensure that the LT3585 series has adequate time to respond to the flyback waveform. All other parameters need to meet or exceed the recommended limits as shown in Table 1. A particularly important parameter is the leakage inductance, L_{LEAK}. When the power switch of the LT3585 series turns off, the leakage inductance on the primary of the transformer causes a voltage spike to occur on the SW pin. **The height of this spike must not exceed 50V**, even though the absolute maximum rating of the SW pin is 60V. The 60V absolute maximum rating is a DC blocking voltage specification, which assumes that the current in the power NPN is zero. Figure 4 shows the SW voltage waveform for the circuit of Figure 8 (LT3585-0). Note that the absolute maximum rating of the SW pin is not exceeded. Make sure to check the SW voltage waveform with V_{OUT} near the target output voltage, as this is the worst-case condition for SW voltage. Figure 5 shows the various limits on the SW voltage during switch turn off.

Table 1. Recommended Transformer Parameters

PARAMETER	NAME	TYPICAL RANGE LT3585-0	TYPICAL RANGE LT3585-1	TYPICAL RANGE LT3585-2	TYPICAL RANGE LT3585-3	UNITS
L_{PRI}	Primary Inductance	>5	>10	>7	>3.5	µH
L_{LEAK}	Primary Leakage Inductance	100 to 300	200 to 500	200 to 500	100 to 300	nH
N	Secondary/Primary Turns Ratio	8 to 12	8 to 12	8 to 12	8 to 12	
V_{ISO}	Secondary to Primary Isolation Voltage	>500	>500	>500	>500	V
I_{SAT}	Primary Saturation Current	>1.6	>0.8	>1.0	>2	A
R_{PRI}	Primary Winding Resistance	<300	<500	<400	<200	mΩ
R_{SEC}	Secondary Winding Resistance	<40	<80	<60	<30	Ω

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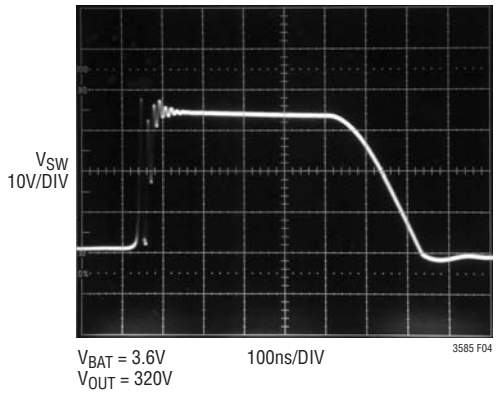

Figure 4. LT3585 SW Voltage Waveform

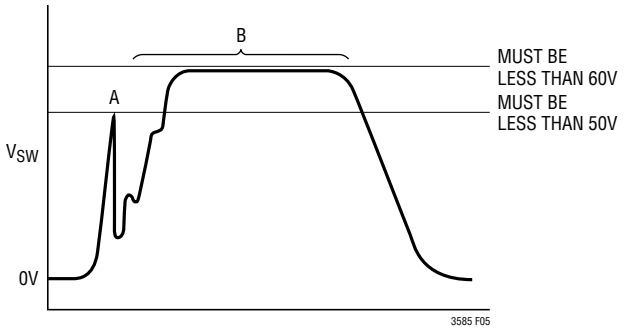

Figure 5. New Transformer Design Check

It is important not to minimize the leakage inductance to a very low level. Although this would result in a very low leakage spike on the SW pin, the parasitic capacitance of the transformer would become large. This will adversely affect the charge time of the photoflash circuit. Linear Technology has worked with several leading magnetic component manufacturers to produce predesigned flyback transformers for use with the LT3585-0 /LT3585-1/LT3585-2/LT3585-3. Table 2 shows the details of several of these transformers.

Output Diode Selection

The rectifying diode(s) should be low capacitance type with sufficient reverse voltage and forward current ratings. The peak reverse voltage that the diode(s) will see is approximately:

$$V_{PK(R)} = V_{OUT} + (N \bullet V_{BAT})$$

The peak current of the diode is simply:

$$I_{PK(SEC)} = \frac{2}{N} \quad (LT3585\text{-}3)$$

$$I_{PK(SEC)} = \frac{1.4}{N} \quad (LT3585\text{-}0)$$

$$I_{PK(SEC)} = \frac{1}{N} \quad (LT3585\text{-}2)$$

$$I_{PK(SEC)} = \frac{0.7}{N} \quad (LT3585\text{-}1)$$

For the circuit of Figure 8 with V_{BAT} of 5V, $V_{PK(R)}$ is 371V and $I_{PK(SEC)}$ is 137mA. The GSD2004S dual silicon diode is recommended for most applications. Table 3 shows the various diodes and relevant specifications. Use the appropriate number of diodes to achieve the necessary reverse breakdown voltage.

Capacitor Selection

For the input bypass capacitors, high quality X5R or X7R types should be used. Make sure the voltage capability of the part is adequate.

Table 2. Predesigned Transformers—Typical Specifications Unless Otherwise Noted

FOR USE WITH	TRANSFORMER DESIGNATION	SIZE (W × L × H) (mm)	LPRI (µH)	LPRI LEAKAGE (nH)	N	R_{PRI} (mΩ)	R_{SEC} (Ω)	VENDOR
LT3585-1 LT3585-0/ LT3585-2	SBL-5.6S-1 SBL-5.6-1	5.6 × 8.5 × 3.0 5.6 × 8.5 × 4.0	24 10	400 Max 200 Max	10.2 10.2	305 103	55 26	Kijima Musen Hong Kong Office 852-2489-8266
LT3585-1 LT3585-0 LT3585-1 LT3585-2 LT3585-3	LDT565620ST-203 LDT565630T-001 LDT565630T-002 LDT565630T-003 LDT565630T-041	5.8 × 5.8 × 2.0 5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0	8.2 6 14.5 10.5 4.7	390 Max 200 Max 500 Max 550 Max 150 Max	10.2 10.4 10.2 10.2 10.4	370 Max 100 Max 240 Max 210 Max 90 Max	11.2 Max 10 Max 16.5 Max 14 Max 6.4 Max	TDK Chicago Sales Office (847) 803-6100 www.components.tdk.com
LT3585-0 LT3585-1 LT3585-2 LT3585-3	TTRN-0530-000-T TTRN-0530-012-T TTRN-0530-021-T TTRN-0530-022-T	5.0 × 5.0 × 3.0 5.0 × 5.0 × 3.0 5.0 × 5.0 × 3.0 5.0 × 5.0 × 3.0	6.6 16.0 11.8 4.0	200 Max 400 Max 300 Max 300 Max	10.3 10.3 10.3 10.3	128 Max 515 Max 256 Max 102 Max	28 Max 32 Max 37 Max 16 Max	Tokyo Coil Engineering Japan Office 0426-56-6262

APPLICATIONS INFORMATION

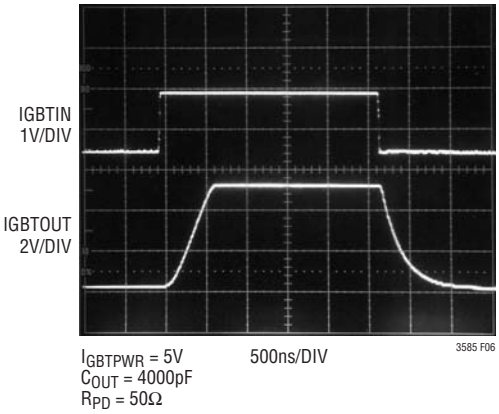

Figure 6. IGBT Driver Output with 4000pF Load

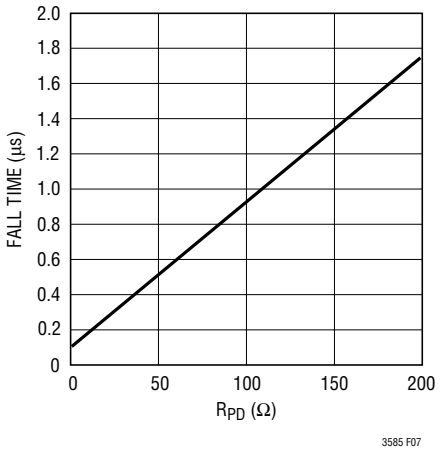

Figure 7. IGBT Turn-Off Delay vs R_{PD}

Table 3. Recommended Output Diodes

PART	MAX REVERSE VOLTAGE (V)	MAX CONTINUOUS FORWARD CURRENT (mA)	CAPACITANCE (pF)	VENDOR
GSD2004S (DUAL DIODE)	2 × 300	225	5	Vishay (402) 563-6866 www.vishay.com
CMSD2004S (DUAL DIODE)	2 × 300	225	5	Central Semiconductor (631) 435-1110 www.centralsemi.con
MMBD3004S (DUAL DIODE)	2 × 350	225	5	Diodes, Inc (816) 251-8800 www.diodes.com

IGBT Drive

The IGBT is a high current switch for the 100A+ current through the photoflash lamp. To create a redeye effect or to adjust the light output, the lamp current needs to be stopped or quenched with an IGBT before discharging the photoflash capacitor fully. The IGBT device also controls the 4kV trigger pulse required to ionize the Xenon gas in the photoflash lamp. Figure 8 is a schematic of a fully functional photoflash application with the LT3585-0 serving as the IGBT driver. An IGBT driver charges the gate capacitance to start the flash. The IGBT driver does not need to pull up the gate significantly fast because of the inherently slow nature of the IGBT. A rise time of 2µs is sufficient to charge the gate of the IGBT and create a trigger pulse. With slower rise times, the trigger circuitry will not have a fast enough edge to create the required 4kV pulse. The fall time of the IGBT driver is critical to the safe operation of the IGBT. The IGBT gate is a network of resistors and capacitors, as shown in Figure 9. When the gate terminal is pulled low, the capacitance closest to the terminal goes low but the capacitance further from the terminal remains high. This causes a smaller portion of the device to handle a larger portion of the current, which can damage the device. The pull-down circuitry needs to pull down slower than the internal RC time constant in the gate of the IGBT. This is easily accomplished with a resistor placed in series with the IGBTPD pin.

The LT3585 series integrated IGBT drive circuit is independent of the charging function and draws its power from the IGBTPWR pin. The drive pulls high to within 200mV of IGBTPWR and pulls down to 100mV. The circuit's switching waveform is shown in Figure 6. The rise and fall times are measured using a 4000pF output capacitor. The typical 10% to 90% rise time is 320ns when IGBTPWR

APPLICATIONS INFORMATION

is 5V and IGBTIN is driven by a 5V signal. The typical 90% to 10% fall time is 125ns but varies with R_{PD} given by Figure 7. The IGBT driver pulls a peak of 50mA when driving an IGBT with minimal quiescent current. In the low state, an active pull-down network is used during the initial transition but is deactivated after an internal time constant. This allows the IGBT driver's quiescent current to drop to approximately 0.1µA during idle conditions. The pull-down circuit will clamp the output below 0.8V for currents not exceeding 10mA in its idle state. The pull-up network is always active when the IGBTIN is greater than 1.5V. Table 4 is a list of recommended IGBT devices for strobe applications. These devices are all packaged in 8-lead TSSOP packages unless otherwise noted.

Table 4. Recommended IGBTs

PART	DRIVE VOLTAGE (V)	BREAKDOWN VOLTAGE (V)	COLLECTOR CURRENT (PULSED) (A)	VENDOR
CY25CAH-8F* CY25CAJ-8F* CY25BAH-8F CY25BAJ-8F	2.5 4 2.5 4	400 400 400 400	150 150 150 150	Renesas (408) 382-7500 www.renesas.com
GT8G133	4	400	150	Toshiba Semiconductor (949) 623-2900 www.semicon.toshiba.co.jp/eng

*Packaged in 8-lead VSON-8 pacakge.

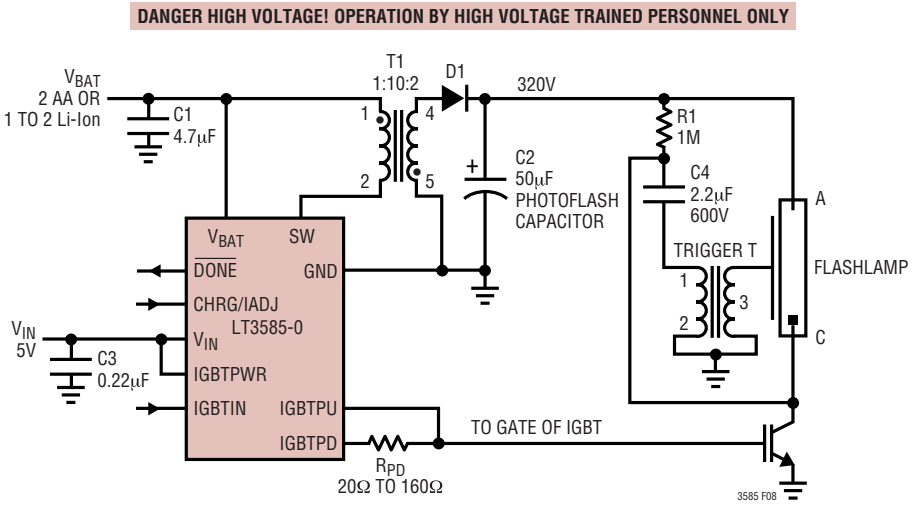

Figure 8. Complete Xenon Circuit

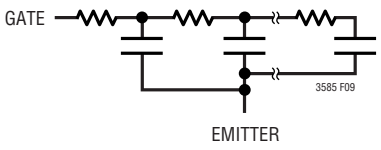

Figure 9. IGBT Gate

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Board Layout

The high voltage operation of these parts demand careful attention to board layout. You will not get advertised performance with careless layout. Figure 10 shows the recommended component placement. Keep the area for the high voltage end of the secondary as small as possible. Also note the larger than minimum spacing for all high voltage nodes in order to meet breakdown voltage requirements for the circuit board. It is imperative to keep the electrical path formed by C1, the primary of T1, and the LT3585 series IC as short as possible. If this path is haphazardly made long, it will effectively increase the leakage inductance of T1, which may result in an overvoltage condition on the SW pin. The CHRG/IADJ pin trace should be kept as short as possible while minimizing the adjacent edge with the SW pin trace. This will eliminate false toggling of the CHRG/IADJ pin during sharp transitions on the SW pin. Thermal vias should be added underneath the Exposed Pad, Pin 11, to enhance the LT3585's thermal performance. These vias should go directly to a large area of ground plane. Acting as a heat sink, the thermal vias/ground plane will lower the device's operating temperature.

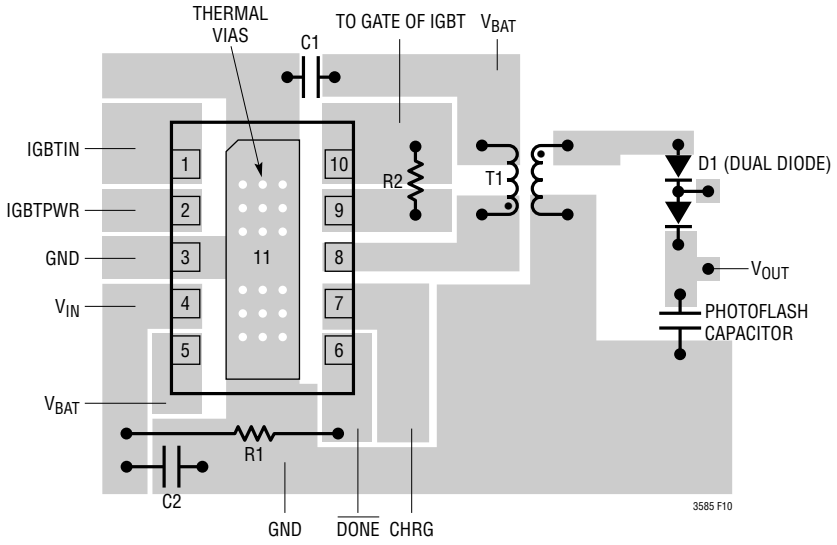
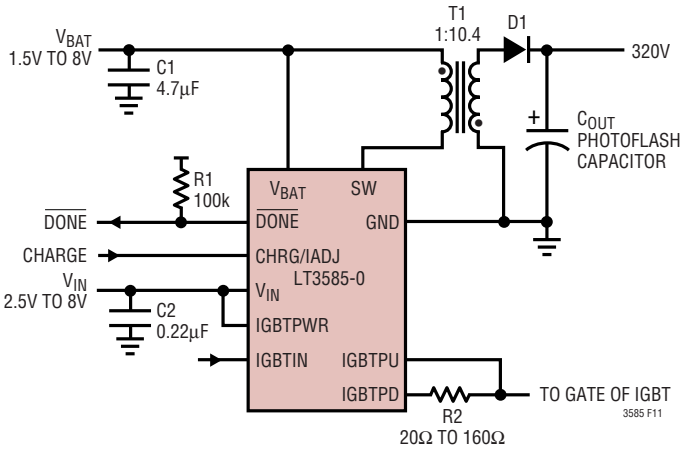


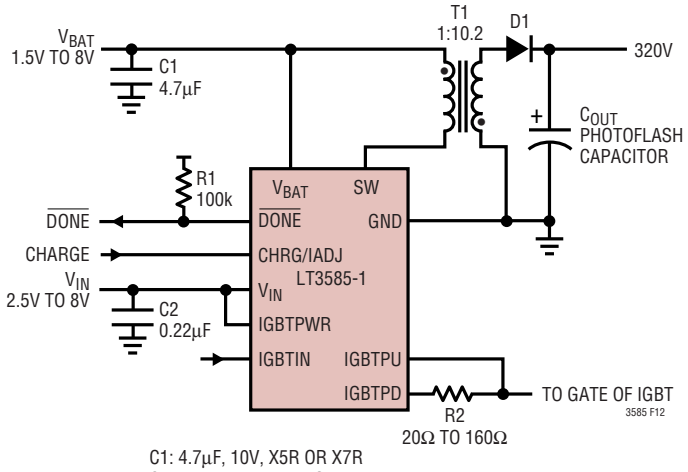
Figure 10. LT3585 Suggested Layout

TYPICAL APPLICATIONS



C1: 4.7µF, 10V, X5R OR X7R
C2: 0.22µF, 10V, X5R OR X7R
C_{OUT}: RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
R1: PULL-UP RESISTOR NEEDED IF DONE PIN USED
T1: TDK LDT565630T-001, L_{PRI} = 6µH, N = 10.4

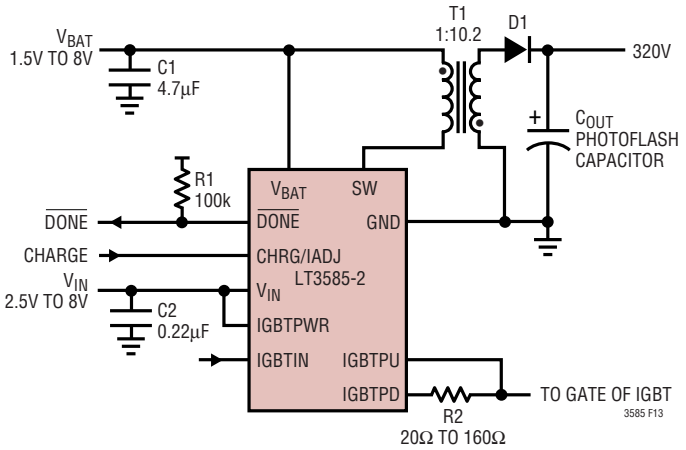
Figure 11. LT3585-0 Photoflash Charger Uses High Efficiency 3mm Tall Transformer



C1: 4.7µF, 10V, X5R OR X7R
C2: 0.22µF, 10V, X5R OR X7R
C_{OUT}: RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
R1: PULL-UP RESISTOR NEEDED IF DONE PIN USED
T1: LTD565620ST-203, L_{PRI} = 8.2µH, N = 10.2

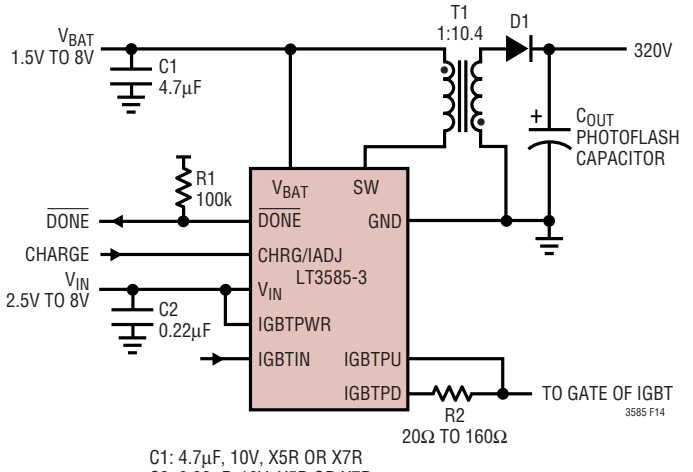
Figure 12. LT3585-1 Photoflash Charger Uses High Efficiency 2mm Tall Transformer

TYPICAL APPLICATIONS



C1: 4.7µF, 10V, X5R OR X7R
C2: 0.22µF, 10V, X5R OR X7R
RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
R1: PULL-UP RESISTOR NEEDED IF DONE PIN USED
T1: TDK LDT565630T-003, L_{PRI} = 10.5µH, N = 10.2

Figure 13. LT3585-2 Uses High Efficiency 3mm Tall Transformers



C1: 4.7µF, 10V, X5R OR X7R
C2: 0.22µF, 10V, X5R OR X7R
RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
R1: PULL-UP RESISTOR NEEDED IF DONE PIN USED
T1: TDK LDT565630T-041, L_{PRI} = 4.7µH, N = 10.4

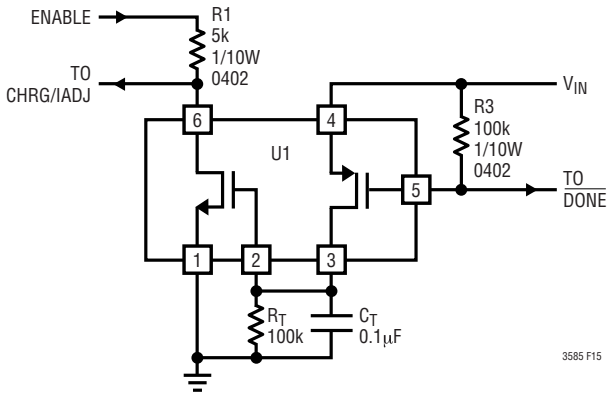
Figure 14. LT3585-3 Uses High Efficiency 3mm Tall Transformers

TYPICAL APPLICATIONS

The LT3585 series can be auto-refreshed using the additional circuitry shown in Figure 15 with its basic operation shown in Figure 16. The ENABLE pin is used to enable or disable the auto-refresh charging mode. Without an auto-refresh circuit, the output voltage will droop due to output capacitor and output diode leakage currents. The circuit in Figure 15 uses the $\overline{\text{DONE}}$ and CHRG/IADJ pins to form an open-loop control scheme. The output voltage target is sensed through the $\overline{\text{DONE}}$ pin with the PFET of U1, Panasonic UP04979 composite transistor. When the $\overline{\text{DONE}}$ pin goes low during the V_{OUT} trip condition, the PFET charges the auto-refresh timing node comprised of R_T and C_T, and in turn, pulls the CHRG/IADJ pin low through a NFET and disables the LT3585 series part. The $\overline{\text{DONE}}$ pin immediately goes high in shutdown, releasing the timing node and allowing the voltage at Pins 2 and 3 to decay. After approximately a R_TC_T time constant, the CHRG/IADJ pin is released and the LT3585 series part is enabled. This cycle is repeated to maintain a constant DC output voltage. The open-loop control method places a constraint on the control loop dominant time constant, $R_T \bullet C_T$, given by:

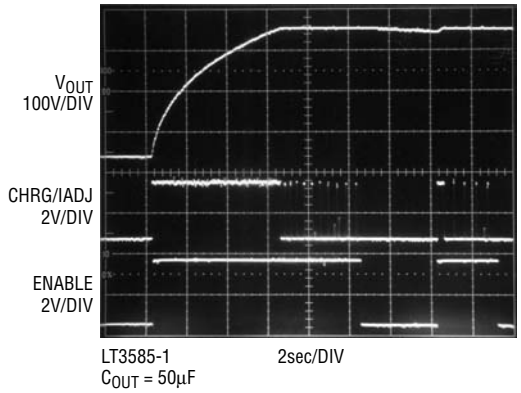
$$R_TC_T > \frac{2 \bullet I_{PK}^{2} \bullet L_{PRI}}{I_{LK} \bullet V_{BAT}}$$

where I_{LK} is the known leakage current, I_{PK} is the transformer peak primary current, and L_{PRI} is the transformer primary inductance. If this condition is not met, a runaway condition could occur. The LT3585 series part would continue to charge the output voltage past the internal output trip voltage. Figure 17 shows the AC ripple of a typical auto-refresh circuit with the proper selection of R_T and C_T.



U1: PANASONIC UP04979 COMPOSITE TRANSISTORS

Figure 15. Auto Refresh Application



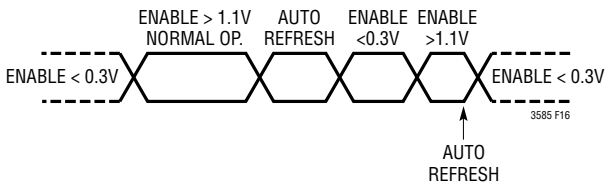


Figure 16. Auto Refresh Basic Operation

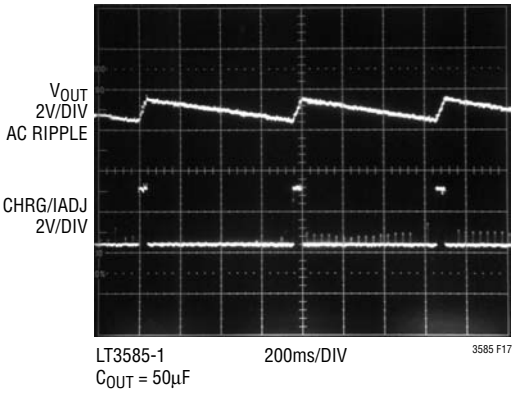
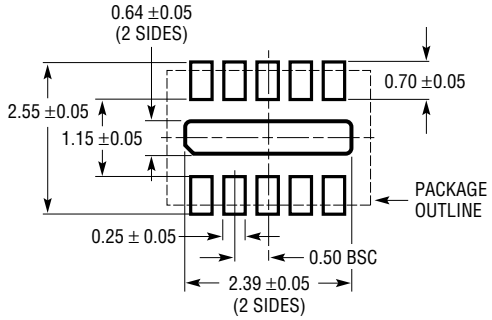


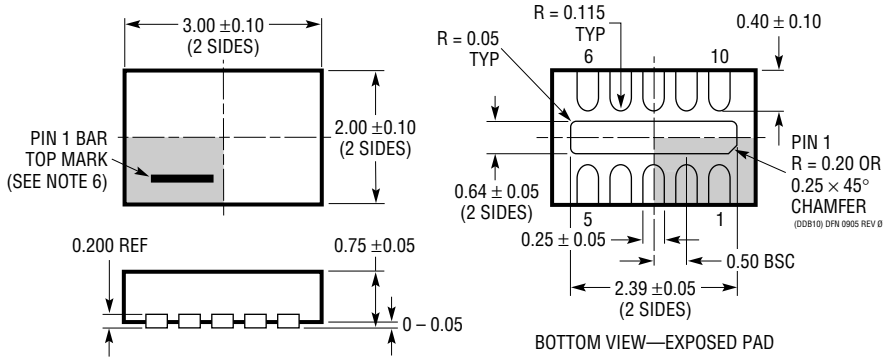
Figure 17. V_{OUT} AC Ripple in Auto Refresh Mode

PACKAGE DESCRIPTION

DDB Package
10-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1722 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE