User guide

### **Document information**

Information	Content
Keywords	BYLMP GUI, FlexGUI
Abstract	This user guide introduces the NXP BYLMP GUI, a GUI based on the common software platform called FlexGUI.



## **NXP Semiconductors**

## **UG10029**

## DEMO-BYL1-EVB software user guide

Revision	Date	Document Changes
1	20220401	Initial release.

## 1 Introduction

This document introduces **NXP BYLMP GUI**. It is based on common software (SW) platform called **FlexGUI**.

The user should follow this workflow:

- 1. Set up hardware. Become familiar with target devices and kits.
- 2. Set up the software.
  - a. Download the SW package from website or other source.
  - b. Program the MCU with provided firmware, using the USB Multilink.
  - c. Install Java dependency on your OS.
  - d. Install the GUI or use portable version.
- 3. Learn how to work with launcher, workspace, script editor, and register map.
- 4. Learn how to use tabs and options specific for FS85<sup>[5]</sup> and PF502x<sup>[6], [7]</sup> devices.
- 5. Learn how to use tabs and options specific for BYLMP system solution.

#### **Recommendation:**

Refer to related hardware user guides and data sheets for details on target devices and evaluation kits. The target devices and evaluation kits are not within the scope of this document. Links to references are found in <u>Section 8</u>.

#### What is FlexGUI?

FlexGUI is a universal SW framework for development of GUI applications for remote evaluation and configuration of target embedded devices controlled by MCU using standard peripherals like SPI, I<sup>2</sup>C, IO, ADC, TMR, and so forth.

This universal framework provides a common user interface for various types of analog devices (for example SBCs, PMICs, GDs, and XSs). It consists of workspace, script editor, register map, and optionally other generic tabs/components, which can be easily customized per device type.

Each device family is supported by custom extension of this framework which handles following specifics.

- Definition of communication between MCU and device.
  - Definition of data frame formats for supported buses.
- Definition of device models and their revisions.
  - Definition of control arguments (adjusting differences in the control logic per device models).
  - Definition of automatically generated scripts into script editor.
  - Definition of register map (register sets, register groups, registers).
  - Definition of required MCU resources (pins, buses, converters, timers, and so forth).
  - Definition of bus routing rules for available register sets or registers.
  - Definition of feature tabs (visualization of device features in terms of configuration and its feedback).
  - Definition of feature sets (initialization behavior, loaded tabs).
- Definition of related kits (evaluation boards).
  - List of supported MCUs.
  - List of supported devices (with constraints on allowed models and revisions).
  - Configuration and wiring (pin mux) of used MCU resources for enumerated devices.

The firmware provided runs on the target MCU, then executes commands from the GUI and translates them into actions on MCU peripherals such as SPI, I<sup>2</sup>C, IO, ADC, and TMR. After completion, it sends a response with the result and optionally additional data back to the GUI.

#### Hardware preparation 2

This hardware preparation section briefly describes how to set up the supported evaluation kits for use with the software GUI.

Note: This section is not meant to be an exhaustive description for the target devices or the evaluation kits used. For a deep dive into the technical details, refer to related user quides, data sheets, schematics, and other device-related deliverables.

### 2.1 XVALEYEQ4ESEVB / KL25Z

The XVALEYEQ4ESEVB / KL25Z kit serves as an NXP reference design for a system solution demonstrating a combination of power management products. It uses an on board MCU with USB interface for the communication with the PC / GUI SW.

#### 2.1.1 System block diagram

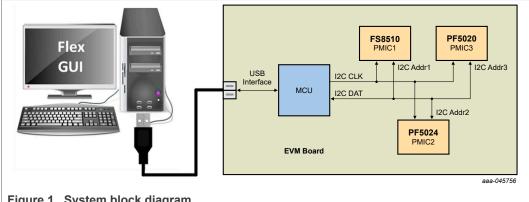


Figure 1. System block diagram

#### 2.1.2 Supported MCUs and devices

Table 1 provides a list of supported MCUs and their interfaces.

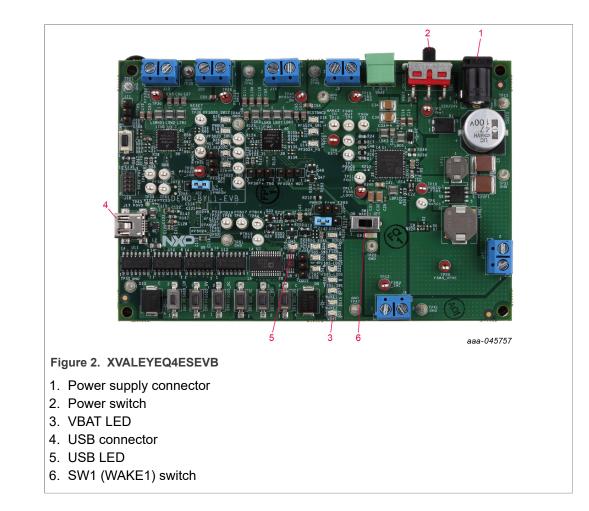
#### Table 1. Supported MCUs

Target MCU	External MCU	Connection	Programming	Notes
KL25Z128VLK4	No	USB HID	USB Multilink	All soldered.

The supported devices are:

- FS8510
- PF5020
- PF5024

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## 2.1.3 Connecting to the kit

This section describes required hardware settings of the kit in order to realize connection with the GUI.

- 1. Connect the USB cable to the PC and the USB port [4] on the kit.
- 2. The LED [5] should be ON which signalizes USB connected.
- 3. Provide external VIN 12 V on available power supply connectors [1].
- 4. Turn on the kit using **switch [2]** into right position depending on used power supply connector.
- 5. The VBAT LED [3] should be ON which signalizes connected power supply.
- 6. Turn on **SW1 [6]** to power up SBC and optionally PMICs (depends on J20 and J22 positions).

## **3** Software preparation

The software preparation section describes how to download the SW package, install Java on your computer. and run the application.

## 3.1 Downloading the SW package

To download the latest version of the GUI SW:

- Visit the NXP website for BYLMP EVB<sup>[1]</sup> / Software Downloads and look for the <u>GUI</u> <u>SW</u>.
- 2. Download the SW package as a (.zip) file.
- Unzip the downloaded file and check to see that the folder contains the files listed in <u>Table 2</u>.

Table 2. Content of the SW package

Folder Name	Folder Contents
GUI	This directory contains GUI application.
NXP_BYLMP_GUI-[version].exe	Executable installer of GUI application for Windows.
MCU	This directory contains firmware for KL25Z MCU.
flexgui-fw-kl25z-usb-hid-BYLMP- [version].bin/.gdbi/.hex/.map/.s19	Firmware binaries (.bin, .s19, and so forth).
flexgui-fw-kl25z-usb-hid-BYLMP-[version]_ USBMULTILINK.bat	GDB programming script for USB Multilink Universal.
LICENSE_FW.txt	License file for MCU firmware.
UG	This directory contains user guide for GUI application.
ChangeLog.txt	Diff list for provided releases.
README.txt	Package content and brief instructions.

## 3.2 Programming the KL25Z onboard MCU

This section describes how to program provided firmware on MCU with use of USB Multilink.

**Note:** Releases and versions of target tools referenced in this section may become outdated in near future. Therefore NXP does not guarantee that the combination of updated releases and versions of target tools work together out of the box. Direct distribution of these tools with our GUI solution is not possible because of licensing restrictions.

## 3.2.1 Creating root folder for GDB tools

In order to program the MCU via Multilink, collect, and prepare several tools.

Create common folder called '**Multilink\_GDB**', where these tools are gathered. There are no constraints on the location of this folder, the folder may be placed in a user directory if desired or other locations of choice.

## 3.2.2 Installing USB multilink system drivers

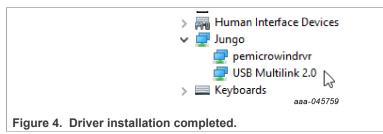
Download the latest drivers from the PEmicro's USB Multilink Universal webpage.

	Downloads
Contains f for USB M	tilink Universal (and FX) Resource CD (10030 KB) rmware config utility, up-to-date firmw <sup>(17)</sup> , technical summary, and other resources for both USB Multilink Universal and USB Multilink Universal FX. Now updated Itilink Universal Rev D and USB Multilink Universal FX Rev C. 17/09/2020 v10.46 - Includes Multilink ARM and Embedded ARM multilink supports - Displays ion of firmware if supported
	eae-045758
	2 Developeding DEmisso LISP multi link

Figure 3. Downloading PEmicro USB multi-link

Follow these steps to install the drivers:

- 1. Run **'multilink\_universal\_install.exe'**, click through the setup and wait for completion.
- Connect BYLMP EVB<sup>[1]</sup> micro-USB port to USB port on your PC in order to provide a power source for the MCU.
- <sup>3.</sup> Connect USB Multilink to BYLMP EVB<sup>[1]</sup> via [PORT G Mini-10 (Kinetis)].
- 4. Connect USB Multilink to USB port on your PC and wait for OS to install it.
- 5. Open **Device Manager** and determine whether the program successfully installed as expected as shown in <u>Figure 4</u>.



After successfully installing the program, proceed with the preparation of required tools.

## 3.2.3 Getting GNU Arm GDB

Download <u>latest package</u> for Win32 (or any other arch) from the <u>GNU Arm Embedded</u> Toolchain webpage<sup>[4]</sup>.

Follow these steps to install GNU Arm GDB.

- 1. Run 'gcc-arm-none-eabi-9-2020-q2-update-win32.exe', click through the setup and wait for completion.
- Locate the file named 'arm-none-eabi-gdb.exe' by navigating to <path-toinstallation-folder>/GNU Arm Embedded Toolchain/9 2020-q2-update/bin folder as shown in Figure 5.

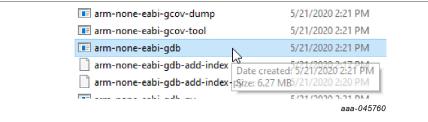


Figure 5. Locating the file arm-none-eabi-gdb.exe

 Copy the 'arm-none-eabi-gdb.exe' file to your 'Multilink\_GDB' root folder and subfolder called 'client'.

## 3.2.4 Getting PEmicro's GDB Server for Arm

Download <u>latest package</u> from the PEmicro's <u>GDB Server Plug-In for Eclipse-based ARM</u> IDEs webpage<sup>[3]</sup>.

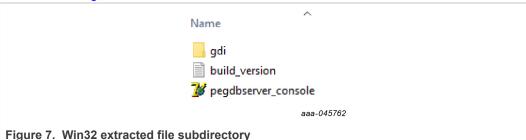
A login prompt or a prompt to a direct download link via email appears. Choose either.

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	PEmicro User Login
	You may also Request a new Password
	Email Password (Case-sensitive) Login
	Or receive a direct download link via email right away
	E-Mail (required) Send me a download link
	© 2020 P&E Microcomputer Systems Inc. Website Terms of Use and Sales Agreement VERIFED & SECURITY UERIFY SECURITY 0 0 0 0 0 0 0 0 0 0 0 0 0
Figure 6. PEmicro user lo	

Follow these steps to obtain PEMicro's GDB Server<sup>[3]</sup> from the downloaded archive.

- 1. Unpack the downloaded zip archive called 'com.pemicro.debug.gdbjtag.pne.updatesite-4.5.8-SNAPSHOT.zip'.
- 2. Go to the plugins subdirectory of unpacked file.
- 3. Extract content of the 'com.pemicro.debug.gdbjtag.pne.expansion\_4.5.8.202003301732.jar' file using a compression tool of your choice.
- 4. Navigate to the win32 subdirectory of the extracted file to view the directory structure shown in Figure 7.



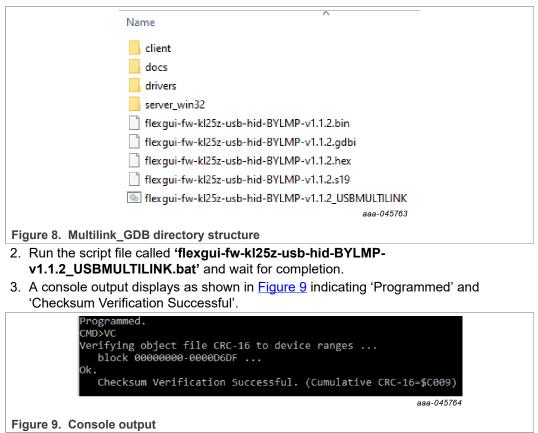
- 5. Create folder named 'server\_win32' in your 'Multilink\_GDB' root folder.
- 6. Copy and paste the files files shown in Figure 7 to the 'server win32' in your 'Multilink\_GDB' root folder.

## 3.2.5 Programming procedure

Follow these steps to program the MCU with provided firmware.

1. Copy content of the MCU folder (see <u>Table 2</u>) to your 'Multilink\_GDB' root folder. The copied content of the MCU folder should have similar directory structure as shown in Figure 8, without the docs and drivers folders.

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4. The console output verifies that the programming of the MCU was successful.

## 3.3 Running the GUI (Windows OS Only)

Follow these steps to install the GUI on your OS.

1. Double-click the installer located in the GUI folder, see Figure 10.

Name	Date modified	Туре	Size
BVXP_BYLMP_GUI-1.3.3	1/10/2022 5:56 PM	Windows Installer	45,267 KB
			aaa-045765
Figure 10. GUI installer			

2. Accept license agreement (Figure 11) and click the Next button.

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🛃 NXP_BYLMP_GUI Setup		-1		×
End-User License Agreement				
Please read the following license agreement careful	y			S
Copyright 2016 - 2022 NXP				^
All rights reserved.				
Redistribution and use in source and bina modification,	ary <mark>f</mark> orms, with	or wit	hout	
are permitted provided that the followin	g conditions a	re met:		
Redistributions of source code m	ust retain the a	above		×
$\ensuremath{\boxdot}$ I accept the terms in the License Agreement				
Print Bac	ck Next	L2	Cano	el
			aaa	-045766

### Figure 11. End-User license agreement

3. Select a destination folder (Figure 12) and click the Next button.

🔀 NXP_BYLMP_GUI Setup	-		×
Destination Folder Click Next to install to the default folder or click Change to choose ar	nother.		Ð
Install NXP_BYLMP_GUI to:			
C:\Users\nxa23158\AppData\Loca\\WXP_BYLMP_GUI\			_
Change			
Back Next	t 🖓	Car	ncel
		aa	a-045767

4. Confirm the installation (Figure 13). Wait for the installation to complete.

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聞 NXP_BYLMP_GUI Setup				×
Ready to install NXP_BYLMP_GUI				Ð
Click Install to begin the installation. Click Back to review of installation settings. Click Cancel to exit the wizard.	or change an	iy of your	r	
Back	Install	<u></u>	Car	ncel
			aa	aa-045768

#### Figure 13. Confirm installation

5. Launch the GUI via the desktop icon or start menu shortcut called **NXP\_BYLMP\_GUI** and wait for the GUI launcher to appear. The GUI displays a splash screen shown in Figure 14.

	FlexGL	JI Evaluatio	on Tool
		<u>رې</u>	
	\$ 2020 NXP B.V.		NP
igure 14. GUI	splash screen		aaa-045769

## 4 Using the software

This section describes how to work with the GUI application, namely how to select a kit for use and how to navigate through the application environment. It uses the FS8510 as the reference and the steps are either similar or the same for the PF5020 and PF5024.

## 4.1 Application launcher

The application provides a dedicated kit selection window that is launched after start, see Figure 15.

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After the splash screen presents and is dismissed, the application launcher provides a dedicated kit selection window, a window launched after start, see <u>Figure 15</u>.

						×
Select a kit, on b	oard device(s)	), target MCU a	and US	SB interface.		
Kit and Device(s)						
▼ X TBD						
▼ SBC						
▼ ✓ FS85	530					
V 0	0					
▶ PF5020						
▶ PF5024						
► EAMUX						
This kit enables a	valuation of ES9	2520 DE5020 and	05502	1 devices		
This kit enables e		3530, PF5020 and	PF5024	4 devices.		
This kit enables e	ttings	3530, PF5020 and	_			
		3530, PF5020 and	_	4 devices. Adjust loaded	tabs, etc.	
▼ Advanced Set	ttings	•	•			
<ul> <li>Advanced Set</li> <li>Feature Set</li> </ul>	production	•	•	Adjust loaded	V setup.	
✓ Advanced Set Feature Set Target MCU	ttings production PKL25Z128V usb_hid	•	¢	Adjust loaded Check your HV	V setup.	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> </ul>	ttings production PKL25Z128V usb_hid	•	∂ 0 0	Adjust loaded Check your HV Check used fin	V setup.	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application M</li> </ul>	ttings production PKL25Z128V usb_hid Iode	- /LK4 - -	∂ 0 0	Adjust loaded Check your HV Check used fin	V setup. mware.	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application M</li> <li>Password</li> <li>Launch Privileges</li> </ul>	ttings production PKL25Z128V usb_hid Iode	✓ /LK4 ← ▼ rovide secret keyw BASIC	∂ 0 0	Adjust loaded Check your HV Check used fin	V setup. mware.	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application M</li> <li>Password</li> <li>Launch Privileges</li> </ul>	ttings production PKL25Z128V usb_hid 1ode pro	✓ /LK4 ← ▼ rovide secret keyw BASIC	∂ 0 0	Adjust loaded Check your HV Check used fin	V setup. mware.	



After making selections, selecting the OK button downloads the selected application workspace. For details on each section of the application launcher window, see <u>Section 4.1.1 "Kit selection"</u>, <u>Section 4.1.2 "Advanced settings"</u>, <u>Section 4.1.3 "Application mode"</u>, and <u>Section 4.1.4 "Default configuration"</u>.

## 4.1.1 Kit selection

It encompasses an area for selecting a kit, a device/s present on the kit and their models and revisions. The kit and device selection area of the application launcher allow users to view and select a kit, the devices included in the kit and view their models and revisions.

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▼ X TBD	
▼ SBC	
🔻 🗸 FS853	0
√ C0	N
PF5020	<i>м</i> <sup>2</sup>
PF5024	
► EAMUX	
This life analytics are	aluation of FS8530, PF5020 and PF5024 devices.

Depending on the kit/device selection, the values in the advanced settings section change to support the kit or device selected, see <u>Section 4.1.2</u>.

**CAUTION:** It is important for user to match this selection of device models and revisions with their physical counterparts, otherwise GUI might display less or more features and also user might experience unexpected behavior.

There are usually two types of kits.

- **Soldered** Without professional equipment, chips soldered to boards cannot be changed out by the user. For soldered kits, the GUI disables any device model and revision selection for the kit in launcher.
- **Socketed** With socketed kits, the user can easily swap different models and revisions of chips. For socket kits, the GUI enables the device model and revision selection for the kit in launcher. For the DEMO-BYL1-EVB kit, socketed kits are not proposed, and only soldered kits are available.

## 4.1.2 Advanced settings

This configuration is for adjusting advanced options. The default values are suitable for the most use cases. See <u>Figure 17</u>.

Feature Set	production	•	🧬 Adjust loaded tabs, etc.
Target MCU	PKL25Z128VLK4	•	i Check your HW setup.
USB Interface	usb_hid	-	i Check used firmware.

Figure 17. Advanced settings.

The feature set represents loaded tabs, default device modes (including polling), and other arguments for default GUI behavior.

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Figure 16. Kit and device selection

Target MCU is self-explanatory, the kit might have an embedded MCU or it can use external shield boards.

**CAUTION:** The target MCU must match the physical MCU counterpart, otherwise the GUI is unable to attach MCU resources.

### 4.1.3 Application mode

This configuration is for differentiation between basic and advanced (internal) version of the GUI. The purpose of basic version is to hide configuration options and features which are not available to the mass market.

The application mode section of the application launcher supports two modes, the basic (Figure 18) and advanced (internal) (Figure 19) versions of the GUI. Basic is the default setting. The basic version hides configuration features and options that are not available to the mass market.

To access the hidden features and options of Advanced mode, click the Elevate button and enter the correct password.

To return to Basic mode after using Advanced mode, click the Drop button to return to basic launch privileges.

	<ul> <li>Application Mode</li> </ul>		
	Password	provide secret keyword	Elevate
	Launch Privileges	BASIC	
			aaa-045773
Figure 1	8. Basic mode		

<ul> <li>Application Mode</li> <li>Password</li> </ul>		Drop
Launch Privileges	ADVANCED	ыор
		aaa-045774
9. Accessing advance	ed mode	

## 4.1.4 Default configuration

The default configuration option (Figure 20) on the application launcher allows the application to start without the application launcher. Checking "Use this configuration and do not ask again" stores the selection and opens the application with the selected default settings. User may disable this feature in the global settings, see sections <u>Section 4.3.1</u> and <u>Section 4.4.1</u>.



## 4.2 Online and Offline configuration

The application allows users to work in either an online or offline operational state.

- **Online** The kit is connected and all user configuration choices are immediately applied to the physical devices on the kit.
- **Offline** The kit is not connected and all user configuration choices are stored locally. The offline configuration can be saved for use later.

*Important:* This duality allows the GUI to serve as an alternative to OTP (one-time programming) configuration tools. These tools are usually in the form of a spreadsheet or dedicated applications that lack the ability to communicate with the kit.

### 4.2.1 Configuration export and import

The current configuration can be exported into the script editor, see <u>Figure 21</u>. See sections <u>Section 5.3</u> and <u>Section 6.3</u> for details on available scripts.

Device:	SBC 👻	SET_REG:SBC:functional:M_FLAG:0x0000
Alias:	No values	SET_REG:SBC:functional:M_REG_CTRL1:0x0000
<ul> <li>Digital pi</li> </ul>	ins	SET_REG:SBC:functional:M_REG_CTRL2:0x0009 SET_REG:SBC:functional:M_AMUX:0x0000
Analog p	ins	SET_REG:SBC:functional:M_CLOCK:0x0000
► Commun	nication	SET_REG:SBC:functional:M_INT_MASK1:0x0000 SET_REG:SBC:functional:M_INT_MASK2:0x0000
Registers	;	SET_REG:SBC:functional:M_FLAG1:0x0000
▶ Mode		SET_REG:SBC:functional:M_FLAG2:0x0000 SET_REG:SBC:functional:M_VMON_REGX:0x0000
▼ Generato	pr	SET_REG:SBC:functional:M_MEMORY0:0x0000
Script:	functional-config 🔹	SET_REG:SBC:functional:M_MEMORY1:0x0000
	Select item	
	functional-config	
	mirror-otp-config	
		aaa-045770

When the 'Append' option is selected (see <u>Figure 22</u>), the generated script is appended to the existing content in commands window.

	▼ Generator	
	Script: functional-config 🔹	
	Append	
	aaa-04577	
Figure 22. Append option on	the generator panel	

The generated script can be modified, exported/imported directly to and from the script editor. See <u>Section 4.5 "Script editor tab"</u> for details.

### 4.2.2 Configuration synchronization with the MCU

Because the user can modify configuration settings in the offline mode, addressing how to handle the offline modified settings when the GUI connects to the MCU, needs to be addressed.

There are thee options that the GUI has to address these changes.

- Attempt to synchronize configuration choices with the physical device.
- Wipe out configuration choices and restore defaults.
- Do nothing. Enabled by default.

The default behavior can be altered on demand for custom application builds and selected products.

## 4.3 Workspace layout

The GUI uses a standard application layout divided into several working areas, see Figure 23.

- Menu (see Section 4.3.1) and Toolbar (see Section 4.3.2)
- Request Log (see <u>Section 4.3.3</u>)
- Device Control Panel (see Section 4.3.4)
- Device Tabs (see TBD) and Script Editor (see Section 4.5)
- Configuration and evaluation tabs (see Section 4.3.5)
- Status bar (see <u>Section 4.3.6</u>)

The areas are described in following subsections.

XVALEYEQ4ESEVB				- ø
File Help				
Vendor ID: 0:1542 Stop				
Filter messages 🔹 🖌 🖬 💾 🔶 🛛	Script editor	ncer 😡 Safety Demo 🔹 S8C/FS8530:00 🔹 PF5020.81 🔹 PF5024.81 🔹 EAMUX:ADG1	io68RUZ:A	
Si	ingle Device Daisy Chain	Commands:	Results	
De	evice: SBC +			
45	as - No values			
	Digital pins			
	Analog pins Registers			
	Mode			
	Generator			
	our control of			
SBC Pins				
Mode				
Switch Mode: user-mode * Apply				
Current Mode: user-mode Poli				
Routing: 12C-routing +				
▼ 12C_MAIN				
Bus: L2C				
Frequency (kHz): 400				
12C address: 0x20 *				
▼ 12C_FS				
Bus: L2C				
Frequency (kHz) 400				
12C address: 0x21 *				
		🖸 🗠 💾 🖿 🚽 🔞	💾 🖿 🌌	
ICU: PKL25Z128VLK4 State: CONNECTED Firmware: 1.0	0.3/1.0.2		Application: Gemini	12.0 FlexGUI: 1.5.4 Build: Tue Sep 29 11:25:44 CEST 20
CO: PRE252128VER4 State: CONNECTED Firmware: 1.C				

Figure 23. Application workspace

#### 4.3.1 Menu

The application menu (Figure 24) provides access to additional windows/dialogs.

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	NP XVALEYEQ4ESEVB
	File Help
	Settings Vendor IC Product II
	Exit Jages
	aaa-045779
Figure 24. Application menu	

The "File" menu currently has only two options. "Settings", which enables users to customize the GUI behavior and "Exit".

### 4.3.2 Main toolbar

The main application toolbar provides access to communication settings. It enables users to control a USB Human Interface Device (HID) connection.

Vendor ID: Unknown Product ID: Unknown	Start	Vendor ID:	0x15A2 0x00D0 Start
	aaa-045780		aaa-045781
Figure 25. No MCU detected		Figure 26. MCU detected and product ids	with valid vendor

Once the GUI detects an MCU with a valid **Vendor ID** and **Product ID**, the user may press the Start button to begin the connection. See <u>Figure 26</u>.

**Note:** When selected, the button to the left of "Vendor ID:" and Product ID:" hides or displays the toolbar panel in order to save space.

#### 4.3.3 Request log

The request log section of the application (Figure 27) documents processed application requests.

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W XVALEYEQ4ESEVB	
File Help	
Vendor ID: Product ID:	0x15A2 0x00D0 Stop
App.Info	
Core.Request	
Service.Request	
Device.Request	
Register.Request	
Register.Read	
Register.Write	
Pin.Request	
Pin.Read	
Pin.Write	
	aaa-045782

Figure 27. Request log section

There are dedicated types of read/write requests for analog/digital pins and device registers.

- For register read and write requests, the message format is: Request Number > Device Name [Register Name:Register Address] [R/W]: Value
- For analog/digital pin read and write requests, the message format is: *Request Number > Device Name [Pin Name] R/W: Value*
- For register requests, users may change log level to FINE to view sent and received data frames. See <u>Section 4.4.2</u> for details on log levels. The requester request format is:

Request Number > in/out [0x Hex Value] [0b Binary Value]

Additionally the following controls are available to modify the behavior of notification area.

- Clean Message Log cleans all logs in the window.
- Pause/Resume Log Processing pauses/resumes adding of new log messages into the area
- Save Log saves logged messages into file.
- Fast Logs Filtering enables user to search for logs based on pre-defined categories or user's input.

In <u>Figure 28</u>, the left image shows only read and write requests while the right image provides details about data frames sent and received. To view more detail, open Settings/ Logs and set the Log Level = FINE).

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Filter messages 🛛 👻 🍯 🛄 🔛	Filter messages 🛛 👻 🍑 🛄 💾 🥈
140> SBC [M_FLAG:0x00] R: 0xF004	140> out [0x4100 0b 01000001 00000000]
141> SBC [M_MODE:0x01] R: 0x0020	140> in [0xF00439]0b 11110000 00000100 0011100
142> SBC [M_REG_CTRL1:0x02] R: 0x0000	140> SBC [M_FLAG:0x00] R: 0xF004
143> SBC [M_REG_CTRL2:0x03] R: 0xC01B	141> out [0x4101 0b 01000001 00000001]
144> SBC [M_AMUX:0x04] R: 0x0000	141> in [0x0020A7 0b 00000000 00100000 1010011
145> SBC [M_CLOCK:0x05] R: 0x0000	141> SBC [M_MODE:0x01] R: 0x0020
146> SBC [M_INT_MASK1:0x06] R: 0x0000	142> out [0x4102 0b 01000001 00000010]
147> SBC [M_INT_MASK2:0x07] R: 0x0000	142> in [0x0000AC]0b 00000000 00000000 1010110
148> PF5020 [DEVICE_ID:0x00] R: 0x58	142> SBC [M_REG_CTRL1:0x02] R: 0x0000
149> PF5020 [REV_ID:0x01] R: 0x21	143> out [0x4103 0b 01000001 00000011]
150> PF5020 [EMREV:0x02] R: 0x00	143> in [0xC01B02 0b 11000000 00011011 0000001
151> PF5020 [PROG_ID:0x03] R: 0x00	143> SBC [M_REG_CTRL2:0x03] R: 0xC01B
152> PF5024 [DEVICE_ID:0x00] R: 0x5C	144> out [0x4104 0b 01000001 00000100]
153> PF5024 [REV_ID:0x01] R: 0x21	144> in [0x0000A9]0b 00000000 00000000 1010100
154> PF5024 [EMREV:0x02] R: 0x00	144> SBC [M_AMUX:0x04] R: 0x0000
155> PF5024 [PROG_ID:0x03] R: 0x00	145> out [0x4105 0b 01000001 00000101]
	145> in [0x000026 0b 0000000 0000000 00100110
	145> SBC [M_CLOCK:0x05] R: 0x0000
	<

### Figure 28. Request log

## 4.3.4 Device control panel

Located below the request log area of the application, the device control panel (Figure 29) enables users to work with device modes, change routing, and communication properties as well as monitor the input and output pins.

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SBC Pins	
Mode	
Switch Mode:	user-mode 🕶 Apply
Current Mode:	user-mode Poll
Routing:	I2C-routing 💌
▼ I2C_MAIN	
Bus:	I2C
Frequency [kHz]:	: 400
I2C address:	0x20 -
▼ I2C_FS	
Bus:	12C
Frequency [kHz]:	: 400
I2C address:	0x21 -
	aaa-045784
Figure 29. Device control panel	

If a kit contains two or more devices, the device control panel contains configuration for last selected device tab (Figure 30).

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File Help									
Vendo		Stop	]						
ilter messages	-	<b>/</b> II		Script e	ditor	E Power See	quencer	🖉 Safety Demo 🧧	SBC:FS8530
9> SBC [SEQ_WAR	(E1) R: 1			000 Registe	r map (	Clocks	Regulators	Montoring	Interrupt Flag
)> SBC [SEQ_WAR	(E2] R: 1			▼ functiona	al			Wite Read	Copy Res
I > SBC [SEQ_VPR				functio	onal				copy (nes
2> SBC [SEQ_VDD				safety					
> SBC [SEQ_VDD				Write_IN	IT_Safety				
I> SBC [SEQ_UC_3 OF CONTRACT OF CONTRACT SEC (SEQ_UC_3)						G		M_FLAG	0x00
5> SBC [SEQ_VBO					1				
SBC [SEQ_D_VI SBC [DCOOD_I									
3> SBC [FS0B] R: ( )> SBC [RSTB] R: 1									
> PF5020 [RESET								M_MODE	0x01
> PF5020 [PF502		1							
> PF5020 [SEQ_D		/							
> PF5020 [SEQ_V									
> PF5020 [SEQ_D									
> PF5020 [SEQ.)	AILB] R: 1							M_REG_CTRL1	0x02
5> PF5024 / F502	4_PGOOD_IC] R:	1							
7> PF_024 [SEQ_V	DD_CORE_1V0]	R: 1		~					
BC Pins									
Mode									
Switch Mode:	user-mode	-	Apply					M_REG_CTRL2	0x03
Current Mode:	user-mode		Poll						
outing:	I2C-routing	-							
VI2C_MAIN									
Bus:	I2C							M_AMUX	0x04
Frequency [kHz]:	400								
2C address:	0x20	-							
✓ I2C_FS									
Bus:	I2C							M_CLOCK	0x05
Frequency [kHz]:	400								
I2C address:	0x21	+							
				HIGH [1]	]	Bit Button			
				LOW [0]	1	Bit Button			
	KA 64-4	NECTED.	Fi						
U: PKL25Z128VL	N4 State: CON	NECTED	rirmwar	e: 1.0.3/1.0.2					

Switch mode (Figure 31) can be used to select the next device mode and must be confirmed by selecting the Apply button. Current mode indicates the current mode in effect. The Poll button is a toggle that enables the validation of the mechanism. It periodically checks whether the device continues to fulfill the conditions for the selected

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mode. If not, the GUI informs the user and disables validation. If validation is enabled, the user can be sure that the current mode is still active.

Mode	
Switch Mode:	user-mode 🔻 Apply
Current Mode:	user-mode Poll
Routina:	test-mode
	aaa-045786
Figure 31. Switch mode	

Device modes are used as wrappers for actions on pins and registers required to get given device into desired state. The GUI is tightly coupled with these and properly reacts on device mode change events, for example, some configuration items might be available only for specific device modes.

Next important setting is routing. It basically instructs the GUI, how to realize communication between MCU and device. Currently there is supported only SPI and  $I^2C$ , which can be further configured.



In case of SPI, only the frequency can be changed. See

	▼ SPI1			
	Bus: Frequency [kHz]:	SPI 5000		
			aaa-045788	
Figure 33. SPI bus option	s			

In case of I<sup>2</sup>C, selecting the device address is also possible.

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Bus:	12C	0x22
Francisco III III	400	0x24
Frequency [kHz]:	400	0x26
I2C address:	0x32 -	0x28
▼ 12C_FS		0x2a
	100	0x2c
Bus:	12C	0x2e
Frequency [kHz]:	400	0x30
I2C address:	0x21 -	0x32
		0x20 -



On the Pins tab, the other device control panel tab shown in Figure 29, users can work directly with the input and output pins of the device.

		▼ Input Pins	
		FSOB:	Low
		PGOOD_FS85:	High
		SEQ_VDD_1V25:	High
		SEQ_VDDM_3V3:	High
		SEQ_UC_3V3:	High
		FS85_INTB:	N/V
		RSTB:	High
WAKE2_KL25Z: High 👻		SEQ_WAKE1:	Low
OV SBC SWITCH: No valu		SEQ_VPRE:	High
		SEQ_VBOOST:	High
DBG_CTRL: High -		SEQ_WAKE2:	High
OC_SBC_SWITCH: No valu 💌		SEQ_D_VDDIO	High
UV_SBC_SWITCH: No valu •		1500 ms	Poll Read
	aaa-045790		aaa-045791
Figure 35. Output pins		Figure 36. Inpu	t pins

For input pins, the user can enable polling for cyclic reading of the pin value with a given time period.

## 4.3.5 Configuration and Evaluation tabs

The configuration and evaluation tabs area of the interface enables user interaction with with all loaded devices. Each device has its own dedicated tab with several subtabs.

- Kit Tab This type of tab interfaces multiple devices at the same time, it is suitable for system solution configuration an evaluation via additional subtabs.
   Script editor, Power Sequencer, and Safety Demo
- Device Tab This type of tab interfaces only to a single device at the same time, it is

suitable for a specific chip configuration and evaluation via additional subtabs.

- SBC, PF5020, PF5024, and EAMUX
  Subtabs contains the following tabs.
  - Register map enables the user to work with device on low-level abstraction of its features/functionality, see <u>Section 4.6</u> for details on this common tab.
- Feature tabs tabs/components enable the user to work with device on highlevel abstraction of its features/functionality, these are specific for each loaded device.

 Script editor
 IE Power Sequencer
 Safety Demo
 SBC:FS8530:C0
 PF5020:81
 EAMUX:ADG16068RUZ:A

 Itt Register map
 Clocks
 Regulators
 Interrupt Flags
 INIT Safety
 Diag Safety
 IE TestMode:Sequencer
 TestMode:Mirrors\_Main
 TestMode:Mirrors\_FailSafe
 C WatchDog

 aaa-045792
 Aaa-045792
 Aaa-045792
 Aaa-045792
 Aaa-045792
 Aaa-045792

#### Figure 37. Configuration and evaluation tabs

Each device tab has its own indicator bullet to inform the user of the state of the device. The states are:

- OFFLINE The device is offline and is not accessible as indicated by a red bullet.
- BOOTING The device is booting and is accessible as indicated by a red bullet.
- ONLINE The device is online, accessible, and responsive as indicated by a green bullet.
- BUSY The device is busy and processing some requests as indicated by a yellow bullet.
- ERROR The device is in an error state. The device is not behaving as expected or communication with the device is faulty, indicated by a red bullet.

#### 4.3.6 Status bar

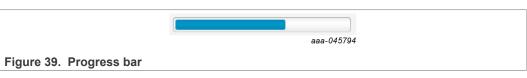
The status bar, located at the bottom of <u>Figure 23</u>, provides a standard overview of application's conditions. The status bar has three areas, left middle, and right.

On the left side of the status bar, the target MCU of the kit is shown along with the state of the connection and the firmware version (loaded on connect event). See <u>Figure 38</u>.



Figure 38. Target MCU status

In the middle of the status bar, the progress bar informs the user about the relative number of processed requests. See <u>Figure 39</u>.



On the right, the status bar displays the application version, FlexGUI platform version and build time. The lcon following the Build status displays a dialog with list of platform modules and versions.

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```
Application: NXP_BYLMP_GUI 1.3.3 FlexGUI: 1.7.2 Build: Mon Jan 10 17:55:31 CET 2022
aaa-045795
Figure 40. Application status
```

## 4.4 Workspace settings

The GUI enables users to customize the GUI behavior for individual preferences. Several areas of the GUI can be configured as described in these sections.

### 4.4.1 Kit/Device loader

When checked, the kit/device loader tab option "Show Loader" (Figure 41) opens the loader at the next application startup. Unchecked, the loader will not automatically open.

Kit/Device Loader	Logs	Register Map	Tabs			
Startup	_					
Show Loader:	(	✓ If enable	ed, load	ler will be shown on next application startup.		
					$\searrow$	
Apply Discard	Defa	ults				

Figure 41. Kit/Device show loader option

## 4.4.2 Logs

<u>Figure 42</u> presents the "Logs" tab of the workspace settings. The log tab contains configuration choices related to request logs. Users are able to select the desire level of detail and set the message limits.

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Kit/Device Loader	Logs Register Map	Tabs				
Behavior	-					
				Legend:		
			SEVERE	fatal, non-recoverable events		
			WARNING	suspicious, recoverable events		
Log Level:	INFO	•	INFO	standard events (register/pin read/write)		
			FINE	verbose variant of above (data frames, crc, etc	.)	
			FINEST	processing output with finest details		
			FIN	$EST \supset FINE \supset INFO \supset WARNING \supset SEVERE$		
Message Limit:	500	*	Limit for nun memory.	nber of cached messages. More items take mor	e	
Apply Discard	Defaults					

#### Figure 42. Log and message limits

The log levels pulldown menu is shown in Figure 43.

	INFO -
	SEVERE
	WARNING
	INFO
	FINE
	FINEST L
	aaa-045798
Figure 43. Log levels	

### 4.4.3 Register map

The register map tab sets configuration settings to generate a register map automatically for target devices. The following options alter the register map appearance and behavior.

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Kit/Device Loader Logs	Register Map	ibs	
User Interface			
Navigator View:	<ul> <li>Tree View</li> <li>List View</li> </ul>	Display register sets and register groups in tree form. Display only register sets in list form.	
Registers Per Page:	8 <b>*</b>	Number of registers to be displayed on single page.	
Sort By Address:		All visible registers will be sorted by address.	
Bit Buttons			
Bit Buttons Per Line:	8		
Uniform Buttons:	$\checkmark$	All bit buttons will use the same fixed width.	
Button Width:	110	Bit button width in pixels.	
Show Bit Position:	$\checkmark$	Display position in related bit group, e.g. [X:Y].	

#### Figure 44. FlexGUI register map tab settings

The GUI works internally with this register structure, describing the register map of the device.

**Register Set** (set of groups of related registers)

Register Group (set of related registers)

Register (single register)

Bit Group (bitwise group in register, which represents configuration item)

Bit Option (possible configuration choice for given bit group)

The Navigator View option is tightly coupled with this structure.

- **Tree View** displays a view where register sets and register groups are displayed in tree form. The tree view option enables users to navigate quickly through the available registers by narrowing down the choices related only to registers.
- List View displays a view where only the register sets are presented, in list form, leaving the user fewer choices for selection. Registers are grouped by the parent register sets.

Note: Figure 45 and Figure 46 present PF5020 registers in tree and list view.

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Object         Image Registers         Image Registers         Object_200         O	Register map ( PMIC Config	🛛 Fu	nctional Safety (	D LDO Reg	gulators	O S	W Regula	itors	♀ Interrupts								
Image: Registers         0 EVICE_ID         0.00         R         0.00         R         0.00         Desc_EAME	▼ functional		Write Read	Copy R	eset												
Synthe         Karly (Low (Low (Low (Low (Low (Low (Low (Low			DEVICE_ID	0x00	0	R	0x0	0	DEVICE_FAM[3]	DEVICE_FAM(2)	DEVICE_FAM[1]	DEVICE_FAM(0)	DEVICE_ID[3]	DEV(CE_) D(2)	DEVICE_ID(1)	DEVICE_D[0]	
Wackdog Configuration Fault Counters AUX Content SWI Content Content SWI Content SWI Content Content SWI Content SWI Content SWI Content Content SWI Content SWI Content Content SWI Content SWI Content Content SWI Content SWI Content SW	Fault Management		REV_ID	0x01	0	R	0x0	0	FULLLAYER, REV[3]	FULLLAYER, REV[2]	FULLLAYERLREV[1]	FULLLAYER_REV[0]	METALLAYER.R.	METALLAYER,R.	METALLAYER_R_	METALLUAYER,R.	
MAUX Control         MAU         MAU <t< td=""><td></td><td></td><td>EMREV</td><td>0x02</td><td>0</td><td>R</td><td>0x0</td><td>0</td><td>PROG_ID[8]</td><td>PROG_ID[2]</td><td>PR06_0[1]</td><td>PRC05_10(0)</td><td>Bit3</td><td>EMREV[2]</td><td>EMREV[1]</td><td>EMREV[0]</td><td></td></t<>			EMREV	0x02	0	R	0x0	0	PROG_ID[8]	PROG_ID[2]	PR06_0[1]	PRC05_10(0)	Bit3	EMREV[2]	EMREV[1]	EMREV[0]	
SWI Control SWI Control LDD Control VSWI Control SWI Control SWI Control Page Select			PROG_ID	0x03	0	R	0x0	0	PROG_ID[7]	PROG_ID[6]	PROG_ID[5]	PROG_ID(4)	PROG_D[3]	PROG_ID[2]	PROG_ID[1]	PROG_ID[0]	
	SW2 Control SWND1 Control LDO1 Control VSNVS Control																
	HIGH [1] Bit Button											4 <b>1</b> b					

functional	Functional Safety			QS	W Regulat	and	Interrupts								
TP_MIRROR	Write Read (		set			_			_				_	_	
DTP_PAGE2		0x00		R	0x0	0	DEVICE_PAM(3)	DEVICE_FAM(2)	DEVICE_FAM[1]	DEVICE_FAM(0)	DEVICE_ID[3]	DEM CELID [2]	DEVICE.JD[1]	DEVICELID(0)	
		0x01		R	0x0	0	FULL_LAYER_REV[3]	FULL_LAYER_REV[2]	PULL_LAYER_REV[1]	FULL_LAYER_REV[0]	METAL_LAYER_R.	METAL_LAYER_R.	METAL_LAYER_R	METAL_LAYER_R .	
		0x02	0	R	0x0	0	PROG_JD[3]	PROG_ID[2]	PROG_ID[1]	PROG_ID(0)	813	EMREV[2]	EMREV[1]	EMREV[0]	
	PROG_ID	0x03	0	R	0x0	0	PROGJD[7]	PROG_ID(6)	PROGUD[5]	PROG_ID(4)	PROGJD[3]	PROG_ID[2]	PROGUD[1]	PROG_ID[0]	
	INT_STATUS1	0x04	0	W R	0x0	0	SDWNU SDWNU	FREQ_RDY_I	CRC_I GRC_I	PWRUP_I PWRUP_I	PWRDN_I PWRDN_I	8/12	PGDOD_I PGDOD_I	VIN_OVLO_I	
					0xfb		SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	8112	PGODD_M	VIN_OVLO_M	
	INT_MASK1	0x05	0	R	0x0	0	SDWNLM	FREQ_RDY_M	CRC_M	PWRUPJM	PWRDN_M	8/12	PGODD_M	VINLOVLOUM	
	INT_SENSE1	0x06	0	R	0x0	0	B≿7	Bit6	Bit5	Bit4	Bit3	8112	PGOOD_S	VIN_OVLO_S	
				w	0x0	_	WDU	PSYNC_FLT_I	THERMLISSU	THERM_140J	THERMLIZEJ	THERM_110J	THERMLISSJ	THERMLOOU	
	INT_STATUS2	0x07	0	R	0x0	0	WDU	PSYNC_RLT_I	THERM_155_J	THERM_140,J	THERM_125_J	THERM_110_J	THERM_95_J	THERM_80_J	
HIGH [1] Bit Button										2 3 4 5 \$					
HIGH [1] Bit Sutton LOW (0) Bit Button									۲ و	2 2 4 5 <b>b</b> 1/12					888-1

## 4.4.4 Tabs

This tab contains configuration options related to all GUI tabs, see Figure 47.

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it/Device Loader Logs Reg	ister Map	Tabs
User Interface		
Show Control Toolbar	$\checkmark$	If enabled, tab will show control toolbar with buttons for read, write and polling of its state as well as specific ones to given tab.
Behavior		
Use Register Init Value:	$\checkmark$	If enabled, tab will use register init value for configuration items as default one for GUI startup or reset (start/stop connection).
Auto-Copy Read To Write:		If enabled, read out value is automatically copied to write selection counterpart.
Auto-Run Read After Write:		If enabled, write to register automatically initiates read of the same register after completion. This option applies only for r/w registers.
Apply Discard Defaults		

Figure 47. GUI tabs configuration

#### Note:

It is guaranteed that these preferences are reflected in any flexible tab (with blue boxes) and register map.

Some device-specific tabs may not implement these preferences, therefore any modification on this tab may not work as expected for those devices.

## 4.5 Script editor tab

The script editor is an embedded tool enabling the sequential execution of commands, which can access registers, and the digital and analog pins of a device. The graphical interface facilitates the creation of and working with commands. Section 4.5.1 through Section 4.5.5 provide detailed information.

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Script editor	cer 🥪 Safety Demo ● SBC:FS8530.C0 ● PF5020.81 ● PF5024.81 ● EAMUX:ADG16068RUZ:A	
Single Device Daisy Chain	Commands:	Results
Inge Device Bog Clean Device SSC	Communic  EC (101536: Americanity I) (ACD:0000 EC (101536: Americanity I) (ADD:0000 EC (101536: Americanity I) (ADD:00000 EC (101536: Americanity I) (ADD:00000 EC (101536: Americanity I) (ADD:000000 EC (101536: Americanity I) (ADD:00000000 EC (101536: Americanity I) (ADD:000000000000000 EC (101536: Americanity I) (ADD:00000000000000000000000000000000000	Rede
		aaa-045803
Figure 48.	Script editor tab	

## 4.5.1 Script editor layout

The script editor layout consists of three blocks as shown in Figure 49.

Script editor	cer 🥪 Safety Demo 🔹 SBC:FS8530.C0 🔹 PF5020:81 🔹 PF5024:81 🔹 EAMUX:ADG16058RUZ:A	
Single Device Daisy Chain	Commands:	Results
Divice SSC + Alas (Totalist) + Alas Anatog prins A Radiog prins A Registrix Registrix Rodide S Generativ	TTT         SIGE Concentration ML (CONCENCE)           STT         SIGE Concentration ML (SIGE CTR 1: 0,0000           STT         SIGE Concentration ML (SIGE CONCENTRATION OF CONCENTRATIO	OC write reg. M_EAG = 0.000           OC write reg. M_EAGC_FR1 = 0.000           OC write reg. M_EAGL = 0.000
	Script Sequence	Script Execution Results
		aaa-045804

Figure 49. Script editor layout

- **Command Builders** assists the user with the creation of commands or allows the user to generate pre-defined script sequences for the current device configuration.
- Script Sequence contains a list of commands prepared for execution, one command per line. Users can modify the script directly or use command builders. The command format is described in <u>Section 4.5.3</u>.

• Script Execution Results - displays the script processing results.

### 4.5.2 First steps

Use the following steps that describe how to create and execute a simple script. For reference, each step is identified in <u>Figure 50</u>:

Device Baisy Chain Commands:	Results:
SBC • 1. SET_REG/SBC/functional/M_MEMORY0.0xFF	OK: write reg. M_MEMORY0 = 0xff
No values 3.	5.
al pins	
og pins	
ters	
Write +	
functional *	
M_MEMORY0 -	
DxFF	
2.	
4.	
	💾 🥅 🧭
erator	

Figure 50. Creation and evaluation of a script

- 1. In the command builders block, select a device. The tool loads the appropriate values into boxes (register names and pin names, for example).
  - a. In the event the script was generated with a different device name, a spreadsheet, for example, an alias name may be used, making the GUI backward compatible. Using the command builders (digital/analog pins, registers, and so forth), automatically generates commands with the selected device name including the alias if provided.
- 2. Create commands to be executed. Users can modify the script sequence directly or utilize command builders which ensure valid options.
  - a. To insert a command, select command attributes and the tool inserts a new line into the script sequence. The write register command requires the Reg. value which is decimal or hexadecimal value (0x prefix, for example, 0x12).
- 3. With the cursor in the write value text field, press enter to include the write command into the script sequence.
- 4. To process the script in a loop, set the run in using the loop option in the controls found under script sequence then run the script. Using the loop option, the script repeats until the user presses Stop.
- The script execution results block is populated with result for each single comment.
   Note: These results are cleared when another process starts.
   The main notification area reports the overall result, see Figure 50.

Users may save the created script into a file or load a prepared script. Likewise the execution results may be saved or loaded from a file. An export button stores write register commands only, all other commands are omitted in ATE format as shown:

<register address>,<register value to be written>,

### 4.5.3 Definition of commands

This section describes commands supported by the script editor and their format. All commands are listed in Table 3.

Command name	Description
SET_REG	Sets value of a defined selected register (either by name or address).
GET_REG	Gets value of a defined selected register (either by name or address).
SET_REG_ND	Sets value of an undefined selected register (only by address).
GET_REG_ND	Gets value of an undefined selected register (only by address).
SET_REG_DC	Sets value of selected register of lead device for the whole daisy chain group.
GET_REG_DC	Gets value of selected register of lead device for the whole daisy chain group.
SET_DPIN	Sets value of a selected digital pin.
GET_DPIN	Gets value of a selected digital pin.
GET_APIN	Gets value of a selected analog pin. Returned value is in mV.
PAUSE	Shows a dialog with a user-defined message. The script execution is paused until the user confirms the dialog.
DELAY	Delays script execution for specified amount of time in milliseconds.
EXIT	Stops execution of the script.
SET_MODE	Sets device mode. List of modes is device-dependent.

Table 3. Script editor commands

**Note:** \*\_**ND** (not defined) commands are intended for internal use only unless otherwise stated. These commands allow communication with any register address, even if it is not explicitly defined (for example, metadata for size, feasible options, and so forth).

### 4.5.4 Format of commands

The general format of script editor commands is:

<command name>:<list of parameters separated by a colon>

Table 4 shows parameters of script editor commands. All parameters are mandatory.

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Command name	1. item	2. item	3. item	4. item
SET_REG	Device	Reg. set	Reg. name or Reg. address	Reg. value
GET_REG	Device	Reg. set	Reg. name or Reg. address	_
SET_REG_ND	Device	Bus (routing rule)	Reg. address	Reg. value
GET_REG_ND	Device	Bus (routing rule)	Reg. address	—
SET_REG_DC	Group	Reg. set	Reg. name	Reg. value
GET_RED_DC	Group	Reg. set	Reg. name	—
SET_DPIN	Device	Pin name	Pin value	—
GET_DPIN	Device	Pin name	_	—
GET_APIN	Device	Pin name		—
PAUSE	Message			—
DELAY	Time [ms]			
EXIT	—	—	—	—
SET_MODE	Device	Mode		<u> </u>

#### Table 4. Parameters of script editor commands

The parameters mentioned in <u>Table 4</u> are described as follows:

- Group: daisy chain group.
- Device: device name.
- **Reg. set:** register set name. Register sets allow users to associate registers having similar function.
- Reg. name: register name as defined in a data sheet.
- Reg. address: register address in the decimal or hexadecimal (with 0x prefix) format.
- Reg. value: register value in the decimal or hexadecimal (with 0x prefix) format.
- Bus (routing rule): bus which should be used for data transfer.
- Pin name: name of a digital or analog pin as defined in a device data sheet.
- Pin value: value of digital pin. Allowed strings are low and high.
- **Message:** a message to be displayed in a dialog. It cannot contain the colon character, which is used as a delimiter of parameters.
- **Time [ms]:** time in milliseconds (max. is 60000) for script execution delay, note that it takes approximately 15 ms to 25 ms to complete a single command.
- Mode: device mode.

#### 4.5.5 Script example

In this example script, the name of registers, register sets, devices, and pins depend on the particular device.

```
// Sets the 'M FLAG' register in the 'functional' register set
to value 0x00.
SET REG:SBC:functional:M FLAG:0x00
```

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// Gets value of the 'M FLAG' register in the 'functional' register set. GET REG:SBC:functional:M FLAG // Sets the register with address '0x01' to value 0x00 and uses SPI1 routing rule. SET REG ND:SBC:SPI1:0x01:0x00 // Gets value of the register with address '0x01' and uses SPI1 routing rule. GET REG ND:SBC:SPI1:0x01 // Sets the 'M FLAG' register in the 'functional' register set to value 0x00 for all devices in chain named as 'Group 0'. SET\_REG\_DC:GROUP\_0:functional:M\_FLAG:0x00
// Gets value of the 'M\_FLAG' register in the 'functional'
register set for all devices in chain named as 'Group 0'. GET REG DC:GROUP 0:functional:M FLAG // Sets value of 'WAKE2 KL25Z' digital pin as high. SET DPIN:SBC:WAKE2 KL25Z:HIGH // Gets value of the 'FSOB' digital pin (low/high). GET DPIN:SBC:FS0B // Gets value of the 'AMUX' analog pin. GET APIN:SBC:AMUX // Shows a dialog with user defined message. PAUSE: "Please continue when jumper XYZ is set as ... and switch XYZ is ON/OFF." // Delays script execution for 1000 ms. DELAY:1000 // Stops script execution. EXIT // Sets SBC's mode as 'test-mode'. SET MODE:SBC:test-mode

## 4.6 Register map tab

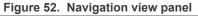
The register map tab is a common tab, enabling users to work with device registers, for example, to read and write (Figure 51). The tab contains a navigation view panel (Figure 52) with a list of register sets or a register tree structure, and pagination with lists of underlaying registers.

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egister map 🕐 Clocks		Write Read			ty Diag Safet	ty I∃ TestMode:Sec	uencer TestMode:	Mirrors_Main Test	Mode:Mirrors_FailSaf	e 🕐 WatchDog				
functional		write Reau	copy Reset			_					_	_	_	
safety				w	0x0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED		
Write_INIT_Safety		M_FLAG	0x00	>		RESERVED	RESERVED	RESERVED	SPUMUCLK	SPUM_REQ	SPI_M_CRC	IZC_M_CRC	I2C_M_REQ	N
				R	0x0	COMLERR	WU_G	VPRE_G	VBOOST_0	V8UCK1_6	VBUCK2_G	VBUCK3_G	VLD01_0	₿
						VLD02,G	RESERVED	RESERVED	SPUM, CLK	SPUM, REQ	SPI_M_CRC	I2C,M,CRC	I2C,M,REQ	
				w	DVD.	RESORVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED		
		M_MODE	0x01	_		RESERVED	EXT_FIN_DIS	RESERVED	RESERVED	RESERVED	W2DIS	W1DIS	GOTOSTBY	
		in jii oo c	0.01	R	0x0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED	PLL_LOCK_RT	
				ĸ	0.0	EXTLANLSEL.RT	RESERVED	MAINLNORMAL	RESERVED	RESERVED	W2DIS	WIDIS		
						VPRE_PD_DIS	VPDIS	BOOSTOIS	BUCKTOIS	BUCK2D/S	BUCKEDIS	LOOIDIS	LDOZDIS	
				w	0x0	RESERVED	VPEN	BOOSTEN	8UCK1EN	BUCK2EN	BUCK3EN	LDO1EN	LDOZEN	
		M_REG_CTRL1	0x02	·		VPRE_PD_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
				R	0x0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
						VBSTSR(1)	VBSTSRIDJ	BOOSTTSDCFG	BUCK1TSDCFG	BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG	
				w	0x9	RESERVED	RESERVED	RESERVED	VPRESRUS[1]	VPRESRUS[0]	RESERVED	VPRESRHS[1]	VPRESRHSJOJ	
		M_REG_CTRL2	0x03	<u>ر</u>		VBSTSR(1)	VBSTSR(0)	BOOSTTSDCPG	BUCK1TSDCFG	BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCRG	LDO2TSDCFG	
				R	0x0	RESERVED	RESERVED	RESERVED	VPRESRLS[1]	VPRESRLS[0]	RESERVED	VPRESRHS[1]	VPRESRHS(D)	
						RESERVED			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
				w	0x0			RATIO	AMUX(4)	AMUX[3]	AMUX[2]	AMUX[1]	AMUX(0)	
		M_AMUX	0x04	2	6	RESERVED		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
				R	0x0	RESERVED		RATIO	AMUX(4)	AMUX(3)	AMUX(2)	AMUX(1)	AMUD([0]	
						MOD_CONF	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT, PHASE[1]	FOUT,PHASE[0]	
				W	0x0	FOUT_CLK_SEL	EXT_FIN_SEL	FINLDLV	MOD_EN	CLK_TUNE[3]	CLK_TUNE[2]	CUK_TUNE(1)	CUC,TUNE(0)	
		M_CLOCK	0x05	<u> </u>		MOD_CONF	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT,PHASE[1]	FOUT_PHASE(0)	
				R	0x0	FOUT_CLK_SEL	RESERVED	FIN_DIV	MOD_EN	CLK_TUNE[3]	CLK_TUNE[2]	CUK_TUNE[1]	CUC,TUNE[0]	
						RESERVED	VPREDC_M	BOOSTOC,M	BUCK10C_M	BUCK2OC_M	BUCK3DC,M	LD010C_M	LDO20C_M	
HIGH [1] Bit Butte	m			W	0x0									
LOW [0] Bit Butte	m								1 2 ► 1/2					
														aaa-04

The left panel in the tab, a flat view enumerates list of register sets (<u>Figure 52</u>). When users click a register set item, the register map displays all underlaying registers.

functional	
safety	
Write_INIT_Safety	
	aaa-045807



Each register item is represented by read and/or write row depending on its definition. A single item consists of register selection checkbox, register name, register address, read/write control, register value help, and bit buttons. Bit buttons represent values of individual bits, green represents logic 1 and red represents logic 0.

For read, click the "R" button (Figure 53) and the read out value appears in button on the right. If clicked, this button, copies and pastes the read out value into write value input box above.

		W 0x0	VPRE_PD_DIS	VPDIS	BOOSTDIS	BUCK1DIS	BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS
NA DEC CENTA			RESERVED	VPEN	BOOSTEN	BUCK1EN	BUCK2EN	BUCKBEN	LDO1EN	LDOZEN
M_REG_CTRL1	0x02 🗸		VPRE_PD_DIS	RESERVED						
		R 0x0	RESERVED		RESERVED	RESERVED	RESERVED	RESERVED		RESERVED

For write, provide write value and click the "W" button (<u>Figure 53</u>). The write value can be provided as raw number (hexadecimal or decimal), with use of bit buttons or register value helper. The status icon changes to modified until a write action happens.

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		W 0x10	_	VPRE_PD_DIS	VPDIS	BOOSTDIS	BUCK1DIS	BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS	
✓ M_REG_CTRL1	0x02	w uxiu		RESERVED	VPEN	BOOSTEN	BUCK1EN	BUCK2EN	BUCK3EN	LDO1EN	LDOZEN	
M_REG_CTRL1		R 0x0		VPRE_PD_DIS	RESERVED	RESERVED	RESERVED	vable request of BUCK1	RESERVED	RESERVED	RESERVED	
		n 000		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
											aa	a-045

Figure 54. FS8xx0 register write example

The register value helper encodes and decodes feasible register value options in userfriendly way.

				w c			VPRE_PD_DIS	VPDIS		BOOSTDIS	BUCK1DIS		BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS
√	M_REG_CTRL1	0x02		w	_	0	VPRE_PD_DIS:	No_effect	*	VPRE_PD_D	IS: No_effect		BUCK2EN	BUCK3EN	LDO1EN	LDO2EN
				R	0x0	- L 2	Click to display hints f	or decoded register value.	*		100000		RESERVED	RESERVED	RESERVED	RESERVED
							BOOSTDIS:	No_effect	*		1000		RESERVED	RESERVED	RESERVED	RESERVED
				w	)×0		BUCK1DIS:	No_effect	-				BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG
	M REG CTRL2	0x03	0			0	BUCK2DIS:	No_effect	-		1000000000000		VPRESRLS[0]	RESERVED	VPRESRHS[1]	VPRESRHS[0]
	m_nLO_CINL2	0XUS	×	R	0x9		BUCK3DIS:	No_effect			Successore <mark>s</mark>		BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG
				IN.	0.5		LDO1DIS:	No_effect	*		100000000		VPRESRLS[0]	Bit2	VPRESRHS[1]	VPRESRHS[0]
					_		LDO2DIS:	No_effect	*		1.00		Bit11	Bit10	Bit9	BitB
		0x04		W		ิด	VPEN:	No_effect	*		2010/004		AMUX[3]	AMUX[2]	AMUX[1]	AMUX[0]
	M_AMUX	0x04	<b>~</b>			U	BOOSTEN:	No_effect	*				RESERVED	RESERVED	RESERVED	RESERVED
				R	0xe		BUCK1EN:	BUCK1_enable_request	*	35005	20000		AMUX[3]	AMUX[2]	AMUX[1]	AMUX[0]
							BUCK2EN:	No_effect	+		The second second second	1	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT_PHASE[1]	FOUT_PHASE[0]
			-	w	x0	_	BUCK3EN:	No_effect	+		10000		CLK_TUNE[3]	CLK_TUNE[2]	CLK_TUNE[1]	CLK_TUNE[0]
	M_CLOCK	0x05	9			0	LDO1EN:	No_effect	*			1	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT_PHASE[1]	FOUT_PHASE[0]
				R	0x0		LDO2EN:	No_effect	*		100000		CLK_TUNE[3]	CLK_TUNE[2]	CLK_TUNE[1]	CLK_TUNE[0]

Figure 55. FS8xx0 register value helper

In case the read or write operation fails, the status icon changes to red cross (Figure 56).

		W 0x10	VPRE_PD_DIS	VPDIS	BOOSTDIS	BUCK1DIS	BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS
A DEC CTRL4	0x02 🗙	W UXIO	RESERVED	VPEN	BOOSTEN	BUCK1EN	BUCK2EN	BUCK3EN	LDO1EN	LDO2EN
M_REG_CTRL1	0x02	R 0x0	VPRE_PD_DIS	RESERVED						
		K 0x0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
										а

Figure 56. FS8xx0 operation fails icon

All value changes are stored locally until user explicitly confirms them via R/W buttons. If user decides to confirm the changes all at once, simply select all register items and use the related operation buttons above the current page. (Figure 57)

W	Vrite	Read	Сору	Reset
				aaa-04581.

Figure 57. FS8xx0 R/W button

The buttons operate as follows:

- Write: writes all selected registers.
- Read: reads all selected registers.
- Copy: copies read out values to write values for all selected registers.
- Reset: resets modified values to their last know values for all selected registers.

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				W	0x0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
7	M_FLAG	0x00				0	RESERVED	RESERVED	RESERVED	SPILMUCLK	SPI_M_REQ	SPLM_CRC	I2C_M_CRC	I2C_M_REQ
		D.		R	0x0		COM_ERR	WU_G	VPRE_G	VBOOST_G	VBUCK1_G	VBUCK2_G	VBUCK3_G	VLDO1_G
							VLDO2_G	Bitő	Bit5	SPIJMUCLK	SPLMLREQ	SPI_M_CRC	I2C_M_CRC	I2C_M_REQ
				w	0x0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
<b>V</b>	M MODE	0x01	0		0.0	0	RESERVED	EXT_FIN_DIS	Bit5	Bit4	Bit3	W2DIS	WIDIS	GOTOSTBY
×	M_WODE	0.01	×	R	0x0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED	PULLOCK.RT
					0.00		EXT_FIN_SEL_RT	Bit6	MAIN_NORMAL	Bit4	Bit3	W2DI5	W1DIS	RESERVED
				w	0.10		VPRE_PD_DIS	VPDIS	BOOSTDIS	BUCK1DIS	BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS
V	M_REG_CTRL1	0x02	1	W	0x10 0x0	0	RESERVED	VPEN	BOOSTEN	BUCK1EN	BUCK2EN	BUCK3EN	LDO1EN	LDOZEN
×	M_REG_CIREI	0.02	1	R			VPRE_PD_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
					0.0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
				W			VBSTSR[1]	VBSTSR[0]	BOOSTTSDCFG	BUCK1TSDCFG	BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG
	M_REG_CTRL2	0x03		w	0x0		RESERVED	RESERVED	RESERVED VPRESRLS[1] VPRESRLS[0] RESERVED	VPRESRHS[1]	VPRESRHS[0]			
×	M_KEG_CIKL2	0x05	•	R	0x9	0	VBSTSR[1]	VBSTSR(0)	BOOSTTSDCFG	BUCK1TSDCFG	BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG
					UX9		Bit7	Bit5	Bit5	VPRESRLS[1]	VPRESRLS[0]	Bit2	VPRESRHS[1]	VPRESRHS[0]
							Bit15	Bit14	Bit13	Bit12	Bie11	Bit10	Bit9	Bit8
				W	Oxe	0	Bit7	Bit6	RATIO	AMUX[4]	AMUX[3]	AMUX[2]	AMUX[1]	AMUX[0]
<b>v</b>	M_AMUX	0x04	0	R	0xe		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
				R	Uxe		RESERVED	RESERVED	RATIO	AMUX(4)	AMUX(3)	AMUX[2]	AMUX[1]	AMUX(0)
				_			MOD_CONF	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT_PHASE[1]	FOUT_PHASE[0]
				W	0x0		FOUT_CLK_SEL	EXT_FIN_SEL	FIN_DIV	MOD_EN	CLK_TUNE[3]	CLK_TUNE[2]	CLK_TUNE[1]	CLK_TUNE[0]
$\checkmark$	M_CLOCK	0x05	<b>S</b>			0	MOD_CONF	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT_PHASE[1]	FOUT_PHASE[0]
				R	0x0		FOUT_CLK_SEL	Bitő	FIN_DIV	MOD_EN	CLK_TUNE[3]	CLK_TUNE[2]	CLK_TUNE[1]	CLK_TUNE[0]

If there are more register items than registers per page limit, use the pagination controls to move over pages. (Figure 59)



### 5 FS8510 tabs and features

This section describes the tabs and features specific to the FS8510.

### 5.1 Working modes

The GUI enables users to evaluate the device in the following modes (besides user mode).

- Normal Mode
- Debug Mode
  - Enter: Apply 5 V on the DBG pin before the power switch is turned ON.
  - Leave: Write DBG\_EXIT bit = '1' in FS\_STATES register.
  - Behavior:
    - The Watchdog window fully opens, the Deep Fail-Safe request from the Fail-safe state machine (DFS = 1) is masked, the 8 s timer monitoring of RSTB pin is disabled, the Failsafe output pin FS0B cannot be released, and the OTP emulation and programming of a raw device by SPI/I<sup>2</sup>C is possible.
    - No watchdog refresh is required. Disabling the watchdog allows an easy debug of the hardware and software routines (i.e SPI/I<sup>2</sup>C commands). However, the whole

User	auide
0001	guide

watchdog functionality is kept on (seed, LFSR, WD refresh counter, WD error counter...). WD errors are detected and counted with reaction on the RSTB pin.

- Test Mode
  - Pre-conditions: Device must be in Debug Mode (DBG pin asserted high).
  - Enter/Leave: Send special key-sequence (embedded in the application).
  - Behavior:
    - In this mode, it is possible to configure mirror registers and apply the configuration either temporarily or permanently. See <u>Section 5.4</u> for details.

### 5.2 Communication

The FS8510 supports communication via SPI or  $I^2C$  (SPI only for FS6600). Data frames are assembled according to description in the <u>Figure 60</u> for SPI and respectively in the <u>Figure 61</u> for  $I^2C$ .

The CRC calculation is handled for both types of communication. See the device data sheet for details on CRC calculation.

If the CRC integrity check fails for received data, it is evaluated as invalid response frame and the user is properly informed.

	B31	B30	B29	B28	B27	B26	B25	B24	Ι							
MOSI	M/FS	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0	R/W								
MISO			G	eneral de	vice statu	IS										
	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	<b>B</b> 9	B8
MOSI	Data_15	Data_14	Data_13	Data_12	Data_11	Data_10	Data_9	Data_8	Data_7	Data_6	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
MISO				Extended	device s	tatus, or	device in	nternal co	ontrol re	gister co	ntent o	, device	flags			
									B7	<b>B</b> 6	B5	B4	B3	B2	B1	B0
MOSI									CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0
MISO									CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0
															aa	a-045815
		0.01														

Figure 60. SPI communication frame

B39	B38	B37	B36	B35	B34	B33	B32	B31	B30	B29	B28	B27	B26	B25	B24
			ID_6-0				R/W	0	0	0 Adr_5-0					
	_	Dev	ice Addre	955			Read/Write			Register Address					
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8
Data_15	Data_14	Data_13	Data_12	Data_11	Data_10	Data_9	Data_8	Data_7	Data_6	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
			Data	a MSB							Data	LSB			
								B7	B6	B5	B4	B3	B2	B1	B0
								CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0
											CI	RC			
														aa	a-045816
Figur	e 61. I	<sup>2</sup> C coi	mmun	icatior	n fram	е									

### 5.2.1 Mirror register aliases / transparent access

The device control logic provides transparent access to the main/fail-safe mirror registers.

In order to read/write the desired configuration, specifying data in the **MIRRORDATA** and address + R/W in **MIRRORCMD** registers is usually required.

The GUI addresses the previously mentioned data specification issue so the user can directly address mirror registers using their aliases (**OTP\_CFG\_XXX**).

### 5.3 Generated scripts

This section identifies scripts which can be generated and exported by the GUI.

Table 5. Scripts for export

Script name	Purpose
mirror-otp-config	Enters Test Mode. Configures mirror registers. Commits CRC.
functional-config	Configures functional registers.

### 5.4 Programming

The GUI enables users to program the device with predefined content of mirror registers. This procedure is temporary and is cleared after a system power-down.

**Note:** Ensure that the correct device model is selected matching the samples being used on the kit.

### 5.4.1 Emulation

The emulation procedure enables users to temporarily program the device with a custom configuration.

In order to temporarily program the device, follow these steps:

- 1. Make sure that GUI is in **Test mode**, see <u>Section 5.1</u> for details.
- 2. Load the custom configuration.
  - a. Make a custom configuration using provided tabs.
    - i. Mirrors:Main see <u>Section 5.5.9</u> for details.
    - ii. Mirrors:FailSafe see <u>Section 5.5.10</u> for details.
  - b. Load previously generated script called "**mirror-otp-config**" into the script editor and run it.
- 3. Release DEBUG pin to GND.
- 4. A custom configuration is temporarily programmed and ready to be evaluated.

### 5.5 FS8510 tabs

This section describes the FS8510 specific tabs.

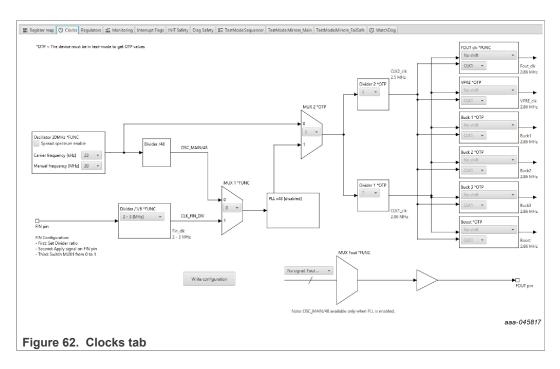
### 5.5.1 Register map tab

See <u>Section 4.6</u> for details on using this tab.

### 5.5.2 Clocks tab

The clocks tab provides clock configuration for voltage regulators. It adapts to selected device modes and enables only accessible options, the rest are grayed out.

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### 5.5.3 Regulators tab

The regulators tab provides configuration options for low voltage regulators and a static calculator for high-voltage buck slope compensation network.

	Lov	v Voltag	Regulators			VPRE compensati	on network calculation
	LV Buck1		LV Buck2 VPRE [V]				
itate in normal mode	Disable	•	State in normal mode	Disable	-	VPRE ILIM [mV]	
ehavior in case of TSD	Regulator_Shutdown	-	Behavior in case of TSD	Regulator_Shutdown	-	Switching Frequency [KHz]	
						Rshunt [mOhm]	
	LV Buck3			LDO1		Cout [uF]	
ate in normal mode	Disable	•	State in normal mode	Disable	-	Lvpre [uH]	
ehavior in case of TSD	Regulator Shutdown	-	Behavior in case of TSD	Regulator Shutdown	•	Rcomp [KOhm]	N/A
				5 -		Ccomp [nF]	N/A
						Chf [pF] Current limit [A]	N/A N/A
	LDO2			VBOOST		Slope compensation [mV/us]	
tate in normal mode	Disable	*	State in normal mode	Disable	-		
ehavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	•		
enavior in case of 13D	Regulator_shutdown	•	benavior in case of 13D	Regulator_shutdown			
		W	ite			C	alculate

### 5.5.4 Monitoring tab

The monitoring tab provides ADC monitoring of possible outputs of the AMUX pin and other pins dedicated for individual voltage regulators.

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	UX Voltages				Measured Input Lines
Input Line           VPDIO           AND_GAP_MAIN           IAND_GAP_FS           VBUCK1           VBUCK2           VBUCK3           VPRE           VBOOST           LDO1           LDO2           VBOSSIN           VAKE1           VAKE2           VANA	Value 3296.0 998.0 998.0 1242.0 1242.0 1242.0 3281.0 4081.0 4081.0 40977.0 33221.0 33221.0 3325.0 40957.0 11592.0	Unit mV mV mV mV mV mV mV mV mV mV mV mV mV	PSVNC - O VPRE O WAKE1 O PSVNC O VDDIO O VDDIO O VDDIG_FS O VBUCK1 O VBOOST	Clear all     VBUCK2     VLDO2     VLDO2     ORAND,GAP_MAIN     VLDO1     VVLDO1     VANA     VLDO1     OVG,MAIN     OBAND,GAP_FS     OVSC5     VSUP1	
DIG_MAIN DIG_FS SYNC	1598.0 1607.0 3300.0 Read	mV mV mV			8- <del>խունադնադնադնադնադնադնադնադնադնադնադնադնադն</del>
Input Line	Value 32:17	Unit *C	DIE_T_	Clear all	Red         V mine         00         V max         00         V mine         00         X max         00         X max         00         V Autoscale X
	Read			0 1 2 3	4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 10 20 21 22 23 24 23 26 27 23 29 30 3 Time[d]

The tab presents two separate charts for monitoring of voltages and temperature.

### 5.5.5 Interrupt flags tab

The interrupt flags tab provides configuration options and an overview for device events. These might be optionally cleared or masked. It can be read out one-time or periodically with polling. Indicators in the status column can be interpreted as no event occurred or event occurred.

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🝿 Register map	Clocks	Regulators	📷 Monitori	ing Interrupt Flags	INIT Safety	Diag Safety	I∃ Test	tMode:Se	equencer	TestMode:Mirrors_
? 🗸 🗘	$\infty$									
		r <mark>/under-vol</mark> atus Clea		Mask			Over-te Status	emperati s Clea		Mask
VSUP UVH	3		_	INT_not_masked	LDO1 shutdo		Status			INT_not_masked
VSUP UVL			_	INT_not_masked	LDO2 shutdo					INT_not_masked
VSUP UV7			_	INT_not_masked	BUCK1 shutd					INT_not_masked
VPRE UVH			_	INT_not_masked	BUCK2 shutd					INT_not_masked
/PRE UVL			_	INT_not_masked	BUCK3 shutd					INT_not_masked
/PRE FB OV	_		_	INT not masked	VBOOST shut					INT not masked
VBOS UVH			_	INT_not_masked	BOS	CO OWN				INT_not_masked
/BOOST UVH				INT not masked	500					intr_not_maskee
VBOOST OV	_			INT not masked						
100031 01	-			INT_HOL_Hasked						
	Write	Read	Poll			V	Vrite	Read	Poll	
		)ver-curren					Misce			
		Over-curren atus Clea		Mask			Misce	llaneou		Mask
.DO1			ar	Mask INT_not_masked	LDO1 ST			llaneou		Mask
			ar		LDO1 ST LDO2 ST			llaneou		Mask
.DO2				INT_not_masked				llaneou		Mask
.DO2 BUCK1				INT_not_masked INT_not_masked	LDO2 ST			llaneou		Mask
LDO2 BUCK1 BUCK2				INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST			llaneou		Mask
LDO2 BUCK1 BUCK2 BUCK3				INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST			llaneou		Mask
LDO1 LDO2 BUCK1 BUCK2 BUCK3 VBOOST VPRE				INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST			llaneou		
LDO2 BUCK1 BUCK2 BUCK3 VBOOST		atus Clea		INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST			ellaneou: Clea	r	INT_not_masked
DO2 BUCK1 BUCK2 BUCK3 /BOOST		atus Clea		INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG			:llaneou: Clea	r	INT_not_maskec
LDO2 BUCK1 BUCK2 BUCK3 VBOOST		atus Clea		INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG			:llaneou: Clea	r	INT_not_masked
JDO2 BUCK1 BUCK2 BUCK3 /BOOST		atus Clea		INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG WK1 RT	v	Status Status	:llaneou: Clea	r	Mask INT_not_masked INT_not_masked

Figure 65. Interrupt flags tab

### 5.5.6 INIT safety tab

The INIT safety tab provides configuration options during the INIT phase. Indicators in the FS0B and RSTB columns can be interpreted as a fault error with impact on (green) or a fault error w/o impact on (red).

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	Fault impact							
Fault source	Settings	FSOB RSTB		Error counters limit		OV/	UV Safe Reaction	n 1
VCOREMON_OV	No_effect 🔻		WD_ERR_LIMIT	8 -	6	VCore ABIST2		No_ABIST
VDDIO_OV	No_effect 🔻		WD_RFR_LIMIT	6 -	6	VDDIO ABIST2 VMon1 ABIST2		No_ABIST No_ABIST
MON1_OV	No_effect 👻		FLT_ERR_CNT_LIMIT	2 👻	6	VMon2 ABIST2		No_ABIST
MON2_OV	No_effect +					VMon3 ABIST2		No_ABIST
VMON3_OV	No_effect 👻					VMon4 ABIST2		No_ABIST
MON4_OV	No_effect 👻							
VCOREMON_UV	No_effect 👻			Safe Inputs			Miscellaneous	
VDDIO_UV	No_effect 👻		FCCU pin config	No_monitoring -	No_monitoring	RSTB pulse duration	10ms -	
MON1_UV	No_effect 👻		FCCU12 polarity FCCU1 polarity		FCCU1_L_FCCU2_H FCCU1_L	Assert RSTB on FS0B sh Disable clock monitorin		RESET_asserted Monitoring_ac
MON2_UV	No_effect -		FCCU2 polarity		FCCU2_L	Disable 8S timer	9	Counter_enabl
/MON3_UV	No_effect 👻				FSOB_RSTB			
MON4_UV	No_effect 👻		ERRMON polarity		Negative_edge			
FCCU12	FSOB 👻		ERRMON timing config	1ms •	8ms			
CCU1	FSOB 👻							
CCU2	FSOB -			Static Voltage Scaling				
RRMON	FSOB -		Static voltage scaling	0mV 👻	OmV			
ND FS IMPACT	No_action 👻							
LT_ERR_IMPACT	No effect 👻							
mpact								
No impact	-							
	Write Read				Write Re	ad		

### 5.5.7 Diag safety tab

The diag safety tab provides configuration options during INIT phase and safety diagnostics.

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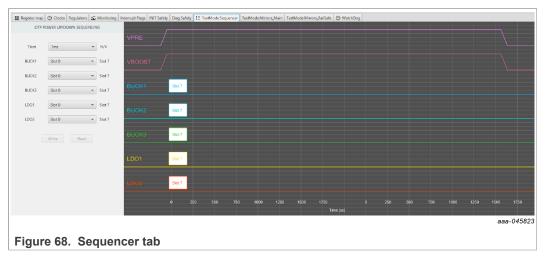
	Safe IO	Diag.	. Safety	INTB	Mask
Report PGOOD event Report PGOOD sense External reset STB driver RSTB sense STB vent STB vent STB request STB request STB driver FSDB driver FSDB sense FSDB diag STSD request	No_failure Power_Good_event_occurred Pad_sensed_high No_external_RESET Command_sensed_high Pad_sensed_high RSET_occurred No_failure Command_sensed_high Pad_sensed_high No_failure	FCCU2 error ERRMON acknowledge ERRMON input error ERRMON input status WD refresh status WD timing SPI CLK status	No_error No_error Low_level Good_WD_refresh Good_WD_refresh No_error No_error Error_detected No_error No_error	VMON4 OV/UV int enable VMON3 OV/UV int enable VMON2 OV/UV int enable VDDIO OV/UV int enable VDDIO OV/UV int enable VCOREMON OV/UV int enable ERRMON int enable FCCU2 int enable FCCU1 int enable	Interruption_NOT_MAS. Interruption_NOT_MAS. Interruption_NOT_MAS. Interruption_NOT_MAS. Interruption_NOT_MAS. Interruption_NOT_MAS. Interruption_NOT_MAS. Interruption_NOT_MAS.
	dog management		V status		nd Status
Vatchdog Type	Simple_WD 👻	VCOREMON OV VCOREMON UV	No_overvoltage Undervoltage_reported	Communication error WD refresh error	Failure Good WD refresh
ood watchdog refresh	WD ANSWER Good	VDDIO OV	No_overvoltage	IO error	No_failure
ad watchdog refresh	WD ANSWER Bad	VDDIO UV	Undervoltage_reported	Voltage monitoring error	Failure
0B release	FS RELEASE FS0B Command	VMON4 OV	No_overvoltage	ABIST1 status	Pass
0B release script	FS0B release script	VMON4 UV	Undervoltage_reported	ABIST2 status	Pass
D ERR CNT	0	VMON3 OV VMON3 UV	No_overvoltage Undervoltage_reported	LBIST_OK status Test Mode Activation Status	Pass Not active
D_RFR_CNT	0	VMON2 OV	No_overvoltage	Leave debug mode	
T_ERR_CNT	0	VMON2 UV	Undervoltage_reported	Debug mode	No_debug
DW_PERIOD	Disable 💌 Disable	VMON1 OV	No_overvoltage	OTP bit corruption	No_error
DW. DC (Duty Cycle)	31.25 - 50	VMON1 UV	Undervoltage_reported	INIT register corruption	No_error
				Fail-safe machine state	NORMAL_FS
	Disable * Disable	rs Osc DRIFT	No_anit		
WDW_DC (Duty Cycle) WDW RECOVERY	31.25 • 50 Disable • Disable	FS DIG REF OV	Undervoltage_reported No_overvoltage No_drift	INIT register corruption Fail-safe machine state	No_error NORMAL_FS

### Figure 67. Diag safety tab

### 5.5.8 Sequencer tab

The sequencer tab provides configuration options for the power-up sequence of regulators.

Each regulator can be assigned to specific slot, which determines power up time during startup.



### 5.5.9 Mirrors:Main tab

The Mirrors:Main tab provides configuration options for the mirror register of the main state machine. It is enabled only if test mode is active.

VPRE				BO	OST				LDOs		
/PRE mode	Force PWM 👻	N/V		Output voltage	5.0V	Ŧ	N/V	VLDO2 current limitation	400mA	~	N/V
Output voltage	3.3V -	N/V		BOOST enable		Ŧ	N/V	VLDO2 output voltage		*	N/V
lope compensation	40mV/us 👻	N/V		BOOST minimum ON time		Ŧ	N/V	LDO2 sequencing slot		~	N/\
Current limitation threshold	50mV -	N/V		VBOOST slope compensation		Ŧ	N/V	Regulator behavior in case of TSD		*	N/\
ow Side slew rate control	130mA -	N/V		Compensation Network Resistor Rcomp		٣	N/V	VLDO1 current limitation		~	N/\
ligh Side slew rate control	130mA -	N/V		Compensation Network Capacitor Ccomp	125pF	٣	N/V	VLDO1 output voltage		~	N/1
/PRE phase (delay) selection	NoDelay 👻	N/V		VBOOST current limitation		v	N/V	LDO1 sequencing slot		~	N/1
Delay to turn OFF VPRE at device power down	250us 👻	N/V		VBOOST Low Side slew rate control		٣	N/V	Regulator behavior in case of TSD		~	N/1
/PRE clock selection	CLK_DIV1 👻	N/V		BOOST phase (delay) selection		٣	N/V				
				BOOST clock selection		٣	N/V				
				Regulator behavior in case of TSD		Y	N/V				
/BUCK1 output voltage	0.8V	÷	N/V	VBUCK2 output voltage	0.8V 👻	N,	v	VBUCK3 output voltage	1.0V	÷	N/
BUCK1	0.91/		NAZ		СК2	L N	N/		UCK3		. NO
BUCK1 inductor selection		v	N/V	BUCK2 inductor selection.	tuH 👻	N,	v	BUCK3 enable		Ŧ	N/
/BUCK1 current limitation		v	N/V	BUCK2 enable	Disabled 👻	N,	v	BUCK3 inductor selection		v	N/
/BUCK1 & VBUCK2 multiphase operation		~	N/V	VBUCK2 current limitation	2.6A 👻	N,	v	VBUCK3 current limitation		÷	N/
BUCK1 Compensation Network		Ť	N/V	BUCK2 compensation network	16.25GM -	N,	v	BUCK3 compensation resistor		÷	N/
BUCK1 sequencing slot		Ť	N/V	BUCK2 sequencing slot	Slot0 -	N,	v	BUCK3 gain control		~	N/
BUCK1 phase (delay) selection		Ť	N/V	BUCK2 phase (delay) selection	NoDelay 👻	N,	v	BUCK3 sequencing slot		Ť	N/
BUCK1 clock selection		×,	N/V	BUCK2 clock selection	CLK_DIV1 -	N,	v	BUCK3 phase (delay) selection		Ť	N/
		Y	N/V	Regulator behavior in case of TSD	BUCK2 shutdown	N,	v	BUCK3 clock selection		Ť	N/
Regulator behavior in case of TSD		Y	N/V					Regulator behavior in case of TSD		Ť	N/
Regulator behavior in case of TSD BUCK1 and BUCK2 Soft start/stop configurability								Soft start/stop configurability		Ť	N/
-					Read			Write	Read		

### 5.5.10 Mirrors:FailSafe tab

The Mirrors:FailSafe tab provides configuration options for mirror registers of the fail-safe state machine. It is enabled only if test mode is active.

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VM	DN1		VMC	0 <b>N2</b>		VMO	NB	
vervoltage threshold [%]	104.5	▼ N/V	Overvoltage threshold [%]	104.5 -	N/V	Overvoltage threshold [%]	104.5	▼ N/V
vervoltage Filtering Timing (us)		- N/V	Overvoltage Filtering Timing (us)	25 -	N/V	Overvoltage Filtering Timing [us]		• N/V
Indervoltage threshold [%]		▼ N/V	Undervoltage threshold [%]	95.5 -	N/V	Undervoltage threshold [%]		* N/V
ndervoltage Filtering Timing [us]		- N/V	Undervoltage Filtering Timing [us]	5 -	N/V	Undervoltage Filtering Timing [us]		- N/V
ssignment to PGOOD		N/V	Assignment to PGOOD		N/V	Assignment to PGOOD		N/V
ssignment to ABIST1		N/V	Assignment to ABIST1		N/V	Assignment to ABIST1		N/V
fonitoring		N/V	Monitoring		N/V	Monitoring		N/V
Write	Read		Write	Read		Write	Read	
VM	DN4		VDI	DIO		vco	RE	
Overvoltage threshold [%]	104.5	⇒ N/V	Overvoltage threshold [%]	104.5 -	N/V	Overvoltage threshold (BUCK1) [%]	104.5	* N/V
Overvoltage Filtering Timing [us]		≁ N/V	Overvoltage Filtering Timing [us]	25 -	N/V	Overvoltage Filtering Timing [us]		- N/V
Indervoltage threshold [%]		- N/V	Undervoltage threshold [%]	95.5 -	N/V	Undervoltage threshold [%]		* N/V
Indervoltage Filtering Timing [us]		* N/V	Undervoltage Filtering Timing [us]	5 -	N/V	Undervoltage Filtering Timing [us]		* N/V
ssignment to PGOOD		N/V	Assignment to PGOOD		N/V	Assignment to PGOOD		N/V
Assignment to ABIST1		N/V	Assignment to ABIST1		N/V	Assignment to ABIST1		N/V
Aonitoring		N/V	Voltage selection	3.3V -	N/V	Monitoring voltage (VBUCK1)		- N/V
Write	Read		Write	Read		Write	Read	
		Misce	llaneous					
VS max value allowed NoSVS	- N		RSTB assignment to PGOOD		N/V			
Vatchdog monitoring			-	ile_WD 👻	N/V			
RRMON monitoring			FCCU monitoring		N/V			
ault recovery strategy			Device I2C address	Ţ	N/V			
		Write	Read					

#### Figure 70. Testmode mirrors fail-safe tab

### 6 PF502x tabs and features

This section describes the specific tabs and features for the PF5020 and PF5024.

### 6.1 Working modes

The GUI supports following modes in addition to user mode:

- · Run mode (called normal mode in the GUI)
  - Enter: If the power-up state is successfully completed, the state machine transitions to the run state. In this state, RESETBMCU is released high, and the MCU is expected to boot up and set up specific registers on the PMIC as required during the system boot up process. PWRON is pulled high, TBBEN pin is pulled low.
  - Behavior:
    - The run mode is intended for use as the normal mode of operation for the system.
    - Each regulator has specific registers to control its output voltage, operation mode, and/or enable/disable state during the run state.
    - In a typical system, each time the processor boots up (PMIC transitions from off mode to run state), all output voltage configurations are reset to the default OTP

configuration and the MCU should configure the PMIC to its desired usage in the application.

- Standby mode (called normal mode in the GUI)
  - Enter: The standby state is entered when the STANDBY pin is pulled high or low as defined by the STANBYINV bit. The STANDBY pin is pulled high/low by the MCU to enter/exit system low-power mode.
  - Behavior:
    - The standby state is intended for use as a low power (state retention) mode of operation. In this state, the voltage regulators can be preset to a specific low power configuration in order to reduce the power consumption during system sleep or state retention modes of operations.
    - Each regulator has specific registers to control its output voltage, operation mode, and/or enable/disable state during the standby state.
    - At power-up, the standby registers are loaded with the same default OTP values as the run mode. The MCU is expected to program the desired standby values during boot up.
- TBB mode
  - Enter: In order to access the TBB mode, pull the the TBBEN high and PWRON low.
  - Behavior:
    - Allows a temporary configuration to debug or test a customized power-up configuration in the system.
    - In TBB mode, the following conditions are valid:
      - $I^2 C$  communication uses standard communication with no CRC and secure write disabled.
      - Default I<sup>2</sup>C address is 0x08 regardless of the address configured by OTP.
      - Watchdog monitoring is disabled (including WDI and internal watchdog timer).
    - The device communicates through I<sup>2</sup>C as long as VDDIO is provided to the PMIC externally.

### 6.2 Communication

The PF502x devices integrate an  $I^2C$  interface for data transfer with speeds up to 3.4 MHz. Common data frame configuration is used: 7bit address with R/W bit, 1 byte for command, and trailing byte for data.

The CRC calculation is handled automatically. See the device data sheet for details on CRC calculation.

In case of CRC integrity check failure when enabled, the data frame is considered invalid and the event is reported via the GUI information panel.

### 6.3 Generated scripts

<u>Table 6</u> identifies the following scripts generated and exported by the GUI.

Script Name	Purpose
tbb-config	Enters TBB mode. Configures mirror registers. Enters run mode in order to apply the configuration.
mirror-registers	Configures mirror registers.
functional-registers	Configures functional registers.

Table 6. Scripts for Export

### 6.4 Programming

The GUI facilitates OTP burning procedures with predefined content of mirror registers. This procedure is temporary and is cleared after a system power-down.

Note: Ensure the correct device model matching the samples used on the kit is selected.

### 6.4.1 Try-Before-Buy evaluation

The Try-Before-Buy evaluation enables users to temporarily program the device with a custom configuration.

Follow these steps to temporarily program the device.

- 1. Ensure sure that the GUI is in **TBB mode**.
- 2. Load the custom configuration.
  - a. Make your custom configuration using the provided tabs. Only relevant configuration items are available or
  - b. Load previously generated script called "**mirror-config**" into the script editor and run it.
- 3. In device panel/scripts, select the script called "**tbb-script**" to be generated into the script editor.
- 4. Run the script.
- 5. The custom configuration is **temporarily** programmed and ready to be evaluated.

### 6.5 PF5020 tabs

This section describes the PF5020 specific tabs.

### 6.5.1 Register map tab

See <u>Section 4.6</u> for details on using this tab.

### 6.5.2 PMIC configuration tab

The PMIC configuration tab provides configuration options for general device operation. It adapts to the selected device mode and enables only accessible options, the rest are grayed out.

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	PWRON Select Value Register Content	OTP Misc Select Value Register Content	Clock Management Select Value Register Content	Watchdog Select Value Register Content
PWRON Function Reset Push Duration	Control Value         Regular Control           Construction         N/V           Shutdown         Shutdown           2 sec         2 sec           22 ms         22 ms	VZALIS Enable INV VALUE Enable INV VGDDO Checks PWRUP VV VGDDO Checks PWRUP VV USANT Time VIII VIII VIIII VIIII VIIII VIIII VIIII VIIII VIIIII VIIIII VIIIII VIIIII VIIIIII	Deskt Value         Deskter         Deskter           SYNCOUT Exable         Diable         D         Duable           SYNCOUT Exable         Deskte         D         Duable           SYNCUT Exable         Deskte         D         D           SYNCUT Exable         Deskte         D         D           Syncut System         D         D         D           Spread System         D         D         D           Spread System         v/. 5%         +         +/- 5%	Watchdog in Rum Mode         Decide         Decide           Watchdog in STIY Mode         Decide         Decide           Caer Window         Imma         N/V           Watchdog inform         Imma         N/V           Watchdog inform         Imma         Imma           Explation Counter         0         0           WD Mac Fail         0         5           WD Fail Counter         0         0           WD Mac Fail         0         2
	Write Read	Write Read	Write Read	Write Read Poll
PGCOD Mode PGCOD in Run Mode PGCOD in Standby Mode	PCOD Seitet Value Register Content COV V I/V Low Low Low Low Write Read	Fault Control         Register Content           Fault Max         Register Content           Fault Count         0         + 0           Fault Timer         1 ms         +           Write         Read         -	Via Oversultage Lockout         Scient VAu         Register Context           Vin OVLO Externa         Enable         Enable         Finable           Vin OVLO beboarne         10 u         100 us         Vin OVLO Mode         Enable         Enable           Win Externa         Write         Read         Vin OVLO Mode         Vin	Even Power Mode & Standty           Grift Mude Setting         Royalse Contract           OFF Mode Setting         N.V           Bandty Policity         High         High           Write         Read
ZC CRC Enable	Communication Solid Yolan Register Content IV Dosate	Thermal Mostlar           Sector Value         Register Contract           Thermal Monte Enable         Enable         Enable           Montesting Mode         Sampli         Arway on	WDI Control         Register Context           VDI Stent in STBY Mode         Deable           WDI Mode         Setting only           WDI Polarity         Falling only           Witte         Read	Power Up Sequencing         Register Content           Power Up Time Base         300 with 5000
Rown Parter Down Made Graup 2 Delay Graup 2 Delay Graup 4 Delay SESTBMLU Delay WH Graup Assignment WH Graup Assignment DOI Group Assignment DOI Group Assignment	Down Sequences         Replace Content           Select Value         Replace Content           Individ.         Hodridual Power Down           120 uz         120 uz           120 uz         120 uz </td <td></td> <td></td> <td></td>			

Figure 71. PMIC configuration options

### 6.5.3 Functional safety tab

The functional safety tab provides configuration options for functional safety features. It adapts to selected device mode and enables only accessible options, the rest are grayed out.

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			Vo	oltage Mo	nitori	ing	H	ardfaults	Fail-Safe Control
	VMON EN								r -
SW1			Ŧ	105%	Ŧ		PU Fail		Fail-Safe Bypass
SW2			Ŧ		Ŧ		WD Fail		Max. Fail-Safe Transitions
SWND1			Ŧ		Ŧ		REG Fail TSD Fail		Fail-Safe Count 0 👻
LDO1			Ŧ		Ŧ		13018		Fail-Safe OK Timer 1 👻
UV Debo	unce	5 us			*				
OV Debo	ounce	25 us			-				
				Write	Read		Write	e Read	Write Read

#### 6.5.4 LDO regulators tab

The LDO regulators tab provides configuration options for LDO regulators and VSNVS. It adapts to the selected device mode and enables only accessible options, the rest are grayed out.

Image: Register map         Image: Philodom Philadom Philodom Philodom Philodom Philadom Philodom	C LDO Regulators O SW Regulators 4 Interrupts	
	LDO 1	VSNVS
Run Mode           Select Value         Register Content           LDO in Run Mode         Enable           Vout Run Mode         1.5 V         1.8 V	Standby Mode         Register Content           LDO in Standby Mode         Enable           Vout Standby Mode         1.5 V         1.8 V	Select Value Register Content Vout OFF
Common Select Value Register Content LDO1 Mode Normal N/V PG Enable Enable	On Fault Behaviour           Select Value         Register Content           Regulator after Fault         Regula •         Return to previous configuration           LDO on ILIM Fault         Disable •         Remain in previous state           LDO on OV Fault         Disable •         Remain in previous state           LDO on UV Fault         Disable •         Remain in previous state           LDO on UV Fault         Disable •         Remain in previous state           LIM Event Bypass Enable         Trigger Enable         Trigger Enable           UV Event Bypass Enable         Remain in previous state         Remain in previous state	
	Write Read	Write Read

Figure 73. LDO regulator configuration options

### 6.5.5 SW regulators tab

The SW regulators tab provides configuration options for SW regulators. It adapts to selected device mode and enables only accessible options, the rest are grayed out.

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		5W1					SW2		
	Run Mode		Standby Mode		Run Mode			Standby Mo	
	Select Value Register Conte		Select Value Register Content		C	Register Content		Select Va	
Vout Run Mode	0.4000 • 1.100000 V	Vout Standby Mode	0.4000 ~ 1.100000 V	Vout Run Mode	0.4000 *	1.100000 V	Vout Standby Mode	0.4000	<ul> <li>1.100000 V</li> </ul>
SW in Normal Mode	OFF + PWM	SW in Standby Mode	OFF - PWM	SW in Normal Mode	OFF +	PWM	SW in Standby Mode	OFF	<ul> <li>PWM</li> </ul>
	Common		On Fault Event Behaviour		Common			On Fault Event Be	ahaviour
	Select Value Register Conte	nt 📃	Select Value Register Content		Select Value	Register Content		Select Value	Register Content
Phase	45° 🕶 45°	Regulator after Fault	Regula · Return to previous configuration	Phase	45° ~	90*	Regulator after Fault	Regula 👻	Return to previous configuration
Current Limit per Reg.	2.1 A * 4.5 A	SW on ILIM Fault	Regula • Remain in previous state	Current Limit per Reg.	2.1 A 👻	4.5 A	SW on ILIM Fault	Regula +	Remain in previous state
DVS	6.25 m., * 6.25 mV/us	SW on OV Fault	Regula • Remain in previous state	DVS	6.25 m +	6.25 mV/us	SW on OV Fault	Regula +	Remain in previous state
PGOOD Control Enable	Enable	SW on UV Fault	Regula • Remain in previous state	PGOOD Control Enable		Enable	SW on UV Fault	Regula *	Remain in previous state
		WD Bypass Enable	Disable	VTT Mode Enable		Disable	WD Bypass Enable		Disable
		ILIM Event Bypass Enable	Enable				ILIM Event Bypass Enable		Enable
		OV Event Bypass Enable	Enable				OV Event Bypass Enable		Enable
		UV Event Bypass Enable	Enable				UV Event Bypass Enable		Enable
		Write Read					Write Read		



			SWND1		
	Run Mode			Standby Mo	ode
	Select Value	Register Content		Select Va	alue Register Content
Vout	1.00 V 👻	3.30 V	SW in Standby Mode	OFF	▼ PWM
SW in Normal Mode	OFF 👻	PWM			
	Common			On Fault Event B	ehaviour
	Select Value	Register Content		Select Value	Register Content
Phase	45° -	135°	Regulator after Fault	Regula 👻	Return to previous configuration
Current Limit per Reg.	2.1 A 🔹	4.5 A	SW on ILIM Fault	Regula 💌	Remain in previous state
PGOOD Control Enable		Enable	SW on OV Fault	Regula 👻	Remain in previous state
			SW on UV Fault	Regula 💌	Remain in previous state
			WD Bypass Enable		Disable
			ILIM Event Bypass Enable		Enable
			OV Event Bypass Enable		Enable
			UV Event Bypass Enable		Enable
			Write Read		
					aaa-04

Figure 75. SWND1 regulator configuration options

### 6.5.6 Interrupts tab

The Interrupts tab provides configuration options and an overview for device events. These may be optionally cleared or masked. It can be read out one-time or periodically with polling.

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	VIN OVLO Status Clear Mask Sens		Thermal Iatus Clear Mask Sense		SW Mode Status Clear	Mask		Regulator Current Limit Status Clear Mask
VIN OVLO NGOOD Nower Down Nower Up IRC Int Down Event	Write Fand Fand	80°C Threshold 95°C Threshold 110°C Threshold 125°C Threshold 140°C Threshold 155°C Threshold 155°C Threshold Frequency Out of Range Watchdog Interrupt	Nasied Masied Masied Masied Masied Masied Masied Masied Masied Masied Masied Masied Masied Masied	SW1 SW2 SWND1	With Read Pot	Masked Masked Masked	SW1 SW2 SWHD1 LD01	Write Read Poll
	Regulator Undervoltage Status Clear Mask Sens		tegulator Oversoltage Iatus Clear Mask Sense		ENx Pin Sense	Sense		PWRON Status Clear Mask
W1 W2 WND1 DO1	Masted Masked Masked Masked	SW1 SW2 SWND1 LD01	Marked Marked Marked Marked	EN1 EN2 EN3 EN4	I		PWRON Pushed PWRON Released PWRON Pushed > 1s PWRON Pushed > 2s PWRON Pushed > 3s PWRON Pushed > 6s Bandgap Fault	Masked Masked Masked Masked Masked Masked Masked Masked
	Write Read Poll	W	rite Read Poll		Read Poll			Write Read Poll
itatus 1 Itatus 2 Viode Current Limit Jindervoltage Overvoltage WRDN	System laterupts Status	PU Fail WD Fail REG Fail TSD Fail	Haribadi Hayi					
arly Warning	Read Poll		rite Read Poll					

### 6.6 PF5024 Tabs

This section describes the tabs specific to the PF5024.

### 6.6.1 Register map tab

See Section 4.6 for details on using this tab.

### 6.6.2 PMIC config tab

The PMIC config tab provides configuration options for general device operation. It adapts to the selected device mode and enables only accessible options, the rest are grayed out.

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	PWRON	OTP Misc	Clock Management	Watchdog
WRON Mode Les WRON Function Shu eset Push Duration 2 s	Steel: Value         Registre Content           el sensitive         NV           stat Down         *           sec         *           ses         *           ses         *           32 ms         32 ms	Selet Value         Register Content           VAUE Encode         N/V           PECODD Check at PWEUP         N/V           EWARN Time         Source         N/V           EWARN Time         Double         N/V           EDMLRS Wide         Antonique         N/V           EGMOR Bypess Double         N/V         N/V	Sover Yake         Register Content           SW Frequency         2500 MHz         2500 MHz         2500 MHz           SWCDUT Finals         Disabled         Disabled         Disabled           SYNCIN Register         2000/Hz - 5000/Hz         2000/Hz - 5000/Hz         SV0/W           Synext Spectra         Disabled         N/W         Disabled         N/W           Synext Spectra         Disabled         Disabled         Disabled         Strabled           Synext Spectrum         Disabled         W         Disabled         Strabled         Strable         Strabled         <	Series V Alue:         Registration           Wetchdog in Tilby Mode         Disabled         Disabled           Clear Window         Full mindow *         N/V           Watchdog Timer         1 ms         1 ms           Upbindton Counter         0 *         0           VID Max Eprice         0 *         5           VID Max Eprice         0 *         2
Wr	ite Resd	Write Read	Write Read	Write Read Poll
300D in Run Mode 300D in Standby Iode	PGOOD Select Value Register Content Cov → NV Low → Low Low te Read	Fault Control           Select V/Suiz         Register Content           Fault Max         0         +           Fault Control         0         +           Fault Timer         1 ms         +           Write         Read	Via Overnostage Lackowt Nov OVLD Enable Enabled Vin OVLD Deboune 10 us + 100 us Vin OVLD Mode No Shutdown - Device Shutdown Write Read	Low Power Mode Js Standby Select Value Register Coalt OT Mode Series With Register Coalt OT Mode Series With Active High Write Read
	ommunication act Value Register Content N/V Secure Write Disabled * N/V	Themsel Manifus           Select Value         Register Context           Themsel Monitor Enable         Enabled           Monitoring Mode         On Eve. •	WDI Control           Select Value         Register Content           WDI Event in         Deabled           Stirr Mode         Deabled           VVD Mode         Soft mode         N/V           WDI Polarity         Falling scips         N/V	Power Up Sequencing           Relate Value:         Relate Value:         Relate Value:           Power Up The Soft Soft Soft Soft Soft Soft Soft Soft
W	ite Read	Write Read	Write Read	RESETBICU Slot Assignment OFF  Vite Read
Rower I over Down Mode crop 1 Delay crop 2 Delay crop 2 Delay crop 2 Delay crop 4 Delay SETEMCU Delay VI Group Assignment VI Group Assignment VI Group Assignment SIGO Group Assignment	Down Scquenday         Replay Could and New Down Low Down And Down And And And And And And And And And An			

Figure 77. PMIC configuration options

### 6.6.3 Functional safety tab

The functional safety tab provides configuration options for functional safety features. It adapts to the selected device mode and enables only accessible options, the rest are grayed out.

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			V	oltage Mo	onito	ring		Ha	rdfaults	Fail-Safe Control
	VMON EN					ABIST UV Sense & Write	ABIST OV Sense & Write		Read / Sense Clear	
5W1			*		Ŧ			PU Fail		Fail-Safe Bypass
SW2			Ŧ		Ŧ			WD Fail REG Fail		Transitions
SW3			-		Ŧ			TSD Fail		Fail-Safe Count 0
SW4			Ŧ		Ŧ					Fail-Safe OK Timer
JV Debo	ounce	5 us			-					
OV Deb	ounce	30 us			-					

#### 6.6.4 SW regulators tab

The SW regulators tab provides configuration options for SW regulators. It adapts to the selected device mode and enables only accessible options, the rest are grayed out.

		SW1					sv	N2		
Run Mode			Standby Mode			Run Mode		S	tandby Mode	
Select Va	and a state of the			gister Content		and the second se	er Content		Select Value	Register Conte
/out Run Mode 0.4000	▼ 1.000000 V	Vout Standby Mode		00000 V	Vout Run Mode	0.4000 + 1.00000	00 V 00	Vout Standby Mode	0.4000 👻	1.000000 V
W in Normal Mode OFF	▼ PWM	SW in Standby Mode	OFF T PW	м	SW in Normal Mode	OFF + PWM		SW in Standby Mode	OFF -	PWM
Common		On Fa	ault Event Behaviour			Common		On Fau	ult Event Behaviou	
	alue Register Content		Select Value R			Select Value Regist	ter Content		-	Register Cont
hase 45*	- 45*	Regulator after Fault		revious Config.	Phase	45* * 90*		Regulator after Fault	Disabled -	Previous Confi
urrent Limit per Reg. 2.1 A		SW on ILIM Fault	Disabled 🔻 P	revious State	Current Limit per Reg.	2.1A = 4.5A		SW on ILIM Fault	Disabled 🔻	Previous State
0.25 m	▼ 6.25 mV/us	SW on OV Fault		revious State	DVS	6.25 m ¥ 6.25 n		SW on OV Fault	Disabled 💌	Previous State
GOOD Control Enable	Enabled	SW on UV Fault		revious State	PGOOD Control Enable Voltage Monitor Enable			SW on UV Fault	Disabled -	Previous State
onage Monitor chapte	chaoleo	WD Bypass Enable ILIM Event Bypass Enabl		lypass rigger Enabled	Voltage Monitor Enable	Enable Disab		WD Bypass Enable ILIM Event Bypass Enable		Bypass Trigger Enable
		OV Event Bypass Enable		rigger Enabled				OV Event Bypass Enable		Trigger Enable
		UV Event Bypass Enable		rigger Enabled				UV Event Bypass Enable		Trigger Enable
	Write	Read					Write	Read		
		SW3					sv	N4		
Run Mode			Standby Mode			Run Mode			tandby Mode	
Select Va	lue Register Content		Select Value Re	gister Content		Select Value Regist	er Content	s	Select Value	
out Run Mode 0.4000	lue Register Content	Vout Standby Mode	Select Value Re 0.4000 ¥ 1.0	00000 V	Vout Run Mode	Select Value         Registre           0.4000         ▼         1.00000	er Content	S Vout Standby Mode	Select Value 0.4000 +	1.000000 V
Select Va 0.4000	lue Register Content		Select Value Re	00000 V	Vout Run Mode SW in Normal Mode	Select Value Regist	er Content	s	Select Value	
Select Va out Run Mode 0.4000 W in Normal Mode OFF Common	v Register Content 1.000000 V PWM	Vout Standby Mode SW in Standby Mode	Select Value Re 0.4000	00000 V /M		Select Value         Regist           0.4000         +         1.00000           OFF         +         PWM           Common         -         -	er Content 20 V	S Vout Standby Mode SW in Standby Mode	Select Value 0.4000 • OFF • ult Event Behavior	1.000000 V PWM
Select Va but Run Mode 0.4000 N in Normal Mode OFF Common Select N	ive Register Content           v         1.000000 V           v         PWM           falue         Register Content	Vout Standby Mode SW in Standby Mode On Fa	Select Value Re 0.4000_ • 1.0 OFF • PW ault Event Behaviour Select Value R	00000 V /M egister Content	SW in Normal Mode	Select Value Regist 0.4000	er Content 20 V	S Vout Standby Mode SW in Standby Mode On Fau	Select Value 0.4000 • OFF • It Event Behavior Select Value	1.000000 V PWM Register Cont
Select Va out Run Mode 04000 W in Normal Mode OFF Common Select N hase 45°	Aue Register Content	Vout Standby Mode SW in Standby Mode On Fa	Select Value Re 0.4000_ V 1.0 OFF V PW ault Event Behaviour Select Value R Disabled V P	egister Content Irevious Config.	SW in Normal Mode	Select Value         Regist           0.4000	er Content 20 V	Vout Standby Mode SW in Standby Mode On Fau Regulator after Fault	Select Value 0.4000 • OFF • Ilt Event Behavior Select Value Disabled •	1.000000 V PWM Register Cont Previous Conf
Select Va out Run Mode 04000 W in Normal Mode OFF Common Select 1 hase 45° urrent Limit per Reg. 2.1 A	Aue Register Content	Vout Standby Mode SW in Standby Mode On Fa Regulator after Fault SW on IUM Fault	Select Value Re 0.4000_ * 1.0 OFF * PW ault Event Behaviour Select Value R Disabled * P Disabled * P	egister Content Irevious Config. Irevious State	SW in Normal Mode Phase Current Limit per Reg.	Select Value         Regist           0.4000         *         1.00000           OFF         *         PWM           Common         Select Value         Regist           45°         *         180°           2.1 A         *         4.5 A	ter Content 20 V ter Content	Vout Standby Mode SW in Standby Mode On Fau Regulator after Fault SW on ILIM Fault	Select Value 0.4000 * OFF * It Event Behavior Select Value Disabled * Disabled *	r Register Cont Previous Confi Previous State
Select Va out Run Mode 04000 W in Normel Mode OFF Common Select V hase 45° urrent Limit per Reg. 2.1 A VS 6.25 m	Aue Register Content • 1.000000 V • PWM Alue Register Content • 135 <sup>s</sup> • 4.5.A • 6.25 mV/us	Vout Standby Mode SW in Standby Mode On Fa Regulator after Fault SW on ILIM Fault SW on OV Fault	Select Value Re 0.4000_ * 1.0 OFF * PW select Value R Disabled * P Disabled * P	ooooo v /M egister Content revious Config. Irevious State Irevious State	SW in Normal Mode Phase Current Limit per Reg. DVS	Select Value         Regist           0.4000,         +         1.00000           OFF         +         PWM           Common           Select Value         Regist           45°         +         180°           2.1 A         +         4.5 A           6.25 m         +         6.25 m.	ter Content 20 V ter Content nV/us	SU Vout Standby Mode SW in Standby Mode On Fau Regulator after Fault SW on ILIM Fault SW on VV Fault	Select Value 0.4000	1.000000 V PWM Register Cont Previous Conf Previous State Previous State
Select Va out Run Mode (24000 W in Normal Mode OFF Common Select V hase 45 urrent Limit per Reg. 21 A WS 625 m GGOD Control Enable ()	Register Content 1.00000 V PWM alue. Register Content 135° 45.4 6.25 mVlus Enabled	Vout Standby Mode SW in Standby Mode Regulator after Fault SW on OV Fault SW on OV Fault	Select Value Re 0.4000_ * 1.0 OFF * PW sult Event Behaviour Select Value R Disabled * P Disabled * P Disabled * P	agoto v IM revious Contig. Irevious State revious State revious State revious State	SW in Normal Mode Phase Current Limit per Reg. DVS PGOOD Control Enable	Select Value         Regist           04000+         1.00000           OFF         PWM           Common         Select Value           Select Value         Regist           45'         180''           2.1 A         4.5 A           6.25 m+         6.25 m.           Enabli         Enabli	ter Content 20 V ter Content mV/us ed	SW in Standby Mode SW in Standby Mode On Fau Regulator after Fault SW on ILIM Fault SW on DV Fault SW on UV Fault	Select Value 0.4000 * OFF * It Event Behavior Select Value Disabled * Disabled *	1.000000 V PWM Register Cont Previous Conf Previous State Previous State Previous State
Select Va out Run Mode (24000 W in Normal Mode OFF Common Select V hase 45 urrent Limit per Reg. 21 A WS 625 m GGOD Control Enable ()	Aue Register Content • 1.000000 V • PWM Alue Register Content • 135 <sup>s</sup> • 4.5.A • 6.25 mV/us	Vout Standby Mode SW in Standby Mode On Fa Regulator after Fault SW on IUM Fault SW on OV Fault SW on OV Fault SW on UV Fault SW on UV Fault	Select Value Re 0.4000. + 10 OFF + PW auti Event Behaviour Select Value R Disabled + P Disabled + P Disabled + P	egister Content revious Config. revious State revious State revious State revious State	SW in Normal Mode Phase Current Limit per Reg. DVS	Select Value         Regist           04000+         1.00000           OFF         PWM           Common         Select Value           Select Value         Regist           45'         180''           2.1 A         4.5 A           6.25 m+         6.25 m.           Enabli         Enabli	ter Content 20 V ter Content mV/us ed	SW in Standby Mode SW in Standby Mode On Fau Regulator after Fault SW on ILIM Fault SW on UV Fault SW on UV Fault SW on UV Fault	Select Value 0.4000 * OFF * It Event Behavior Select Value Disabled * Disabled * Disabled *	1.00000 V PWM Register Cont Previous Conf Previous State Previous State Previous State Bypass
Select Va out Run Mode 04200 W in Normal Mode 0FF Common Select V Nase 45° urrent Limit per Reg. 2.1 A VS 6.25 m CSOD Control Enable	Register Content 1.00000 V PWM alue. Register Content 135° 4.5.4 6.255 mV/us Enabled	Vout Standby Mode SW in Standby Mode Regulator after Fault SW on OV Fault SW on OV Fault SW on OV Fault	Select Value Re 0.4000	agoto v IM revious Contigu revious State revious State revious State revious State	SW in Normal Mode Phase Current Limit per Reg. DVS PGOOD Control Enable	Select Value         Regist           04000+         1.00000           OFF         PWM           Common         Select Value           Select Value         Regist           45'         180''           2.1 A         4.5 A           6.25 m+         6.25 m.           Enabli         Enabli	ter Content 20 V ter Content mV/us ed	SW in Standby Mode SW in Standby Mode On Fau Regulator after Fault SW on ILIM Fault SW on DV Fault SW on UV Fault	Select Value 0.4000 * OFF * It Event Behavior Select Value Disabled * Disabled * Disabled *	1.00000 V PWM Register Cont Previous Confi Previous State Previous State Previous State Bypass Trigger Enable
Select Va out Run Mode (24000 W in Normal Mode OFF Common Select V hase 45 urrent Limit per Reg. 21 A WS 625 m GGOD Control Enable ()	Register Content 1.00000 V PWM alue. Register Content 135° 4.5.4 6.255 mV/us Enabled	Vout Standby Mode SW in Standby Mode On 1- Regulator after Fault SW on IUM Fault SW on UV Fault SW on UV Fault SW on UV Fault IUM Event Bypas Fabile IUM Event Bypas Fabile	Select Value Re 0.4000. + 1.0 OFF + PW select Value R Disabled + P Disabled + P Disabled + P Disabled + P Disabled + P Disabled + T Select Value R Disabled + P Disabled + P	ogister Content revious Config. revious State revious State revious State revious State revious State revious State revious State revious State	SW in Normal Mode Phase Current Limit per Reg. DVS PGOOD Control Enable	Select Value         Regist           04000+         1.00000           OFF         PWM           Common         Select Value           Select Value         Regist           45'         180''           2.1 A         4.5 A           6.25 m+         6.25 m.           Enabli         Enabli	ter Content 20 V ter Content mV/us ed	SW in Standby Mode SW in Standby Mode On Stan Regulator after Fault SW on IUM Fault SW on IV Fault SW on IV Fault UM Event Synas Enable	Select Value 0.4000 * OFF * It Event Behavior Select Value Disabled * Disabled * Disabled *	1.000000 V PWM Register Conf Previous Conf Previous State Previous State Previous State Bypass Trigger Enable Trigger Enable
Select Va out Run Mode (24000 W in Normal Mode OFF Select V hate 45° urrent Limit per Reg. (21 A WS 625 m GGOD Control Enable	Register Content 1.00000 V PWM alue. Register Content 135° 4.5.4 6.255 mV/us Enabled	Vout Standby Mode SW in Standby Mode On Fr Regulator after Fault SW on UM Fault SW on UV Fault VO Dypes Enable ILIM Event Bypas Enable	Select Value Re 0.4000. + 1.0 OFF + PW select Value R Disabled + P Disabled + P Disabled + P Disabled + P Disabled + P Disabled + T Select Value R Disabled + P Disabled + P	egister Content Ind revious Config. Irevious State Irevious State Irevious State Irevious State Irevious State Irevious State Irgger Enabled	SW in Normal Mode Phase Current Limit per Reg. DVS PGOOD Control Enable	Select Value         Regist           04000+         1.00000           OFF         PWM           Common         Select Value           Select Value         Regist           45'         180''           2.1 A         4.5 A           6.25 m+         6.25 m.           Enabli         Enabli	ter Content 20 V ter Content mV/us ed	S Vout Standby Mode SW in Standby Mode On Fair Regulator after Fault SW on UV Fault SW on UV Fault SW on UV Fault SW on UV Fault UIM Event Spass Enable UIM Vor Vernt Spass Enable	Select Value 0.4000 * OFF * It Event Behavior Select Value Disabled * Disabled * Disabled *	PWM Register Cont Previous Confi Previous State Previous State Previous State
Select Va but Run Mode 04200 Vin Normal Mode 0FF Common Select V Mate 45° 2.1.A VS 625 m 6.25 m	Register Content 1.00000 V PWM alue. Register Content 135° 4.5.4 6.255 mV/us Enabled	Vout Standby Mode SW in Standby Mode On Fr Regulator after Fault SW on UM Fault SW on UV Fault SW on UV Fault VO Dypes Enable UV Event Bypas Enable UV Event Bypas Enable	Select Value Re 0.4000. + 1.0 OFF + PW select Value R Disabled + P Disabled + P Disabled + P Disabled + P Disabled + P Disabled + T Select Value R Disabled + P Disabled + P	egister Content Ind revious Config. Irevious State Irevious State Irevious State Irevious State Irevious State Irevious State Irgger Enabled	SW in Normal Mode Phase Current Limit per Reg. DVS PGOOD Control Enable	Select Value         Regist           04000+         1.00000           OFF         PWM           Common         Select Value           Select Value         Regist           45'         180''           2.1 A         4.5 A           6.25 m+         6.25 m.           Enabli         Enabli	ter Content 20 V ter Content mV/us ed	S Vout Standby Mode SW in Standby Mode On Fair Regulator after Fault SW on UV Fault SW on UV Fault SW on UV Fault SW on UV Fault UIM Event Spass Enable UIM Vor Vernt Spass Enable	Select Value 0.4000 * OFF * It Event Behavior Select Value Disabled * Disabled * Disabled *	1.000000 V PWM Register Conf Previous Conf Previous State Previous State Previous State Bypass Trigger Enable Trigger Enable

### 6.6.5 Interrupts tab

The interrupts tab provides configuration options and overview for device events. These may be optionally cleared or masked. It can be read out one-time or periodically with polling.

	VIN OVLO		Thermal			SW Mode			Regulator Current Limit	
	Status Clear Mask	Sense	Status Clear Ma			Status Clear	Mask		Status Clear	Mask Se
VIN OVLO	Masked	80°C Threshold	Mask		SW1		Masked	SW1		Masked
SOCD	Masked	95°C Threshold	Mask		SW2		Masked	SW2		Masked
ower Down	Masked	110°C Threshold	Mask		SW3		Masked	SW3		Masked
ower Up	Masked	125°C Threshold	Mask	ed 🖉	SW4		Masked	SW4		Masked
RC	Masked	140°C Threshold	Mask	ed 🖉						
equency Ready	Masked	155°C Threshold	Mask	ed 🔤						
aut Down Event	Masked	Frequency Out of F	ange 📃 🦳 Mask	ed						
		Watchdog Interrup	t 🗾 Mask	ed 🛛						
	Write Read Poll		Write Read Poll			Write Read Poll			Write Read Pol	
	Regulator Undervoltage		Regulator Overvoltage			ENx Pin Sense			PWRON	
	Status Clear Mask	Sense	Status Clear Ma			_	Sense		Status Clear	Mask S
V1	Masked	SW1	Mask		EN1			PWRON Pushed		Masked
V2	Masked	SW2	Mask		EN2			PWRON Released		Masked
13	Masked	SW3	Masi		ENB			PWRON Pushed > 1s		Masked
14	Masked	SW4	Mask	ed 🔤	EN4			PWRON Pushed > 2s		Masked
								PWRON Pushed > 3s		Masked
								PWRON Pushed > 4s		Masked
								PWRON Pushed > 8s		Masked
								Bandgap Fault		Masked
	Write Read Poll		Write Read Poll			Read Poll			Write Read Pol	

Figure 80. Interrupt configuration options



## BYLMP GUI specific tabs and features

This section describes the tabs and features specific to the BYLMP EVB<sup>[1]</sup>.

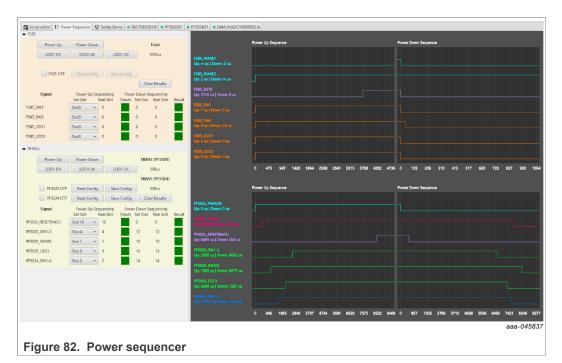
### 7.1 Multi-PMIC / power sequencer

The multi-PMIC / power sequencer tab allows users to evaluate the power up/down sequences of FS85 and PF502x on the BYLMP EVB<sup>[1]</sup>. Both sequencing events are visualized in separate charts for FS85 and PF502x. It also provides a simple table with comparison of set and real-time slots for configurable regulators. Additionally, users are allowed to inject OV/UV/OC faults on selected regulators and evaluate triggered power down sequence.

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**Power Up/Down Control** enables users to regularly power up/down FS85/PF502x. Both actions trigger the signal state capture routine on the MCU. The results are then sent back to the GUI for post-processing (charts, set/real slot comparison).

**Fault Injection** enables users to inject an OV/UV/OC fault either on the FS85 LDO1 or on the PF5020's LDO1 regulator. This action might lead to a device power down event (depends on device configuration). The sequence is captured and processed similarly as above.

**Signal Table** enables users to read and set slots for configurable regulators and clear current results.

**Notice:** If GUI runs fast polling for pin or register values, it might influence accuracy of results due to MCU being clogged with higher priority requests. Solution is to not use polling when working with the power sequencer.

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Device Us	Denver D				Talat	
Power Up	Power D	own			Tslot	
LDO1 OV	LDO2	JV	LDO1 OC		250us	
FS85 OTP	Read Co	nfig	Save Config Set Defaults	Cle	ar Results	]
Signal	Power U Set Slot	p Sequence Real S	-	er Down S Set Slot	equencing Real Slot	Result
FS85_SW1		- 0		6	6	
FS85_SW3		- 0		6	6	
FS85_LDO1		- 0		6	6	
FS85_LDO2		- 0		6	6	
						aaa

In order to read out or modify FS85 OTP values used for slot selection, users must perform the following steps:

- 1. If powered up, power down the PF502x, otherwise the PF502x prevents the FS85 from powering down.
- 2. Ensure the SW1 (WAKE1) on the board is off, otherwise it prevents the FS85 from powering down.
- 3. Power down the FS85 using the dedicated button.
- 4. Set jumper J7 on the board to position 2-3 so the GUI can operate the DBG\_CTRL pin.
- 5. Check the FS85 OTP. The GUI instructs the FS85 to transition into debug/test mode.
- 6. Wait for completion. Once completed, the GUI enables the signal slot selection combo boxes. If transition to debug/test mode fails for any reason, the combo boxes remain disabled (grayed out).
- 7. Modify the signal slot selection as needed.
  - a. Read the configuration to view what the default values are.
  - b. Select the custom slot signal configuration and save the configuration.
  - c. Read the configuration to confirm that the choices were applied as expected.
- 8. Uncheck the FS85 OTP to leave debug/test mode.
- 9. Power up the FS85 with custom signal slot configuration.

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Power Up	Power Do	wn			TBAS	GE (PF5020)	
LDO1 OV	LDO1 U	V	LDC	D1 OC		500us	
					TBAS	SE (PF5024)	
PF5020 OT	P Read Con	ıfig	Save	Config		500us	
PF5024 OT	P Read Con	ıfig	Save	Config	Cle	ar Results	]
Signal	Power Up Set Slot		ncing I Slot		r Down S Set Slot	equencing Real Slot	Result
PF502x_RESETBMCU	Slot 16	• 16	5		0	0	
PF5020_SW1-2	Slot 4	<del>•</del> 4			12	12	
PF5020_SWND	Slot 1	• 1			15	15	
PF5020_LDO1	Slot 3	<b>-</b> 3			13	13	
PF5024_SW1-4	Slot 2	<b>~</b> 2			14	14	

The PF502x allows users to read out and modify the signal slot configuration in both normal mode and TBB (try before buy) mode.

- In normal mode, the PF502x is already powered up, therefore custom changes are only applied to the power down sequence and then the provided configuration is lost.
- In TBB mode, PF502x is not powered up yet, therefore custom changes are applied to power up sequence and possibly also to the power down sequence (if not further modified).

In order to read out or modify the PF502x OTP values used for slot selection, perform the following steps:

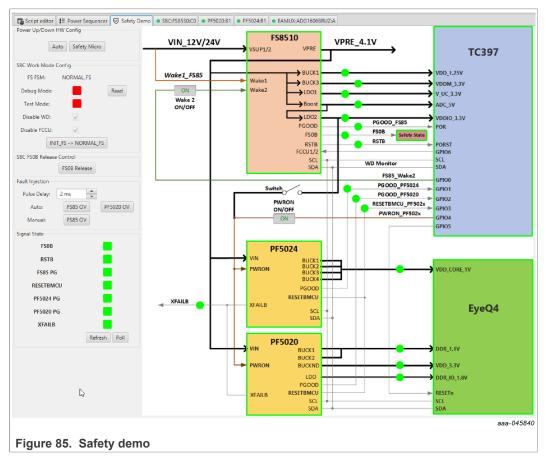
- 1. Power down the PF502x with the dedicated button.
- Check the PF502x OTP. The GUI instructs the PF502x to transition into TBB (try before buy) mode.
- 3. Wait for completion.
- 4. Modify the signal slot selection as needed.
  - a. Read the configuration to view what the default values are.
  - b. Select the custom slot signal configuration and save the configuration.
  - c. Read the configuration to confirm that the choices were applied as expected.
- 5. Uncheck the PF502x OTP to leave TBB mode.
- 6. Power up the PF502x with the custom signal slot configuration.

**Note:** Checking the PF5020 OTP and PF5024 OTP simultaneously is not possible because in TBB mode the PF502x device uses the default  $I^2C$  address and would create ambiguity on  $I^2C$  bus.

**Note:** If the RESETBMCU slot configuration is changed, the RESETBMCU slot configuration for both the PF5020 and the PF5024 device should also be changed. This signal is shared with both chips and different configurations may cause unexpected behavior.

### 7.2 Multi-PMIC / safety demo

The safety demo tab shows the BYLMP Multi-PMIC power solution system block diagram. It facilitates understanding of BYLMP system architecture. Users can check the status of all signals and power rails, operate WAKE2 and PWRON virtual switches, change SBC working mode, release the FS0B, and inject faults on selected regulators.



**Note:** This architecture can be used by multiple MCUs with different pin names, therefore the TC397, and EyeQ4 box names and all related signal names can manually be changed. The GUI remembers the change and will use it for the next run.

**Power Up/Down HW Config** box enables users to control the state of SBC and PMICs. Selection between Auto and Safety Micro should correspond to configuration of jumpers **J20** and **J22** on the BYLMP EVB<sup>[1]</sup>.

- Auto corresponds to the setup when the PF502x PMICs power up/down is triggered by the FS85 LDO2.
- **Safety Micro** corresponds to the setup when the PF502x PMICs power up/down is triggered by the KL25Z output pin (PWRON).

**SBC Work Mode Config** box informs about the current the SBC work mode and enables users to initialize the SBC. Both the mandatory watchdog and FCCU are disabled during this action.

• **FS FSM** stands for fail-safe finite state machine and can enter one of following states (*INIT\_FS, WAIT\_ABIST2, ABIST2, ASSERT\_FS0B and NORMAL\_FS*).

- **Debug Mode** indicator reflects whether the SBC entered Debug mode during startup (DBG = 1).
- **Test Mode** indicator reflects whether the SBC entered test mode, which is mandatory for access to mirror registers.

These values are taken from safety/FS\_STATES register, FSM\_STATE, TM\_ACTIVE and DBG\_MODE bit groups.

**INIT\_FS -> NORMAL\_FS** button performs the following:

- 1. Configure the WD window to be disabled.
- 2. Disable the FCCU.
- 3. Set VMON3 to LDO1.
- 4. Initial good WD refresh to leave INIT\_FS state.
- 5. Leave Debug mode.

SBC power up/down can be operated by both WAKE1 and WAKE2 pins.

In case of **WAKE1**, when turned ON via SW1 on BYLMP EVB<sup>[1]</sup>, DBG is also set to 1 during SBC startup. This leads to a scenario, when SBC ends up in INIT\_FS state, but w/ o constraints on SBC initialization during 256 ms window. In this situation, the user can provide a custom fail-safe configuration which is accessible only in this phase. Once SBC is properly configured (or the defaults are used), later on the user can manually initiate the transition to NORMAL\_FS.

In case of **WAKE2** (assume that WAKE1 = 0), when turned ON via MCU GPIO, DBG remains at 0 during SBC startup. This leads to the scenario when SBC also ends up in INIT\_FS state, but with a constraint on SBC initialization during 256 ms window. Since it would not be possible for the user to meet this timing constraint manually, the MCU handles SBC initialization. It is triggered when WAKE2 and RSTB rising edges are detected. This SBC auto-init feature is available only for WAKE2 and can be useful when RSTB is asserted low due to expiration of the fault error counter (fault injection, wrong watchdog refresh, and so forth).

**<u>SBC FS0B Release Control</u>** box enables the user to execute the FS0B release routine when the FS0B has been asserted low as a configured impact for a fault event.

FS0B release button performs the following:

- 1. Clears the fault error counter.
- 2. Reads the WD seed, reverses it and writes it back.

Basically the **INIT\_FS -> NORMAL\_FS** represents lines 1-4 and **FS0B release** represents lines 5-11 in Figure 86.

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allenger W	Simple WD					
me	Register Name	Data				
	FS_WD_WINDOW	0x0200				
8	FS_NOT_WD_WINDOW	0xFDFF				
	FS_WD_ANSWER	0xA54D				
	FS_STATES	0x4000				
	FS_WD_ANSWER	0x4A9A				
	FS_WD_ANSWER	0x9535				
	FS_WD_ANSWER	0x2A6A				
	FS_WD_ANSWER	0x54D4				
	FS_WD_ANSWER	0xA9A9				
	FS_WD_ANSWER	0x5353				
	FS_RELEASE_FS0B	0x6565				

Figure 86. FS0B release sequence after POR from Debug mode

**Fault Injection** box enables the user to inject OV fault either on the FS85 LDO1 or the PF5020's LDO1 regulator. In the case of the FS85, each fault injection increments the fault error counter. Depending on the configuration, it might assert FS0B and RSTB. Once the fault error counter expires, SBC is shut down. This leads to a change in the signal states represented by indicators. If SBC was operated via WAKE1, it ends up in 4 s auto-retry loop (or shutdown) due to DBG=0, therefore missing the mandatory 256 ms window for SBC initialization. If the SBC was operated via WAKE2, the auto-init feature kicks in and reinitializes the SBC.

- **Pulse Delay** can be used for customization of the fault injection pulse length on given power rail.
- Auto triggers the fault injection pulse with a specified delay.
- Manual triggers the fault injection until the user releases the button.

<u>Signal State</u> box reflects the state of all signals used in this setup. It can be manually refreshed or polled each second.

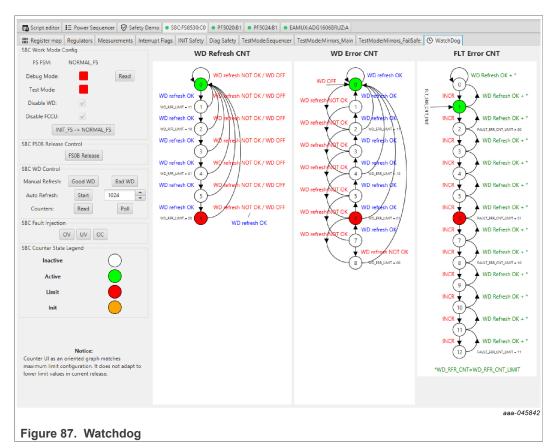
#### Conditions used for box colors.

- The FS85 box is set to green if VPRE went up, otherwise it remains gray.
- The TC397 box is set to green if RSTB went up, otherwise it remains gray.
- The PF5020 box is set to green if PWRON, VPRE, PF5020\_PGOOD, and RESETBMCU went up, otherwise it remains gray.
- The PF5024 box is set to green if PWRON, VPRE, PF5024\_PGOOD, and RESETBMCU went up, otherwise it remains gray.
- The EyeQ4 box is set to green if PGOOD and RESETBMCU went up, otherwise it remains gray.
- The FS0b box is set to green if FS0B went up, otherwise it remains red.

### 7.3 FS85 (SBC) / watchdog

The watchdog tab enables users to evaluate the SBC watchdog, which is considered to be an essential safety feature. It can be operated in both work modes of the SBC, debug and normal.

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**<u>SBC Work Mode Config</u>** box informs the user about the current work mode of the SBC and enables the user to initialize the SBC. Both mandatory watchdog and FCCU are disabled during this action. See <u>Section 7.2</u> for a full description of this box.

**<u>SBC FS0B Release Control</u>** box enables users to execute the FS0B release routine when the FS0B has been asserted low as a configured impact for a fault event. See <u>Section 7.2</u> for a full description of this box.

**<u>SBC WD Control</u>** box enables the user to operate the watchdog either manually or automatically via MCU timers.

- **Manual Refresh** sends single watchdog good/bad refresh command, which results in WD refresh/error counter change.
- Auto Refresh enables/disables the timer on the MCU, which periodically executes the routine sending a good watchdog refresh.
- Counters can be read only once or polled with a period matching the auto refresh. The minimum is set to 100 ms due to GUI ⇔ MCU communication speed limits. The maximum is set to 1000 ms and the value can be adjusted with 50 ms steps. These values are taken from the Write\_INIT\_Safety/FS\_I\_WD\_CFG and FS\_I\_FSSM registers.

**SBC Fault Injection** box enables the user to inject OV, UV, or OC fault on the FS85's LDO1 regulator. Each fault injection increments the fault error counter, and depending on the configuration, might assert FS0B and RSTB. Once the fault error counter expires, the SBC is shut down. If the SBC was operated via WAKE1, it ends up in 4 s auto-retry loop (or shutdown) due to DBG=0, therefore missing the mandatory 256 ms window for SBC initialization. If the SBC was operated via WAKE2, the auto-init feature kicks in and reinitializes the SBC.

**<u>SBC Counter State Legend</u>** describes the color code used in state machines representing WD refresh, WD error, and fault error counters.

### 7.4 ADG1606BRUZ (EAMUX) / Monitoring

The ADG1606BRUZ (EAMUX) / monitoring tab provides users with all possible measured inputs on EAMUX in a visual format. Refer to the BYLMP EVB<sup>[1]</sup> schematics for details.

EAMU	X Voltages							Measu	red Inpu	ut Lines							
Input Line           VD0 1V/5 ADC           //D0M,33/3_ADC           //D0M,33/3_ADC           //D0M,33/3_ADC           //B0AC           //B0AC           //B0AC           //B0AC           //D0AC           //D0AC           //D0AC           //D0AC           //D0AC           //D0AC           //D0AC           //D0AC	Value 1243.0 3289.0 3299.0 3300.0 2496.0 2038.0 1097.0 3270.0 3270.0 3270.0 3270.0 3291.0 995.0	Unit mV mV mV mV mV mV mV mV mV mV	TELE.         +         -           O VPRE_ADC         VDDM_3V3_ADC         VDD_3V3_ADC           O VDD_3V3_ADC         O VDD_3V3_ADC         O VDD_3V3_ADC           O DDR_1V4_ADC         O VDD_CORE_1V0_ADC         V VDD_CORE_1V0_ADC           O VDD_CORE_1V0_ADC         O VDD_1V25_ADC         O VDD_1V25_ADC           O VDDD_1V55_ADC         O VDD_1V1_ADC         O VDD_1V3_ADC	Clear all 3.500 3.000 2.500 2.500 1.000 500 0 1.000		0.0 •	Y max: 0.		Y X mi	in: 0.0	X ma	x 30.0	vtoscale	X	• • • •	• • • •	<b>1 1 1 1 1 1 1 1 1 1</b>
	Read										Time [s]						 a-04:

### 8 References

- [1] **BYLMP EVB** *HW Product Summary Page* TBD
- [2] BYLMP GUI SW SW Product Summary Page <u>https://www.nxp.com/design/analog-expert-software-and-tools/flexgui-software-tool-for-evaluation-of-reference-design-kits:FLEXGUI-SW</u>
- [3] **PEmicro's GDB server** *PEmicro's GDB server for Arm download page* <u>http://www.pemicro.com/downloads/download\_file.cfm?download\_id=412</u>
- [4] **GNU Arm GDB** GNU Arm GDB download page https://developer.arm.com/open-source/gnu-toolchain/gnu-rm/downloads
- [5] **FS85** *HW Product Summary Page* <u>https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-for-s32-microcontrollers-fit-for-asil-d:FS8500</u>
- [6] **PF5020** *HW Product Summary Page* <u>https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/multi-channel-5-pmic-for-automotive-applications-4-high-power-and-1-low-power-fit-for-asil-b-safety-level:PF5020</u>
- [7] **PF5024** *HW Product Summary Page* <u>https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/multi-channel-4-pmic-for-automotive-applications-4-high-power-fit-for-asil-b-safety-level:PF5024</u>

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