# BGT60LTR11AIP shield

## XENSIV™ 60 GHz radar system platform

Board version V2.0

## About this document

### Scope and purpose

This application note describes the function, circuitry, and performance of the 60 GHz radar BGT60LTR11AIP shield, part of Infineon's XENSIV™ 60 GHz radar system platform. The shield provides the supporting circuitry to the on-board BGT60LTR11AIP monolithic microwave integrated circuit (MMIC) Infineon's 60 GHz radar chipset with antenna-in-package (AIP). In addition to the autonomous mode configuration, the shield offers a digital interface for configuration and transfer of the acquired radar data to a microcontroller board, e.g., Radar Baseboard MCU7.

### Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems, working with Infineon's XENSIV™ 60 GHz radar sensors.

### Related documents

Additional information can be found in the documentation provided with the Radar Development Kit tool in the Infineon Developer Center (IDC), or from www.infineon.com/60GHz.

# Table of contents

# 1 Introduction

## 1.1 60 GHz radar system platform

The BGT60LTR11AIP MMIC is a fully integrated microwave motion sensor including AIP elements, built-in motion and direction of motion detectors and a state machine allowing fully autonomous operation of the MMIC without any external microcontroller. An integrated frequency divider with a Phase-Locked Loop (PLL) provides VCO frequency stabilization. These features make the small-sized radar solution a compelling, smart and cost-effective replacement for conventional passive infrared (PIR) sensors in low-power or battery-powered applications. The MMIC is designed to operate as a Doppler motion sensor in the 60 GHz ISM-band.

The MMIC has four quad-state (QS1-4) input pins that give the performance parameters flexibility even when it is running in autonomous mode. These pins are used for configuration of the MMIC as explained in section 3.8.

The MMIC supports multiple operation modes, including autonomous mode and SPI mode, which can be selected via the QS1 pin (see Table 4).

In autonomous mode, the detection threshold (or sensitivity) is set via QS2 pin (see Table 5) and has 16 different levels to fulfill a configurable detection range from 0.5 m up to 7 m with a typical human target Radar Cross-Section (RCS). The hold time is also configurable in 16 levels via QS3 pin (see Table 6), which allows detection status holding up to 30 minutes. The device operating frequency can be configured via QS4 pin (see Table 8) and has 4 different possible frequencies between 61.1 and 61.4 GHz for BGT60LTR11AIP MMIC. In this mode, the integrated detectors deliver digital output signals indicating motion and direction of motion (approaching or departing) of a human target.

In SPI mode, a full flexibility regarding radar MMIC parameters configuration e.g., detection threshold, hold time and operating frequency…, is offered by writing into the MMIC registers the wanted configuration, using an external microcontroller unit (MCU). In this mode, the integrated detectors, if not disabled, will also deliver digital outputs indicating motion and direction of motion. If further signal processing is needed, the radar raw data can be extracted and sampled from BGT60LTR11AIP MMIC and then used for developing customized algorithms for maximum performance.

The BGT60LTR11AIP shield demonstrates the features of the BGT60LTR11AIP MMIC and gives the user a “plug and play” radar solution. The shield can also be attached to an Arduino MKR board or an Infineon Radar Baseboard MCU7. A Graphical User Interface (GUI) is available via Infineon Developer Center (IDC) in order to display and analyze acquired data in time and frequency domain.

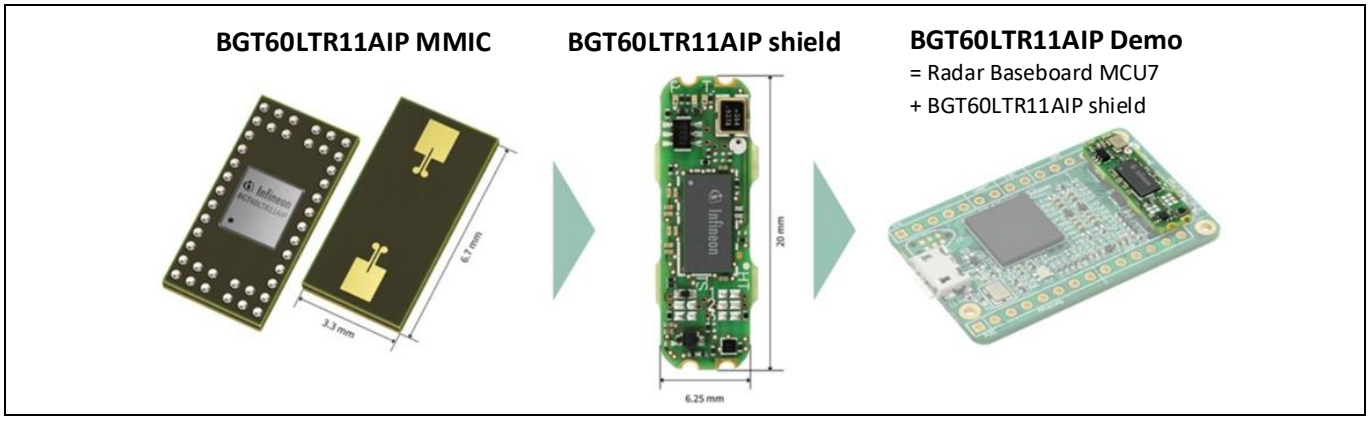



**Figure 1 BGT60LTR11AIP shield using BGT60LTR11AIP MMIC**

## 1.2 Key features

The BGT60LTR11AIP shield is optimized for fast prototyping designs and system integrations, as well as initial product feature evaluations. In addition, the sensor can be integrated into systems like laptops, tablets, TVs, speakers etc. to 'wake' them up based on motion (or direction of motion) detection, put them to sleep or auto-lock when no motion is detected for a defined amount of time. This way, it can be a smart power saving feature for these devices and might also eliminate the need for keyword-based activation of systems. Radar sensors offer the possibility to hide them inside the end product since they operate through non-metallic materials. Therefore, it enables a seamless integration of technology in our day-to-day lives.

Some key features of the BGT60LTR11AIP shield are as follows:

- Form factor of 20 mm x 6.25 mm for the BGT60LTR11AIP shield
- Features an AIP MMIC of small size (6.7 mm x 3.3 mm x 0.56 mm), thereby eliminating antenna design complexity at the user end
- Detects motion and direction of movement (approaching or departing) for a human target
- Works standalone (autonomous mode) or also with SPI mode to interface with an external microcontroller
- Configurable settings like operation mode, detector threshold, detector hold time, operating frequency
- Low-power consumption
- Option to solder onto other PCBs such as Arduino MKR for extra flexibility

# 2 System specifications

Table 1 gives the specification of the BGT60LTR11AIP shield.

**Table 1 BGT60LTR11AIP shield specifications**

| Parameter | Unit | Min. | Typ. | Max. | Comments |
|---|---|---|---|---|---|
| **System performance** | | | | | |
| Detection range | m | – | 5 | 7 | Typical motion detection range for human target at low threshold (in both E-plane and H-plane orientations) |
| **Power supply** | | | | | |
| Supply voltage | V | 1.5 | 3.3 | 5.0 | |
| Current consumption | mA | | 3.48 | | At 3.3V supplied via castellated holes<br>Pulse Repetition Time (PRT) = 500µs<br>Pulse Width (PW) = 5µs<br>(LEDs off) |
| **Antenna characteristics (measured)** | | | | | |
| Antenna type | | | 1 x 1 | | Antenna-in-Package (AIP) |
| Horizontal – 3 dB beamwidth (HPBW) | Degrees | | 80 | | At frequency = 61.25 GHz |
| Elevation – 3 dB beamwidth (HPBW) | Degrees | | 80 | | At frequency = 61.25 GHz |

# 3 Hardware description

This section presents a detailed overview of the BGT60LTR11AIP shield's hardware building blocks, such as BGT60LTR11AIP MMIC, power supply, crystal, and board interfaces.

## 3.1 Overview

The BGT60LTR11AIP shield is a very small PCB of 20 x 6.25 mm size. Mounted on top of the PCB is a BGT60LTR11AIP, Infineon's 60 GHz radar sensor. The antennas are integrated into the chip package; therefore, the PCB can be manufactured using a standard FR4 laminate. The bottom side of the shield has the connectors to the Radar Baseboard MCU7 [1] (P1 and P2 in Figure 2). On the top side of the shield, there is a marker that must be aligned with the marker on the Radar Baseboard MCU7 for correct alignment, as shown in Figure 3. The castellated holes on the edges of the PCB provide additional access to the detector outputs and power supply signals of the shield. By using these castellated holes and removing P1 and P2, the BGT60LTR11AIP shield can be soldered onto other PCBs.

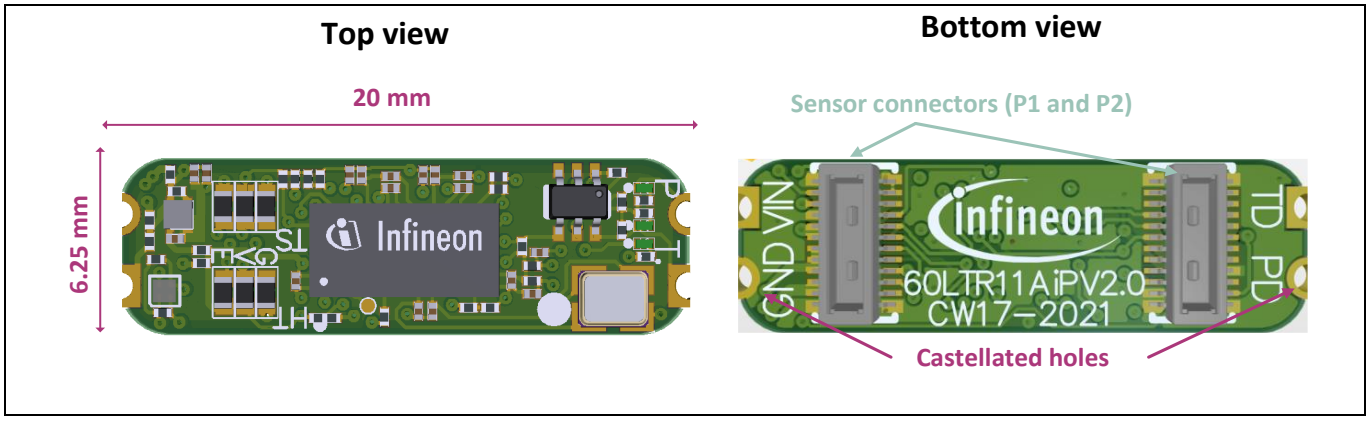



**Figure 2 Top and bottom views of the BGT60LTR11AIP shield**

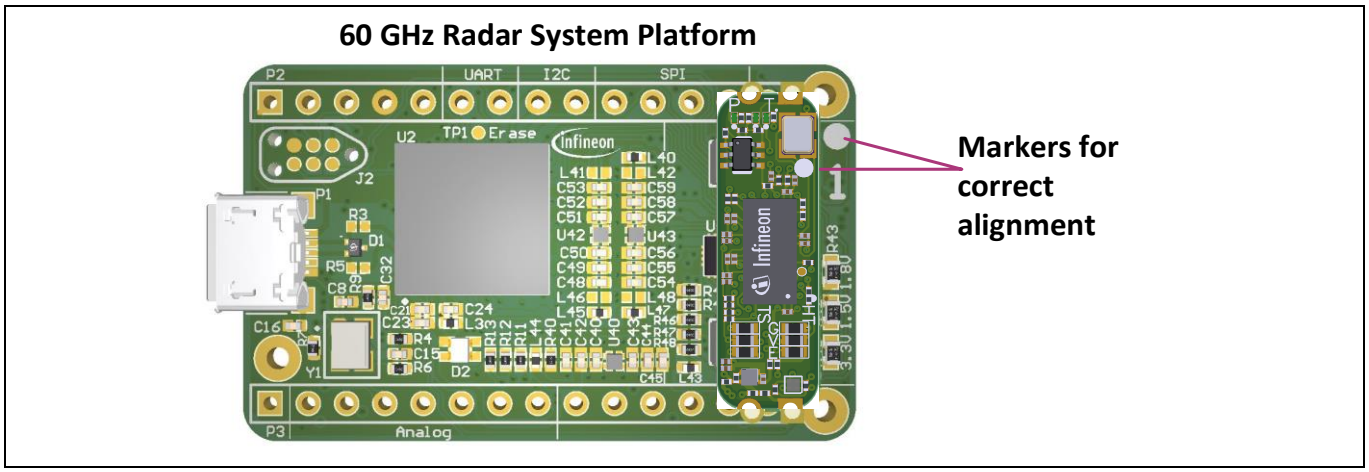



**Figure 3 Markers on Radar Baseboard MCU7 and BGT60LTR11AIP shield for alignment**

*Note: There is a risk of the connectors wearing out when regularly plugged into and unplugged from the shield. To prevent this, do not lift the shield on the short side out of the connector. Instead, simply pull on the long side of the sensor, thereby tilting the short side. This will significantly increase the lifetime of the connectors.*

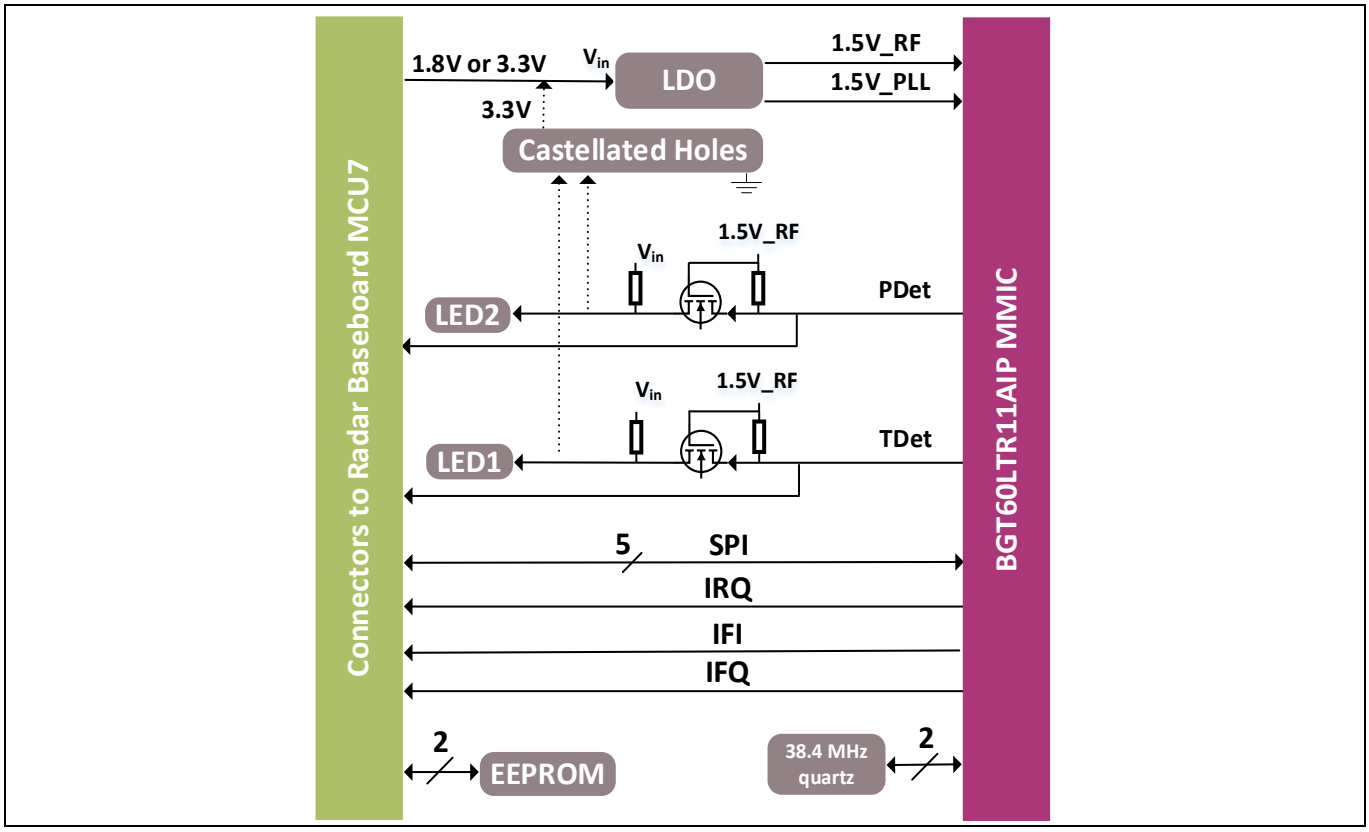



**Figure 4 BGT60LTR11AIP shield block diagram**

The block diagram in Figure 4 depicts the configuration of the shield. When the shield is plugged into the Radar Baseboard MCU7, the MMIC's supplies are initially deactivated. Only the EEPROM is powered. The MCU reads the content of the EEPROM's memory to determine which shield is plugged into the connectors. MMIC's supplies are activated only when the shield has been correctly identified.

Communication with the MMIC is mainly performed via a Serial Peripheral Interface (SPI). The BGT_RTSN allows the MCU to perform a hardware reset of the MMIC. The BGT_SELECT and BGT_RTSN lines of the SPI should be pulled up with 10 kΩ resistors. The interrupt request (IRQ) line can be used to trigger the MCU when new data needs to be fetched.

## 3.2 BGT60LTR11AIP MMIC

The BGT60LTR11AIP MMIC (Figure 5) serves as the main element on the BGT60LTR11AIP shield. The MMIC has one transmit antenna and one receive antenna integrated into the package. The package dimensions are 6.7 mm (± 0.1 mm) x 3.3 mm (± 0.1 mm) x 0.56 mm (± 0.05 mm), as illustrated in Figure 6 and Figure 7.

The MMIC has an integrated Voltage Controlled Oscillator (VCO) and Phase Locked Loop (PLL) for high-frequency signal generation. The transmit section consists of a Medium Power Amplifier (MPA) with configurable output power, which can be controlled via the SPI.

The chip features a low-noise quadrature receiver stage. The receiver uses a Low Noise Amplifier (LNA) in front of a quadrature homodyne down-conversion mixer in order to provide excellent receiver sensitivity. Derived from the internal VCO signal, an RC Poly-Phase Filter (PPF) generates quadrature LO signals for the quadrature mixer.

The Analog Base Band (ABB) unit consists of an integrated sample and hold circuit for low-power duty-cycled operation followed by an externally configurable high-pass filter, a Variable Gain Amplifier (VGA) stage and a low-pass filter.

The integrated target detector circuits in the MMIC indicate the detection of movement in front of the radar and the direction of movement with two digital signals (BGT_TARGET_DET and BGT_PHASE_DET). See section 3.9 for more details. The detector circuit offers a user-configurable hold-time for maximum flexibility.

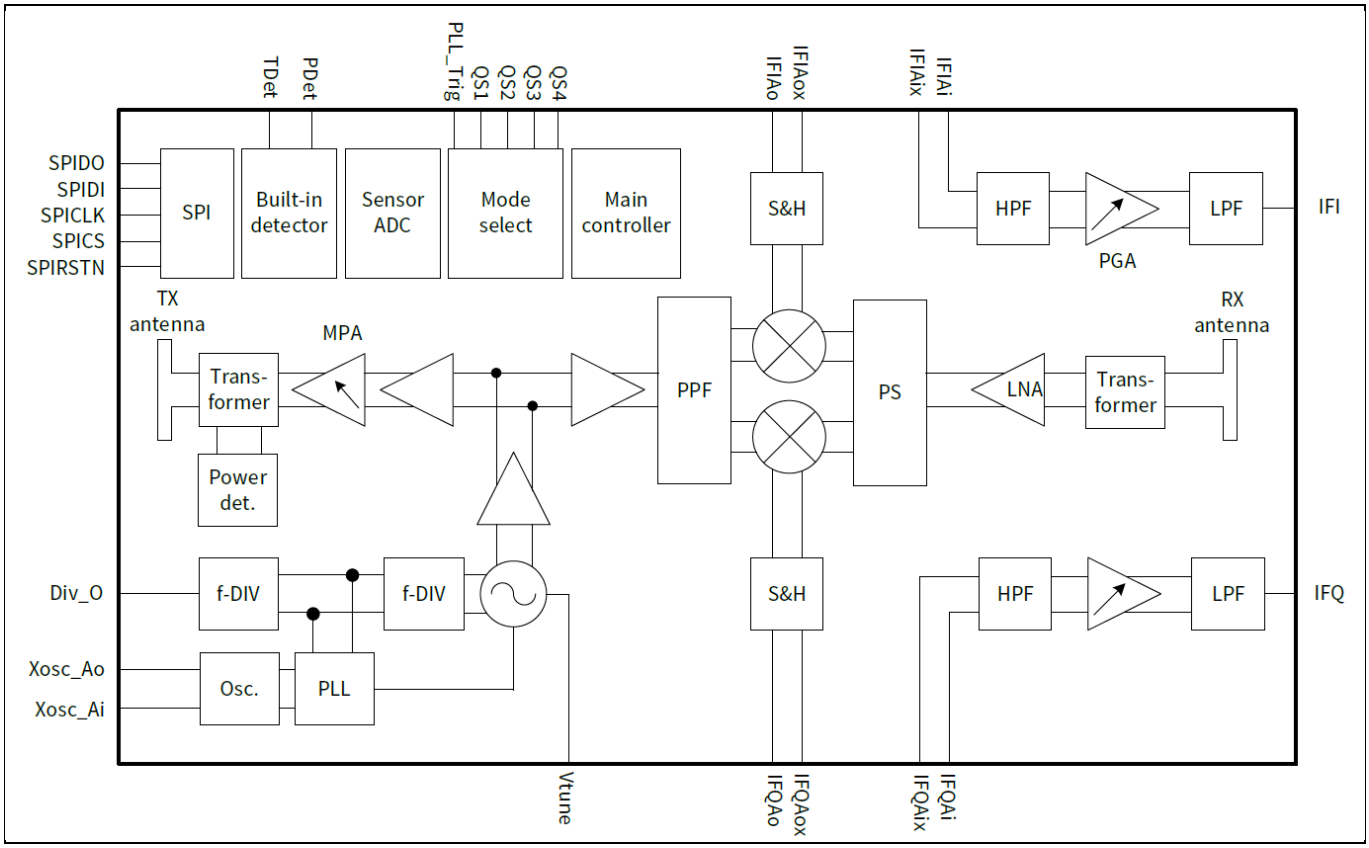



**Figure 5 BGT60LTR11AIP MMIC block diagram**

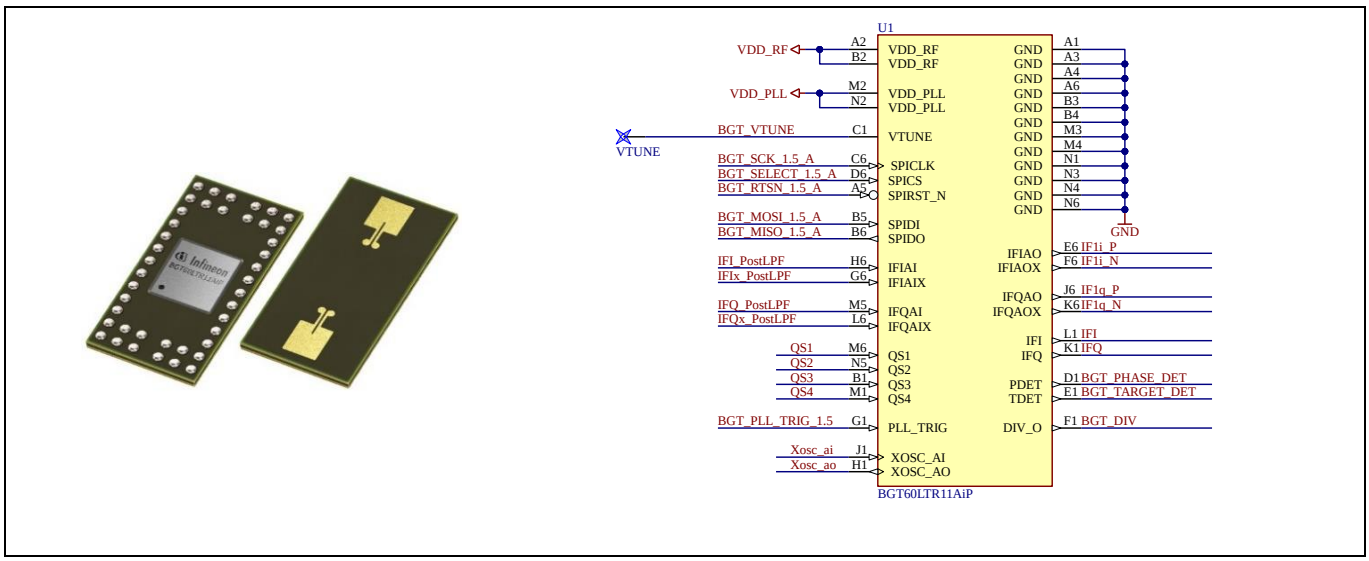



**Figure 6 Package and pin-signal assignment of the BGT60LTR11AIP MMIC**

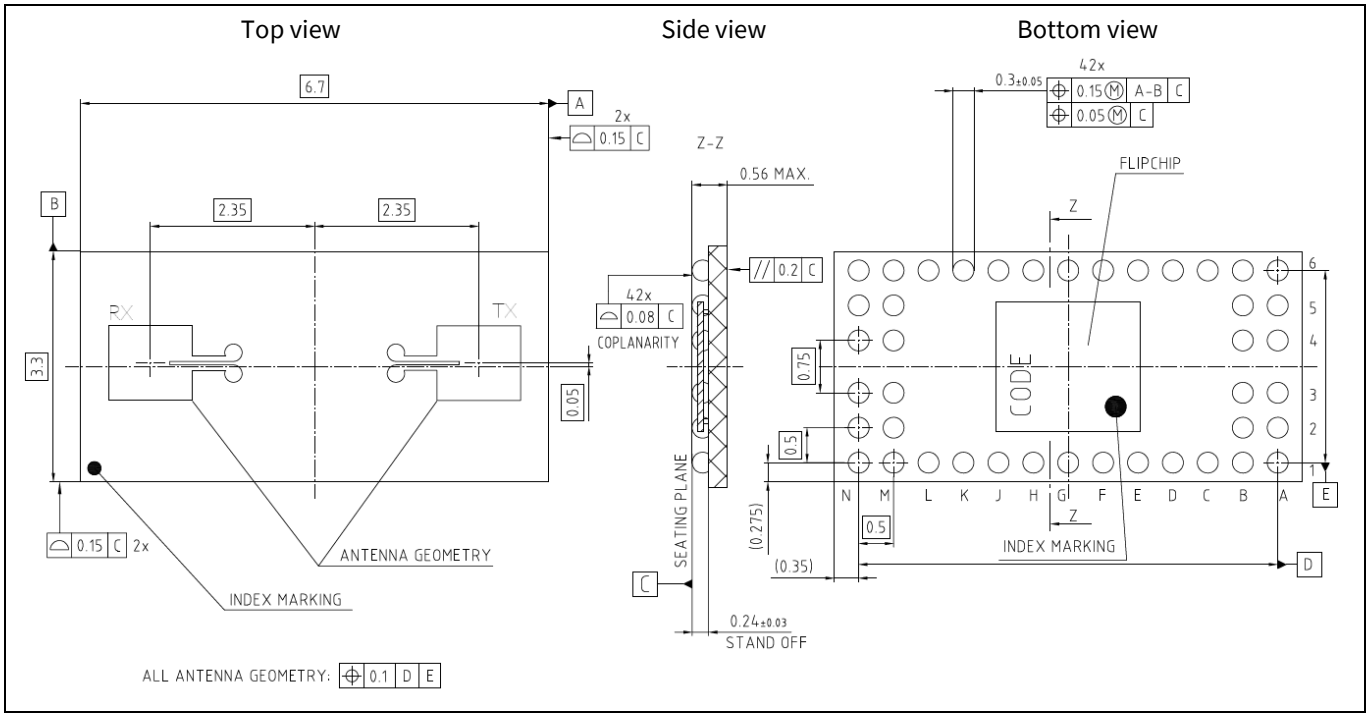



**Figure 7 Top, side, and bottom views of the BGT60LTR11AIP MMIC package – all dimensions in mm**

## 3.3 Sensor supply

Since radar sensors are very sensitive to supply voltage fluctuations or crosstalk between different supply domains, a low-noise power supply as well as properly decoupled supply rails are vital. The Radar Baseboard MCU7 provides a low-noise supply. Figure 8 depicts the schematics of the low-pass filters employed to decouple the supplies of the different power rails in the BGT60LTR11AIP shield. High attenuation of voltage fluctuations in the MHz regime is provided by ferrite beads (L1, L3 and L5). For example, the SPI which runs up to 50 MHz, induces voltage fluctuations on the digital domain, which would then couple into and interfere with the analog domain without the decoupling filters. The ferrite beads are chosen such that they can handle the maximum current of the sensor with a low DC resistance (below 0.25 Ω) and an inductance as high as possible. The high inductance will reduce the cut-off frequency of the low-pass filter, which provides better decoupling for lower frequencies.

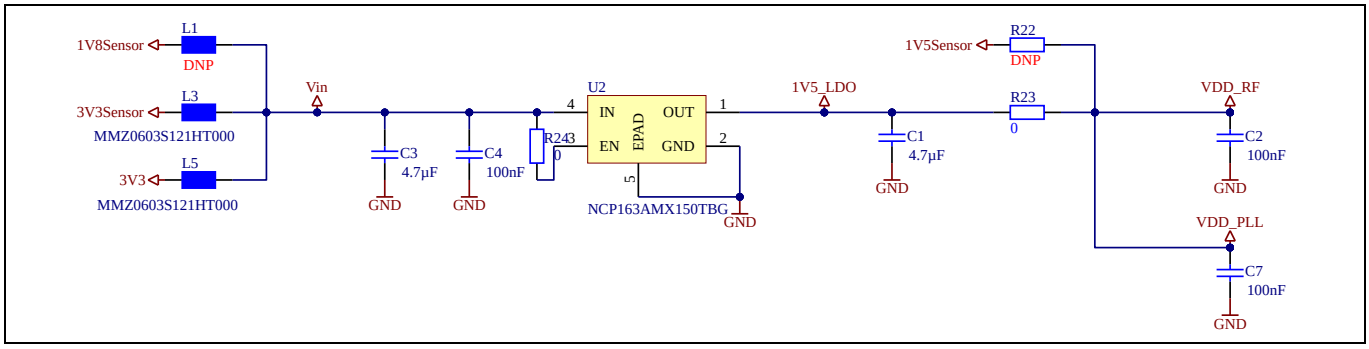



**Figure 8 Schematics of the sensor supply and low-pass filters**

## 3.4 Crystal

The MMIC requires an oscillator source with a stable reference clock providing low phase jitter and low phase noise. The oscillator is integrated inside the MMIC. This saves current consumption, as crystal oscillators consume only a few milliamperes (mA) and run continuously. The BGT60LTR11AIP shield uses a 38.4 MHz crystal oscillator, as shown in Figure 9.

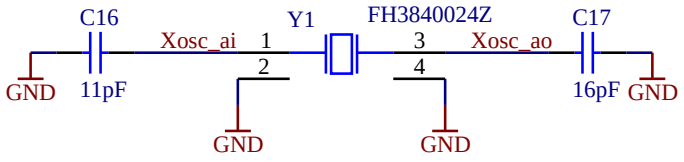



**Figure 9 The crystal circuit on the BGT60LTR11AIP shield**

## 3.5 External capacitors

The BGT60LTR11AIP MMIC is duty-cycled and performs a sample and hold (S&H) operation for lower power consumption. The S&H switches are integrated in chip at each differential IQ mixer output ports. They are controlled synchronously via the internal state machine. The capacitors between S&H and the high-pass filter (HPF) are external (Figure 10). C10, C11, C14 and C15 are 5.6 nF capacitors used as “hold” capacitors for the S&H circuitry. They can be configured for different pulse width settings, as shown in Table 2. C8, C9, C12 and C13 are the DC blocking (or High Pass) capacitors. They should have a value of 10 nF in order to get a high-pass of 4 Hz (if internal high pass resistor, $R_{HP}$ = 4 MΩ). It is not recommended to use higher values as it will affect the Analog Base Band (ABB) settling time. The DC blocking capacitors are important because the mixer output has a different DC voltage than the internal ABB. In Figure 10 the external hold ($C_{hold}$) and high-pass capacitors ($C_{HP}$) are shown for all four branches in the differential IQ configuration.

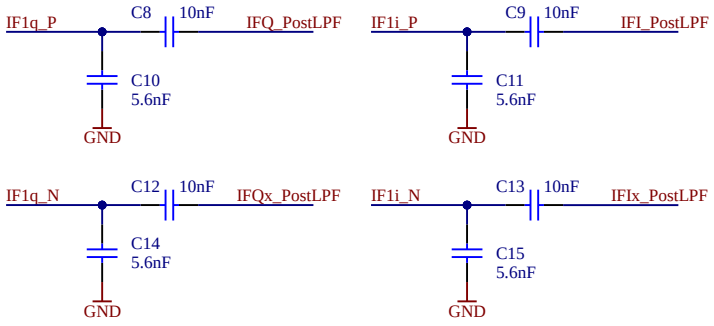



**Figure 10 External capacitors**

**Table 2 Recommended hold capacitors (C10, C11, C14 and C15) for different pulse width values**

| Pulse width (µs) | Hold capacitor value (nF) |
|---|---|
| 3 | 4.7 |
| 4 | 5.6 |
| 5 (default) | 5.6 (default) |
| 10 | 15 |

Charging time of the hold capacitor ($C_{hold}$) is limited to the selected pulse width. Shorter pulse widths require smaller $C_{hold}$ to get it ~ 90% charged during one pulse. Rise-time is controlled by the $C_{hold}$ itself and the internal mixer output resistance ($R_{mixer\_out}$) of 300 Ω in each branch.

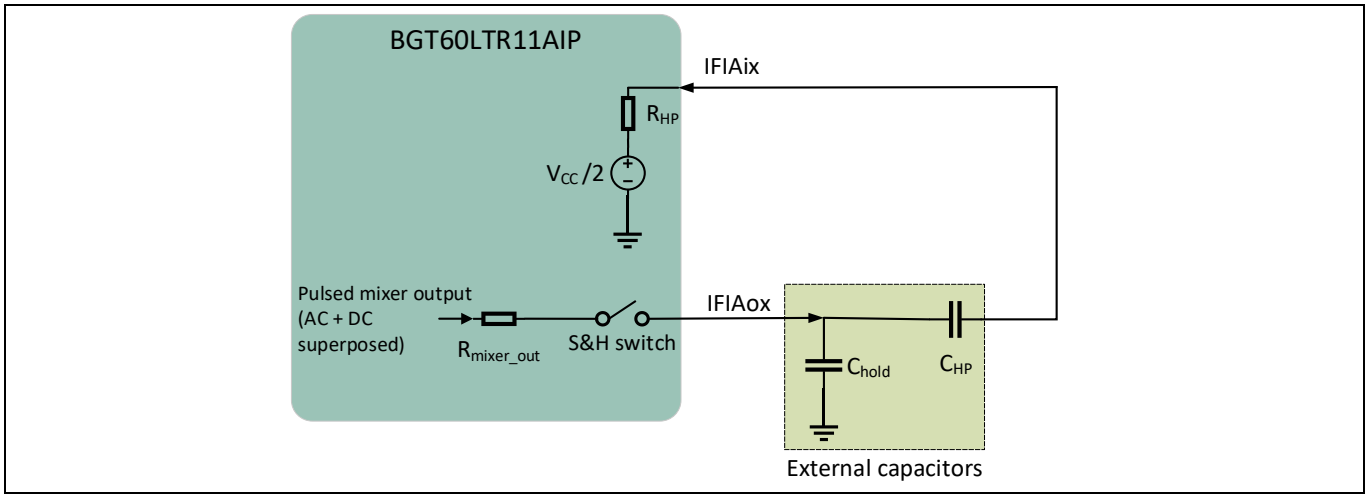



**Figure 11 External capacitors for BGT60LTR11AIP**

Longer pulse width can have a higher $C_{hold}$ value. This leads to a reduced bandwidth (BW) of the RC filter ($R_{mixer\_out}$& $C_{hold}$). Consequently, there will be a lower baseband noise because of reduced noise folding bandwidth.

For this RC structure, the low-pass 3dB cutoff frequency ($f_{LP_{3dB}}$) can be calculated under the following conditions:

$t_{rise}$ = 10% / 90% = S&H ON time = 4µs
Pulse width = 5 µs
$R_{mixer\_out}$ = 300 Ω

$$f_{LP_{3dB}} = \frac{0.35}{t_{rise}} = \frac{0.35}{4\mu s} = 87.5\ kHz$$

Or based on the formula:

$$f_{LP_{3dB}} = \frac{1}{2\pi \times R_{mixer\_out} \times C_{hold}}$$

$C_{hold} = 6.1\ nF$
$\rightarrow 5.6\ nF$ (closest E12 series value)

The high-pass 3dB cutoff frequency ($f_{HP_{3dB}}$) can be calculated under the following conditions:

$C_{HP}$ = 10 nF
$R_{HP}$ = 4 MΩ

$$f_{HP_{3dB}} = \frac{1}{2\pi \times R_{HP} \times C_{HP}} = \frac{1}{2\pi \times 4M\Omega \times 10nF} = 4\ Hz$$

## 3.6 Connectors

The BGT60LTR11AIP shield can be connected to an MCU board, like the Radar Baseboard MCU7, with the P1 and P2 connectors. Visible on the top and bottom side of the PCB are the castellated holes (P3 and P4). TD and PD pins of the castellated holes correspond to the internal detector outputs of the MMIC.

The shield contains two Hirose DF40C-20DP-0.4V connectors, P1 and P2. The corresponding DF40C-20DS-0.4V connectors are on the Radar Baseboard MCU7. Figure 12 illustrates the pin-out of the Hirose connectors of the BGT60LTR11AIP shield.

The signal IRQ is connected with a R5 resistor (0 Ω) to the divider output (BGT_DIV) of the MMIC. In SPI pulsed mode, BGT_DIV generates a signal that acts as an interrupt signal for the MCU to start ADC acquisition. BGT_DIV could also be used to measure divider frequency.

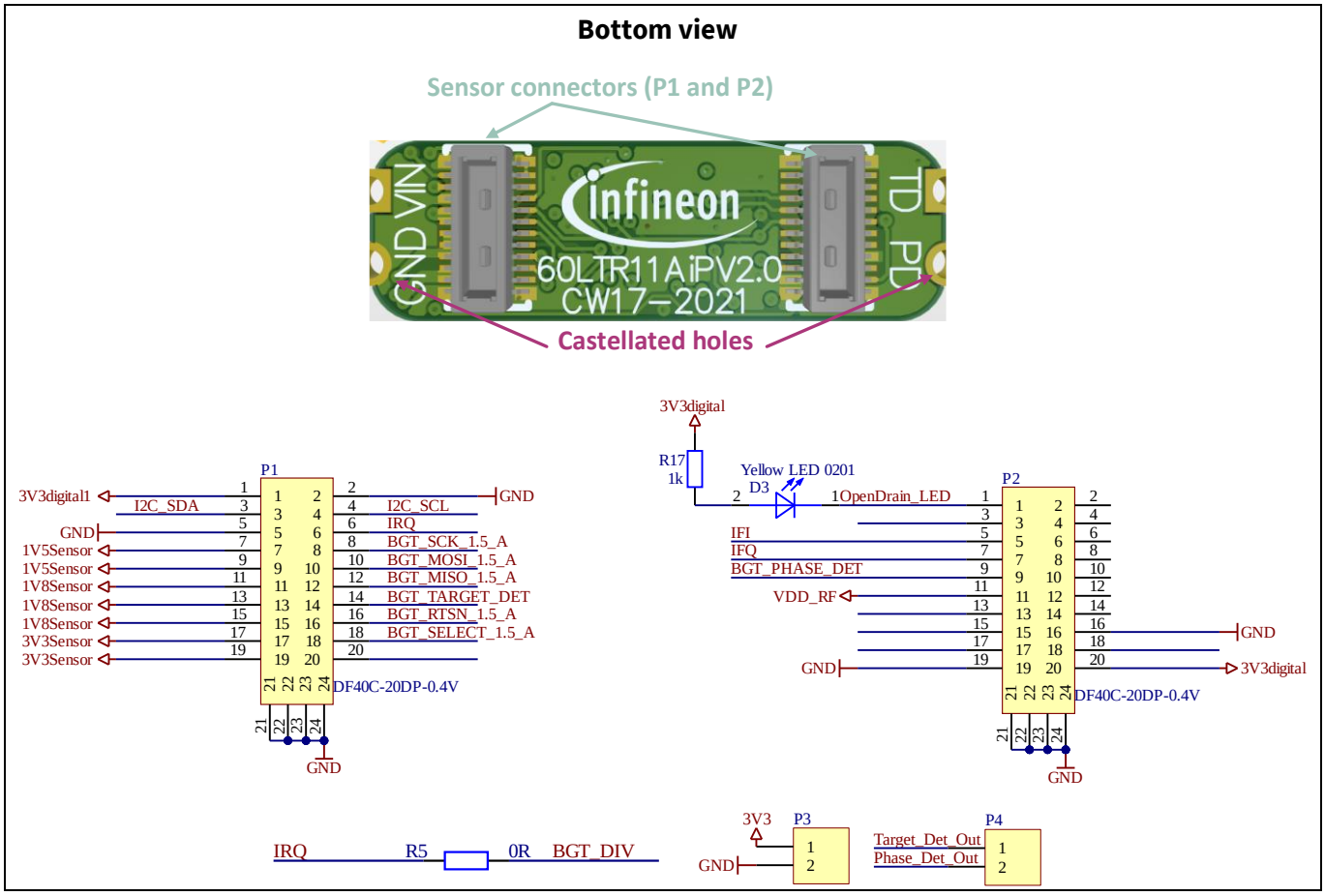



**Figure 12 Connectors on the BGT60LTR11AIP shield, and their pinouts**

## 3.7 EEPROM

The BGT60LTR11AIP shield contains an EEPROM (24CW1280T-I/CS0668) connected via an I²C interface to store data like a board identifier. Its connections can be seen in Figure 13. This EEPROM contains a descriptor indicating the type of the shield board and MMIC. This is used by the firmware to communicate properly with the shield.

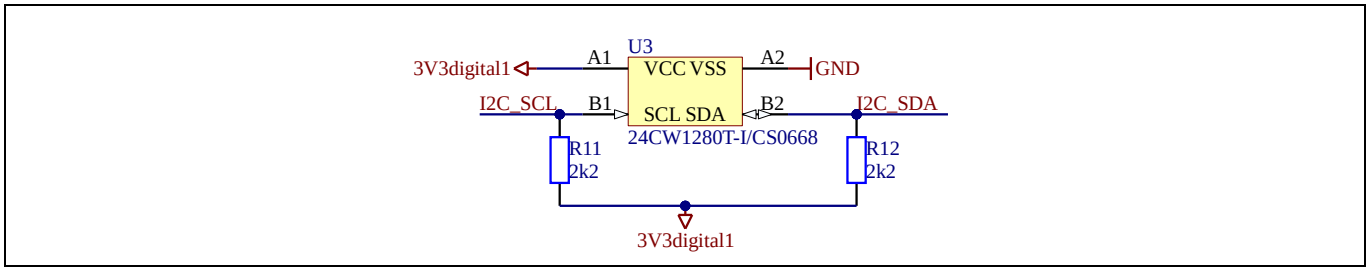



**Figure 13 Schematics of the EEPROM**

## 3.8 LEDs and level shifters

The shield has two LEDs to indicate the motion detection (green) and target's direction of motion (red), as shown in Figure 14, where R1 and R2 are limiting resistors. The digital block within the detector in the MMIC evaluates and sets the Target detect/Phase detect outputs of the BGT60LTR11AIP MMIC. Target detect (TDet) output is active low. Phase detect (PDet) output is used to show the direction of the detected target. It is set to high for approaching targets, otherwise low. The default state for PDet is low.

The outputs from MMIC are at the voltage level of 1.5 V. They are level-shifted to the voltage level of $V_{in}$ by using the circuit shown in Figure 14. In the circuit, BGT_TARGET_DET and BGT_PHASE_DET are outputs of MMIC (1.5 V voltage level). $V_{DD\_RF}$ is 1.5 V and $V_{in}$ is 3.3 V (when connected with Radar Baseboard MCU7).

- When BGT_TARGET_DET is high (1.5 V), NMOS is off ($V_{gs}$ = 0 V), and Target_Det_Out is 3.3V through the R14 pull-up resistor.
- When BGT_TARGET_DET is low (0 V), NMOS is on ($V_{gs}$ = 1.5 V), and Target_Det_Out is pulled down to 0 V.

The same applies to the BGT_PHASE_DET signal.

**Table 3 LED detection**

| LED | Mode | Comments |
|---|---|---|
| Green | On – target detected<br>Off – target not detected | Target_Det_Out is an active low signal |
| Red | On – target departing<br>Off – target approaching | Phase_Det_Out is an active low signal |

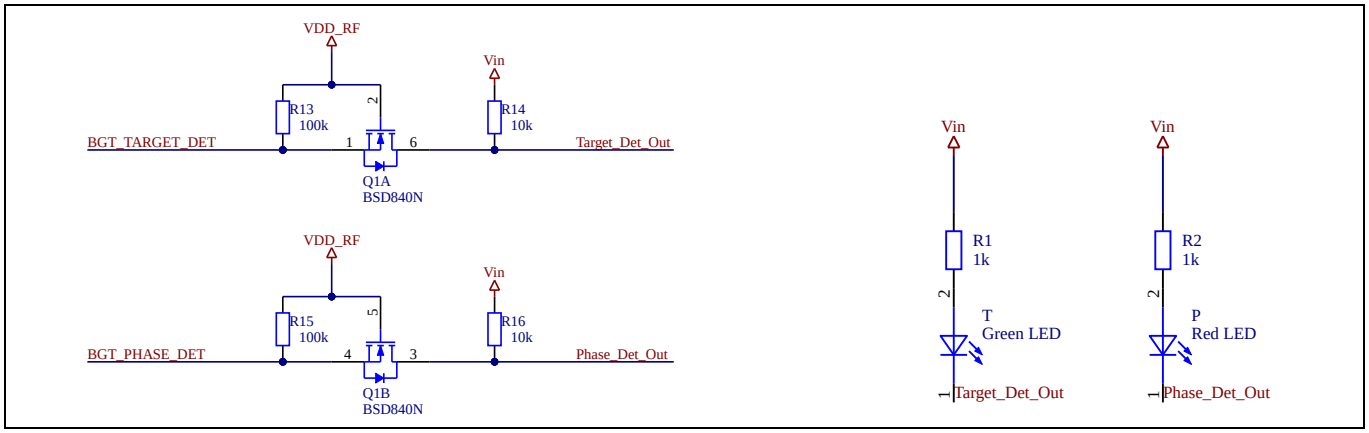



**Figure 14 Connections of the LEDs and level shifter**

## 3.9 MMIC quad state inputs

The BGT60LTR11AIP MMIC has four quad-state inputs QS1-4, used in autonomous mode to set the device configuration. Figure 15 shows the default settings of these QS pins on the BGT60LTR11AIP shield.

To offer more flexibility, to the autonomous mode, an “Advance mode” is enabled when the BGT_PLL_TRIG pin is kept “1” during chip boot and QS1 is either GND or OPEN, where BGT_MOSI and BGT_SCK pins are also sampled to determine the PRT. In addition, pins QS2 and QS3 are evaluated by the ADC and converted in 4-bit values each before each “mean window”.

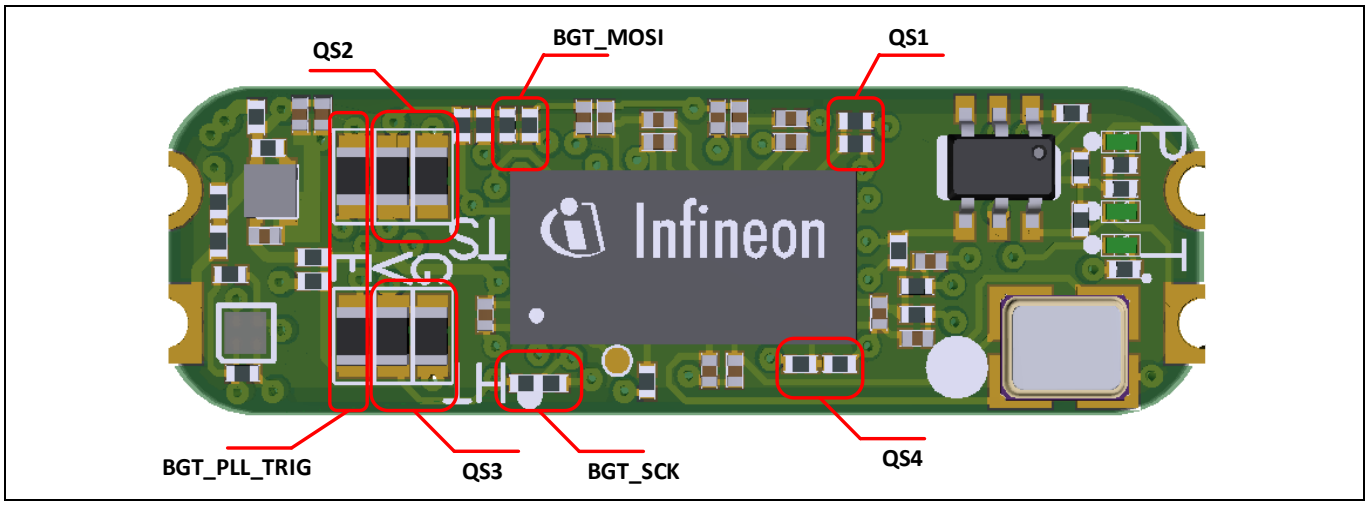
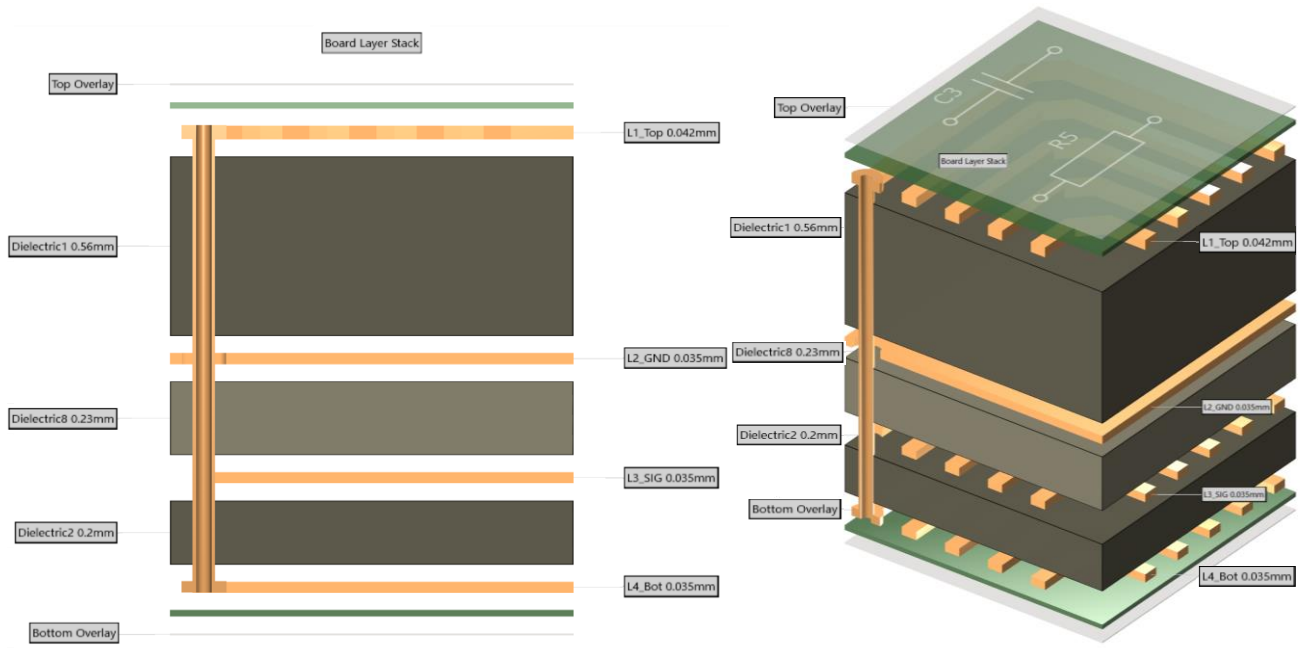



**Figure 15 MMIC QS1 to QS4 quad state inputs**

For more details on the BGT60LTR11AIP MMIC quad state inputs, please refer to the AN625 – User's guide to BGT60LTR11AIP.

## 3.10 Layer stackup and routing

The PCB is designed with a 4-layer stackup with standard FR4 material. Figure 16 shows the different layers and their thicknesses.




| # | Name | Material | Type | Thickness | Dk |
|---|---|---|---|---|---|
| | Top Overlay | | Overlay | | |
| | Top Solder | Solder Resist | Solder Mask | 0.02mm | 3.5 |
| 1 | L1_Top | | Signal | 0.042mm | |
| | Dielectric1 | FR-4 | Core | 0.56mm | 4.2 |
| 2 | L2_GND | | Plane | 0.035mm | |
| | Dielectric8 | FR-4 | Prepreg | 0.23mm | 4.2 |
| 3 | L3_SIG | | Signal | 0.035mm | |
| | Dielectric2 | FR-4 | Core | 0.2mm | 4.3 |
| 4 | L4_Bot | | Signal | 0.035mm | |
| | Bottom Solder | Solder Resist | Solder Mask | 0.02mm | 3.5 |
| | Bottom Overlay | | Overlay | | |

**Figure 16 PCB layer stack-up in 2D and 3D views**

In the routing on the PCB, the VTUNE pin on BGT60LTR11AIP MMIC should be left floating. Any components added to the line, or a long wire connected, can result in spurs.

# 4 Radar MMIC settings configuration

The radar MMIC can be configured in both operation modes. In autonomous mode, the sensor configuration parameters are set via QS pins and external resistors. In SPI mode, the connection to a microcontroller allows setting the sensor configuration parameters by writing in the internal registers through SPI.

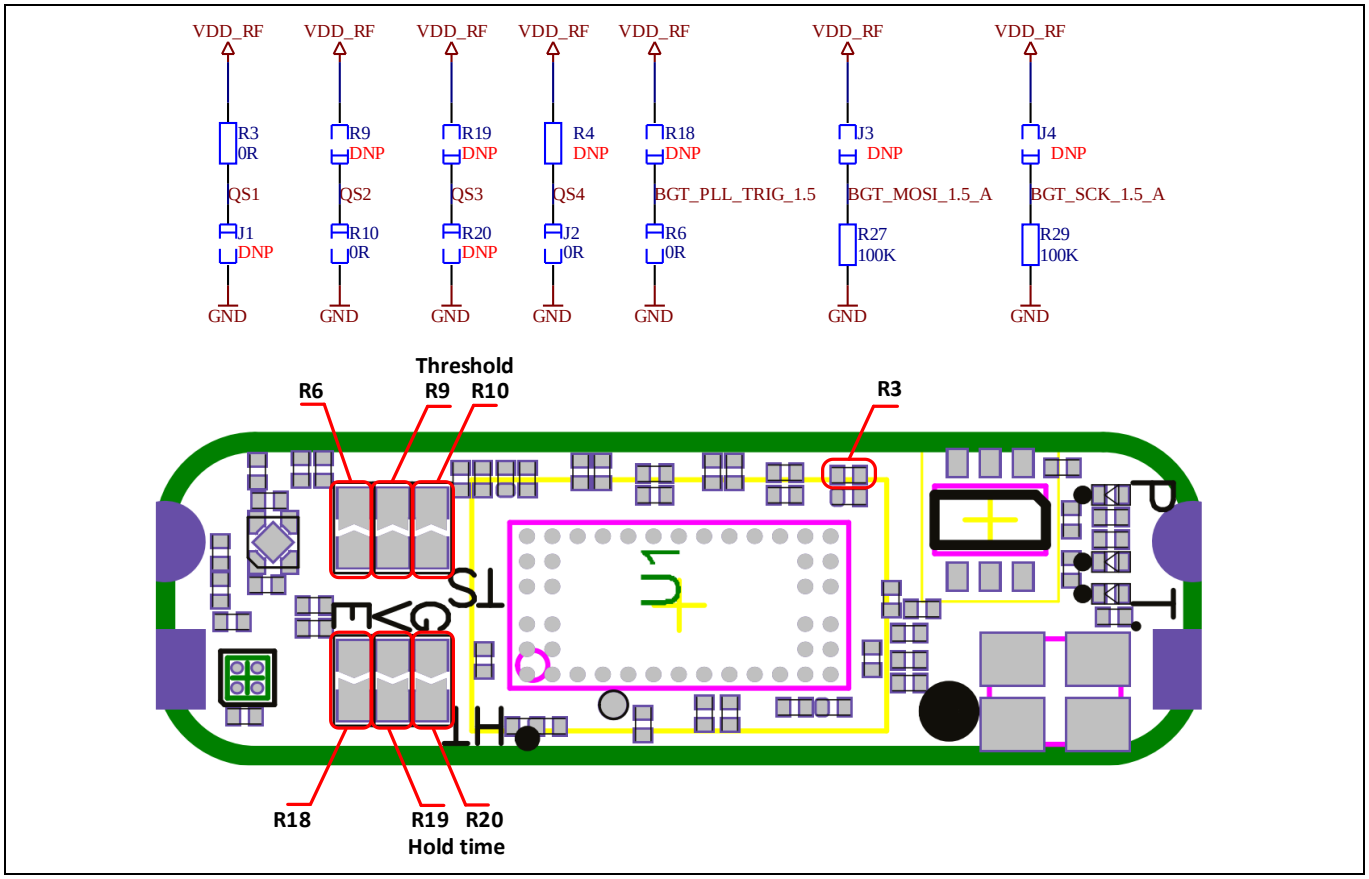



**Figure 17 QS1 to QS4 schematic and layout connections**

## 4.1 Operation mode

The QS1 pin allows choosing the operation mode of the radar MMIC, as detailed in Table 4.

**Table 4 QS1 settings**

| QS1 | Operation mode of the MMIC | PCB configuration | |
|---|---|---|---|
| ground | Autonomous continuous wave (CW) mode | J1 = 0 Ω | R3 = DNP* |
| open | Autonomous pulsed mode | J1 = DNP* | R3 = DNP* |
| 100 kΩ to $V_{DD}$ | SPI mode with external 9.6 MHz clock enabled | J1 = DNP* | R3 = 100 kΩ |
| $V_{DD}$ (default) | SPI mode | J1 = DNP* | R3 = 0 Ω |

*DNP : Do Not Populate/Do Not Place

The DEMO BGT60LTR11AIP comes with the BGT60LTR11AIP shield configured in SPI mode, to enable the radar MMIC configuration via the firmware running on the Radar Baseboard MCU7 microcontroller.

To make the shield work in autonomous mode, you need to remove R3 resistor as shown in Figure 18.

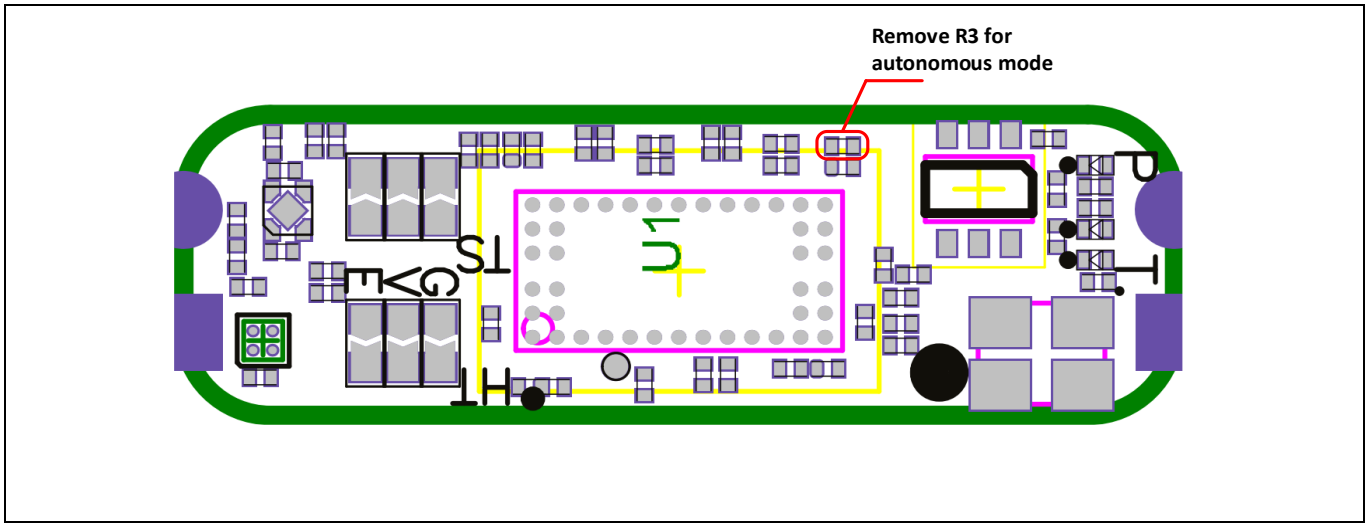



**Figure 18 Converting the shield to autonomous mode**

*Note: Once a BGT60LTR11AIP shield is converted to autonomous mode, it should NOT be connected to a Radar Baseboard MCU7 to change the settings via the GUI. Only, resistor values mentioned in Table 5 and Table 6 are recommended to be soldered on the shield in order to achieve the desired settings.*

## 4.2 Detector threshold

The internal detector threshold is the minimum signal strength that has to be reached to trigger a detection event. The lower the threshold set, the higher the sensitivity and therefore also the detection range.

*Note: To avoid triggering false detections, it would be better to increase the detector threshold, hence reduce the sensor sensitivity, especially in "noisy" environment.*

### Autonomous mode

QS2 is used to select the detector threshold value for the autonomous mode. In order to have up to 16 threshold values, the PLL_TRIG should be connected to VDD by removing R6 and placing R18 = 0 Ω. This will put the MMIC into "Advance mode". The default QS2 setting on the shield is for threshold 80.

Recommended resistor values for changing the QS2 on the autonomous shield are detailed in Table 5.

**Table 5 QS2 settings**

| Resistors settings | | Detector Threshold (Radar Fusion GUI setting) | Sensitivity (Radar GUI setting) |
|---|---|---|---|
| **R9** | **R10** | | |
| 10 kΩ | 330 Ω | 61 | 15* |
| 10 kΩ | 1 kΩ | 66 | 14* |
| 10 kΩ | 1.8 kΩ | 80 | 13 |
| 10 kΩ | 2.7 kΩ | 90 | 12 |
| 10 kΩ | 3.9 kΩ | 112 | 11 |
| 10 kΩ | 5.6 kΩ | 136 | 10 |
| 10 kΩ | 6.8 kΩ | 192 | 9 |
| 10 kΩ | 8.2 kΩ | 248 | 8 |
| 10 kΩ | 12 kΩ | 320 | 7 |
| 10 kΩ | 15 kΩ | 284 | 6 |
| 10 kΩ | 18 kΩ | 480 | 5 |
| 10 kΩ | 27 kΩ | 640 | 4 |
| 10 kΩ | 39 kΩ | 896 | 3 |
| 10 kΩ | 56 kΩ | 1344 | 2 |
| 10 kΩ | 100 kΩ | 1920 | 1 |
| 10 kΩ | 220 kΩ | 2560 | 0 |

*High sensitivity levels could lead to false detections, are not shown on the Radar GUI settings.

### SPI mode

In SPI operation mode, the user can set the internal detector threshold by writing to *thrs* (Reg2[12:0]) bit fields of the MMIC SPI registers.

## 4.3 Detector hold time

The internal detector hold time, is the time for which the internal detector outputs remain active after target detection.

### Autonomous mode

QS3 is used to select the detector hold time value for the autonomous mode. In order to have up to 16 hold time values, the PLL_TRIG should be connected to VDD by removing R6 and placing R18 = 0 Ω. This will put the MMIC into “Advance mode”. The default QS3 setting on the shield for the hold time is 1s. Recommended resistor values for changing the QS3 on the autonomous shield are detailed in Table 6.

**Table 6 QS3 settings**

| Resistors setting | | Detector Hold time |
|---|---|---|
| **R19** | **R20** | |
| 10 kΩ | 330 Ω | Minimum (16 ms, 32 ms, 64 ms or 128 ms) dep. on PRT |
| 10 kΩ | 1 kΩ | 500 ms |
| 10 kΩ | 1.8 kΩ | 1 s |
| 10 kΩ | 2.7 kΩ | 2 s |
| 10 kΩ | 3.9 kΩ | 3 s |
| 10 kΩ | 5.6 kΩ | 5 s |
| 10 kΩ | 6.8 kΩ | 10 s |
| 10 kΩ | 8.2 kΩ | 30 s |
| 10 kΩ | 12 kΩ | 45 s |
| 10 kΩ | 15 kΩ | 1 min |
| 10 kΩ | 18 kΩ | 90 s |
| 10 kΩ | 27 kΩ | 2 min |
| 10 kΩ | 39 kΩ | 5 min |
| 10 kΩ | 56 kΩ | 10 min |
| 10 kΩ | 100 kΩ | 15 min |
| 10 kΩ | 220 kΩ | 30 min |

### SPI mode

In SPI operation mode, the user can set the internal detector hold time by writing to *hold* (Reg10[15:0]) bit fields of the MMIC SPI registers.

## 4.4 Operating frequency

### Autonomous mode

QS4 is used to set the operating frequency for the MMIC in the 60 GHz ISM band, which is important to meet worldwide regulation requirements, possible settings are detailed in Table 7.

**Table 7 QS4 settings**

| QS4 | Device operating frequency | PCB configuration | |
|---|---|---|---|
| ground (default) | 61.1 GHz | J2 = 0 Ω | R4 = DNP* |
| open | 61.2 GHz | J2 = DNP* | R4 = DNP* |
| 100 kΩ to $V_{DD}$ | 61.3 GHz | J2 = DNP* | R4 = 100 kΩ |
| $V_{DD}$ | 61.4 GHz | J2 = DNP* | R4 = 0 Ω |

*DNP : Do Not Populate/Do Not Place

### SPI mode

In SPI operation mode, the user can set the device operation frequency by writing to *pll_fcw* (Reg5[11:0]) bit fields of the MMIC SPI registers. The BGT60LTR11AIP device operates in the frequency band from 61 GHz to 61.5 GHz.

*Note: Please keep a 50 MHz guard band, each side from the band edge, to avoid outside of ISM band emission.*

*Note: Sensors operating in close vicinity at the same operating frequency can interfere. To avoid that, please set different operating frequency for each device, with at least a difference of 12 MHz.*

## 4.5 Pulse repetition time

The Pulse Repetition Time (PRT) is the duty cycle repetition rate, which means the time until the next pulsing sequence starts in pulsed mode.

### Autonomous mode

The PRT can be configured in autonomous pulsed mode (QS1 is either GND or OPEN as shown in Table 4) only if the “Advance mode” is enabled by keeping the PLL_Trig pin to “1”. The SPI pins BGT_MOSI and BGT_SCK are sampled during chip boot-up and determine the PRT setting, as detailed in Table 8.

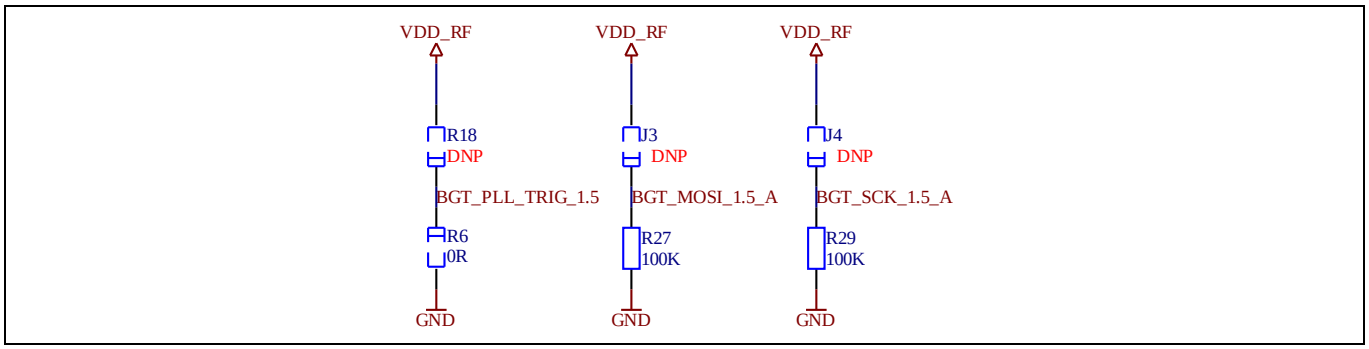



**Figure 19 Configuring Pulse Repetition Time (PRT)**

**Table 8 PRT configuration in (pulsed) autonomous mode**

| BGT_PLL_TRIG* | BGT_MOSI | BGT_SCK | PRT | PCB components | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 500 µs | J3 = DNP* | R27 = 100 kΩ | J4 = DNP* | R29 = 100 kΩ |
| 1 | 0 | 1 | 2000 µs | J3 = DNP* | R27 = 100 kΩ | J4 = 100 kΩ | R29 = DNP* |
| 1 | 1 | 0 | 250 µs | J3 = 100 kΩ | R27 = DNP* | J4 = DNP* | R29 = 100 kΩ |
| 1 | 1 | 1 | 1000 µs | J3 = 100 kΩ | R27 = DNP* | J4 = 100 kΩ | R29 = DNP* |

*R6 = DNP, R18 = 0 Ω, DNP = Do Not Populate/Do Not Place

### SPI mode

In SPI pulsed operation mode, the user can set the PRT value by writing to *dc_rep_rate* (Reg7[11:10]) bit fields of the MMIC SPI registers.

The user can also enable the Adaptive Pulse Repetition Time (APRT) by writing to *aprt* (Reg2[6]) bit field of the MMIC SPI registers. The PRT multiplier factor, of 2, 4, 8 or 16, is also set by writing to *prt_mult* (Reg13[1:0]) bit fields.

# 5 Autonomous mode operation

In the autonomous mode operation, the MMIC uses only internal detectors for motion and direction of motion indication. The BGT60LTR11AIP autonomous shield can be powered directly through the castellated holes on the sides of the shield or through a baseboard platform like the Radar Baseboard MCU7.

## 5.1 Battery-powered operation

The BGT60LTR11AIP autonomous shield, can operate independently with a battery that supplies to the VIN, GND pins of the castellated holes, and will generate internal detector outputs on TD (TDet) and PD (PDet) castellated holes depending on the movement of the target. As shown in Figure 20, the output signals TDet and PDet are connected to LEDs, which glow according to target movement (TD) and direction of movement (PD).

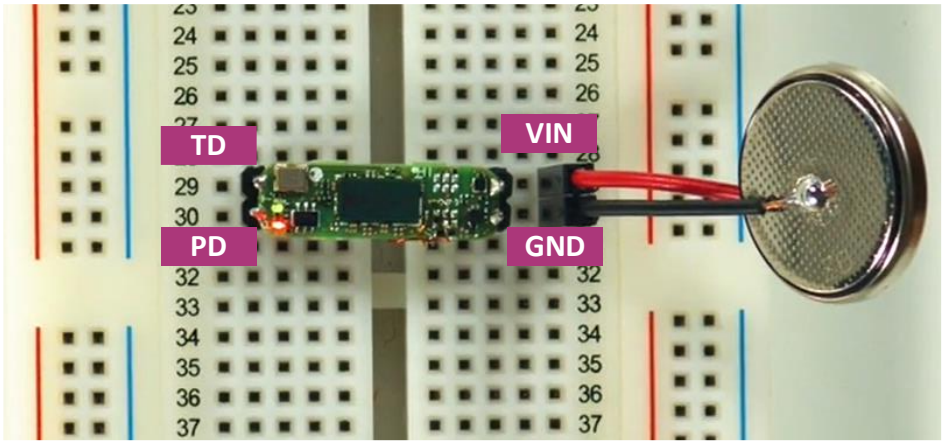



**Figure 20 Radar shield working independently with a battery power supply**

## 5.2 Arduino MKR operation

The shield has dimensions such that it can be mounted onto an Arduino MKR series board as shown in Figure 21 as a plug-on motion sensor.

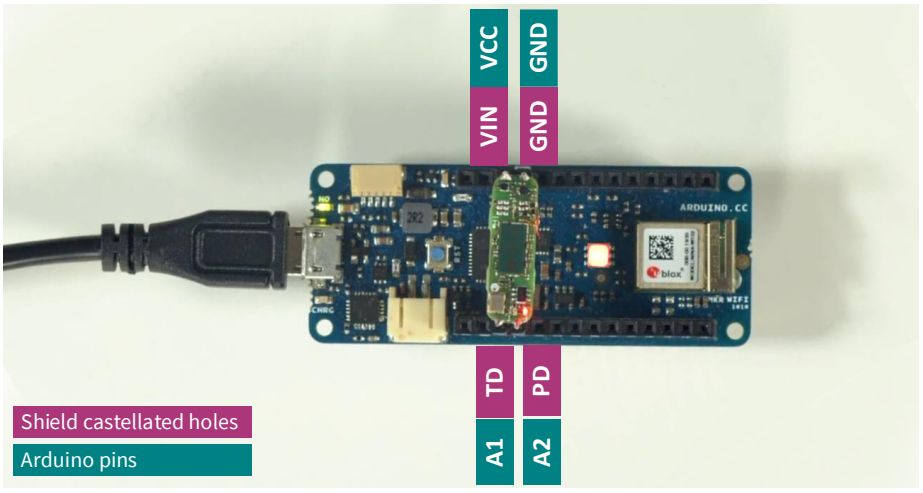



**Figure 21 Radar shield mounted on an Arduino MKR Wifi1010 board**

Find the BGT60LTR11 Radar Arduino Library and get started instructions on Infineon's GitHub repository.

# 6 Firmware

## 6.1 Overview

The Radar Baseboard MCU7 comes with a default firmware which is intended to serve as a bridge between a host (typically a PC) and the BGT60LTR11AIP RF shield, which is mounted on the sensor connectors.

When the firmware detects a BGT60LTR11AIP shield, it automatically configures the driver layer for the BGT60LTR11AIP sensor. This includes configuring the chip, as well as setting up the MCU to initiate a serial peripheral interface (SPI) transfer when the BGT signals the availability of new data via the IRQ line. The firmware will also configure the communication layer so that radar and BGT60LTR11AIP specific messages are understood.

For more details, please refer to the AN599 - Radar Baseboard MCU7 application note.

## 6.2 SPI MISO arbitration

The BGT60LTR11AIP MMIC V3.0 implements a new internal digital detector, using the internal ADC samples from I/Q signals. Thus, the internal access to the ADC values must be multiplexed with the external SPI access (from the Radar Baseboard MCU7), in a process known as “SPI MISO arbitration”.

### 6.2.1 Use cases

The SPI MISO line arbitration is active when:

- BGT60LTR11AIP device is active after hard or soft reset and after boot-up time in any autonomous mode.
- After activation of SPI “Pulsed mode” (set *start_pm* (Reg15[14]) bit to “1”)
- After activation of SPI “CW mode” (set *start_pm* (Reg15[14]) bit and *start_cw* (Reg15[12]) bit to “1”)

The SPI MISO line arbitration is by default in High-Z after reset, to avoid disturbance in Multi-Client SPI setup, and needs to be set explicitly into driving mode by setting *miso_drv* (Reg15[6]) bit to “1”, to be active outside SPI access.

So, the consequences are:

- If the BGT60LTR11AIP registers need only to be set once, before the “Pulsed mode” is activated, MISO arbitration could be ignored. Recommended to use Hard-Reset pin, instead of Soft-Reset via Reg15, to avoid SPI access.
- If the BGT60LTR11AIP registers need to be updated when device is “running”, MISO line arbitration needs to be respected.
- If a clear synchronization to the RF-Pulse is wanted, the MISO arbitration could be used. Synchronization could be setup, just before starting “Pulsed mode” (with raising edge of MISO indicates a good sampling point).
- If already “div-out”-RF-Pulse-sync is used or implemented, it could still be continued to be used.

For more details on the BGT60LTR11AIP MMIC registers, please refer to the BGT60LTR11AIP datasheet.

### 6.2.2 Implementation

If MISO arbitration is required to be implemented, then you need best a raising and falling edge IRQ on GPIO line. Multiplexing on MISO pin should be considered.

Also, the implementation of a GUARD timer is highly recommended, to prevent access some time before the next pulse is required. If only a **defined** sequence of SPI accesses is performed, and if it is ensured that the arbitration timing is ensured, the usage of a guard time might be neglected.

Here below the recommended procedure to synchronize the access with the pulsing.

After starting Pulse/CW Mode, register raising edge IRQ, to synchronize with pulse; block-out SPI access.

1. Wait for raising edge on MISO (via IRQ):
    a. Deactivate raising edge IRQ
    b. Start Guard timer with “pulse repletion rate – guard time”
    c. Activate falling edge IRQ
2. After falling edge:
    a. Deactivate falling edge IRQ
    b. MCU SPI communication allowed
    c. Start read-out of internal ADC registers (Reg40 and Reg41) if needed
    d. Perform other SPI register access
3. Guard Timer expires:
    a. Block SPI communication
    b. Activate raising edge IRQ

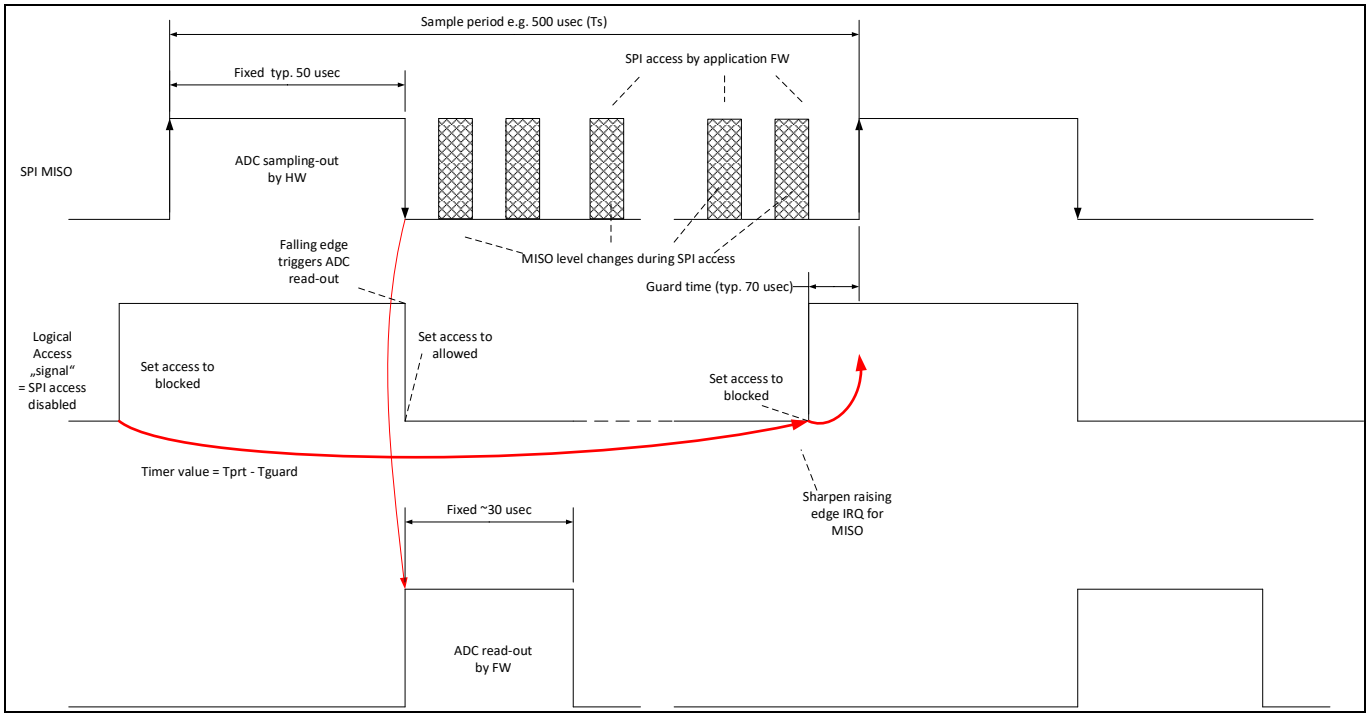



**Figure 22 Synchronized SPI access time diagram**

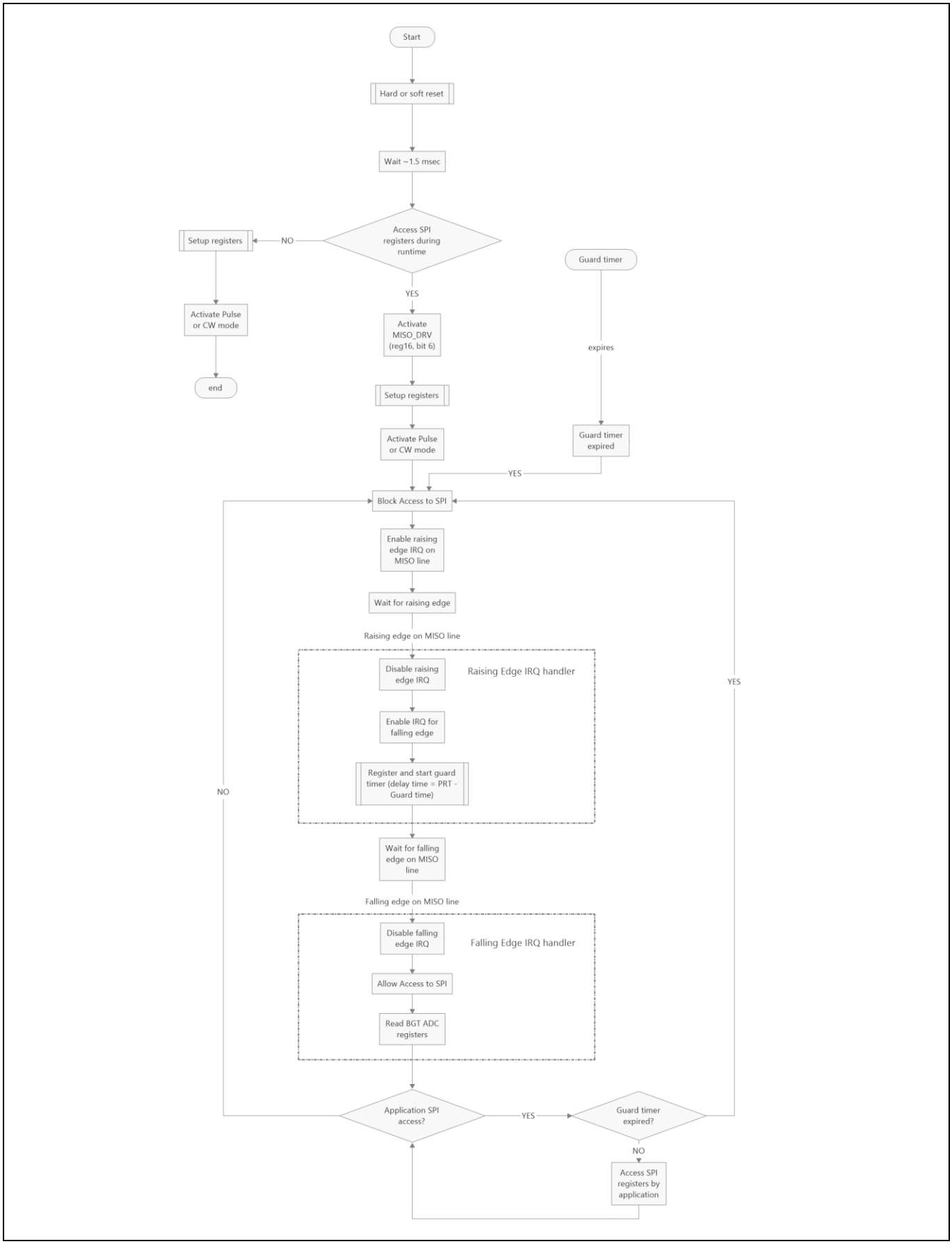



**Figure 23 SPI arbitration flow diagram**

Please note that:

- MISO line is high-Z if CS is inactive (default)
- MISO arbitration can be enabled via *miso_drv* (Reg15[6]) bit.
- Without respecting MISO arbitration, device functionality is NOT ensured.
- Only I/Q channel (Reg40 and Reg41) is sampled via internal state machine. For other ADC channels, explicit ADC conversion needs to be triggered manually.
- If external ADC is used for sampling, the best time for Sample&Hold activation would be at the raising edge of MISO arbitration signal. Conversion could be done later.

Here below a typical access screenshot in Figure 24.

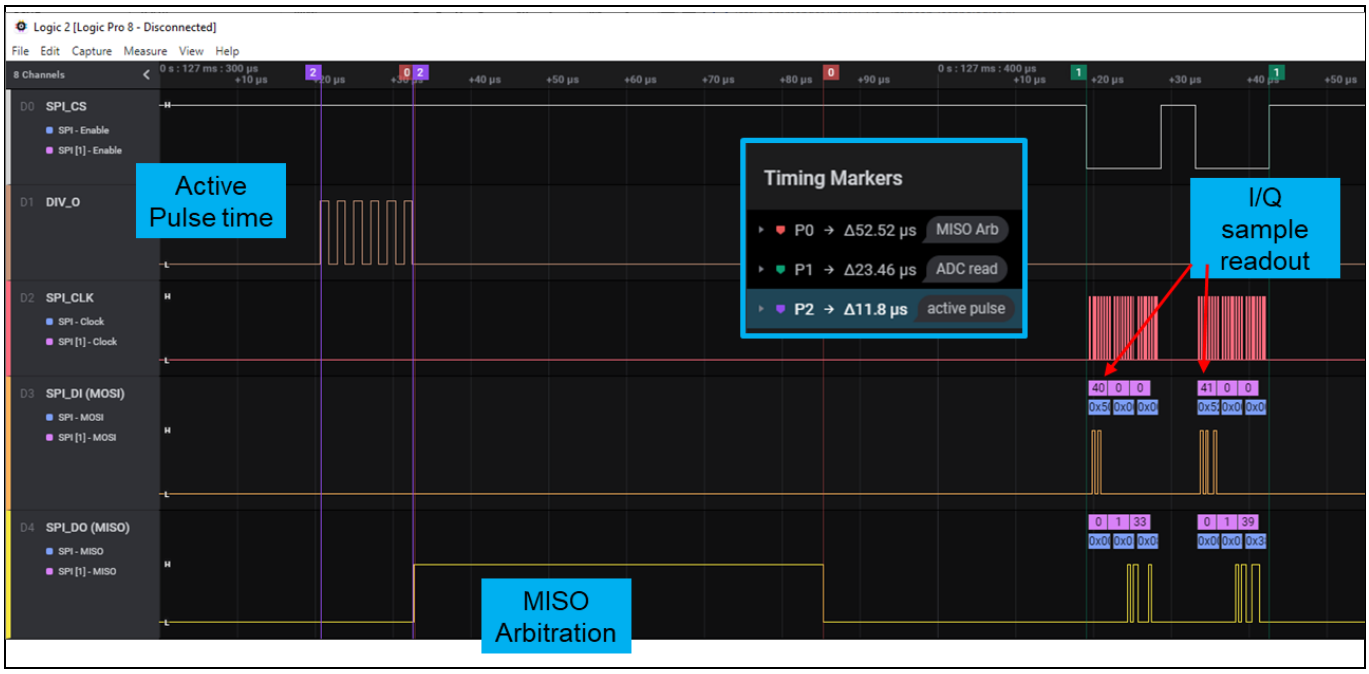



**Figure 24 Typical SPI access**

# 7 Measurement results

## 7.1 Radiation pattern

To analyze the sensor radiation characteristics, the radiation pattern of the BGT60LTR11AIP shield, configured in CW mode, is simulated along the H-plane and E-plane of the sensor. The realized gain of the transmitting antenna, in H-plane and E-plane at a frequency of 61 GHz, is shown in Figure 25a. The antenna characteristics of the receiving antenna in H-plane and E-plane at a frequency of 61 GHz, is illustrated in Figure 25b.

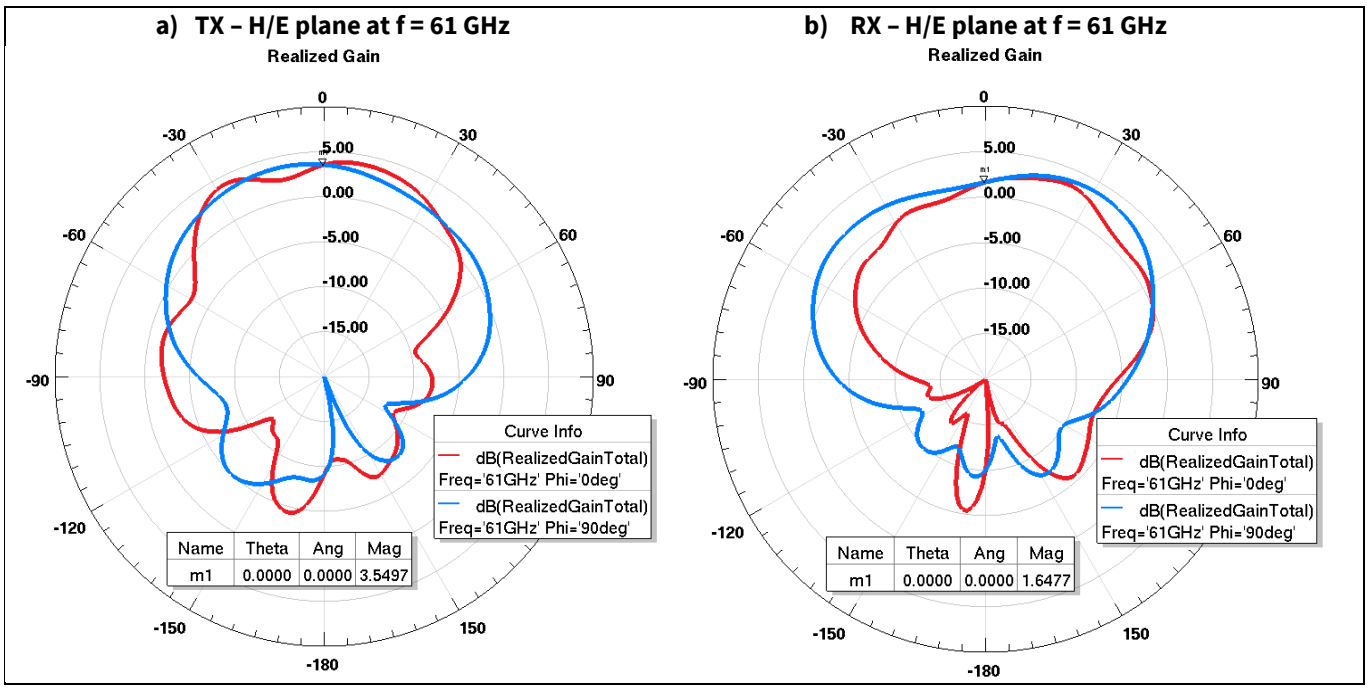



**Figure 25 Radiation pattern simulations of the BGT60LTR11AIP shield in CW mode**

## 7.2 Motion detection area

The measurements are conducted for different MMIC operation modes, and settings.
Figure 26 below shows the possible operating modes, and how the detection status is driven.

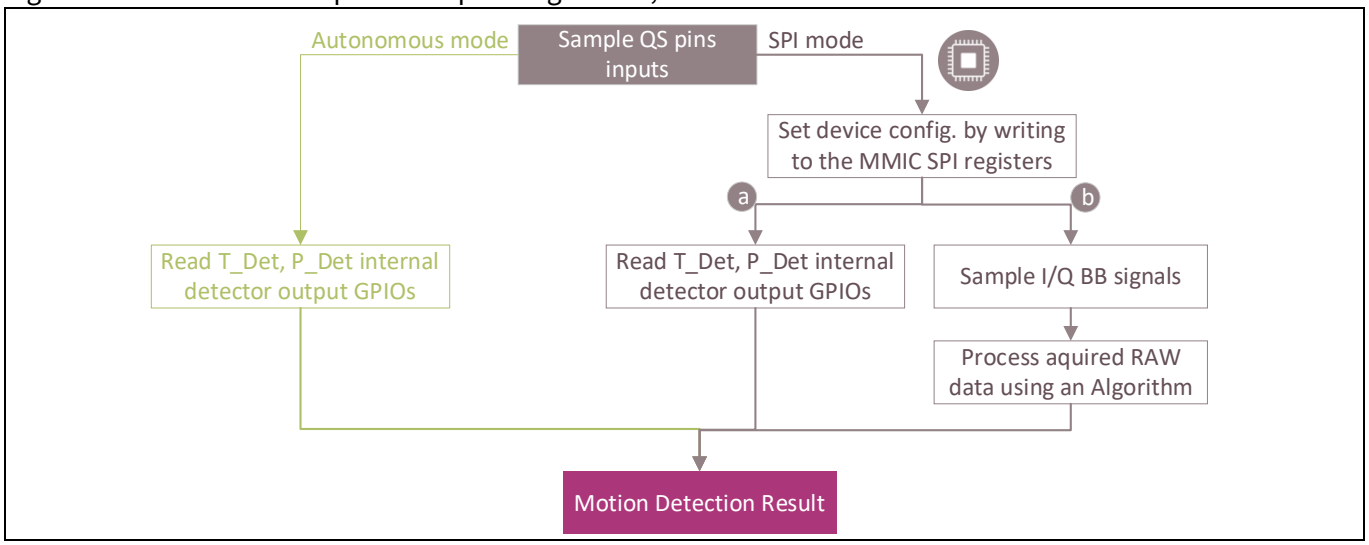



**Figure 26 Shield operation modes and motion detection status**

### 7.2.1 Autonomous mode

- **Hardware**
  SHIELD_AUTONOM_BGT60, consisting of a BGT60LTR11AIP shield (configured by default in autonomous pulsed mode). For more details, please refer to section 5.
- **Firmware**
  No firmware is needed for the autonomous shield.
- **Height**
  Board is placed at 1.2 m
- **Scenario**
  Measure the max. detection range of a human target along the H-plane of the sensor, for different angles.
- **Detection status**
  It is driven from the internal detector output (TDet). Figure 27 shows the measurement results in H-plane and E-plane, and the right shield orientation.

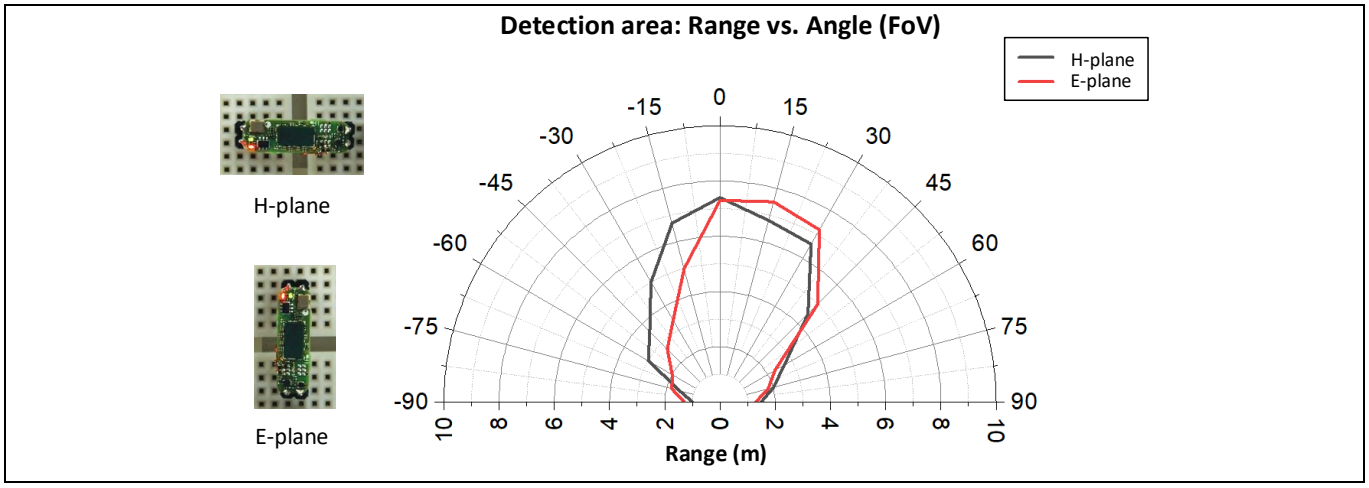



**Figure 27 H-plane and E-plane Human target detection area for BGT60LTR11AIP autonomous shield**

### 7.2.2 SPI mode and MMIC internal detector

- **Hardware**
  Radar Baseboard MCU7 and BGT60LTR11AIP shield (configured by default in SPI pulsed mode)
- **Firmware**
  Is only used to set the shield configuration by writing to the MMIC SPI registers, as shown in Figure 26a. The “Radar Integrated Motion Sensing” application available from the Radar Fusion GUI is used.
- **Height**
  Board is placed at 1.2 m
- **Scenario**
  Measure the max. detection range of a human target along the H-plane and E-plane of the sensor, for different threshold values, which can be selected from the GUI, and different angles.
- **Detection status**
  It is driven from the internal detector output (TDet). Figure 28 and Figure 29 show respectively the measurement results in H-plane and E-plane, and the right shield orientation.

H-plane

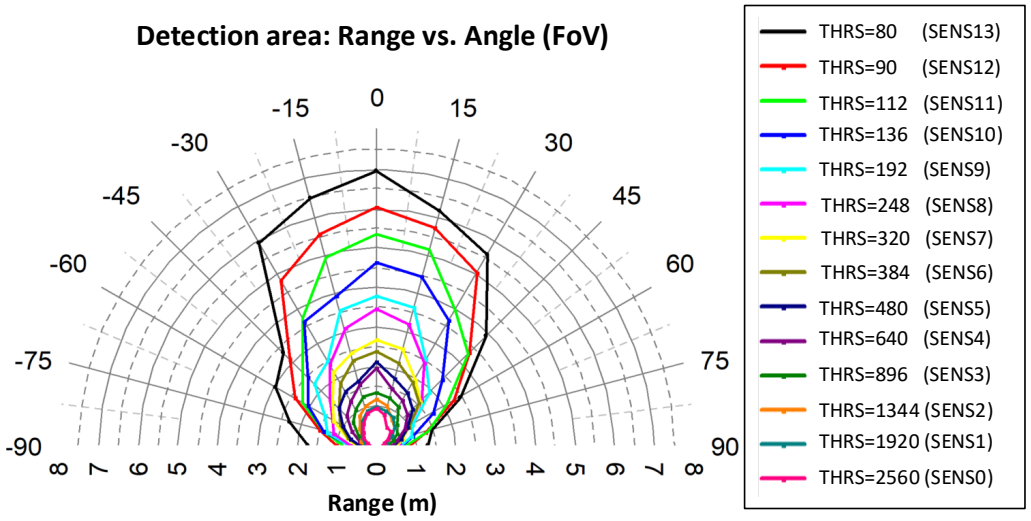



**Figure 28 H-plane Human target detection area, in SPI mode, using MMIC internal detector**

E-plane

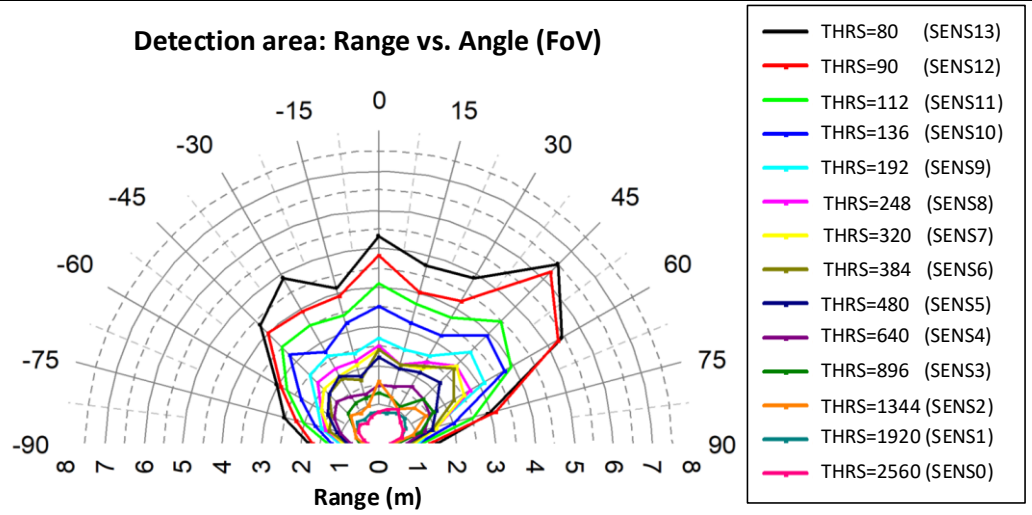



**Figure 29 E-plane Human target detection area, in SPI mode, using MMIC internal detector**

### 7.2.3 SPI mode and motion detection algorithm

- **Hardware**
  Radar Baseboard MCU7 and BGT60LTR11AIP shield (configured by default in SPI pulsed mode)
- **Firmware**
  Is used to set the shield configuration by writing to the MMIC SPI registers, sample the I&Q baseband signals, and process the acquired RAW data through a motion detection algorithm, as shown in Figure 26b.
  The “Radar Advanced Motion Sensing with SPI” application available from the Radar Fusion GUI is used.
- **Height**
  Board is placed at 1.2 m
- **Scenario**
  Measure the max. detection range of a human target along the H-plane and E-plane of the sensor for different angles, with the default configuration, and with an algorithm set threshold value of 15, which can be selected from the Radar Fusion GUI.
- **Detection status**
  It is driven from the advanced motion detection algorithm output. Figure 30 shows the measurement results in H-plane and the right shield orientation.

H-plane

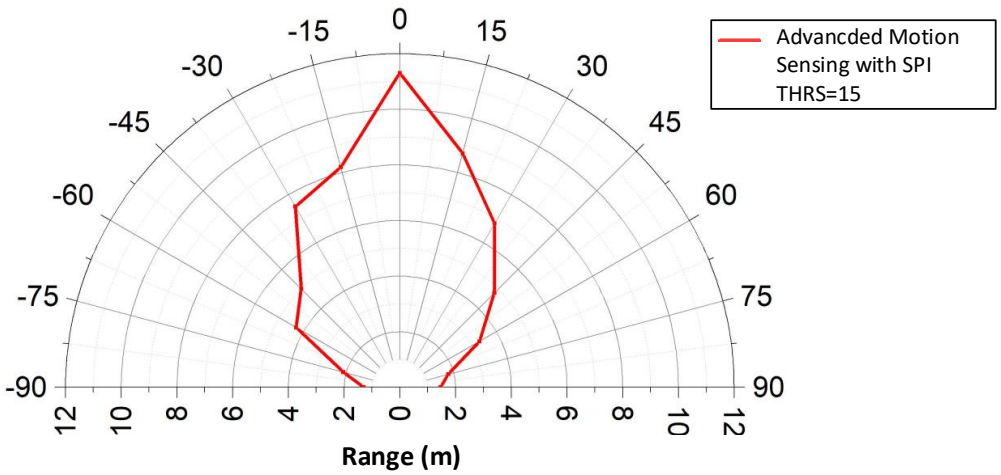



**Figure 30 H-plane Human target detection area, in SPI mode, using advanced motion sensing (AMS) algorithm**

# 8 Power consumption analysis

## 8.1 Duty cycling

The current consumption of the BGT60LTR11AIP MMIC can be optimized by configuring the duty cycle Pulse width (PW) and the Pulse Repetition Time (PRT). With the default PW of 5 µs, which means the time BGT is active during one pulsing event, the current consumption values of the MMIC are listed in Table 9.

**Table 9 Average current consumption of the BGT60LTR11AIP shield in SPI pulsed mode**

| PW (µs) | PRT (µs) | Current consumption (mA) |
|---|---|---|
| 5 | 250 | 6.752 |
| 5 | 500 (default) | 3.776 |
| 5 | 1000 | 2.288 |
| 5 | 2000 | 1.544 |

The current consumption of the BGT60LTR11AIP shield is measured, as shown in Figure 31.

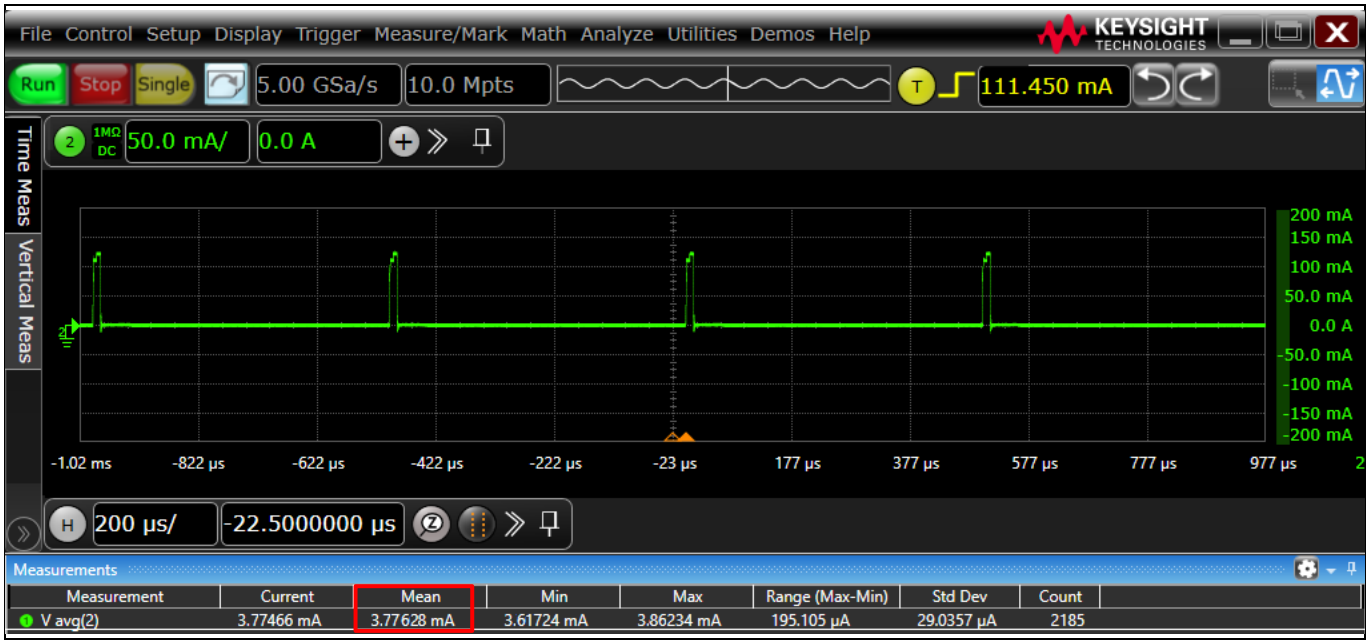



**Figure 31 Current consumption of shield with PW = 5 µs and PRT = 500 µs**

## 8.2 Adaptive pulse repetition time

The Adaptive Pulse Repetition Time (APRT) is a power-saving option of the BGT60LTR11AIP MMIC. It consists of multiplying the PRT by a factor, of 2, 4, 8 or 16, when no target is detected by the internal detector. When a target is detected, the PRT returns to the default value to ensure reliable detection.

Enabling the APRT, as an additional power-saving option, effectively reduces the ON-time of the MMIC since the default PRT is only used when a target is detected, hence reducing the overall power consumption. Depending on the use-case and the multiplier value selected, the power consumption of the shield can be reduced significantly. The following figures show how the set PRT = 500 µs, is changing when the APRT is enabled with different multiplier factors and when a target is detected or not.

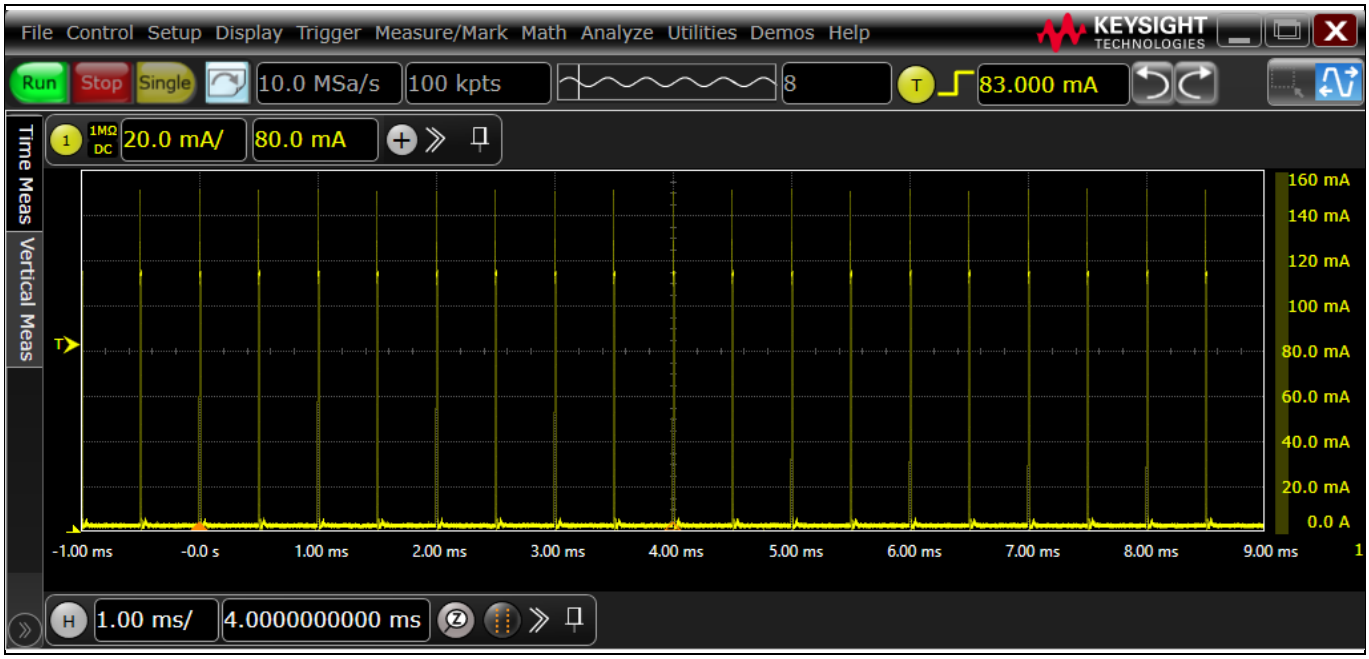



**Figure 32 APRT disabled, target detected/no target detected, PRT remains 500 µs**

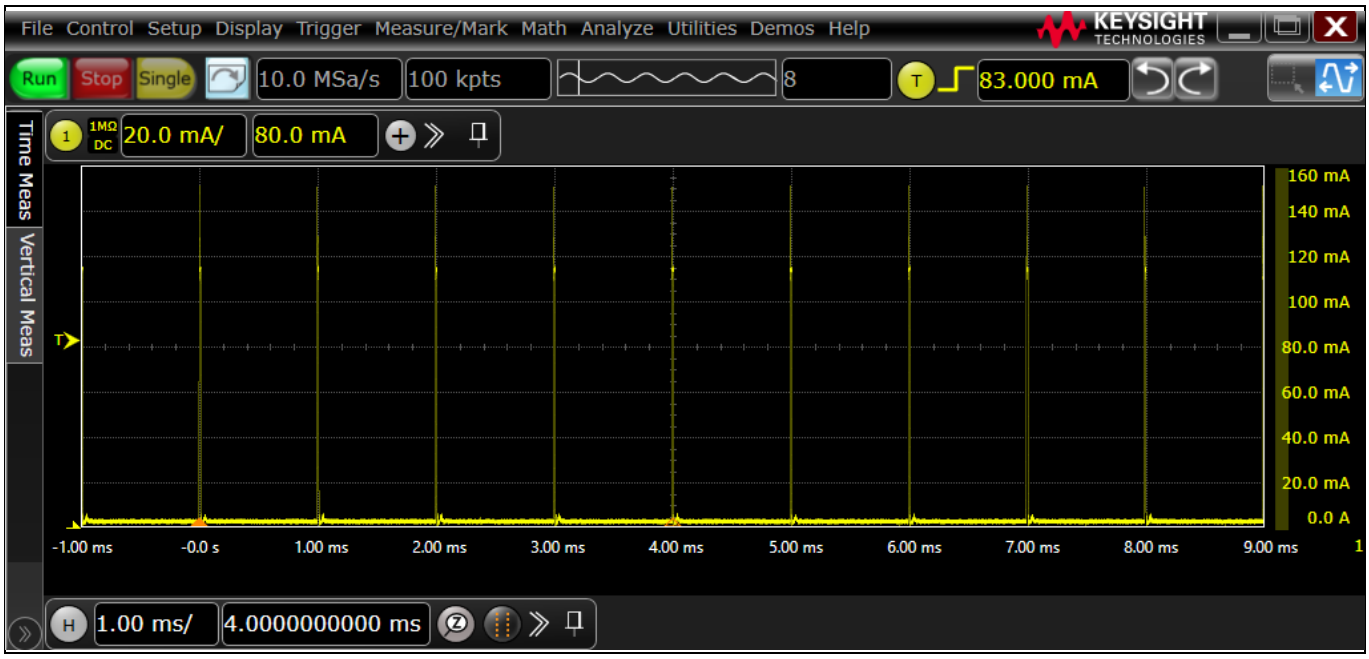



**Figure 33 APRT enabled, Multiplier x2, no target detected, PRT switches to 1 ms**

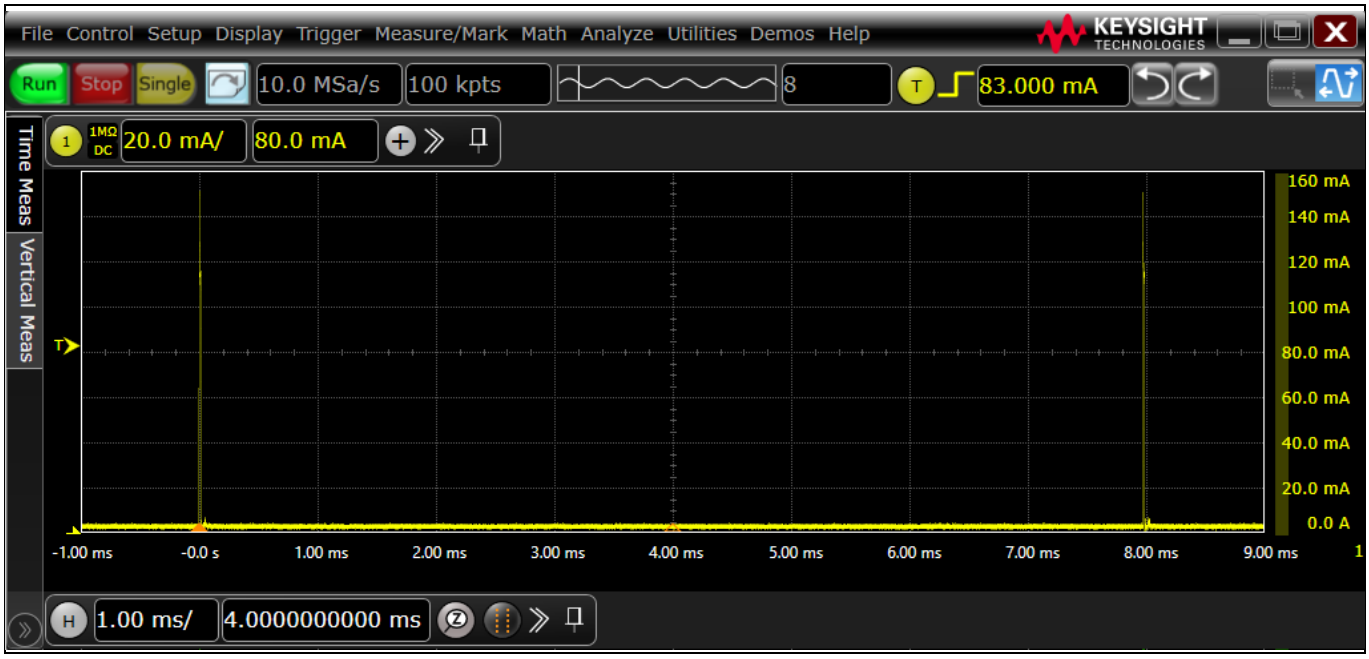



**Figure 34 APRT enabled, Multiplier x16, no target detected, PRT switches to 8 ms**

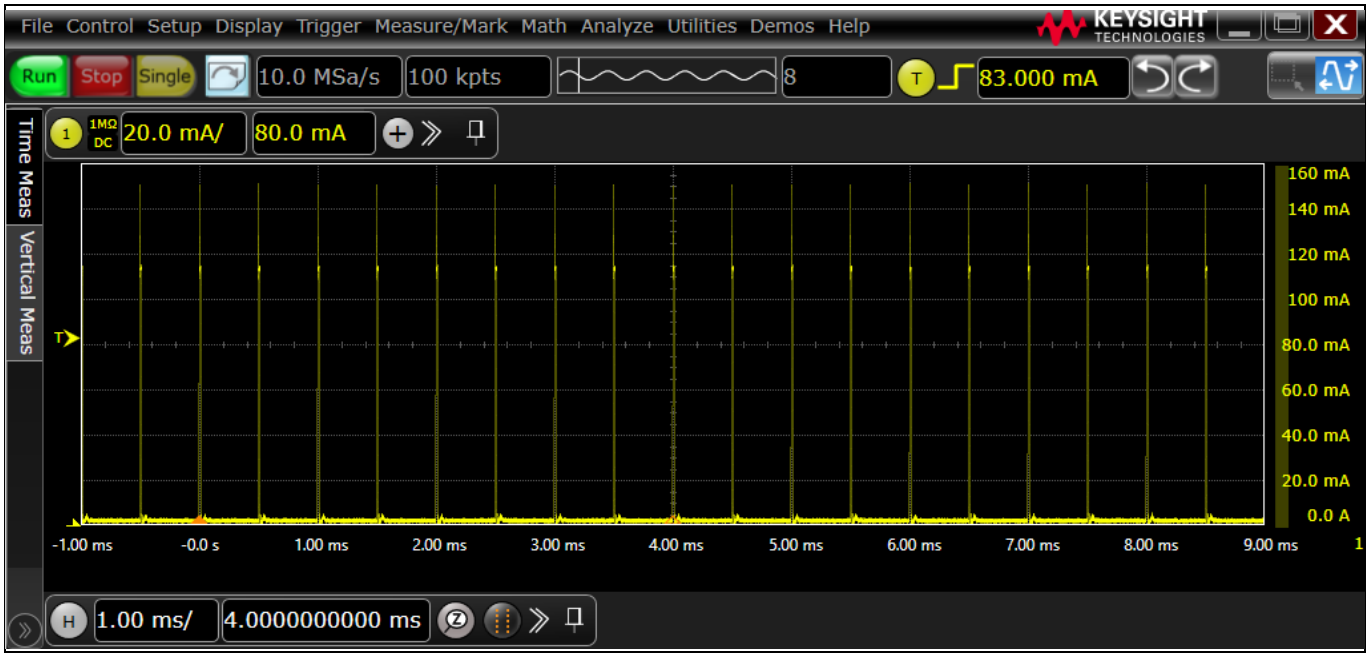



**Figure 35 APRT enabled, Multiplier x16, target detected, PRT switches back from 8 ms to 500 µs**

## References

[1] Infineon Technologies AG. BGT60LTR11AIP MMIC Datasheet

[2] Infineon Technologies AG. AN625: User's guide to BGT60LTR11AIP

[3] Infineon Technologies AG. AN599: Radar Baseboard MCU7

## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| 1.00 | 2020-06-03 | Initial version |
| 1.10 | 2020-10-20 | Mass market version |
| 1.20 | 2020-11-17 | Updated autonomous mode info |
| 1.30 | 2021-03-16 | Updated “Figure 14” |
| 1.40 | 2021-07-15 | Major document updates to support shield V2.0 |
| 1.50 | 2021-07-29 | Updated “Table 8” |
| 1.60 | 2021-10-11 | Added “2. Getting Started” section |
| 1.70 | 2022-08-01 | Changes all over the document<br>Removed “Getting started” section<br>Updated “Table 5” and “Table 6” resistor values<br>Added “Radar MMIC settings configuration” section<br>Added “Measurements results” section<br>Added “Power consumption analysis” section |
| 1.80 | 2023-02-14 | Added “Firmware” section<br>Miscellaneous document cleanup updates |