19-4727; Rev 2; 6/99

MAXIM

Improved, Dual, High-Speed Analog Switches

General Description

Maxim's redesigned DG401/DG403/DG405 analog switches now feature guaranteed low on-resistance matching between switches (2Ω max) and guaranteed on-resistance flatness over the signal range (3Ω max). These low on-resistance switches (20Ω typ) conduct equally well in either direction and are guaranteed to have low charge injection (15pC max). The new design offers lower off leakage current over temperature (less than 5nA at +85°C).

The DG401/DG403/DG405 are dual, high-speed switches. The single-pole/single-throw DG401 and double-pole/single-throw DG405 are normally open dual switches. The dual, single-pole/double-throw DG403 has two normally open and two normally closed switches. Switching times are 150ns max for t_{ON} and 100ns max for t_{OFF}, with a maximum power consumption of 35µW. These devices operate from a single +10V to +30V supply, or bipolar supplies of ±4.5V to ±20V. Maxim's improved DG401/DG403/DG405 are fabricated with a 44V silicon-gate process.

Applications

- Sample-and-Hold Circuits
- Guidance and Control Systems
- Communications Systems
- Battery-Operated Systems
- Military Radios
- Test Equipment
- Heads-Up Displays
- PBX, PABX
- Audio Signal Routing

New Features

- **Plug-In Upgrade for Industry-Standard DG401/DG403/DG405**
- **Improved $r_{DS(ON)}$ Match Between Channels (2Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (3Ω max)**
- **Improved Charge Injection (15pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**

Existing Features

- **Low $r_{DS(ON)}$ (30Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling Capability**
- **TTL/CMOS-Logic Compatible**

Ordering Information

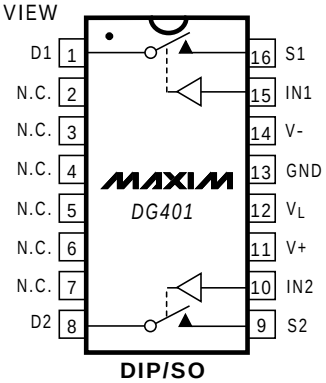
PART	TEMP. RANGE	PIN PACKAGE
DG401CJ	0°C to +70°C	16 Plastic DIP
DG401CY	0°C to +70°C	16 Narrow SO
DG401C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

**Contact factory for dice specifications.*

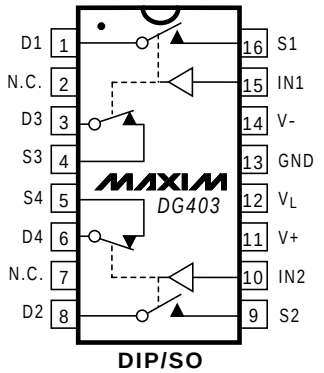
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



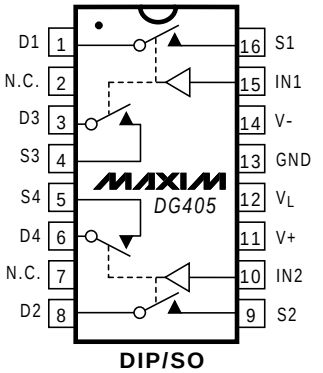
DIP/SO

DG401	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

DG403		
LOGIC	SWITCHES 1, 2	SWITCHES 3, 4
0	OFF	ON
1	ON	OFF



DIP/SO

DG405	
LOGIC	SWITCH
0	OFF
1	ON

LCC packages on last page.

SWITCHES SHOWN FOR LOGIC "0" INPUT

N.C. = NOT INTERNALLY CONNECTED

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L .....(GND - 0.3V) to (V+ + 0.3V)
Digital Inputs, V_S, V_D (Note 1) .....(V- - 2V) to (V+ + 2V) or 20mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP(derate 10.53mW/°C above +70°C)...842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin CERDIP (derate 10.00mW/°C above 70°C) 800mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
DG40_C_ .....0°C to +70°C
DG40_D_ .....-40°C to +85°C
DG40_A_ .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on S, D or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			-15		+15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = ±10V, V_{INH} = 2.4V, V_{INL} = 0.8V	T_A = +25°C	C,D		20	45	Ω
				A		20	30	
			T_A = T_{MIN} to T_{MAX}	C,D			55	
				A			45	
Drain-Source On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 15V, V- = -15V, I_S = -10mA, V_D = ±10V	T_A = +25°C	C, D, A		0.5	2	Ω
			T_A = T_{MIN} to T_{MAX}				3	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, I_S = -10mA, V_D = ±5V, 0V	T_A = +25°C	C, D, A			3	Ω
			T_A = T_{MIN} to T_{MAX}				6	
Source-Off Leakage Current (Note 7)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ∓15.5V, V_S = ±15.5V,	T_A = +25°C	C, D	-0.50	-0.01	0.50	nA
				A	-0.25	-0.01	0.25	
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-Off Leakage Current (Note 7)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D	-0.50	-0.01	0.50	nA
				A	-0.25	-0.01	0.25	
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-On Leakage Current (Note 7)	$I_{D(ON)}$ or $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	T_A = +25°C	C, D	-1.0	-0.04	1.0	nA
				A	-0.4	-0.04	0.4	
			T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
				A	-20		20	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		-1.0	0.005	1.0	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-1.0	0.005	1.0	µA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2	T_A = +25°C		100	150	ns
Turn-Off Time	t_{OFF}	Figure 2	T_A = +25°C		60	100	ns
Break-Before-Make Delay (Note 3)	t_D	DG403 only, Figure 3	T_A = +25°C	10	20		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	T_A = +25°C		10	15	pC
Off Isolation (Note 5)	OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		72		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		90		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		12		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		12		pF
Channel-On Capacitance	$C_{D(ON)}$ or $C_{S(ON)}$	f = 1MHz, Figure 8	T_A = +25°C		39		pF

Note 2: This data sheet uses the algebraic convention, where the most negative value is a minimum and the most positive value is a maximum.

Note 3: Guaranteed by design.

Note 4: $\Delta r_{ON} = \Delta r_{ON}(max) - \Delta r_{ON}(min)$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Off isolation = 20log (V_S/V_D), V_D = output, V_S = input to off switch.

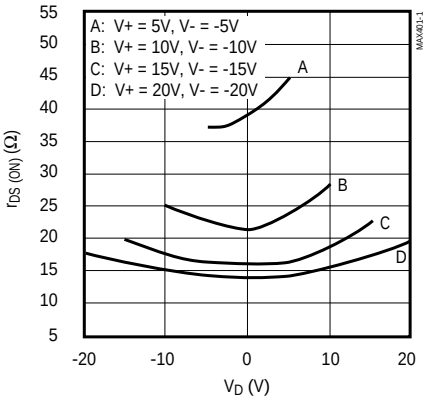
Note 6: Between any two switches.

Note 7: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

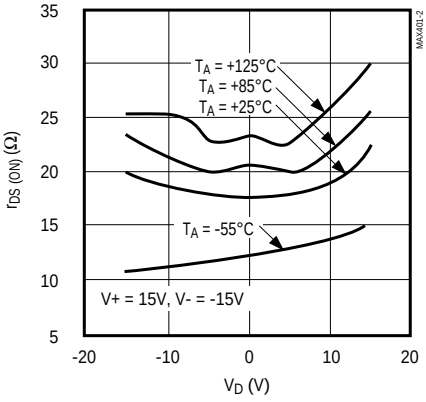
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

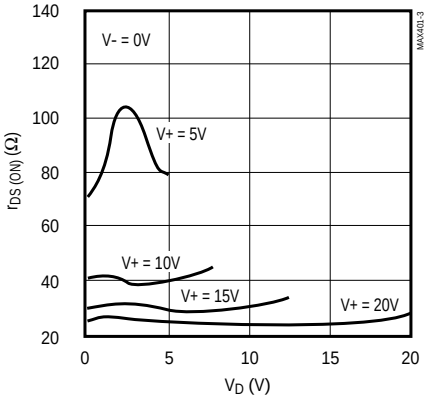
ON-RESISTANCE vs. V_D (DUAL SUPPLIES)



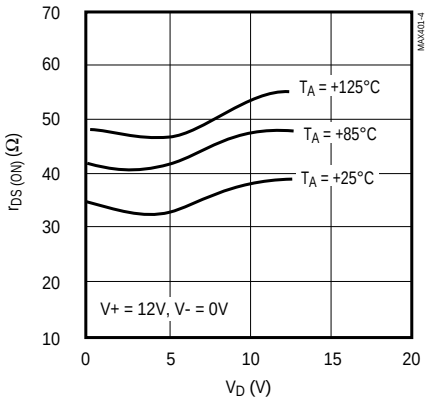
ON-RESISTANCE vs. V_D AND TEMPERATURE (DUAL SUPPLIES)



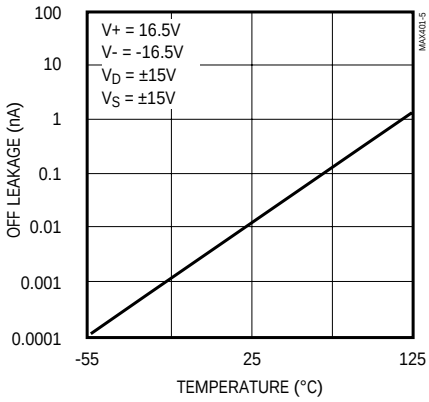
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



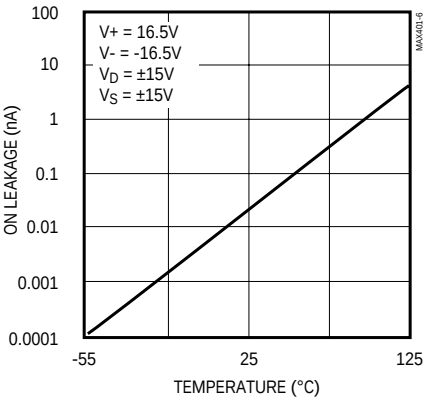
ON-RESISTANCE vs. V_D AND TEMPERATURE (SINGLE SUPPLY)



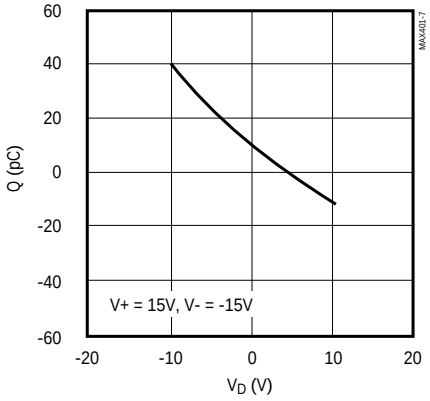
OFF LEAKAGE CURRENTS vs. TEMPERATURE



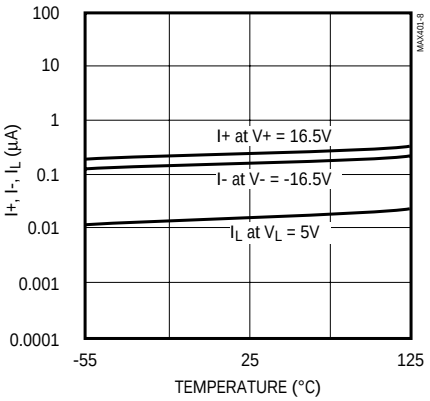
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

DG401		NAME	FUNCTION
DIP/SO	LCC		
1, 8	2, 10	D1, D2	Drain (Analog Signal)
2-7	1, 3-9, 11, 16	N.C.	Not internally connected
9, 16	12, 20	S2, S1	Source (Analog Signal)
10, 15	13, 19	IN2, IN1	Digital Logic Inputs
11	14	V+	Positive Supply-Voltage Input—connected to substrate
12	15	V_L	Logic Supply-Voltage Input
13	17	GND	Ground
14	18	V-	Negative Supply-Voltage Input
DG403		**NAME**	**FUNCTION**
DIP/SO	**LCC**		
1, 8, 3, 6	2, 10, 4, 8	D1-D4	Drain (Analog Signal)
2, 7	1, 3, 6, 9, 11, 16	N.C.	Not internally connected
16, 9, 4, 5	20, 12, 5, 7,	S1-S4	Source (Analog Signal)
10, 15	13, 19	IN2, IN1	Digital Logic Inputs
11	14	V+	Positive Supply-Voltage Input—connected to substrate
12	15	V_L	Logic Supply-Voltage Input
13	17	GND	Ground
14	18	V-	Negative Supply-Voltage Input
DG405		**NAME**	**FUNCTION**
DIP/SO	**LCC**		
1, 8, 3, 6	2, 10, 4, 8	D1-D4	Drain (Analog Signal)
2, 7	1, 3, 6, 9, 11, 16	N.C.	Not internally connected
16, 9, 4, 5	20, 12, 5, 7,	S1-S4	Source (Analog Signal)
10, 15	13, 19	IN2, IN1	Digital Logic Inputs
11	14	V+	Positive Supply-Voltage Input—connected to substrate
12	15	V_L	Logic Supply-Voltage Input
13	17	GND	Ground
14	18	V-	Negative Supply Voltage

Applications Information

Operation with Supply Voltages Other than ±15V

The DG401/DG403/DG405 switches operate with ±4.5V to ±20V bipolar supplies or with a +10V to +30V single supply. In either case, analog signals ranging from V+ to V- can be switched. The *Typical Operating Characteristics* graphs illustrate typical analog-signal and supply-voltage on-resistance variations. The usual on-resistance temperature coefficient is 0.5%/°C (typ).

Logic Inputs

These devices operate with a single positive supply or with bipolar supplies. They maintain TTL compatibility with supplies anywhere in the ±4.5V to ±20V range as long as V_L = +5V. If V_L is connected to V+ or another supply at voltages other than +5V, the devices will operate at CMOS-logic-level inputs.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V_L, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog-signal range to 1V below V+ and 1V below V-, without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

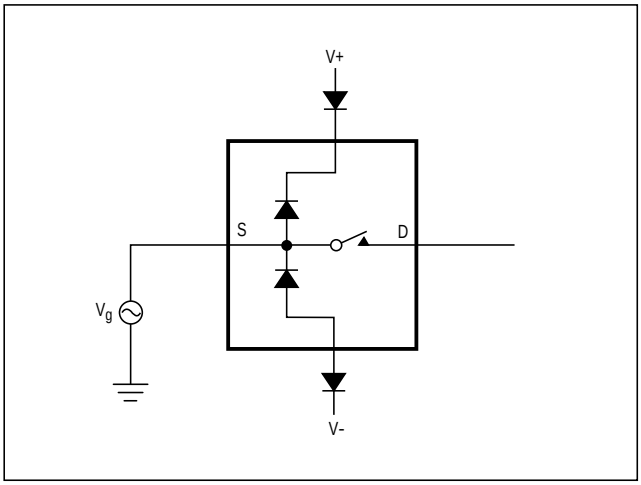


Figure 1. Overvoltage Protection Using External Blocking Diodes

Timing Diagrams/Test Circuits

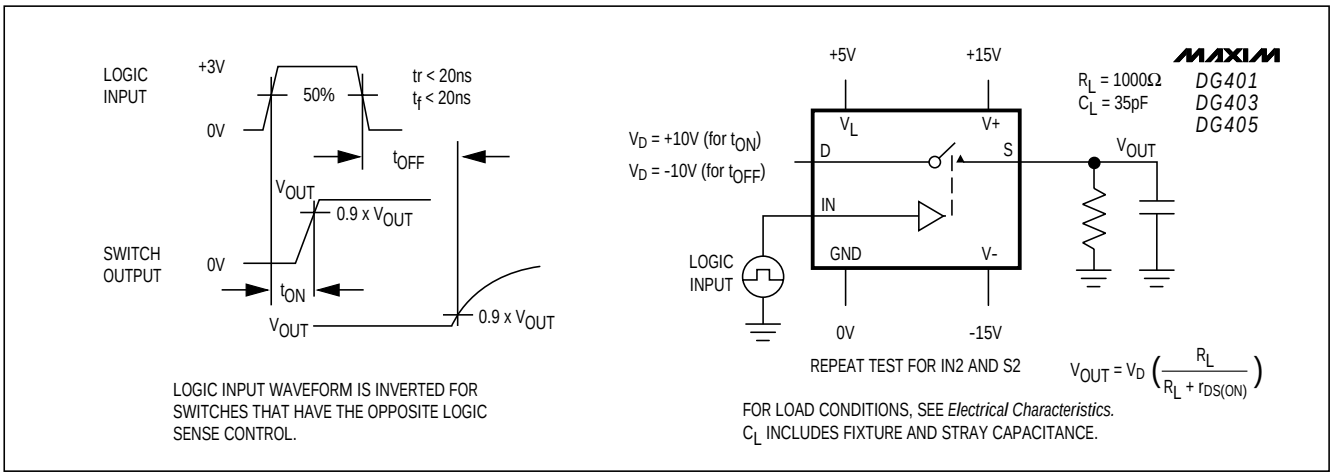


Figure 2. Switching Time

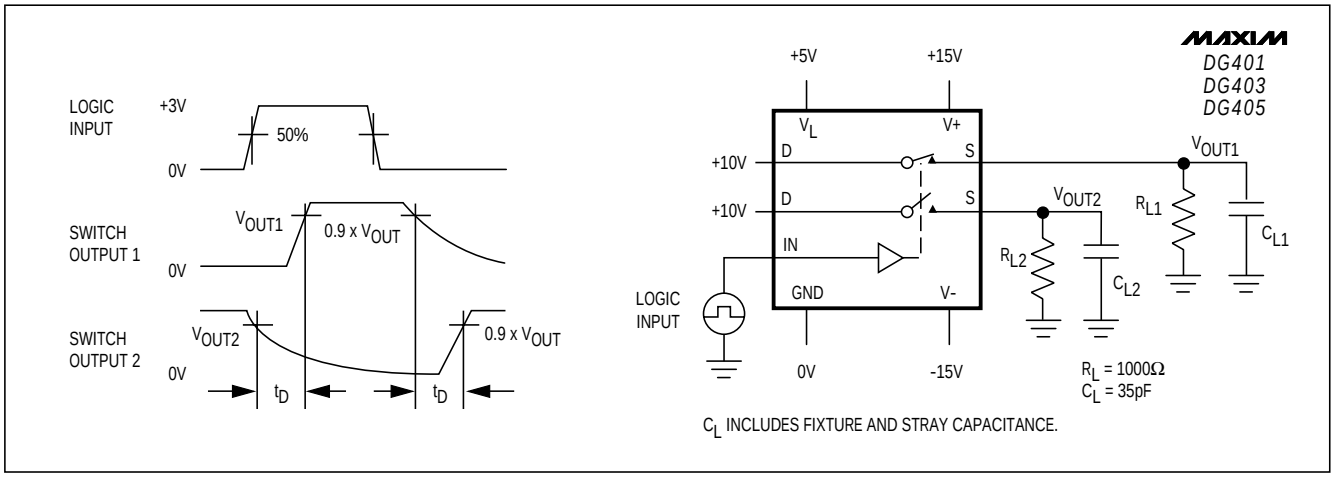


Figure 3. Break-Before-Make Interval

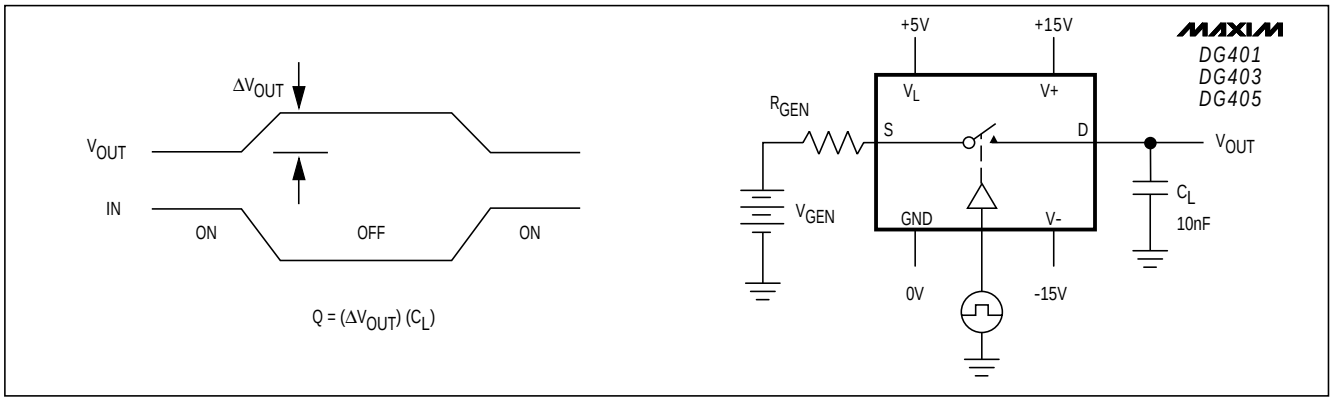
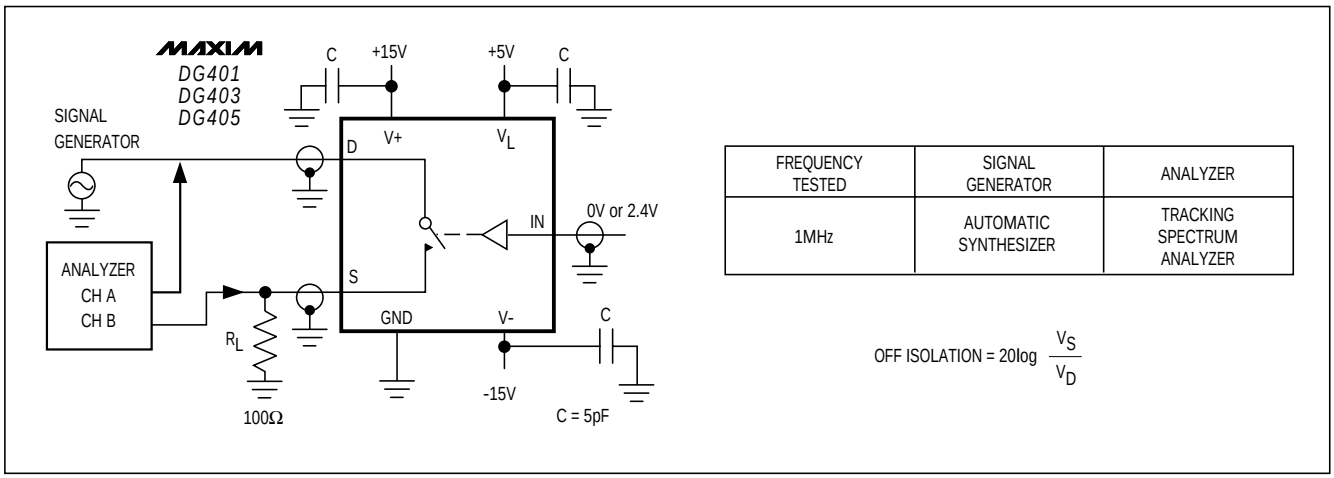


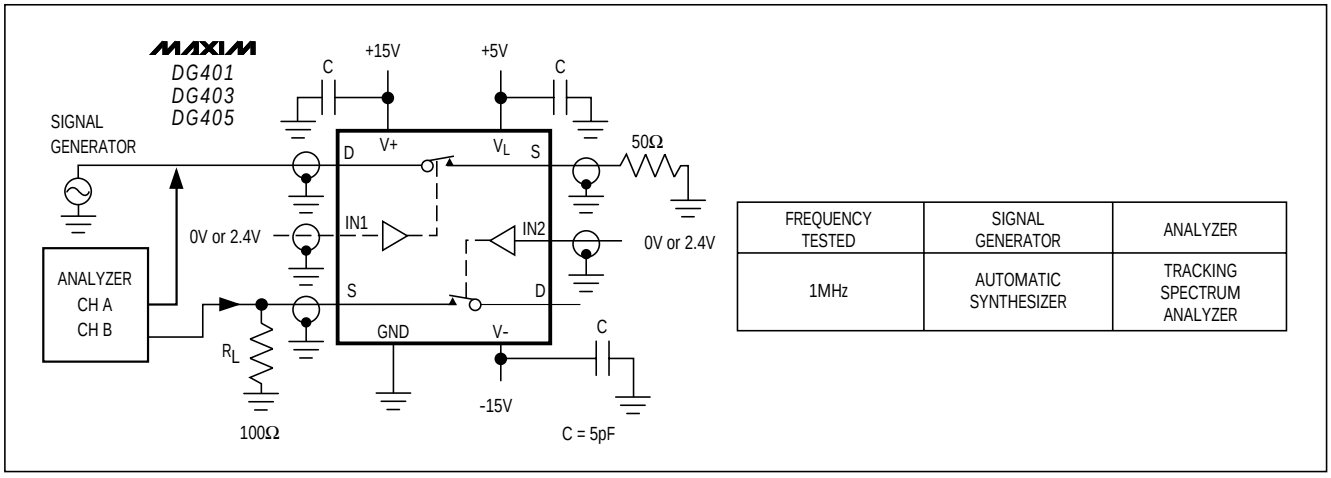
Figure 4. Charge Injection

Timing Diagrams/Test Circuits (continued)



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
1MHz	AUTOMATIC SYNTHESIZER	TRACKING SPECTRUM ANALYZER

Figure 5. Off Isolation



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
1MHz	AUTOMATIC SYNTHESIZER	TRACKING SPECTRUM ANALYZER

Figure 6. Crosstalk

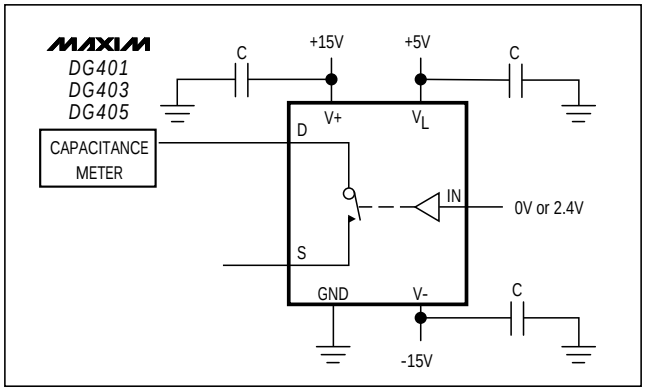


Figure 7. Channel-Off Capacitance

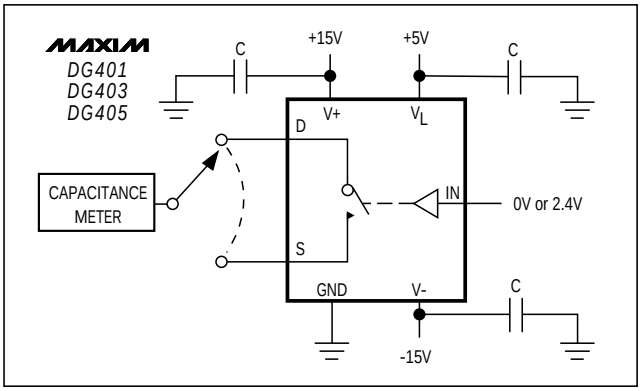


Figure 8. Channel-On Capacitance