DIO5833
Dual H-Bridge Motor Driver

Features

- Dual H-Bridge Motor Driver With Current Control
  - 1 or 2 DC Motors or 1 Stepper Motor
  - Low On-Resistance: HS + LS = 850mΩ (Typical, 25°C)
- Output Current Capability (at V_M=5V, 25°C)
  - PWP (HTSSOP) Package
    - 0.7A RMS, 1A Peak per H-Bridge
    - 1.4A RMS in Parallel Mode
  - RTE (QFN) Package
    - 0.6A RMS, 1A Peak per H-Bridge
    - 1.2A RMS in Parallel Mode
- Wide Power Supply Voltage Range
  - 2.7 to 15V
- Integrated Current Regulation
- Easy Pulse-Width-Modulation (PWM) Interface
- 1.6μA Low-Current Sleep Mode (at 5V)
- Small Package and Footprint
  - EP-TSSOP16
  - QFN 3*3-16
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Indication Pin (nFAULT)

Descriptions

The DIO5833 provides a dual-bridge motor driver solution for toys, printers, and other mechatronic applications.

The device has two H-bridges and can drive two DC brushed motors, a bipolar stepper motor, solenoids, or other inductive loads.

Each H-bridge output consists of a pair of N-channel and P-channel MOSFETs, with circuitry that regulates the winding current. With proper PCB design, each H-bridge of the DIO5833 can drive up to 700mA RMS (or DC) continuously, at 25°C with a V_M supply of 5V. The device can support peak currents of up to 1A per bridge. Current capability is reduced slightly at lower V_M voltages.

Internal shutdown functions with a fault output pi are provided for overcurrent protection, short-circuit protection, UVLO, and overtemperature. A low-power sleep mode is also provided.

Applications

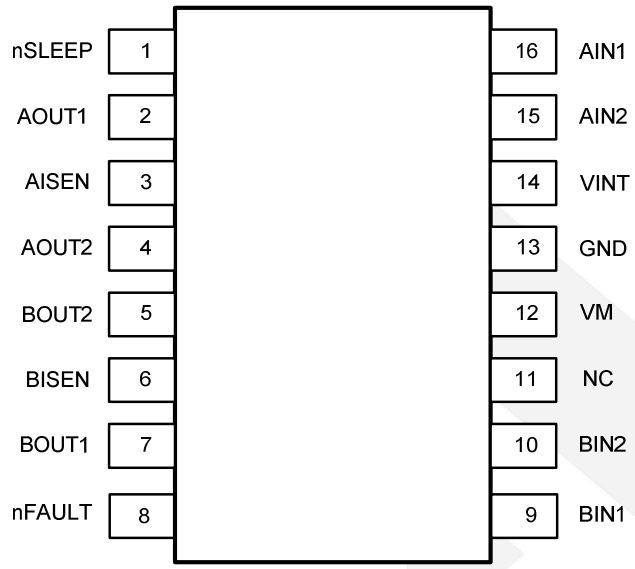
- Point-of –Sale Printers
- Video Security Cameras
- Office Automation Machines
- Gaming Machines
- Robotics
- Battery-Powered Toys

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO5833XT16	DIO5833	Green	-40 to +85°C	EP-TSSOP16	Tape & Reel, 2500
DIO5833CL16	D5833	Green	-40 to +85°C	QFN3*3-16	Tape & Reel, 5000

Pin Assignments

EP-TSSOP16



QFN3*3-16

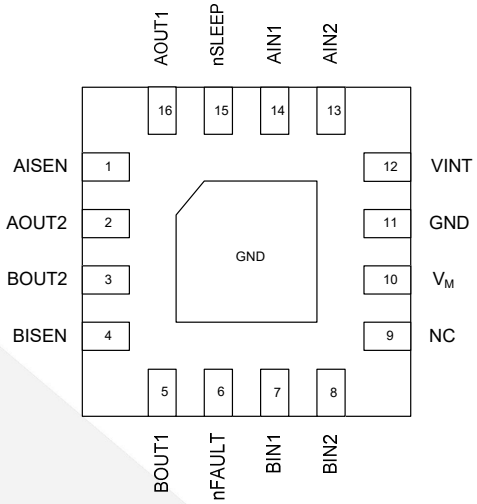


Figure 1 Top View

Pin Definitions

Pin Name	Description
GND	Device ground, Both the GND pin and device Power PAD must be connected to ground.
VINT	Internal regulator (4.5V), Internal supply voltage; bypass to GND with 2.2μF, 6.3V capacitor.
VM	Power supply, Connect to motor supply voltage; bypass to GND with a 10μF (minimum) capacitor rated for V_M.
AIN1	H-bridge A PWM input, Control the state of AOUT1 and AOUT2; internal pulldown.
AIN2	
BIN1	H-bridge B PWM input, Control the state of BOUT1 and BOUT2; internal pulldown.
BIN2	
nSLEEP	Sleep mode input, Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown.
nFAULT	Fault indication pin, Pulled logic low with fault condition; open-drain output requires an external pullup.
AISEN	Bridge A sense, Sense resistor to GND sets PWM current regulation level.
AOUT1	Bridge A output, Positive current is AOUT1 → AOUT2.
AOUT2	
BISEN	Bridge B sense, Sense resistor to GND sets PWM current regulation level.
BOUT1	Positive current is BOUT1 → BOUT2.
BOUT2	

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Power supply (V_M)		-0.3 to 16	V
Internal regulator (VINT)		-0.3 to 5.5	V
Control pins (AIN1, AIN2, BIN1, BIN2, nSLEEP, nFAULT)		-0.3 to 7	V
Voltage Continuous phase node pins (AOUT1, AOUT2, BOUT1, BOUT2)		-0.3 to V_M+0.5	V
Pulsed 10 μs phase node pins (AOUT1, AOUT2, BOUT1, BOUT2)		-1 to V_M+1	V
Continuous shunt amplifier input pins (AISEN, BISEN)		-0.3 to 0.5	V
Pulsed 10 μs shunt amplifier input pins (AISEN, BISEN)		-1 to 1	V
Operating junction temperature (T_J)		-40 to 150	°C
Storage temperature range (T_{stg})		-65 to 150	°C
Package Thermal Resistance (EP-TSSOP16)	Θ_{JA}	40.5	°C/W
	Θ_{JC}	32.9	
Package Thermal Resistance (QFN-16)	Θ_{JA}	44.7	°C/W
	Θ_{JC}	48.5	
ESD	HBM	±2000	V
	CDM	±1000	

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Rating	Unit
Power supply voltage range		2.7 to 15	V
Logic level input voltage		0 to 5.5	V
Motor RMS current	PWP package	0 to 0.7	A
	RTE package	0 to 0.6	A
Applied PWM signal to AIN1, AIN2, BIN1, or BIN2		0 to 200	kHz
Operating ambient temperature		-40 to 85	°C

Electrical Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLIES (V_M, V_{INT})						
V_M	V_M operating voltage		2.7		15	V
I_{VM}	V_M operating supply current	V_M=5V, xINx low, nSLEEP high		1.7	3	mA
I_{VMQ}	V_M sleep mode supply current	V_M=5V, nSLEEP low		1.6	4	μA
t_{SLEEP}	Sleep time	nSLEEP low to sleep mode		10		μs
t_{WAKE}	Wake-up time	nSLEEP high to output transition		110		μs
t_{ON}	Turn-on time	V_M>V_{UVLO} to output transition		100		μs
VINT	Internal regulator voltage	V_M=5V	4	4.5	5	V
CONTROL INPUTS (AIN1, AIN2, BIN1, BIN2, nSLEEP)						
V_{IL}	Input logic low voltage	xINx	0		0.7	V
		nSLEEP	0		0.5	
V_{IH}	Input logic high voltage	xINx	2		5.5	V
		nSLEEP	2.5		5.5	
VHYS	Input logic hysteresis		350	400	650	mV
IIL	Input logic low current	V_{IN} = 0 V	-1		1	μA
IIH	Input logic high current	V_{IN} = 5 V			50	μA
R_{PD}	Pulldown resistance	xINx	100	150	250	kΩ
		nSLEEP	380	500	750	
t_{DEG}	Input deglitch time			575		ns
t_{PROP}	Propagation delay INx to OUTx	V_M = 5 V		1.2		μs
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	R_{PULLUP} = 1 kΩ to 5 V	-1		1	μA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on-resistance	V_M = 5 V, I = 0.2 A, T_A = 25°C		500		mΩ
		V_M = 5 V, I = 0.2 A, T_A = 85°C		600	1475	
		V_M = 2.7 V, I = 0.2 A, T_A = 25°C		700		
		V_M = 2.7 V, I = 0.2 A, T_A = 85°C		800	1975	

$R_{DS(ON)}$	Low-side FET on-resistance	V_M = 5 V, I = 0.2 A, T_A = 25°C		350		mΩ
		V_M = 5 V, I = 0.2 A, T_A = 85°C		400	705	
		V_M = 2.7 V, I = 0.2 A, T_A = 25°C		450		
		V_M = 2.7 V, I = 0.2 A, T_A = 85°C		500	815	
I_{OFF}	Off-state leakage current	V_M = 5 V	-1		1	µA
t_{RISE}	Output rise time	V_M = 5 V; R_L = 16Ω to GND		70		ns
t_{FALL}	Output fall time	V_M = 5 V; R_L = 16Ω to V_M		80		ns
t_{DEAD}	Output dead time	Internal dead time		450		ns
PWM CURRENT CONTROL (AISEN, BISEN)						
V_{TRIP}	xISEN trip voltage		160	200	240	mV
t_{OFF}	Current control constant off time	Internal PWM constant off time		20		µs
PROTECTION CIRCUITS						
V_{UVLO}	V_M undervoltage lockout	V_M falling; UVLO report			2.6	V
		V_M rising; UVLO recovery			2.7	
$V_{UVLO,HYS}$	V_M undervoltage hysteresis	Rising to falling threshold		90		mV
I_{OCP}	Overcurrent protection trip level		1			A
t_{DEG}	Overcurrent deglitch time			2.3		µs
t_{OCP}	Overcurrent protection period			1.4		ms
T_{TSD}	Thermal shutdown temperature	Die temperature, T_J	150			°C
T_{HYS}	Thermal shutdown hysteresis	Die temperature, T_J		20		°C

Specifications subject to change without notice.

Overview

The DIO5833 device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two PMOS + NMOS H-bridges and current regulation circuitry. The DIO5833 can be powered with a supply voltage from 2.7 to 15V and can provide an output current up to 700mA RMS.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation is a 20-μs fixed off-time slow decay.

The device includes a low-power sleep mode, which lets the system save power when not driving the motor.

Functional Block Diagram

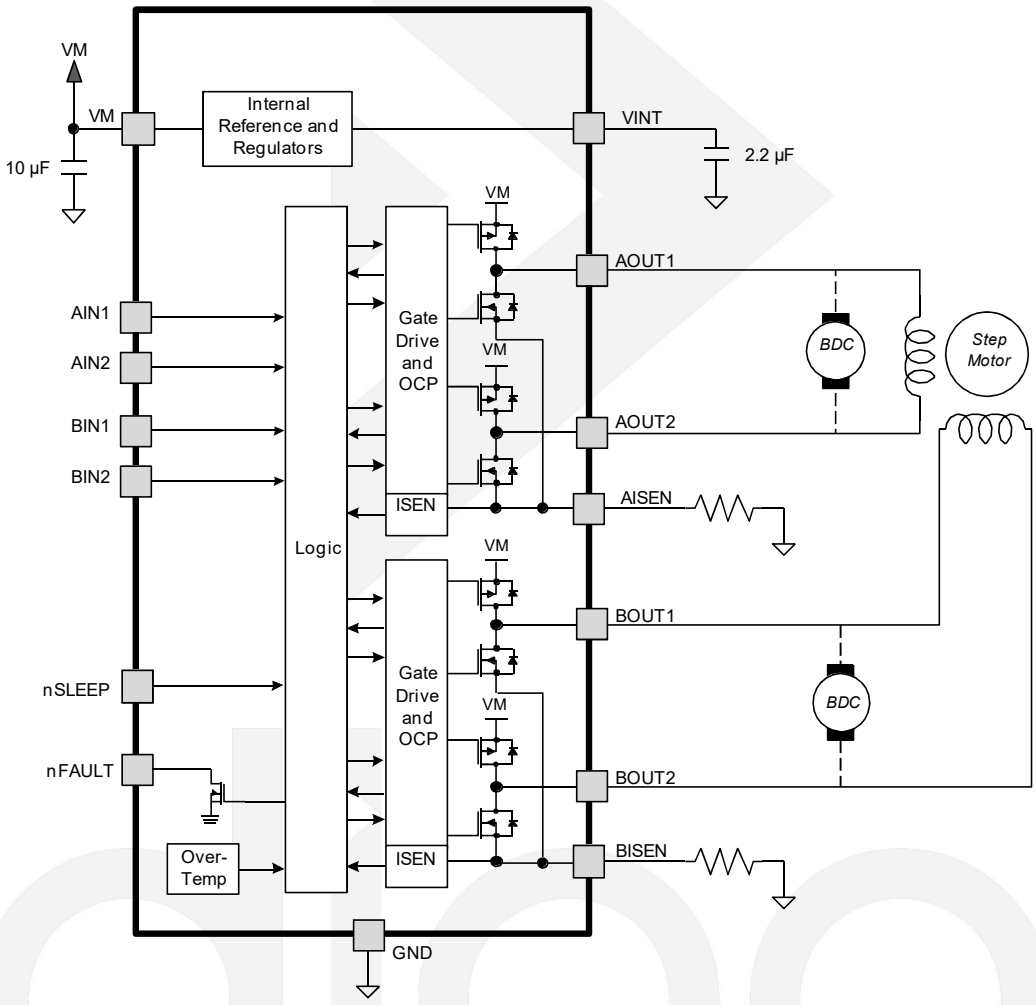


Figure 2 Function Block Diagram

Feature Description

PWM Motor Drivers

The DIO5833 contains drivers for two full H-bridges. Figure 3 shows a block diagram of the circuitry.

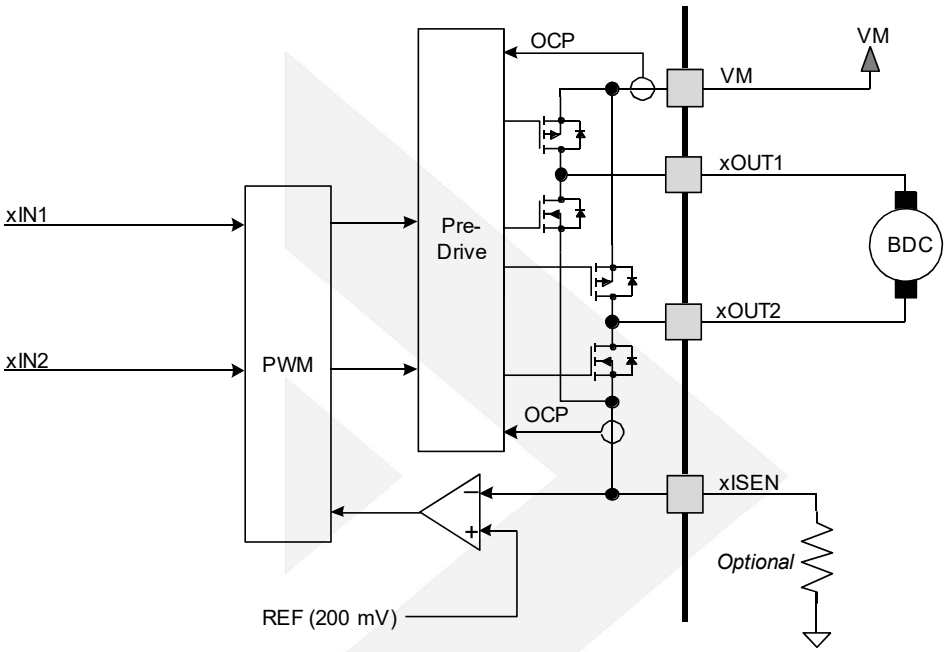


Figure 3 H-Bridge and Current-Chopping Circuitry

Bridge Control and Decay Modes

The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2 outputs; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 outputs (see Table 1).

Table 1 H-Bridge Logic

xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	0	Z	Z	Coast/fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake/slow decay

The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM and the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow (called recirculation current). To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast-decay mode, the H-bridge is disabled and recirculation current flows through the body diodes. In slow-decay mode, the motor winding is shorted by enabling both low-side FETs.

To externally pulse-width modulate the bridge in fast-decay mode, the PWM signal is applied to one xIN pin while the other is held low; to use slow-decay mode, one xIN pin is held high. See Table 2 for more information.

Table 2 PWM Control of Motor Speed

xIN1	xIN2	FUNCTION
0	0	Forward PWM, fast decay
0	1	Forward PWM, slow decay
1	0	Reverse PWM, fast decay
1	1	Reverse PWM, slow decay

The internal current control is still enabled when applying external PWM to xIN. To disable the current control when applying external PWM, the xISEN pins should be connected directly to ground. Figure 4 show the current paths in different drive and decay modes.

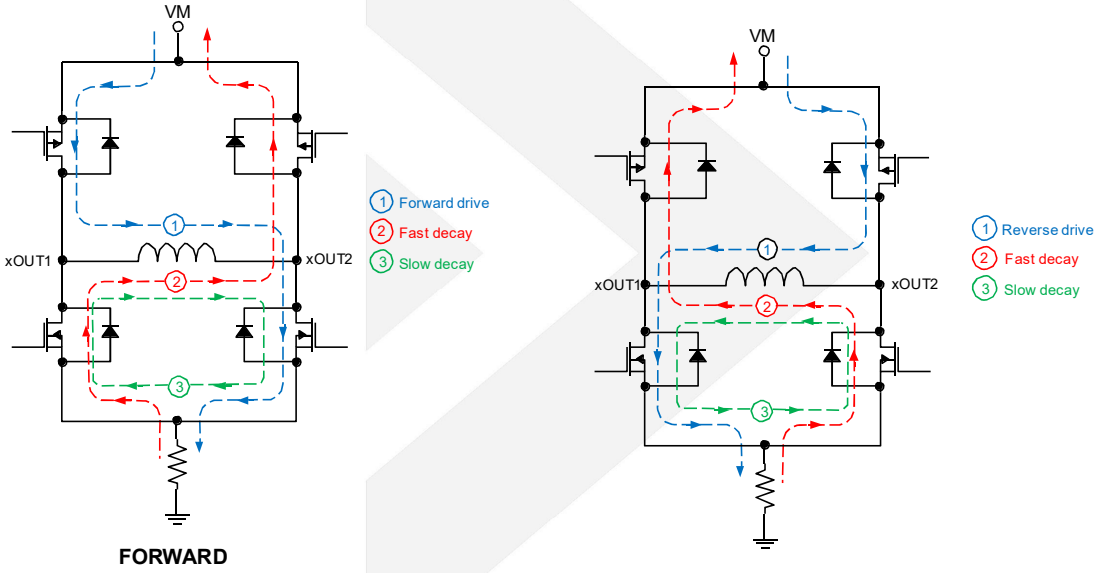


Figure 4 Drive and Decay Modes

Current Control

The current through the motor windings may be limited, or controlled, by a 20μs constant off-time PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Note that immediately after the output is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μs.

The PWM chopping current is set by a comparator that compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage, V_{TRIP}, is is fixed at 200 mV nominally.

The chopping current is calculated as in Equation 1.

$$I_{CHOP} = \frac{200mV}{R_{XISEN}} \quad (1)$$

Example: IF a 1Ω sense resistor is used, the chopping current will be 200mV/1Ω=200mA.

Delay Mode

After the chopping current threshold is reached, the H-bridge switches to slow-decay mode. This state is held for t_{off} (20 μs) until the next cycle to turn on the high-side MOSFETs.

Slow Decay

In slow-decay mode, the high-side MOSFETs are turned off and both of the low-side MOSFETs are turned on. The motor current decreases while flowing in the two low-side MOSFETs until reaching its fixed off time (typically 20 μs). After that, the high-side MOSFETs are enabled to increase the winding current again.

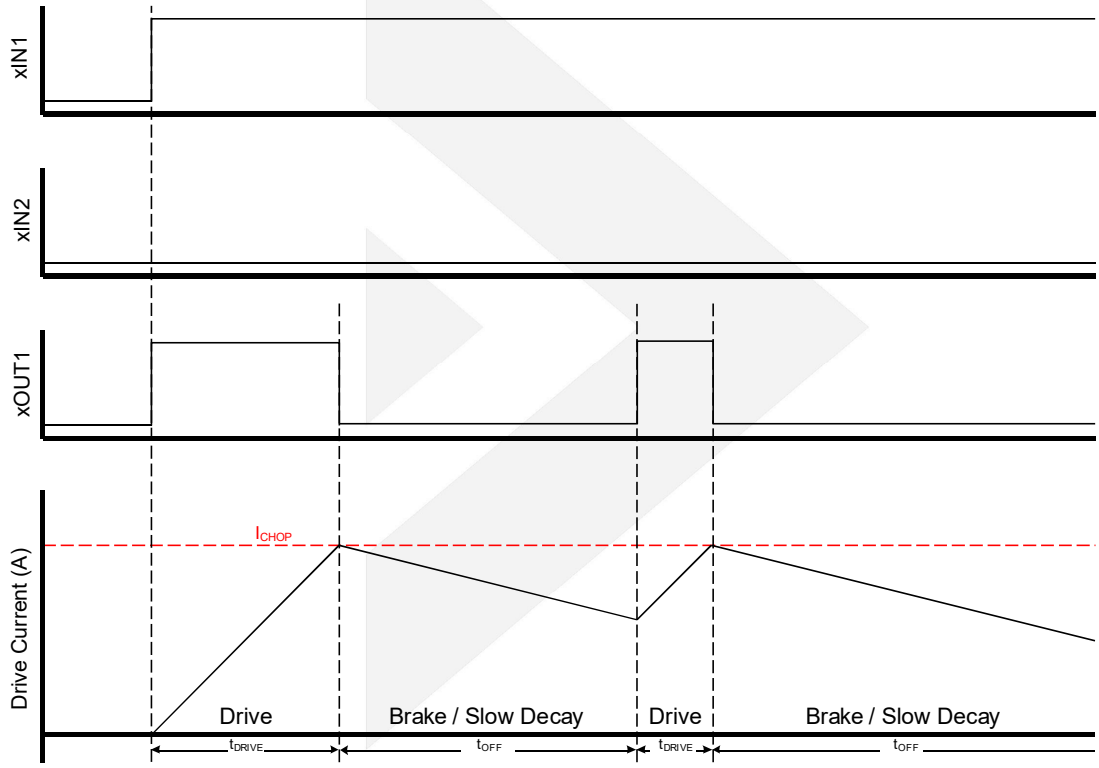


Figure 5 Current Chopping Operation

Sleep Mode

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridges are disabled, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time, t_{WAKE}, needs to pass before the motor driver becomes fully operational. To make the board design simple, the nSLEEP can be pulled up to the supply (V_M). TI recommends to use a pullup resistor when this is done. This resistor limits the current to the input in case V_M is higher than 6.5V. Internally, the nSLEEP pin has a 500kΩ resistor to GND. It also has a clamping Zener diode that clamps the voltage at the pin at 6.5V. Currents greater than 250μA can cause damage to the input structure. Therefore, TI recommends a pullup resistor between 20 to 75kΩ.

Parallel Mode

The two H-bridges in the DIO5833 can be connected in parallel for double the current of a single H-bridge. The internal dead time in the DIO5833 prevents any risk of cross-conduction (shoot-through) between the two bridges due to timing differences between the two bridges. Figure 6 shows the connections.

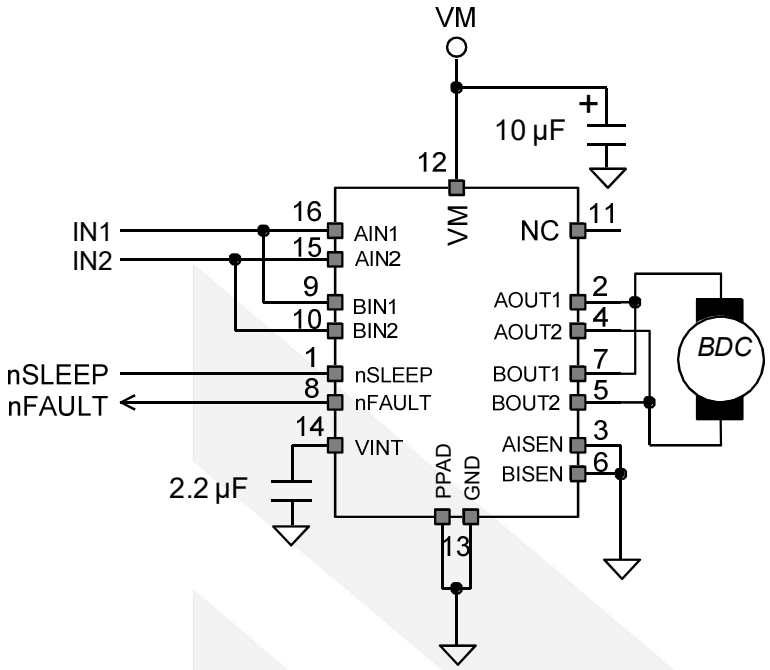


Figure 6 Parallel Mode Schematic

Protection Circuits

The DIO5833 is fully protected against overcurrent, overtemperature, and undervoltage events.

Overcurrent Protection (OCP)

An analog current limit (I_{OCP}) circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time (t_{DEG}), all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The driver is re-enabled after the OCP retry period (t_{OCP}) has passed. nFAULT becomes high again after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted. Note that only the Hbridge in which the OCP is detected will be disabled while the other bridge functions normally.

Overcurrent conditions are detected independently on both high-side and low-side devices; a short to ground, supply, or across the motor winding all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, so it functions even without presence of the xISEN resistors.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen below the specified hysteresis (T_{HYS}), operation automatically resumes. The nFAULT pin is released after operation has resumed.

UVLO

If at any time the voltage on the VM pin falls below the UVLO threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V_M rises above the UVLO threshold. The nFAULT pin is not driven low during an undervoltage condition.

Table 3 Device Protection

Fault	Condition	Error Report	H-Bridge	Internal Circuits	Recovery
V_M undervoltage (UVLO)	V_M<2.6V	None	Disabled	Disabled	V_M>2.7V
Overcurrent (OCP)	I_{OUT}>I_{OCP}	FAULTn	Disabled	Operating	OCP
Thermal Shutdown (TSD)	T_J>T_{TSD}	FAULTn	Disabled	Operating	T_J<T_{TSD}-T_{HYS}

Device Functional Modes

The DIO5833 is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled (Hi-Z). Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DIO5833 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the outputs change state after wake-up.

Table 4 Modes of Operation

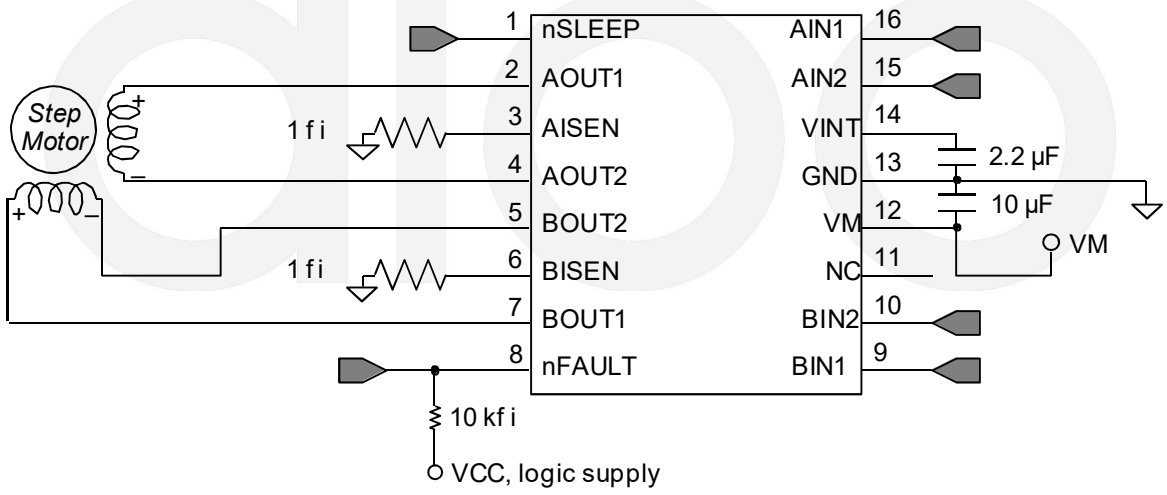
Fault	Condition	H-Bridge	Internal Circuits
Operating	nSLEEP pin high	Operating	Operating
Sleep mode	nSLEEP pin low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See Table 3

Application and Implementation

Application Information

The DIO5833 is used in stepper or brushed DC motor control. The following design procedure can be used to configure the DIO5833 in a bipolar stepper motor application.

Typical Application



Design Requirements

Table 5 gives design input parameters for system design.

Table 5 Design Parameters

Design Parameter	Reference	Example Value
Supply voltage	V_M	9V
Motor winding resistance	R_L	12Ω/phase
Motor winding inductance	L_L	10mH/phase
Motor full step angle	Θ_{step}	1.8°/step
Target stepping level	n_m	2 (half-stepping)
Target motor speed	V	120rpm
Target chopping current	I_{CHOP}	200mA
Sense resistor	R_{ISEN}	1Ω

Detailed Design Procedure

Stepper Motor Speed

The first step in configuring the DIO5833 requires the desired motor speed and stepping level. The DIO5833 can support full- and half-stepping modes using the PWM interface.

If the target motor speed is too high, the motor does not spin. Ensure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}(steps/s) = \frac{v(rpm) \times n_m(steps) \times 360°/rot}{\theta_{step}(°/step) \times 60s/\min} \quad (2)$$

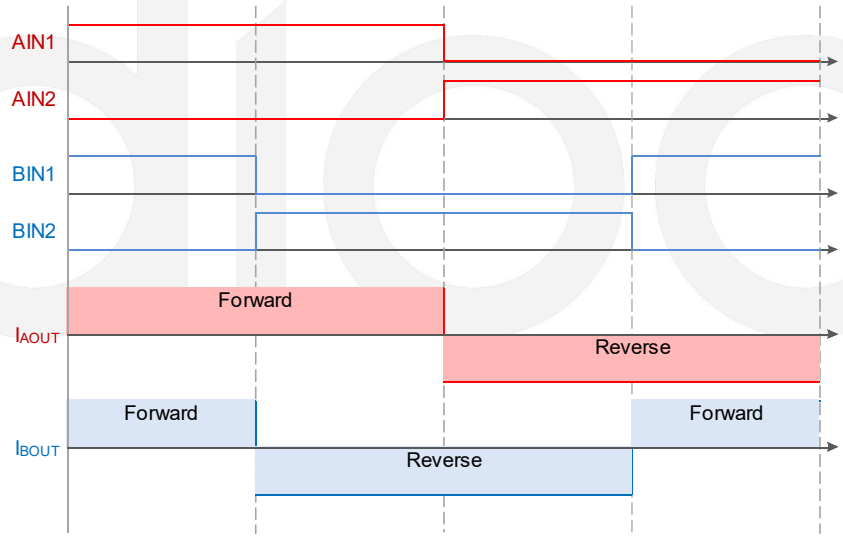


Figure 7 Full-Step Mode

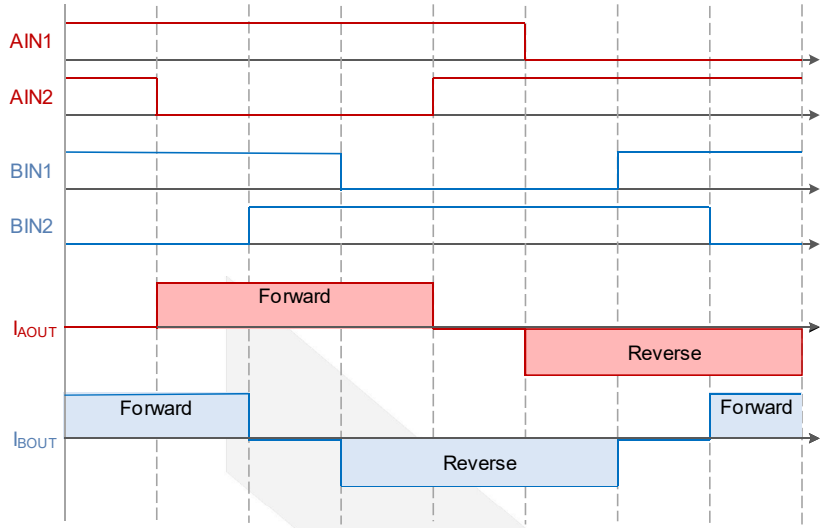


Figure 8 Half-Step Mode

Current Regulation

The chopping current (I_{CHOP}) is the maximum current driven through either winding. This quantity depends on the sense resistor value (R_{XISEN}).

$$I_{CHOP} = \frac{200mV}{R_{XISEN}} \quad (3)$$

I_{CHOP} is set by a comparator which compares the voltage across R_{XISEN} to a reference voltage. Note that I_{CHOP} must follow Equation 4 to avoid saturating the motor.

$$I_{FS}(A) < \frac{VM(V)}{R_L(\Omega) + R_{DS(ON)}HS(\Omega) + R_{DS(ON)}LS(\Omega)}$$

Where

- V_M is the motor supply voltage.
- R_L is the motor winding resistance.

Power Supply Recommendations

The DIO5833 is designed to operate from an input voltage supply (V_M) range between 2.7 to 15 V. A 10μF ceramic capacitor rated for V_M must be placed as close to the DIO5833 as possible.

Sizing Bulk Capacitance for Motor Drive System

Bulk capacitance sizing is an important factor in motor drive system design. It depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)

- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

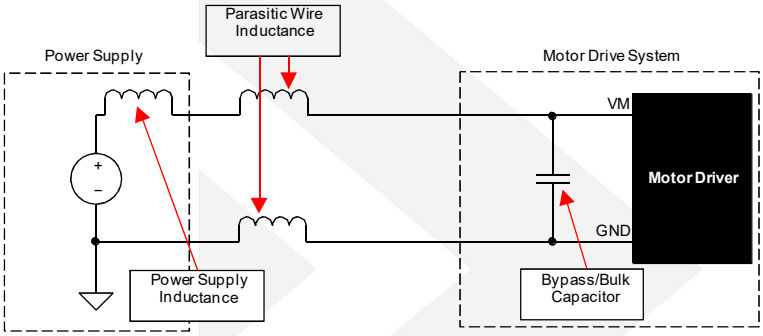


Figure 9 Setup of Motor Drive System With External Power Supply

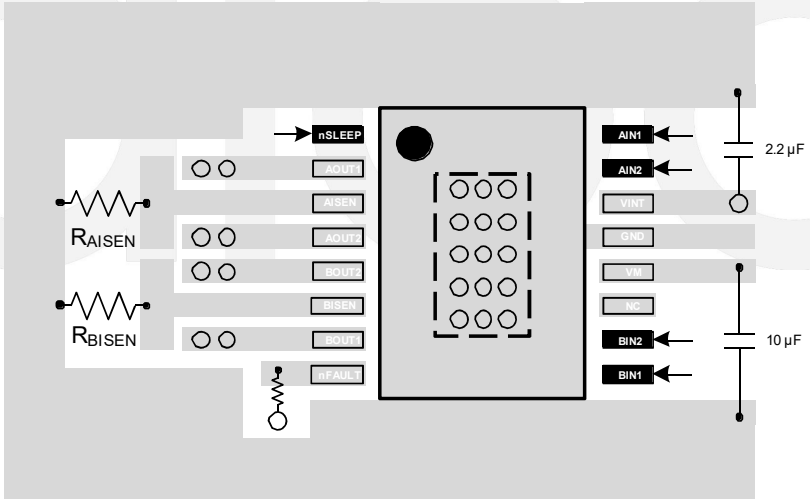
Layout

Layout Guidelines

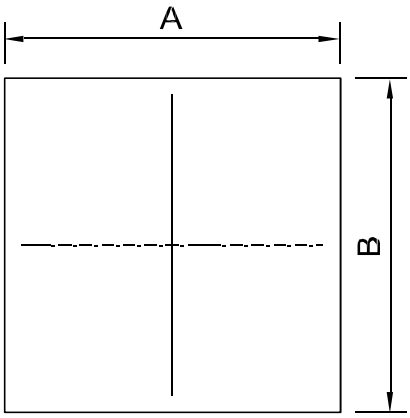
Bypass the V_M terminal to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10μF rated for V_M. This capacitor should be placed as close to the V_M pin as possible with a thick trace or ground plane connection to the device GND pin and PowerPAD.

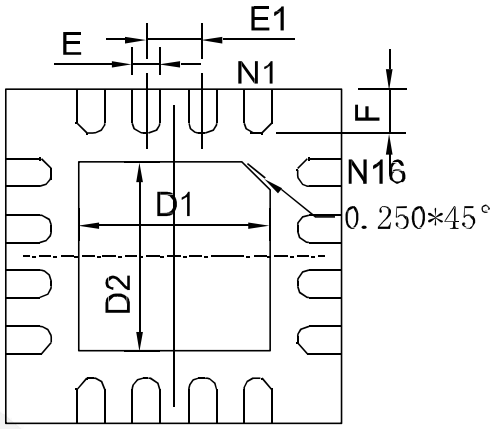
Bypass VINT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

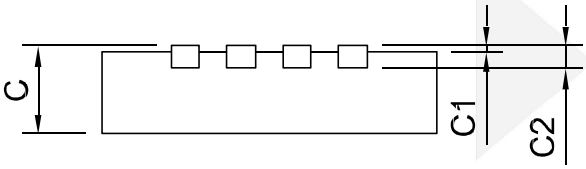
Layout Example



Physical Dimensions:QFN3*3-16

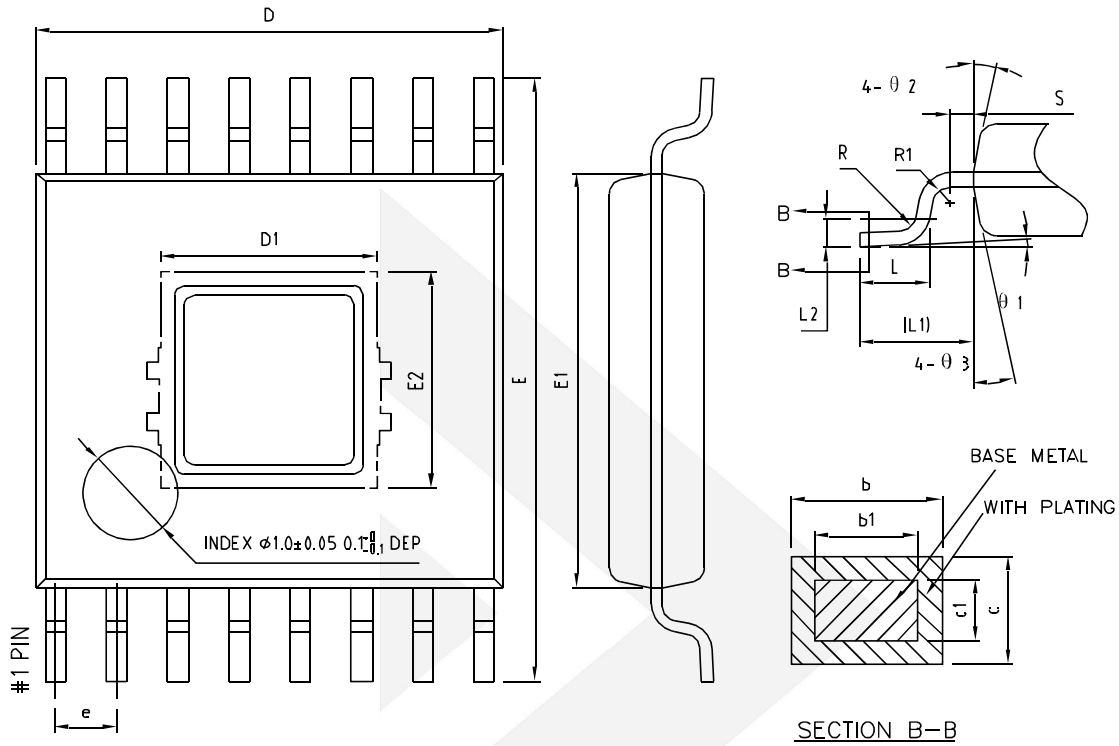


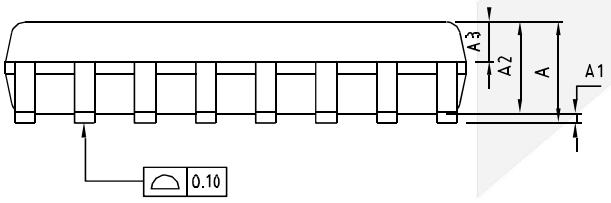




COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
Symbol	**MIN**	**NOM**	**MAX**
A	2.9	3.0	3.1
B	2.9	3.0	3.1
C	0.70	0.75	0.80
C1	0	0.025	0.05
C2	0.203TYP		
D1	1.70 TYP		
D2	1.70TYP		
E	0.25TYP		
E1	0.50TYP		
F	0.40TYP		

Physical Dimensions: EP-TSSOP16





COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
Symbol	**MIN**	**NOM**	**MAX**
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	4.86	4.96	5.06
D1	2.20	2.30	2.40
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.20	2.30	2.40
e	0.50	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2	10°	12°	14°
Θ3	10°	12°	14°