Rev 1.1

DIO59120A/B/C/D
USB-Compliant Single-cell Li-Ion 2A Switching Charger with USB-OTG Boost Regulator

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy: ±0.5% (A:4.2V,B:4.3V,C:4.35V,D:4.4V)
- ±6% Input Current Regulation Accuracy
- ±4% Charge Current Regulation Accuracy
- 26V Absolute Maximum Input Voltage
- 6V Maximum Input Operating Voltage
- 2A Charge Rate
- 1.5MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1μH External Inductor
- Dynamic Input Voltage Control
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5V, 1A Boost Mode for USB OTG for 3.2V to 4.5V Battery Input
- Available in DFN3*3-12 Package.

Descriptions

The DIO59120X combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charger regulator circuits switch at 1.5MHz to minimize the size of external passive components.

The DIO59120X provides battery charging in three phases: pre-charge, constant current and constant voltage.

To ensure USB compliance, the input current limit can be set at 500mA.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode, preventing leakage from the battery to the input.

Charge current is reduced when the die temperature reaches at 120°C, protecting the device and PCB from damage.

The DIO59120X can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery and uses the same external components used for charging the battery.

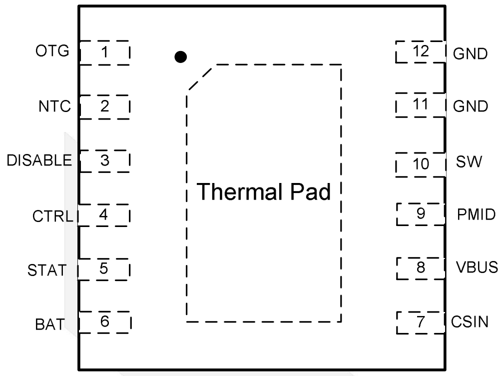
Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO59120XCD12	59120X	Green	-40 to +85°C	DFN3*3-12	Tape & Reel, 5000

Pin Assignments



DFN3*3-12

Figure 1. Pin Assignment (Top View)

Pin Definitions

Name	Description
OTG	On-The-Go, high active.
NTC	Monitor battery temperature input connected to the battery NTC resistor (10kΩ).
DISABLE	Charging enable input, charging start when disable is low.
CTRL	CTRL=0, input current limit is 500mA. CTRL=1, input current is no limit.
STAT	Status. Open-drain output indicating charge status. The IC pulls this pin LOW when charging, and pulses STAT pin when fault.
BAT	Battery Voltage. Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1μF capacitor to GND if the battery is connected through long leads.
CSIN	Charging current detection input terminal.
VBUS	Charger Input Voltage and USB-OTG output voltage. Bypass with a 1μF capacitor to PGND.
PMID	Power Input Voltage. Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 4.7μF, 6.3V capacitor to PGND.
SW	Switching Node. Connect to output inductor.
GND	Ground.
Thermal Pad	Exposed pad beneath the IC for heat dissipation. Always solder thermal pad to the board, and have via on the thermal pad plane star-connecting to GND.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
VBUS Voltage	Continuous	-1.4 to 26.0	V
	Pulsed, 100ms Maximum Non-Repetitive	-2.0 to 26.0	
STAT Voltage		-0.3 to 26.0	V
PMID Voltage		6.5	V
SW, CSIN, VBAT, DISABLE Voltage		-0.3 to 6.5	
Voltage on Other Pins		-0.3 to 6.5	V
Maximum V_{BUS} Slope above 5.5V when Boost or Charger are Active		4	V/μs
ESD	HBM	2000	V
	CDM	500	
Junction Temperature		-40 to 150	°C
Storage Temperature		-65 to 150	°C
Lead Soldering Temperature, 10 Seconds		260	°C

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Rating	Unit
Supply Voltage		4 to 6	V
Maximum Battery Voltage when Boost enabled		4.5	V
Negative VBUS Slew Rate during VBUS Short Circuit, $C_{MID} \leqslant 4.7\mu F$	$T_A \leqslant 60°C$	4	V/μs
	$T_A \geqslant 60°C$	2	
Ambient Temperature		-30 to +85	°C
Junction Temperature		-30 to +120	°C

Electrical Characteristics

V_{IN} = 5V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
I_{VBUS}	VBUS Current	V_{BUS}>$V_{BUS(min)}$, PWM Switching		10		mA
		V_{BUS}> $V_{BUS(min)}$; PWM Enabled, Not Switching		0.2		mA
		DISABLE=1		96		μA
I_{LKG}	VBAT to VBUS Leakage Current	0°C<T_J<85°C, V_{BAT}=4.2V,V_{BUS}=0V		1.6	15.0	μA
I_{BAT}	Battery is charge Current in High-Impedance Mode	DISABLE=1, 0°C<T_J<85°C, V_{BAT}=4.2V		12	20	μA
Charger Voltage Regulation						
V_{OREG}	Charge Voltage Range		4.2		4.4	V
	Charge Voltage Accuracy	T_A=25°C	-0.5%		+0.5%	
		T_J=0 to 125°C	-1%		+1%	
Charging Current Regulation						
I_{OCHRG}	Output Charge Current Range	I_{OCHRG} =101.9mV/ R_{SENSE} R_{SENSE}=51mΩ		2		A
	Charge Current Accuracy Across R_{SENSE}		-4		4	%
Logic Levels: DISABLE, OTG						
V_{IH}	High-Level Input Voltage		1.05			V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input=5V		5.0		μA
Charge Termination Detection						
$I_{(TERM)}$	Termination Current Range	$I_{(TERM)}$ =9.38mV/ R_{SENSE} R_{SENSE}=51mΩ		184		mA
	Termination Current Accuracy		-3		+3	%
	Termination Current Deglitch Time			30		ms
Input Power Source Detection						
$V_{IN(MIN)}$	VBUS Input Voltage Rising	To Initiate and Pass VBUS Validation	3.75	4	4.25	V
V_{hys}				0.3		V
t_{VBUS_VALID}	VBUS Validation Time			30		ms
Special Charger (V_{BUS})						
V_{SP}	Special Charger VBUS Voltage			4.5		V

	Special Charger Set point Accuracy		-4		+4	%
Input Current Limit						
I_{INLIM}	Input Current Limit Threshold	CTRL=0	470	500	530	mA
		CTRL=1		No limit		
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold	Below $V_{(OREG)}$	70	100	130	mV
	Deglitch Time	V_{BAT} Falling Below V_{RCH} Threshold		30		ms
STAT Output						
$V_{STAT(OL)}$	STAT Output Low	I_{STAT}=10mA			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	V_{STAT}=5V			1	μA
Sleep Comparator						
V_{SLP}	Sleep-Mode Entry Threshold, $V_{BUS}– V_{BAT}$	$4V \leqslant V_{BAT} \leqslant V_{OREG}$, V_{BUS} Falling	0	0.04	0.1	V
$V_{SLP-EXIT}$	Sleep-Mode Exit Threshold, $V_{BUS}– V_{BAT}$			0.1		V
t_{SLP_EXIT}	Deglitch Time for VBUS Rising Above V_{BAT} by V_{SLP}	Rising Voltage		30		ms
Power Switches						
$R_{DS(ON)}$	Q3 On Resistance(VBUS to PMID)	$I_{IN(LIMIT)}$=500mA		86		mΩ
	Q1 On Resistance(PMID to SW)			85		
	Q2 On Resistance(SW to GND)			75		
Charger PWM Modulator						
f_{SW}	Oscillator Frequency			1.5		MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			6		%
I_{SYNC}	Synchronous to Non-Synchronous Current Cut-Off Threshold	Low-Side MOSFET(Q2) Cycle-by-Cycle Current Limit		300		mA
Boost Mode Operation						
V_{BOOST}	Boost Output Voltage at VBUS	2.5V < V_{BAT}<4.5V, I_{LOAD} from 0 to 200mA	4.85	5.05	5.2	V
		3.0V < V_{BAT}<4.5V, I_{LOAD} from 0 to 500mA	4.8	5.05	5.2	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{BAT}=3.6V, I_{OUT}=0		500		μA
$I_{LIMPK(BST)}$	Q2 Valley Current Limit			2.5		A
$UVLO_{BST}$	Minimum Battery Voltage for Boost	While Boost Active		2.6		V

	Operation	To Start Boost Regulator		2.7		
Battery Detection						
I_{DETECT}	Battery Detection Sink Current	Begins after Charge Termination Detected		10		mA
t_{DETECT}	Battery Detection Time			30		ms
Protection and Timers						
$VBUS_{OVP}$	VBUS Over-Voltage Shutdown	V_{BUS} Rising	5.82	6	6.2	V
	Hysteresis	V_{BUS} Falling		200		mV
$I_{LIMPK(CHG)}$	Q1 Cycle-by-Cycle Peak Current Limit	Charge Mode		3.4		A
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	1.95	2	2.05	V
	Hysteresis	V_{BAT} Falling		100		mV
I_{SHORT}	Linear Charging Current	$V_{BAT}<V_{SHORT}$	20	30	40	mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold	T_J Rising		145		℃
	Hysteresis	T_J Falling		10		℃
T_{CF}	Thermal Regulation Threshold	Charge Current Reduction Begins		120		℃
t_{INT}	Detection Interval			30		ms
NTC						
T_{DET_RANGE}	Detected temperature range	R_{NTC}=10 KΩ	0		50	℃
V_{NTC_HOT}	High temperature detection voltage threshold	Battery temperature rise		0.12		V
	High temperature detection voltage hysteresis	Battery temperature drop		40		mV
V_{NTC_COLD}	Low temperature detection voltage threshold	Battery temperature drop		0.9		V
	Low temperature detection voltage hysteresis	Battery temperature rise		60		mV

Block Diagram

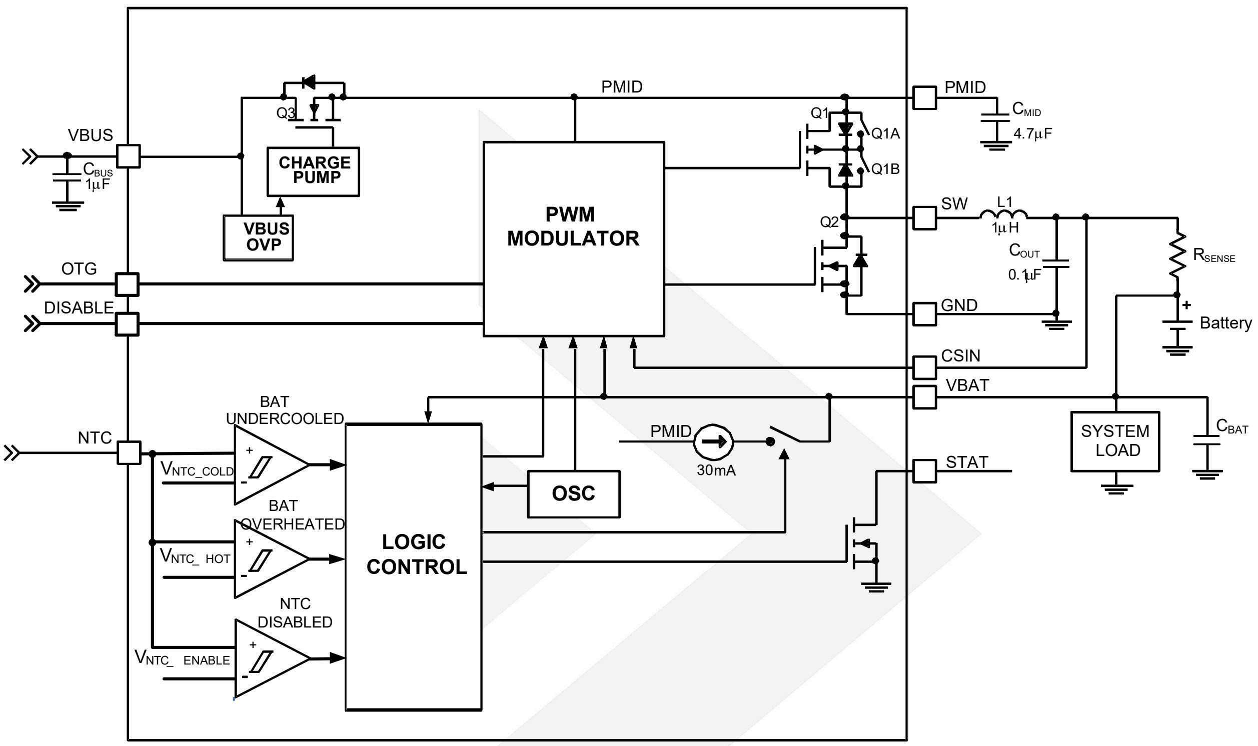


Figure 2. IC and System Block Diagram

Typical Application

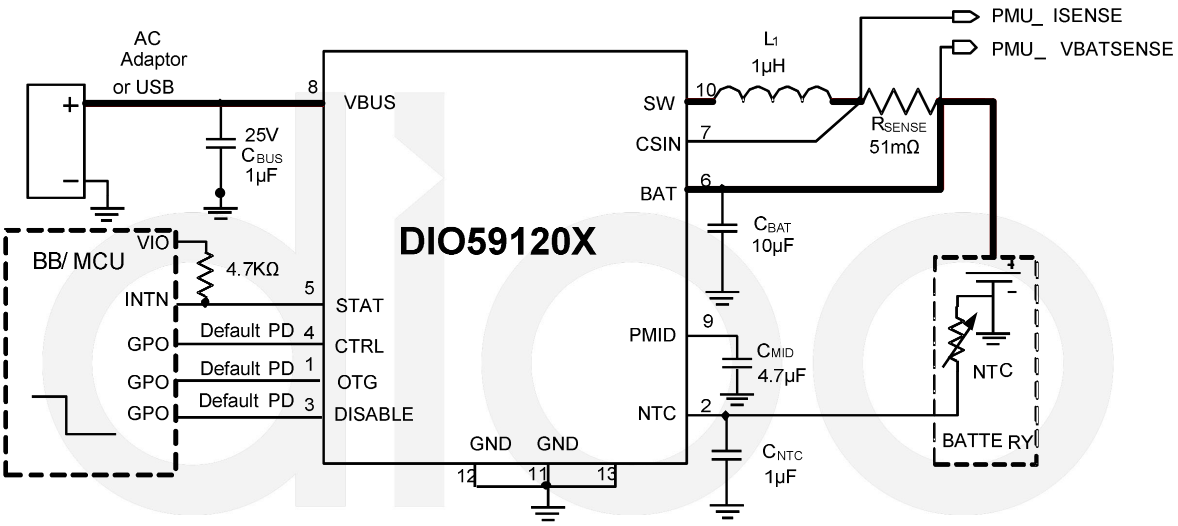


Figure 3. Typical Application

Application Information

Circuit Description/Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

DIO59120X combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5V to USB On-The-Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The DIO59120X has three operating modes:

1. Charge Mode:
   Charge a signal-cell Li-ion or Li-polymer battery.
2. Boost Mode:
   Provide 5V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.
3. High-Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery.

Charge Mode

In charge Mode, DIO59120X employs four regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be set by CTRL pin.
2. Charging Current: Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
3. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage roses, the battery's internal impedance and R_{SENSE} work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the I_{TERM} threshold.
4. Temperature: If the IC's junction temperature reaches 120℃,charge current is reduced until the IC's temperature stabilizes at 120℃.
5. An additional loop limits the amount of drop on VBUS to a voltage (V_{SP}) to accommodate "special chargers" that limit current to a lower current than might be available from a "normal" USB wall charger.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre-charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The DIO59120X is designed to work with a current-limited input source at VBUS. During the current regulation phase of charging, I_{INLIM} limits the current available to charge the battery and power the system. The effect of I_{INLIM} on I_{CHARGE} can be seen in Figure 5.

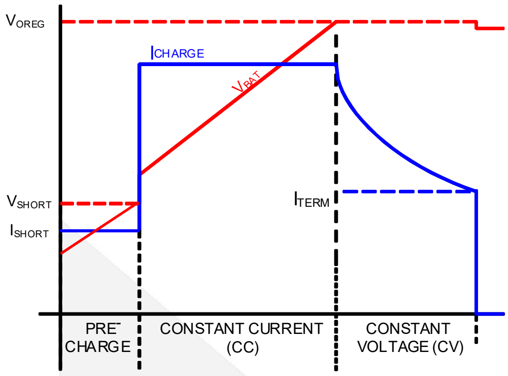


Figure 4. Charge Curve, I_{CHARGE} Not Limited by I_{INLIM}

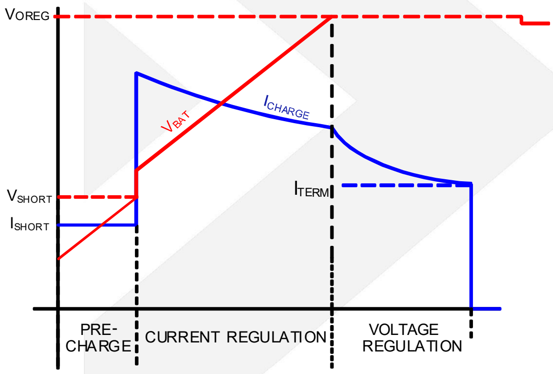


Figure 5. Charge Curve, I_{INLIM} Limits I_{CHARGE}

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to I_{TERM} value, the charge cycle is complete.

A new charge cycle begins when one of the following occurs:

- The battery voltage falls below V_{OREG}-V_{RCH}
- VBUS Power on Reset (POR) clears and the battery voltage is below the V_{SHORT}.
- Reset DISABLE pin.

PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulator the output voltage and battery charge currents. The synchronous rectifier (Q2) has a current limit that which off the FET when the current is negative by more than 400mA peak. This prevents current flow from battery.

V_{BUS} POR/Non-Compliant Charger Rejection

When the IC detects that VBUS has risen above $V_{IN(MIN)}$ (4.3V), the IC applies a 250Ω load from VBUS to GND. To clear the VBUS POR (Power-On-Reset) and begin charging, VBUS must remain above $V_{IN(MIN)}$ and below $VBUS_{OVP}$ for t_{VBUS_VALID} (30ms) before the IC initiates Charging. The VBUS validation sequence always occurs charging is initiated or re-initiated (for example, after a VBUS OVP fault or a V_{RCH} recharge initiation).

t_{VBUS_VALID} ensures that unfiltered 50/60Hz chargers and other non-compliant chargers are rejected.

Special Charger

The DIO59120X has additional functionality to limit input current in case a current-limited "special charger" is supplying VBUS. These slowly increase the charging current until either.

- I_{INLIM} or $I_{OCHARGE}$ is reached

or

- V_{BUS}=V_{SP}.

If V_{BUS} collapses to V_{SP} when the current is ramping up, the DIO59120X charge with an input current that keeps V_{BUS}=V_{SP}.

Thermal Regulation and Protection

When the IC's junction temperature reaches T_{CF} (about 120℃), the charger reduces its output current to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, and STAT is pulsed. Charging resumes after the die cools to about 120℃.

Charge Mode Input Supply Protection

Sleep Mode

When V_{BUS} falls below V_{BAT}+V_{SLP} and V_{BUS} is above $V_{IN(MIN)}$, the IC enters Sleep Mode to prevent the battery from draining into VBUS. During Sleep Mode, reverse current is disabled by body switching Q1.

Input Supply Low-Voltage Detection

The IC continuously monitors VBUS during charging. If V_{BUS} falls below $V_{IN(MIN)}$, the IC:

1. Terminates charging.
2. Pulses the STAT pin.

If V_{BUS} recovers above the $V_{IN(MIN)}$ rising threshold after time 30ms, the charging process is repeated. This function prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low-current-capable OTG device.

Input Over-Voltage Detection

When the V_{BUS} exceeds $VBUS_{OVP}$, the IC:

1. Turns off Q3
2. Suspends charging
3. Pulses the STAT pin.

When V_{BUS} falls about 200mV below $VBUS_{OVP}$, the fault is cleared and charging resumes after V_{BUS} is revalidated (see VBUS POR/Non-Compliant Charger Rejection).

Charge Mode Battery Detection & Protection

VBAT Over-Voltage Protection

The OREG voltage regulation loop prevents V_{BAT} from overshooting the OREG voltage when the battery is removed. If the VBAT Pin voltage is higher than 4.8V, the STAT pin pulses.

Battery Detection During Charging

The IC can detect the presence, absence, or removal of a battery. During normal charging, once VBAT is close to VOREG and the termination charge current is detected, the IC terminates charging and turns on a discharge current, I_{DETECT}, for 30ms. If VBAT is still above 2V, the battery is present. If VBAT is below 2V, the battery is absent and IC enters No Battery Mode.

Battery Short-Circuit Protection

If the battery voltage is below the short-circuit threshold (V_{SHORT}); a linear current source, I_{SHORT}, supplies V_{BAT} until $V_{BAT}>V_{SHORT}$.

NTC protection

NTC pin output 30uA current to NTC resistor (typical 10kΩ). When battery temperature rises to 50℃ (VNTC=120mV) or falls to 0℃(VNTC=0.9V), the IC stops charging, and IC pulses the STAT pin. If NTC protection is not used, NTC pin must connect to 10kΩ normal resistor to ground.

System Operation with No Battery

The DIO59120X continues charging after VBUS POR, regulating the V_{BAT} line to typical 3.8V. In this way, the DIO59120X can start the system without a battery. Re-connect power to VBUS or reset DISABLE pin, IC can exit No Battery Mode.

Charger Status/Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 1. STAT Pin Function

Charge State	STAT Pin
No Charging	OPEN
Charging	LOW
Fault	2Hz Pulse

The types of fault in Charge Mode (see Table 2).

Table 2. Fault Status During Charge Mode

Fault Description
VBUS OVP
Sleep Mode
Poor Input Source
Battery OVP
Thermal Shutdown
No Battery
NTC protection

Boost Mode

Boost Mode can be enabled if OTG pin is high.

Boost COT Control

The IC uses a constant on-time and valley current detect to regulate VBUS. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During COT Mode, the output voltage drops slightly as the input current rises.

PFM Mode

If VBUS>$VREF_{BOOST}$ (nominally 5.05V) when the valley current comes to 0, the regulator enters PFM Mode. Boost pulses are inhibited until V_{BUS}<$VREF_{BOOST}$. Once V_{BUS}<$VREF_{BOOST}$, boost pulses are allowed for one or several times until V_{BUS}>$VREF_{BOOST}$. Therefore the regulator behaves like a burst mode regulator, with the average of its output voltage ripple at 5.05V in PFM Mode.

Table 3. Boost PWM Operating States

Mode	Description	Invoked When
LIN	Linear Startup	V_{BAT}>V_{BUS}
SS	Boost Soft-Start	V_{BUS}<V_{BST}
BST	Boost Operation Mode	V_{BAT}>$UVLO_{BST}$ and SS Completed

Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from V_{BUS} to V_{BAT}.

LIN State

When EN rises, if V_{BAT}>$UVLO_{BST}$, the regulator attempts to bring PMID within 200mV of VBAT using an internal 800mA current source from VBAT (LIN State). If PMID has not achieved V_{BAT}- 200mV after 500μs, a FAULT state is initiated.

SS State

When PMID>V_{BAT}-200mV, the boost regulator begins switching with a SS modulator. The output slews up slowly and smoothly until V_{BUS}=$VREF_{BOOST}$.

If the output fails to achieve set point (VBST) within SS time, normally 128μs, a fault state is initiated.

BST State

This is the normal operating mode of the regulator. The regulator uses a constant on-time and valley current detect modulation scheme. The minimum t_{ON} is proportional to $\frac{V_{OUT} - V_{IN}}{V_{OUT}}$, which keeps the regulator's switching frequency reasonably constant in CCM.

To ensure the VBUS does not pump significantly above the regulation point, the boost switch remains off as long as FB>V_{REF}.

Restart After Boost Faults

If boost was enabled and the fault condition persists, restart is attempted every 10ms until the fault clears.

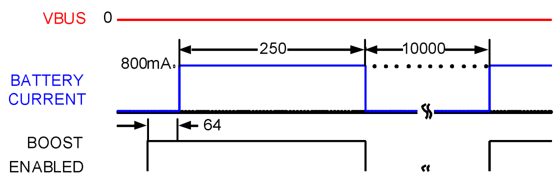
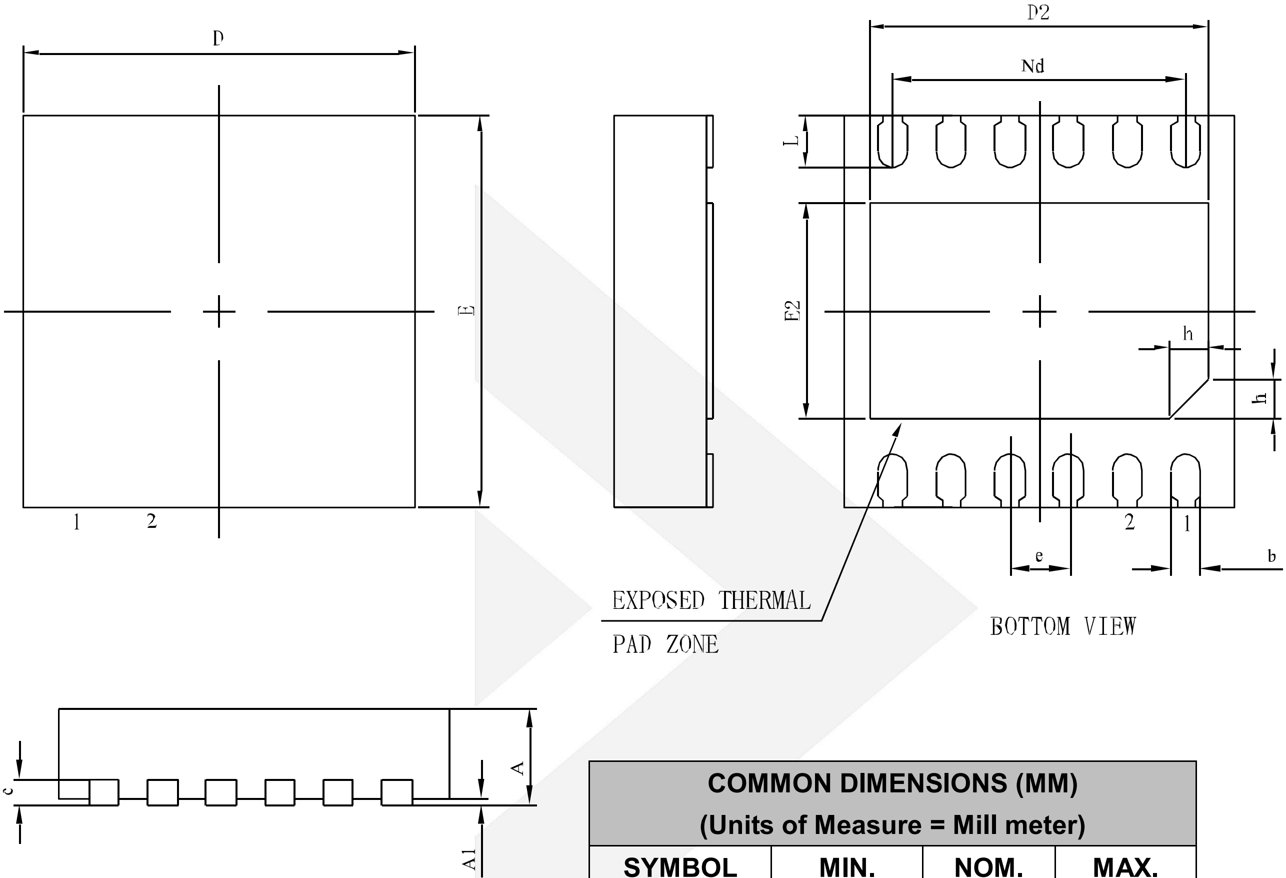


Figure 7. Boost Response Attempting to Start into VBUS Short Circuit (Times in μs)

PCB Layout Recommendations

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. All power and ground pins must be routed to their bypass capacitors, using top copper whenever possible. Copper area connecting to the IC should be maximized to improve thermal performance if possible.

Physical Dimensions: DFN3*3-12



COMMON DIMENSIONS (MM) (Units of Measure = Mill meter)			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.16	0.23	0.28
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e	0.45BSC		
Nd	2.25BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30
L/F 载体尺寸（Mil）	106*75		