DK-START-GW1NR9 V1.1

User Guide

DBUG361-1.2E, 2019/12/19

Disclaimer

Revision History

Date	Version	Description
03/19/2019	1.0E	Initial version published.
11/29/2019	1.1E	MIPI input function removed.
12/19/2019	1.2E	The version of DK-START-GW1NR9 added.

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1 About This Guide

1.1 Purpose

The DK-START-GW1NR9 V1.1 user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the function, circuit, and pin distribution of each module;
3. Attentions in use of the development board;
4. An introduction to the usage of the FPGA development software.

1.2 Supported Products

The information in the guide applies to GW1NR series of FPGA products: GW1NR-9.

1.3 Related Documents

The user manuals are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com

1. DS117, GW1NR Series FPGA Products Data Sheet
2. UG119, GW1NR Series of FPGA Products Package and Pinout Manual
3. UG801, GW1NR-9 Devices Pinout Manual
4. UG290, Gowin FPGA Products Programming and Configuration Manual
5. SUG100, Gowin YunYuan Software User Guide

1.4 Terminology and Abbreviation

The terminology and abbreviation used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviation and Terminology

Terminology and Abbreviation	Meaning
FPGA	Field Programmable Gate Array
SIP	System in Package
SDRAM	Synchronous Dynamic RAM
PSRAM	Pseudo static random access memory
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	Four-input Look-up Tables
LUT5	Five-input Look-up Tables
LUT6	Six-input Look-up Tables
LUT7	Seven-input Look-up Tables
LUT8	Eight-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input / Output Block
S-SRAM	Shadow SRAM
B-SRAM	Block Static Random Access Memory
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
LQ144	LQFP144 package

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

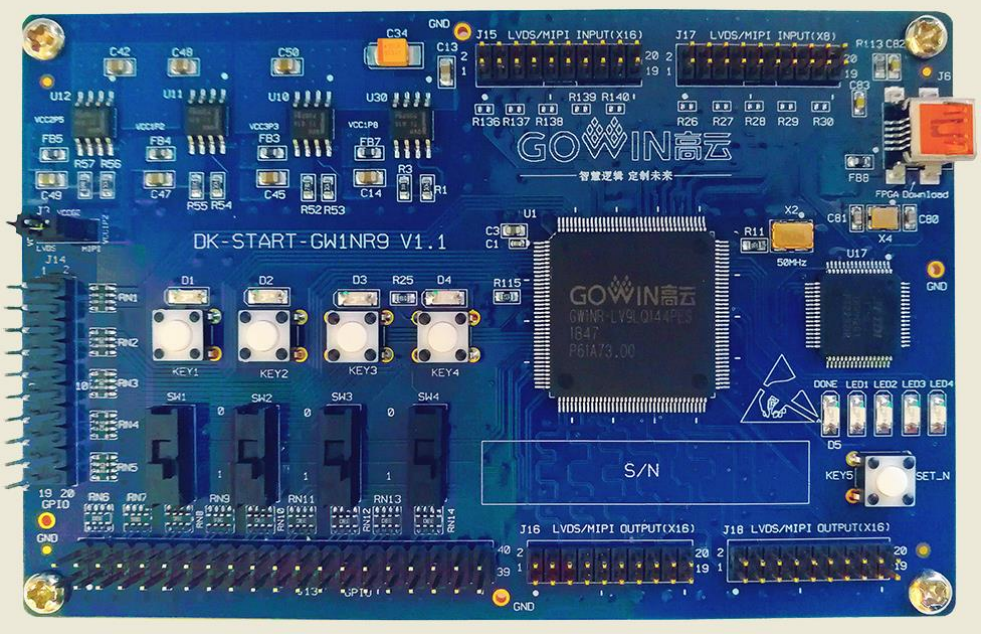
E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

2 Development Board Introduction

2.1 Overview

Figure2-1 DK-START-GW1NR9 V1.1 Development Board



The development board adopts the GW1NR-9 device, which is embedded with PSRAM of 64Mbit, user flash memory and other resources. The GW1NR series of FPGA products are the first generation of the Gowin LittleBee® family and it is a SIP chip. Based on GW1N, GW1NR series integrates abundant PSRAM. At the same time, it has the characteristics of low power consumption, instant-start, low cost, non-volatility, high security, rich packages, convenient and flexible usage, etc., which can effectively reduce the learning cost and help users quickly enter the design and development field of programmable logic devices.

The development board offers abundant external interfaces, including MIPI/LVDS interfaces, GPIO interfaces, etc. There are also sliding switch,

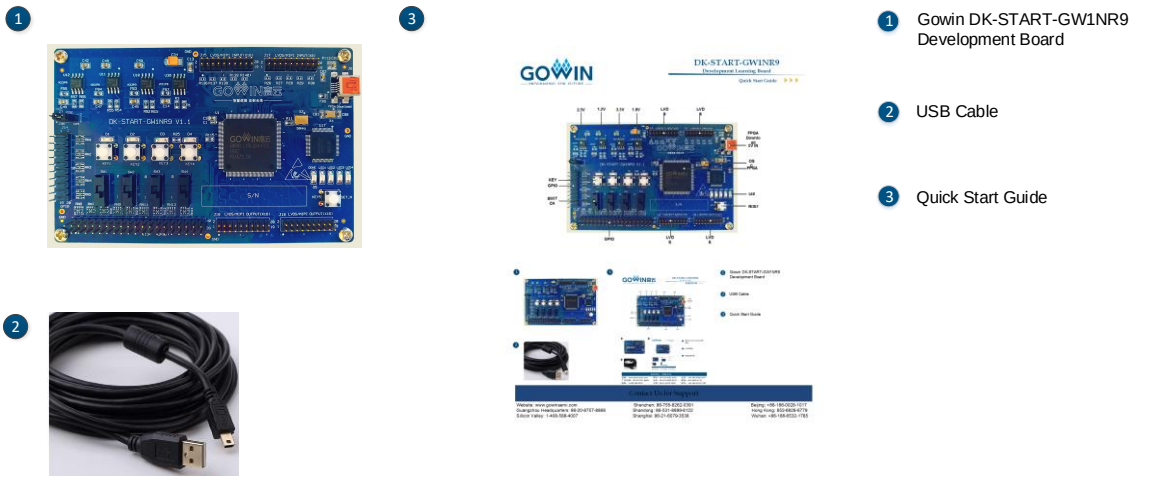
button switch, LED, clock, reset and other resources for developers or fans to learn to use.

2.2 A Development Board Suite

A development board suite includes the following items:

- DK-START-GW1NR9 V1.1 Development Board
- USB Cable
- Quick Start Guide

Figure2-2A Development Board Suite



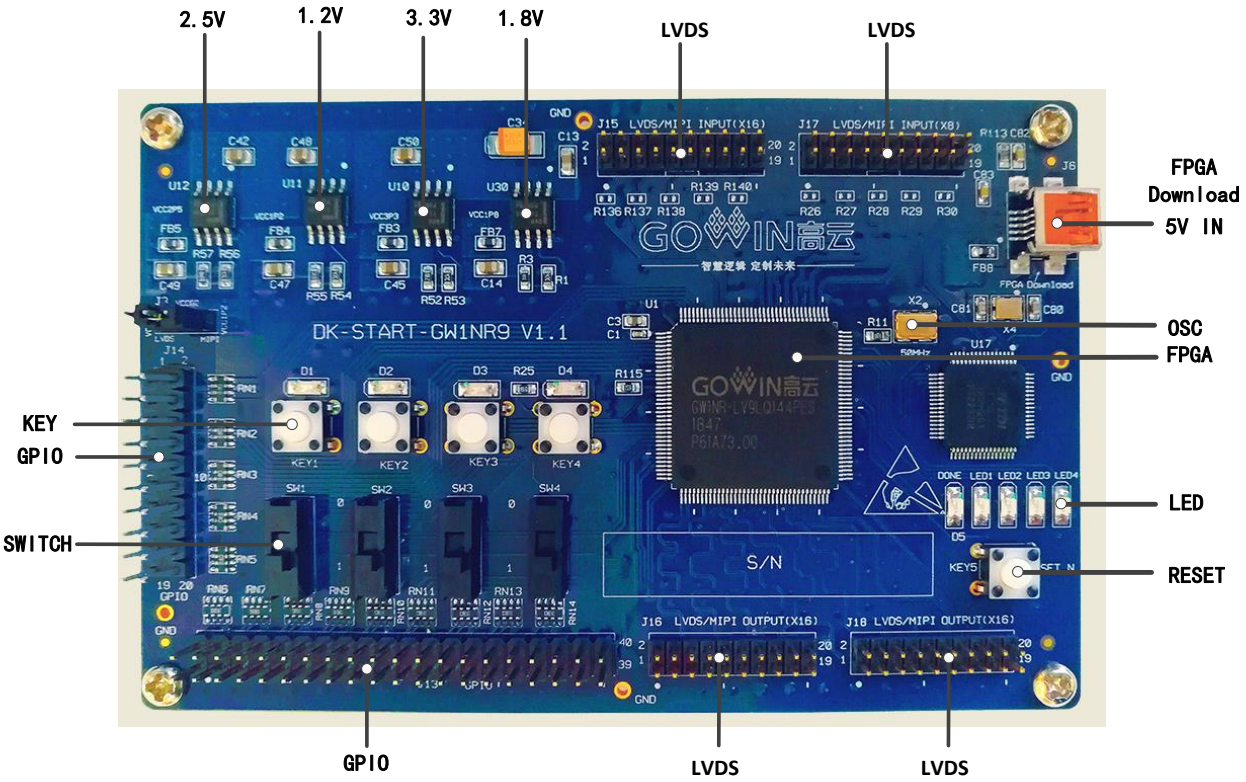
① DK-START-GW1NR9 V1.1 Development Board

② USB Cable

③ Quick Start Guide

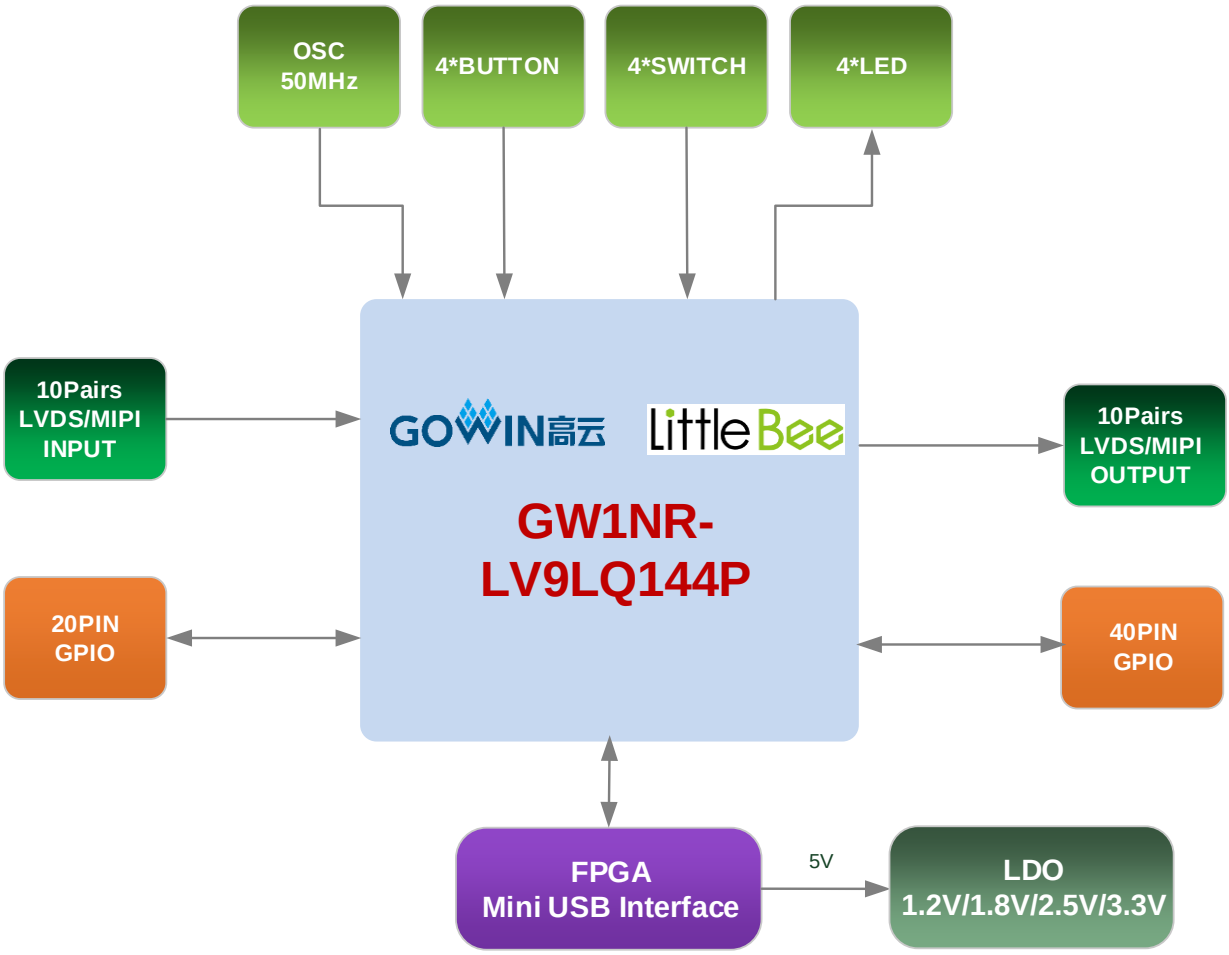
2.3 PCB Components

Figure2-3 PCB Components



2.4 System Diagram

Figure2-4 System Diagram



2.5 Feature

The structure and feature of the development board are as follows:

1. FPGA
   - LQFP144 package
   - Up to 120 user I/O
   - Embedded flash, data not easily lost if power down
   - Abundant LUT4 resources
   - Multiple modes and capacities of B-SRAM
2. FPGA Configuration Mode
   - JTAG
   - AUTO BOOT
3. Clock resource

   50MHz Clock Crystal Oscillator
4. Key switch and slide switch
   - One reset button
   - Four key switches
   - Four Slide switch
5. LED
   - One power indicator (green)
   - One DONE indicator (green)
   - Four LEDs (green)
6. Memory
   - 1Mbit embedded Flash
   - 64Mbit embedded PSRAM
7. MIPI/LVDS

   10 pairs of LVDS differential input; 10 pairs of MIPI/LVDS differential output
8. GPIO

   55 I/O extended resources
9. LDO Power

   3.3 V, 2.5V, 1.8V, and1.2V supported

2.6 Development Board Specification

Table 2-1 Development Board Specification

No.	Item	Functional Description	Technical Condition	Remarks
1	FPGA	Core chip	–	–
2	Download	Support an USB interface; Support JTAG, AUTOBOOT	USB to JTAG chip integrated on board	–
3	Power Supply	3.3 V, 2.5V and 1.2 V output via LDO circuit	● Input power: 5V ● Provide power for FPGA, download circuit and other circuits via 5V–3.3 V circuit; ● Provide power for FPGA via 5V to 2.5V circuit; ● Provide power for FPGA via 5 V–1.2 V circuit.	–
4	Slide Switches	Available for testing	4	–
5	Key Switches	Available for testing	4	–
6	Reset button	Reset for FPGA	1	–
7	LED	Test indicator, DONE indicator, Power indicator	● Four Test indicators, green ● One DONE indicator, green ● One Power indicator, green	–
8	Crystal Oscillator	Provide 50MHz clock for FPGA	Package5032	–
9	Memory	Provides abundant Flash and PSRAM for design	● 1Mbit embedded Flash ● 64Mbit embedded PSRAM	–
10	GPIO	I/O, convenient for user extension and test	36	–
11	MIPI/LVDS	MIPI/LVDS, used for testing	10 pairs of input, 10 pairs of output	–
12	Protection	USB interface: ESD protection; Power interface: Inverse current and over current protection	● USB interface ESD protection: ±15kV non-contact discharge, ± 8kV contact discharge; ● Schottky diode is connected between positive and negative anodes of power interface; ● 2A self-recovery fuses are connected at power inlet	–
13	Voltage	–	Input Voltage: 5V	–
14	Humidity	–	95%	–

No.	Item	Functional Description	Technical Condition	Remarks
15	Temperature	–	Operating range: –20°~70°	–

3 Development Board Circuit

3.1 FPGA Module

3.1.1 Overview

The resources of GW1NR series of FPGA products are shown in Table 3-1.

Table 3-1 GW1NR-9 FPGA Resources List

Device	GW1NR-9
LUT4	8,640
Flip-Flop (FF)	6,480
Shadow SRAM S-SRAM (bits)	17,280
Block Static Random Access Memory B-SRAM (bits)	468K
B-SRAM quantity B-SRAM	26
User Flash (bits)	608K
PSRAM(bits)	64M
18 x 18 Multiplier	20
PLLs+DLLs	2+4
Total number of I/O banks	4
Max. user I/O[1]	120
Core Voltage (LV)	1.2V

Note!

See DS117, *GW1NR series of FPGA Products Data Sheet* for further details.

3.1.2 I/O BANK Introduction

There are four I/O Banks in the GW1NR series of FPGA products, as shown in Figure 3-1.

Figure 3-1 GW1NR series FPGA Products I/O Bank Distribution

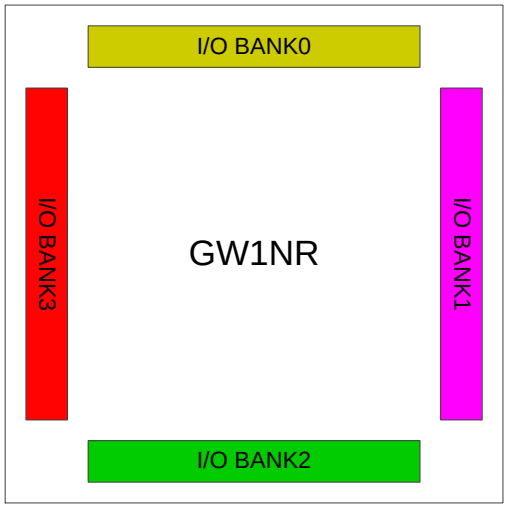


Figure3-2 GW1N-9 LQ144 Package Pins Distribution (Top View)

Table 3-2 FPGA I/O Pins Distribution

I/O BANK No.	Modules Connected
I/O BANK0	● Pins selection for download mode ● LVDS differential input ● GPIO
I/O BANK1	● GPIO ● 50MHz clock input ● LED ● Slide Switches ● Key Switches ● Reset
I/O BANK2	● MIPI/LVDS differential output ● GPIO
I/O BANK3	● GPIO Interface ● JTAG download

3.2 Download

3.2.1 Overview

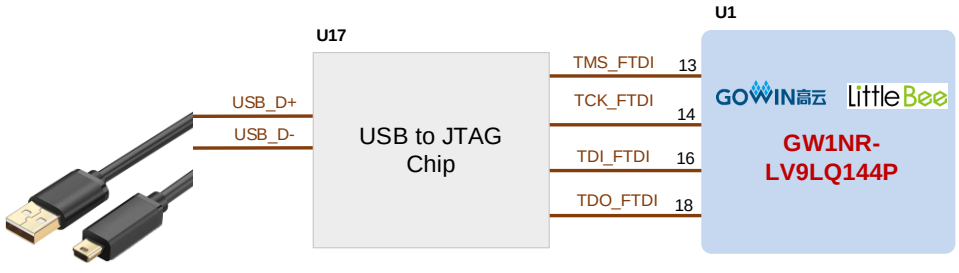
The development board provides an USB download interface. The data stream file can be downloaded to the internal SRAM, or internal flash as needed.

Note!

- When downloaded to SRAM, the data stream file will be lost if the device is powered down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the data stream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure3-3 Connection Diagram for FPGA USB Download



3.2.3 Download Flow

Please plug USB download cable into the USB interface (J6) of the development board to download FPGA, and then open Programmer, click SRAM mode or Embedded flash mode to download bit stream file to SRAM or flash.

3.2.4 Pins Distribution

Table 3-3 FPGA Download Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O Level
TMS_FTDI	13	3	JTAG Signal	1.8V

Signal Name	Pin No.	BANK	Description	I/O Level
TCK_ FTDI	14	3	JTAG Signal	1.8V
TDI_ FTDI	16	3	JTAG Signal	1.8V
TDO_ FTDI	18	3	JTAG Signal	1.8V
MODE0	144	0	Mode selection pin	2.5V
MODE1	143	0	Mode selection pin	2.5V
RECONFIG_N	20	3	RECONFIG_N	1.8V
DONE	21	3	One DONE indicator	1.8V
READY	22	3	READY	1.8V

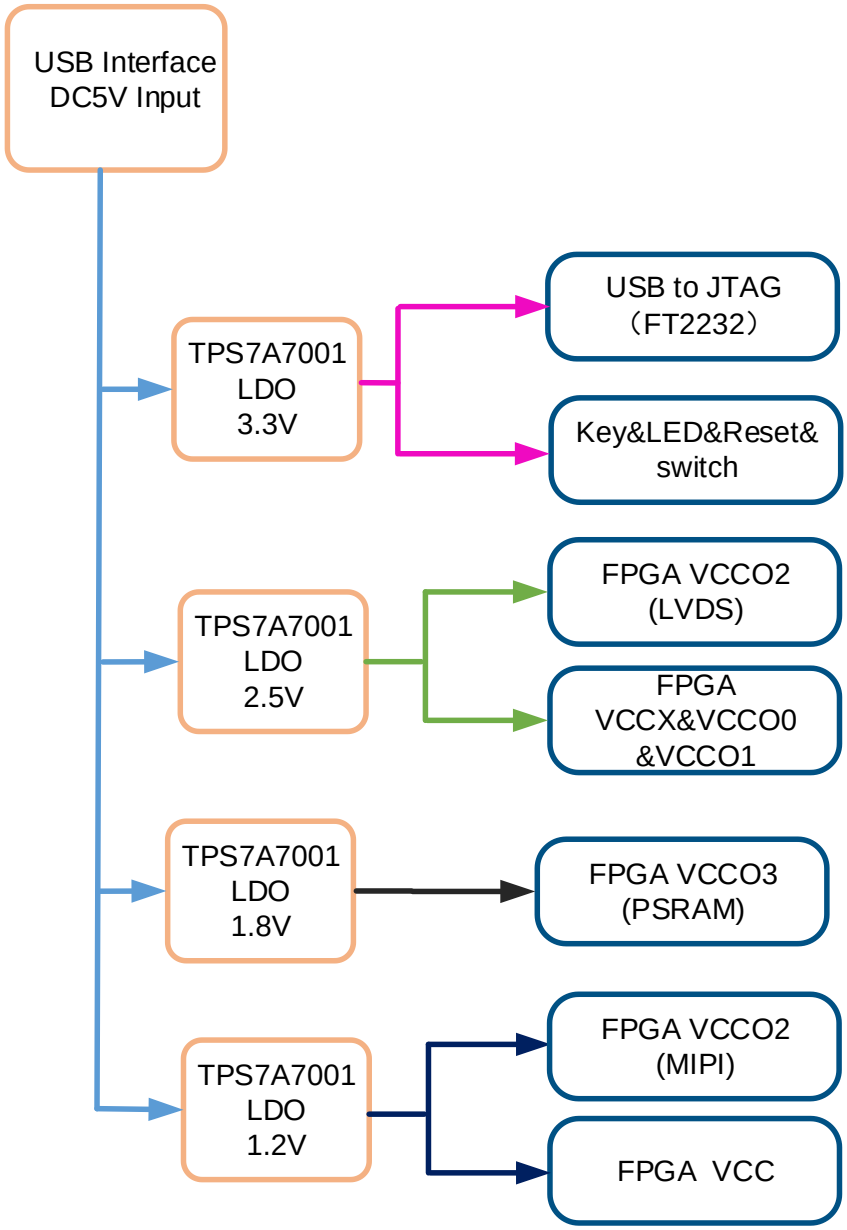
3.3 Power Supply

3.3.1 Overview

DC5V is input by USB interface. The TI LDO power supply chip is used to step down voltage from 5V to 3.3V, 2.5V, 1.8V and 1.2V, which can meet the power demand of the development board.

3.3.2 Power System Distribution

Figure3-4 Power System Distribution



3.3.3 Pins Distribution

Table 3-4 FPGA Power Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O Level
VCCO0	109, 127	0	I/O Bank Voltage	2.5V
VCCO1	91, 103	1	I/O Bank Voltage	2.5V

Signal Name	Pin No.	BANK	Description	I/O Level
VCCO2	37, 55	2	I/O Bank Voltage	2.5V/1.2V
VCCO3	9, 19	3	I/O Bank Voltage	1.8V
VCCX	31, 77	-	Auxiliary voltage	2.5V
VCC	1, 36, 73, 108	-	Core voltage	1.2V
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107	-	GND	-

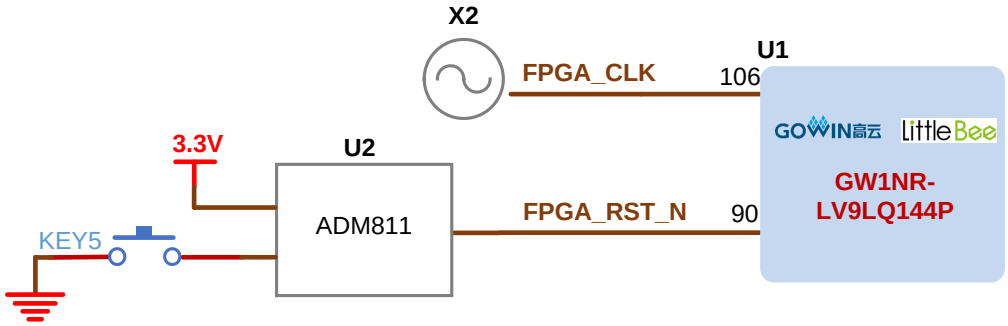
3.4 Clock, Reset

3.4.1 Overview

The development board provides a 50MHz crystal oscillator connected to the PLL input pin. This can be employed as the input clock for the PLL in FPGA. Frequency division and multiplication of PLL can output the clock required by the user.

3.4.2 Clock, Reset

Figure3-5 Clock, Reset



3.4.3 Pins Distribution

Table 3-5 FPGA Clock and Reset Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O Level
FPGA_CLK	106	1	50MHz Crystal Oscillator Input	2.5V
FPGA_RST_N	90	1	Reset Signal, Active Low	2.5V

3.5 LED

3.5.1 Overview

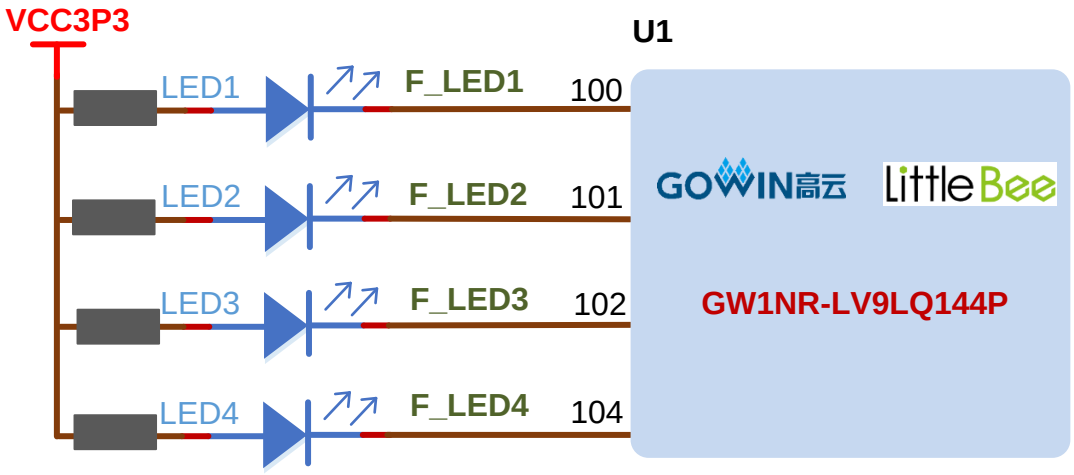
There are four green LEDs in the development board and users can display the required status through the LED. There are two LEDs left to facilitate the observation of power supply and FPGA loading status.

Users can test the LEDs in the following ways:

- When the FPGA corresponding pin output signal is logic low , the LED is lit;
- If the signal is high, LED is off.

3.5.2 LED Circuit

Figure3-6 LED Circuit



3.5.3 Pins Distribution

Table 3-6 LED Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O Level
F_LED1	100	1	LED1	2.5V
F_LED2	101	1	LED2	2.5V
F_LED3	102	1	LED3	2.5V
F_LED4	104	1	JESD 4	2.5V

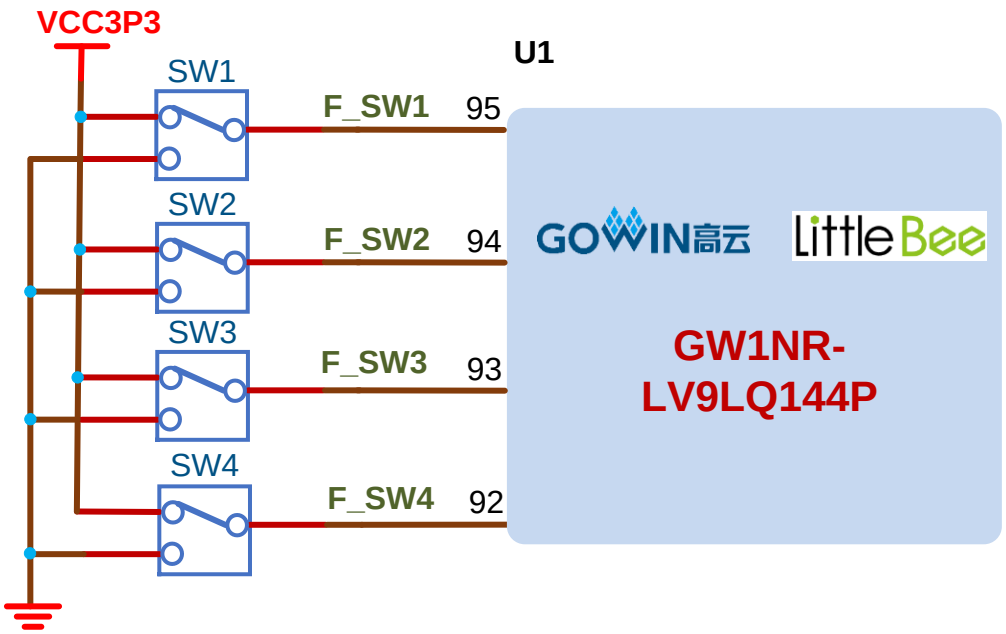
3.6 Switches

3.6.1 Overview

There are four slide switches in the development board to control input during testing.

3.6.2 Switch Circuit

Figure3-7 Switch Circuit



3.6.3 Pins Distribution

Table 3-7 Switch Circuit Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O Level
F_SW1	95	1	Slide Switch1	2.5V
F_SW2	94	1	Slide Switch2	2.5V
F_SW3	93	1	Slide Switch3	2.5V
F_SW4	92	1	Slide Switch2	2.5V

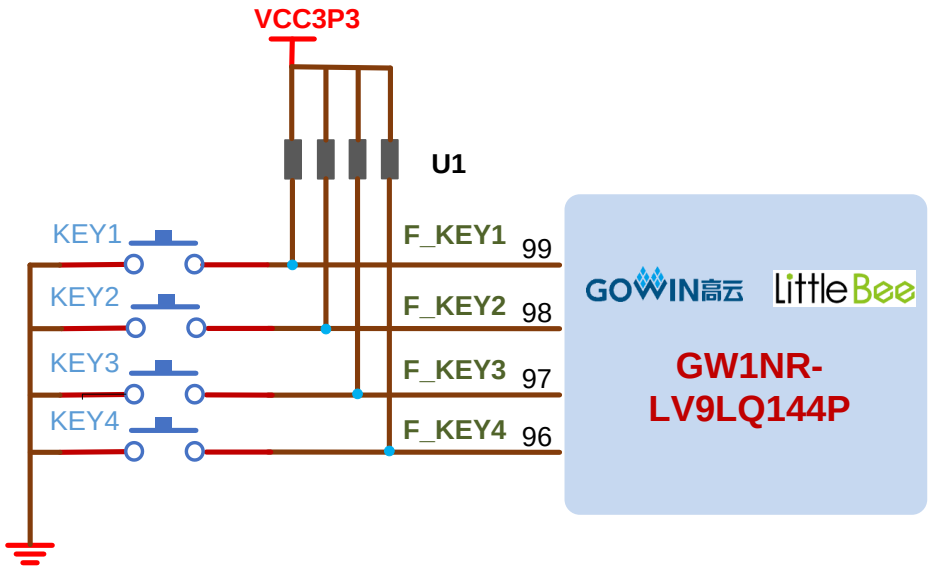
3.7 Key

3.7.1 Overview

There are four key switches in the development board. Users can manually input low level to the corresponding FPGA pins for testing purposes.

3.7.2 Key Circuit

Figure3-8 Key Circuit Diagram



3.7.3 Pins Distribution

Table 3-8 Key Circut Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O Level
F_KEY1	99	1	KEY1	2.5V
F_KEY2	98	1	KEY2	2.5V
F_KEY3	97	1	KEY3	2.5V
F_KEY4	96	1	KEY4	2.5V

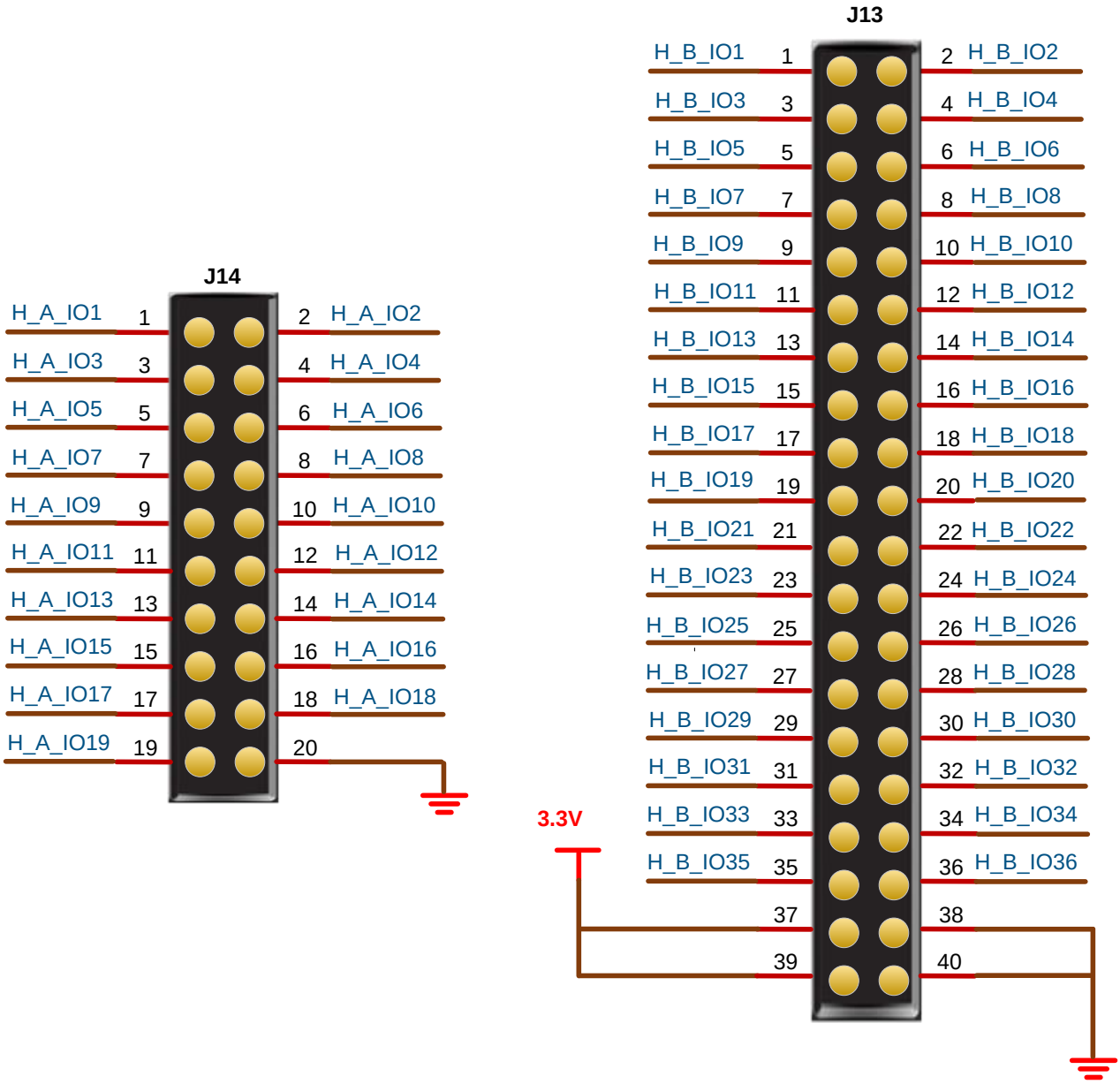
3.8 GPIO

3.8.1 Overview

One 2.54mm DC3-20P socket and one 2.54mm DC3-40P socket are reserved in the development board to facilitate the users to do the function expansion and testing.

3.8.2 GPIO Circuit

Figure3-9 GPIO Circuit



3.8.3 Pins Distribution

Table 3-9 J14 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
H_A_IO1	139	1	3	General I/O	1.8V
H_A_IO2	140	2	3	General I/O	1.8V
H_A_IO3	141	3	3	General I/O	1.8V
H_A_IO4	142	4	3	General I/O	1.8V
H_A_IO5	3	5	3	General I/O	1.8V
H_A_IO6	4	6	3	General I/O	1.8V
H_A_IO7	5	7	3	General I/O	1.8V
H_A_IO8	6	8	3	General I/O	1.8V
H_A_IO9	8	9	3	General I/O	1.8V
H_A_IO10	10	10	3	General I/O	1.8V
H_A_IO11	11	11	3	General I/O	1.8V
H_A_IO12	12	12	3	General I/O	1.8V
H_A_IO13	15	13	3	General I/O	1.8V
H_A_IO14	23	14	3	General I/O	1.8V
H_A_IO15	24	15	3	General I/O	1.8V
H_A_IO16	25	16	3	General I/O	1.8V
H_A_IO17	26	17	3	General I/O	1.8V
H_A_IO18	27	18	3	General I/O	1.8V
H_A_IO19	28	19	3	General I/O	1.8V
GND	-	20	-	GND	-

Table3-10 J13 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
H_B_IO1	132	1	0	General I/O	2.5V
H_B_IO2	131	2	0	General I/O	2.5V
H_B_IO3	130	3	0	General I/O	2.5V
H_B_IO4	129	4	0	General I/O	2.5V
H_B_IO5	128	5	0	General I/O	2.5V
H_B_IO6	126	6	0	General I/O	2.5V
H_B_IO7	88	7	1	General I/O	2.5V
H_B_IO8	87	8	1	General I/O	2.5V
H_B_IO9	86	9	1	General I/O	2.5V

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
H_B_IO10	85	10	1	General I/O	2.5V
H_B_IO11	84	11	1	General I/O	2.5V
H_B_IO12	83	12	1	General I/O	2.5V
H_B_IO13	82	13	1	General I/O	2.5V
H_B_IO14	81	14	1	General I/O	2.5V
H_B_IO15	80	15	1	General I/O	2.5V
H_B_IO16	79	16	1	General I/O	2.5V
H_B_IO17	68	17	2	General I/O	VCCO2
H_B_IO18	69	18	2	General I/O	VCCO2
H_B_IO19	76	19	2	General I/O	VCCO2
H_B_IO20	78	20	2	General I/O	VCCO2
H_B_IO21	44	21	2	General I/O	VCCO2
H_B_IO22	45	22	2	General I/O	VCCO2
H_B_IO23	48	23	2	General I/O	VCCO2
H_B_IO24	49	24	2	General I/O	VCCO2
H_B_IO25	65	25	2	General I/O	VCCO2
H_B_IO26	64	26	2	General I/O	VCCO2
H_B_IO27	61	27	2	General I/O	VCCO2
H_B_IO28	60	28	2	General I/O	VCCO2
H_B_IO29	57	29	2	General I/O	VCCO2
H_B_IO30	56	30	2	General I/O	VCCO2
H_B_IO31	54	31	2	General I/O	VCCO2
H_B_IO32	52	32	2	General I/O	VCCO2
H_B_IO33	32	33	2	General I/O	VCCO2
H_B_IO34	34	34	2	General I/O	VCCO2
H_B_IO35	40	35	2	General I/O	VCCO2
H_B_IO36	41	36	2	General I/O	VCCO2
VCC3P3	-	37	-	3.3V	-
GND	-	38	-	GND	-
VCC3P3	-	39	-	3.3V	-
GND	-	40	-	GND	-

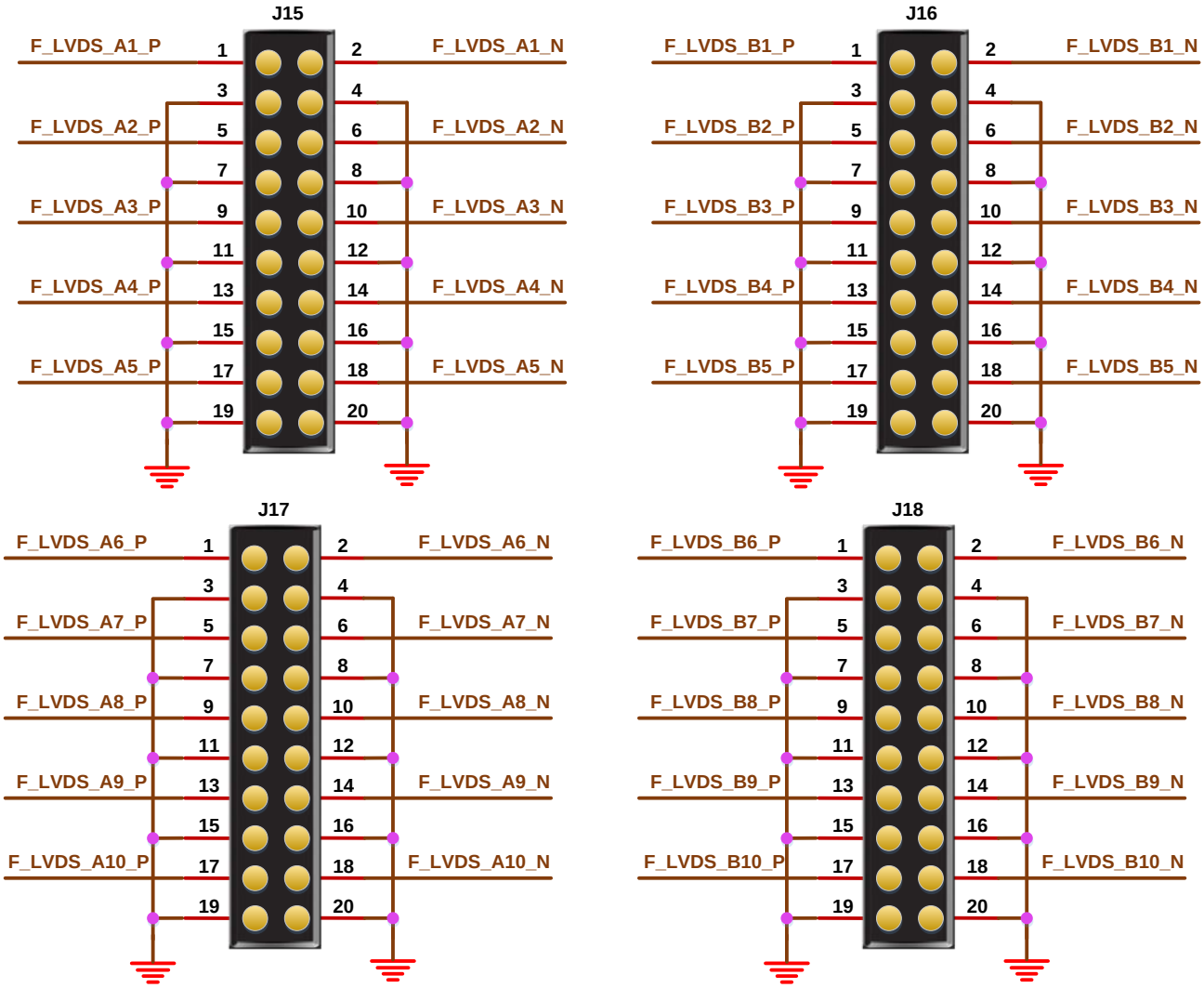
3.9 MIPI/LVDS

3.9.1 Overview

Two 2 mm DC3-20P sockets are reserved in the development board for MIPI/LVDS input/output performance testing and high-speed data transmission. Up to 10 pairs of differential input and 10 pairs of differential output can be satisfied.

3.9.2 MIPI/LVDS Circuit

Figure3-10 LVDS Circuit



3.9.3 Pins Distribution

Table 3-11 J15 FPGA Pin Distribution (IDES16:1 Supported)

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
F_LVDS_A1_P	136	1	0	Differential input channel 1+	2.5V(LVDS)
F_LVDS_A1_N	135	2	0	Differential input channel 1-	2.5V(LVDS)
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_A2_P	134	5	0	Differential input channel 2+	2.5V(LVDS)
F_LVDS_A2_N	133	6	0	Differential input channel 2-	2.5V(LVDS)
GND	-	7	-	-	-
GND	-	8	-	-	-
F_LVDS_A3_P	125	9	0	Differential input channel 3+	2.5V(LVDS)
F_LVDS_A3_N	124	10	0	Differential input channel 3-	2.5V(LVDS)
GND	-	11	-	-	-
GND	-	12	-	-	-
F_LVDS_A4_P	123	13	0	Differential input channel 4+	2.5V(LVDS)
F_LVDS_A4_N	122	14	0	Differential input channel 4-	2.5V(LVDS)
GND	-	15	-	-	-
GND	-	16	-	-	-
F_LVDS_A5_P	115	17	1	Differential input channel 5+	2.5V(LVDS)
F_LVDS_A5_N	114	18	1	Differential input channel 5-	2.5V(LVDS)
GND	-	19	-	-	-
GND	-	20	-	-	-

Table 3-12 J17 FPGA Pin Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
F_LVDS_A6_P	121	1	0	Differential input channel 6+	2.5V(LVDS)
F_LVDS_A6_N	120	2	0	Differential input	2.5V(LVDS)

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
				channel 6-	
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_A7_P	119	5	0	Differential input channel 7+	2.5V(LVDS)
F_LVDS_A7_N	118	6	0	Differential input channel 7-	2.5V(LVDS)
GND	-	7	-	-	-
GND	-	8	-	-	-
F_LVDS_A8_P	117	9	1	Differential input channel 8+	2.5V(LVDS)
F_LVDS_A8_N	116	10	1	Differential input channel 8-	2.5V(LVDS)
GND	-	11	-	-	-
GND	-	12	-	-	-
F_LVDS_A9_P	113	13	1	Differential input channel 9+	2.5V(LVDS)
F_LVDS_A9_N	112	14	1	Differential input channel 9-	2.5V(LVDS)
GND	-	15	-	-	-
GND	-	16	-	-	-
F_LVDS_A10_P	111	17	1	Differential input channel 10+	2.5V(LVDS)
F_LVDS_A10_N	110	18	1	Differential input channel 10-	2.5V(LVDS)
GND	-	19	-	-	-
GND	-	20	-	-	-

Table 3-13 J16 FPGA Pin Distribution (IDES16:1 Supported)

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
F_LVDS_B1_P	29	1	2	Differential output channel 1+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B1_N	30	2	2	Differential output channel 1-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_B2_P	38	5	2	Differential output channel 2+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B2_N	39	6	2	Differential output channel 2-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	7	-	-	
GND	-	8	-	-	
F_LVDS_B3_P	42	9	2	Differential output channel 3+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B3_N	43	10	2	Differential output channel 3-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	11	-	-	
GND	-	12	-	-	
F_LVDS_B4_P	46	13	2	Differential output channel 4+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B4_N	47	14	2	Differential output channel 4-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	15	-	-	
GND	-	16	-	-	
F_LVDS_B5_P	50	17	2	Differential output channel 5+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B5_N	51	18	2	Differential output channel 5-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	19	-	-	

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
GND	-	20	-	-	

Table 3-14 J18 FPGA Pin Distribution (IDES16:1 Supported)

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
F_LVDS_B6_P	58	1	2	Differential output channel 6+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B6_N	59	2	2	Differential output channel 6-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_B7_P	62	5	2	Differential output channel 7+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B7_N	63	6	2	Differential output channel 7-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	7	-	-	
GND	-	8	-	-	
F_LVDS_B8_P	66	9	2	Differential output channel 8+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B8_N	67	10	2	Differential output channel 8-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	11	-	-	
GND	-	12	-	-	
F_LVDS_B9_P	70	13	2	Differential output channel 9+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B9_N	71	14	2	Differential output channel 9-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	15	-	-	
GND	-	16	-	-	
F_LVDS_B10_P	72	17	2	Differential output channel 10+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B10_N	75	18	2	Differential output channel 10-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	19	-	-	
GND	-	20	-	-	

4 Precautions

Attentions in use of the development board:

1. Handle with care and pay attention to electrostatic protection;
2. VCCO2 Bank voltage needs to be set as 2.5V when the Bank2 output differential pairs serve as LVDS output; VCCO2 Bank voltage needs to be set as 1.2V when the Bank2 output differential pairs serve as MIPI output.
3. DK-START-GWS1NR9 V1.1 does not support MIPI input.

5 Gowin YunYuan Software

Please refer to SUG100, *Gowin Software User Guide* for details.