DK-START-GW1NS2 V2.1

User Manual

DBUG358-1.4E, 12/19/2019

Disclaimer

Revision History

Date	Version	Description
12/18/2018	1.0E	Initial version published.
04/22/2019	1.1E	● Data stream download updated; ● Precautions updated.
08/22/2019	1.2E	One precaution for DK-START-GW1NS2 V2.1 added.
08/30/2019	1.3E	The new device of GW1NSE-2C added.
12/19/2019	1.4E	The version of DK-START-GW1NS2 added.

Contents

Contents i

List of Figures iv

List of Tables v

1 About This Guide 1

1.1 Purpose 1

1.2 Supported Products 1

1.3 Related Documents 1

1.4 Abbreviations and Terminology 2

1.5 Support and Feedback 3

2 Development Board Description 4

2.1 Overview 4

2.2 A Development Board Suite 5

2.3 PCB Components 6

2.4 System Architecture 7

2.5 Features 8

2.6 Development Board Specification 9

3 Development Board Circuit 11

3.1 FPGA Module 11

3.1.1 Overview 11

3.1.2 I/O BANK Introduction 12

3.2 Download 14

3.2.1 Overview 14

3.2.2 USB Download Circuit 14

3.2.3 Downloading the Data Stream 14

3.2.4 Pins Distribution 15

3.3 Power Supply 16

3.3.1 Overview 16

3.3.2 Power System Distribution 16
3.3.3 Pins Distribution 17
3.4 Clock, Reset 17
3.4.1 Overview 17
3.4.2 Clock, Reset 17
3.4.3 Pins Distribution 18
3.5 LED 19
3.5.1 Overview 19
3.5.2 LED Circuit 19
3.5.3 Pins Distribution 19
3.6 Seven-segment digital tubes 20
3.6.1 Overview 20
3.6.2 Seven-segment Digital Tube Circuit 20
3.6.3 Pins Distribution 21
3.7 Switches 22
3.7.1 Overview 22
3.7.2 Switch Circuit 22
3.7.3 Pins Distribution 22
3.8 Key 22
3.8.1 Overview 22
3.8.2 Key Circuit 23
3.8.3 Pins Distribution 23
3.9 GPIO 24
3.9.1 Overview 24
3.9.2 GPIO Circuit 24
3.9.3 Pins Distribution 24
3.10 MIPI/LVDS 26
3.10.1 Overview 26
3.10.2 MIPI/LVDS Circuit 27
3.10.3 Pins Distribution 28
3.11 ADC 30
3.11.1 Overview 30
3.11.2 ADC Circuit 30
3.11.3 Pins Distribution 30
3.12 RS232 31

3.12.1 Overview 31
3.12.2 RS232 Circuit 31
3.12.3 Pins Distribution 31
4 Precautions 32
5 Gowin YunYuan Software 33

List of Figures

Figure 2-1 DK-START-GW1NS2 V2.1 4
Figure 2-2A Development Board Suite 5
Figure 2-3 PCB Components 6
Figure 2-4 System Architecture 7
Figure 3-1 GW1NS I/O Bank Distribution 12
Figure 3-2 View of GW1NS-2/GW1NS-2C LQ144 Pins Distribution (Top View) 12
Figure 3-3 Connection Diagram for FPGA USB Downloading 14
Figure 3-4 Power System Distribution 16
Figure 3-5 Clock, Reset 17
Figure 3-6 LED Circuit 19
Figure 3-7 Seven-segment Digital Tube Circuit 20
Figure 3-8 Switch Circuit 22
Figure 3-9 Key Circuit Diagram 23
Figure3-10 GPIO Circuit 24
Figure 3-11 LVDS Circuit 27
Figure 3-12 ADC Circuit 30
Figure 3-13 RS232 Download Connection 31

List of Tables

Table 1-1 Abbreviations and Terminology 2
Table 2-1 Development Board Specification 9
Table 3-1 GW1NS-2/GW1NS-2C FPGA Resources List 11
Figure 3-2 FPGA I/O Pins Distribution 13
Table 3-3 FPGA Download and Pins Distribution 15
Table 3-4 FPGA Download and Pins Distribution 17
Table 3-5 FPGA Clock and Reset Pins Distribution 18
Table 3-6 LED Pins Distribution 19
Table 3-7 LED Pins Distribution 21
Table 3-8 Switch Circuit Pins Distribution 22
Table 3-9 Key Pins Distribution 23
Table 3-10 J14 GPIO Pins Distribution 24
Table3-11 J17 GPIO Pins Distribution 26
Table 3-12 J15 FPGA Pin Distribution 28
Table 3-13 J16 FPGA Pin Distribution 29
Table 3-14 J1 ADC Pins Distribution 30
Table 3-15 RS232 Pins Distribution 31

1 About This Guide

1.1 Purpose

The DK-START-GW1NS2 V2.1 user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the hardware circuits functions, circuit, and pins distribution;
3. Precautions to be taken when using the development board;
4. Introduction to the use of the FPGA development software.

1.2 Supported Products

The information in the guide applies to GW1NS series of FPGA products: GW1NS-2, GW1NS-2C, GW1NSE-2C.

1.3 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1NS series of FPGA Products Datasheet
2. GW1NSE series of SecureFPGA Products Datasheet
3. GW1NS series of FPGA Products Package and Pinout
4. GW1NSE series of SecureFPGA Products Package and Pinout
5. GW1NS-2&2C Pinout
6. GW1NSE-2C Pinout
7. Gowin FPGA Products Programming and Configuration User Guide
8. Gowin YunYuan Software User Guide

1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
SoC	System On Chip
ARM	Advanced RISC Machines
AHB	Advanced High performance Bus
APB	Advanced Peripheral Bus
Timer	Timer
RS232	Universal Asynchronous Receiver/Transmitter
NVIC	Nested Vector Interrupt Controller
DAP	Debug Access Port
Watchdog	Watchdog
TimeStamp	TimeStamp
DWT	Data Watchpoint Trace
ITM	Instrumentation Trace Module
TUIP	Trace Port Interface Unit
USB	Universal Serial Bus
PHY	Physical Layer
ADC	Analog to Digital Converter
SAR	Successive Approximation Register
SFDR	Spurious-free Dynamic Range
SINAD	Signal to Noise And Distortion
LSB	Least Significant Bit
INL	Integral Nonlinearity
DNL	Differential Nonlinearity
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register

Abbreviations and Terminology	Full Name
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
LQ144	LQFP144

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

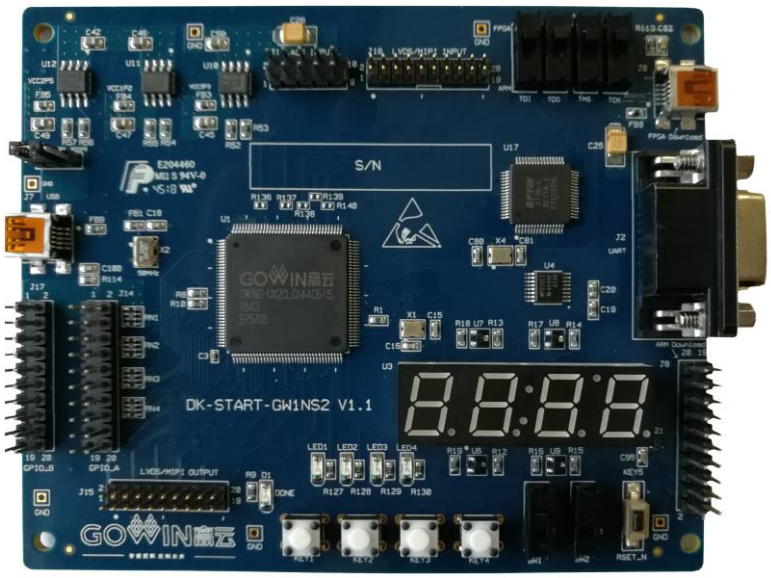
+Tel: +86 755 8262 0391

2 Development Board Description

Taking GW1NS-2C for example, this chapter introduces the function, features, and components of DK-START-GW1NS2 V2.1. GW1NS-2/GW1NSE-2C pins are compatible with GW1NS-2C pins. Compared with GW1NS-2C, GW1NS-2 has no built-in Cortex-M3 processor and GW1NSE-2C offers the new feature of one time programming and authentication code.

2.1 Overview

Figure 2-1 DK-START-GW1NS2 V2.1



The development board adopts the GW1NS-2 SoC FPGA. SoC FPFA is embedded with an ARM Cortex-M3 hard core processor, USB2.0 PHY, 32Mbit PSRAM, 1Mbit User Flash and eight-channel ADC converter, etc. When the ARM Cortex-M3 hard-core processor is employed as the core, the needs of the Min. memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions,

which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits.

The development board offers abundant external interfaces, including MIPI/LVDS interfaces, GPIO interfaces, ADC interfaces, USB TYPE-C interfaces, slide switches, key switches, LED, Seven-segment digital tube, etc.

2.2 A Development Board Suite

A development board suite includes the following items:

- DK-START-GW1NS2 V2.1
- USB cable
- Quick Start

Figure 2-2 A Development Board Suite

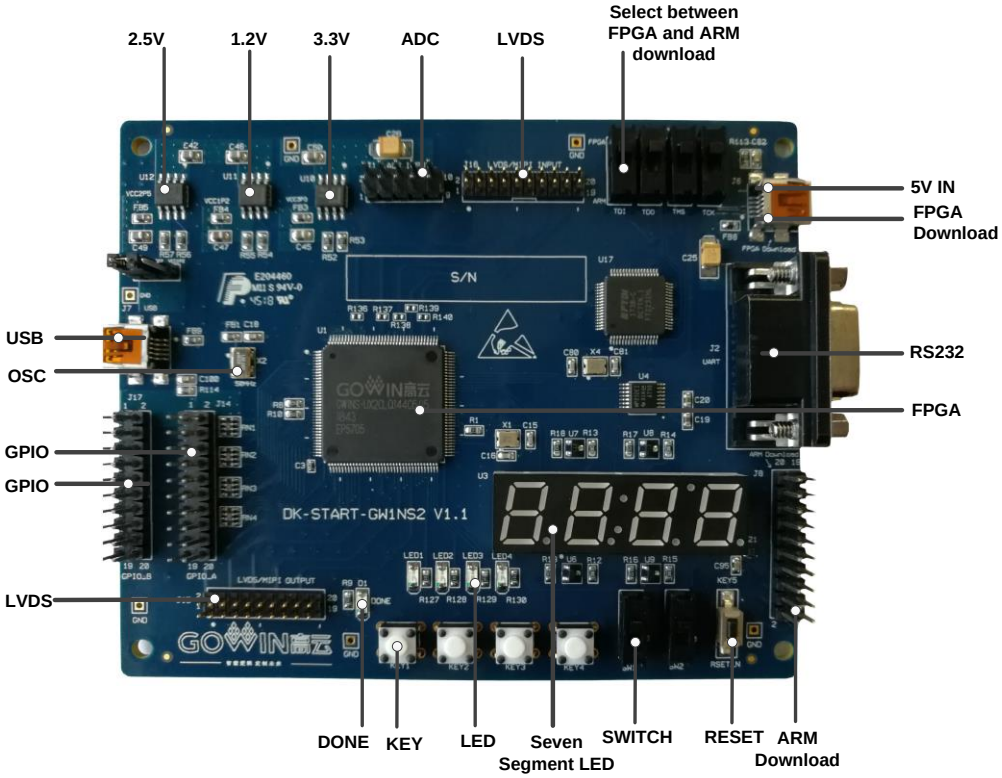
① DK-START-GW1NS2 V2.1

② USB Cable

③ Quick Start Guide

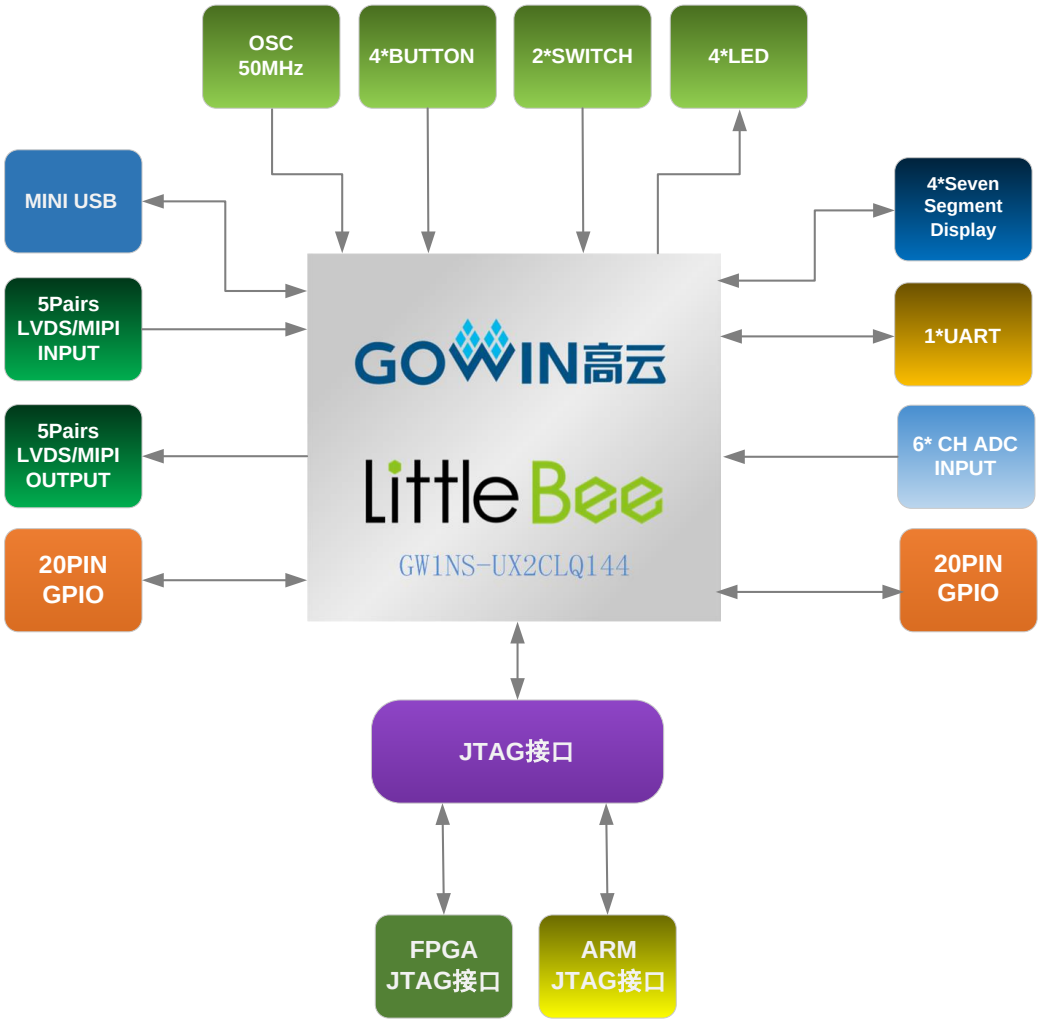
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Architecture

Figure 2-4 System Architecture



2.5 Features

The structure and features of the development board are as follows:

1. FPGA
   - LQFP144 package
   - Up to 95 user I/O
   - Embedded flash, data not easily lost if power down
   - Abundant LUT4 resources
   - Multiple modes and capacities of B-SRAM
2. FPGA Configuration Mode
   - JTAG
   - AUTO BOOT
3. Clock resource

   50MHz Clock Crystal Oscillator
4. Key switch and slide switch
   - One reset button
   - Four key switches
   - Two slide switches
5. LED
   - One power indicator (green)
   - One DONE indicator (green)
   - Four LEDs (green)
   - 4 seven-segment digital tubes
6. Memory

   1Mbit built-in Flash
7. MIPI/LVDS

   5 pairs of MIPI/LVDS differential input; 5 pairs of MIPI/LVDS differential output
8. GPIO

   36 I/O expansion resources
9. RS232

   1 RS232
10. LDO Power

    Supports 3.3 V, 2.5 V, and1.2V

2.6 Development Board Specification

Table 2-1 Development Board Specification

No.	Item	Functions	Technical Conditions	Remarks
1	FPGA	Core chip	–	–
2	Download	Support an USB interface; Support JTAG, AUTOBOOT	USB-JTAG module on board	–
3	Power Supply	3.3 V, 2.5V and 1.2 V output via LDO circuit	● Provide DC 5V input; ● Provide power for FPGA, download circuit and other circuits via 5V–3.3 V circuit; ● Provide power for FPGA via 5V–2.5V circuit; ● Provide power to FPGA core via 5 V–1.2 V circuit.	–
4	Slide Switches	Available for testing	2	–
5	Key Switches	Available for testing	4	–
6	Reset button	Reset for FPGA	1	–
7	LED	Test indicator, DONE indicator, Power indicator	● Four Test indicators, green ● One DONE indicator, green ● One Power indicator, green	–
8	Seven-segment digital tube	Functional test output display	Seven-segment digital tubes	–
9	Crystal Oscillator	Provide 50MHz clock for FPGA	Package5032	–
10	Memory	Provides abundant Flash for designs	1Mbit built-in Flash	–
11	GPIO	I/O, convenient for user extension and test	36	–
12	MIPI/LVDS	MIPI/LVDS, used for testing	5 pairs of input, 5 pairs of output	–
13	RS232	Used for testing	1 RS232	–
14	Protection	USB interface: ESD protection; Power interface: Inverse current and over current protection	● USB interface ESD protection: ±15kV non-contact discharge, ± 8kV contact discharge; ● Schottky diode is connected between positive and negative anodes of power outlet; ● 2A self-recovery fuses are connected at power inlet	–
15	Voltage	–	Input Voltage: 5V	–

No.	Item	Functions	Technical Conditions	Remarks
16	Humidity	–	95%	–
17	Temperature	–	Operating range: –20°~70°	–

3 Development Board Circuit

3.1 FPGA Module

3.1.1 Overview

The resources of GW1NS/GW1NSE series of FPGA products are listed in Table 3-1.

Table 3-1 GW1NS-2/GW1NS-2C FPGA Resources List

Device	GW1NS-2	GW1NS-2C	GW1NSE-2C
LUT4	1,728	1,728	1,728
Flip-Flop (FF)	1,296	1,296	1,296
Block SRAM B-SRAM (bits)	72K	72K	72K
B-SRAM quantity B-SRAM	4	4	4
S-SRAM (bits)	-	-	4608
User Flash (bits)	1M	1M	1024
PLLs+DLLs	1+2	1+2	1+2
OSC	1, ±5% accuracy	1, ±5% accuracy	1, ±5% accuracy
Hard core processor	-	1，Cortex-M3	1，Cortex-M3
USB PHY	1，USB 2.0 PHY	1，USB 2.0 PHY	1，USB 2.0 PHY
ADC[1]	1	1	1
Total number of I/O banks	4	4	4
Max. user I/O[1]	95	95	95
Core voltage	1.2V	1.2V	1.2V

Note!

- See *GW1NS series of FPGA Products Data Sheet* for further details;
- See *GW1NSE series of SecureFPGA Products Data Sheet* for further details;.

3.1.2 I/O BANK Introduction

There are four I/O Banks in the GW1NS series of FPGA products, as shown in Figure 3-1.

Figure 3-1 GW1NS I/O Bank Distribution

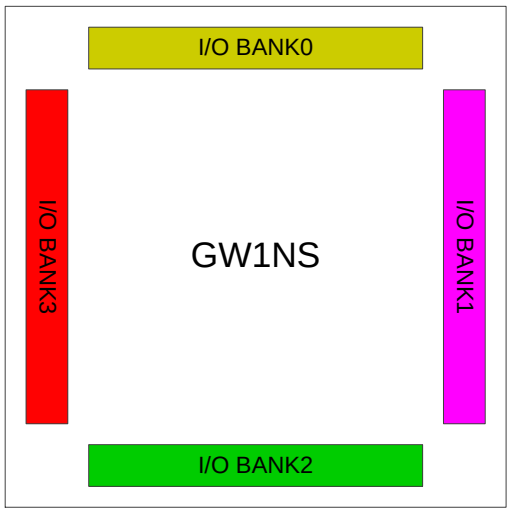


Figure 3-2 View of GW1NS-2/GW1NS-2C LQ144 Pins Distribution (Top View)

Figure 3-2 FPGA I/O Pins Distribution

I/O BANK No.	Modules Connected
I/O BANK0	● Pins used for download mode selection ● MIPI/LVDS differential input ● ADC input ● GPIO
I/O BANK1	● GPIO ● RS232 ● Seven-segment digital tubes ● USB interface
I/O BANK2	● Slide Switches ● Key Switches ● MIPI/LVDS differential output ● LED ● GPIO
I/O BANK3	● GPIO Interface ● JTAG download ● 50MHz clock input ● Reset

3.2 Download

3.2.1 Overview

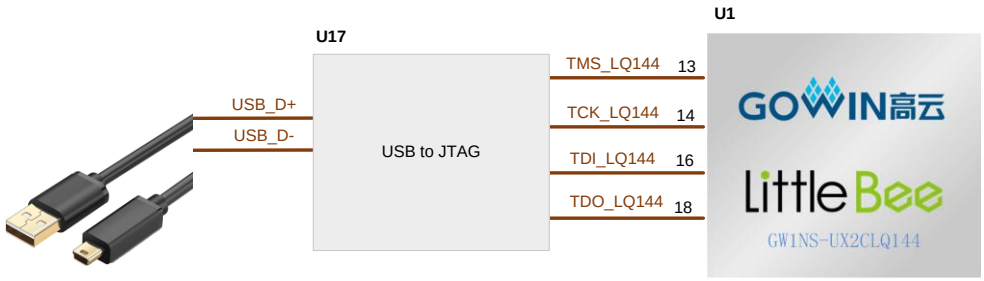
The development board provides an USB download interface. The data stream file can be downloaded to the internal SRAM, or internal flash as needed.

Note!

- When downloaded to SRAM, the data stream file will be lost if the device is power down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the data stream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure 3-3 Connection Diagram for FPGA USB Downloading



3.2.3 Downloading the Data Stream

1. FPGA and MCU download mode:
   Plug the USB cable to the development board USB interface (J6).

   Note!

   Before downloading, switch the SW3, SW4, SW5, and SW6 on the development board to the FPGA Download side.
2. MCU Debugging mode:
   Connect the J-Link ARM emulator to the ARM JTAG interface (J8).

   Note!

   Before debugging, switch the SW3, SW4, SW5, and SW6 on the development board to the ARM Download side.

3.2.4 Pins Distribution

Table 3-3 FPGA Download and Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
TMS_LQ144	13	3	JTAG Signal	3.3V
TCK_LQ144	14	3	JTAG Signal	3.3V
TDI_LQ144	16	3	JTAG Signal	3.3V
TDO_LQ144	18	3	JTAG Signal	3.3V
MODE0	143	0	One Mode selection pin	3.3V
MODE1	141	0	One Mode selection pin	3.3V
MODE2	142	0	One Mode selection pin	3.3V
RECONFIG_N	20	3	RECONFIG_N	3.3V
DONE	21	3	One DONE indicator	3.3V
READY	22	3	READY	3.3V

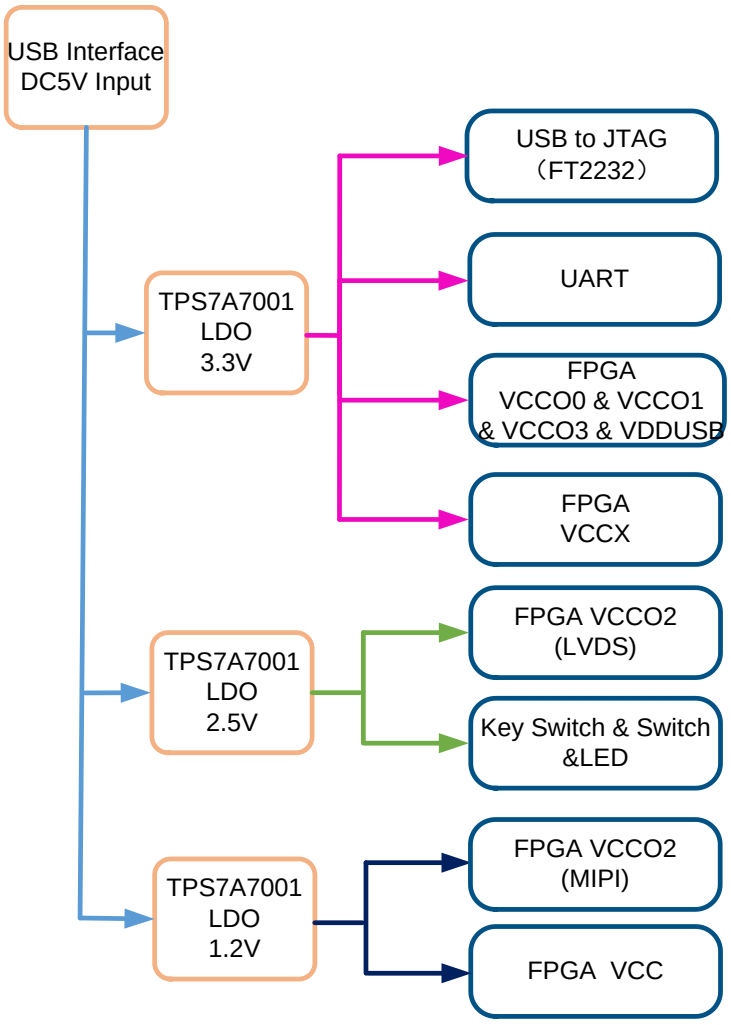
3.3 Power Supply

3.3.1 Overview

DC5V is input by USB interface. The TI LDO power supply chip is used to step down voltage from 5V to 3.3V, 1.8V, and 1.2V, which can meet the power demand of the development board.

3.3.2 Power System Distribution

Figure 3-4 Power System Distribution



3.3.3 Pins Distribution

Table 3-4 FPGA Download and Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
VCCO0	109, 127, 144	0	I/O Bank Power	3.3V
VCCO1	91	1	I/O Bank Power	3.3V
VCCO2	37, 55	2	I/O Bank Power	2.5V/1.2V
VCCO3	5, 26	3	I/O Bank Power	3.3V
VCCX	31, 78, 103	-	Auxiliary voltage	3.3V
VCC	1, 36, 73, 108	-	Core voltage	1.2V
VDDUSB	85	-	USB PHY power	3.3V
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107, 125	-	GND	-

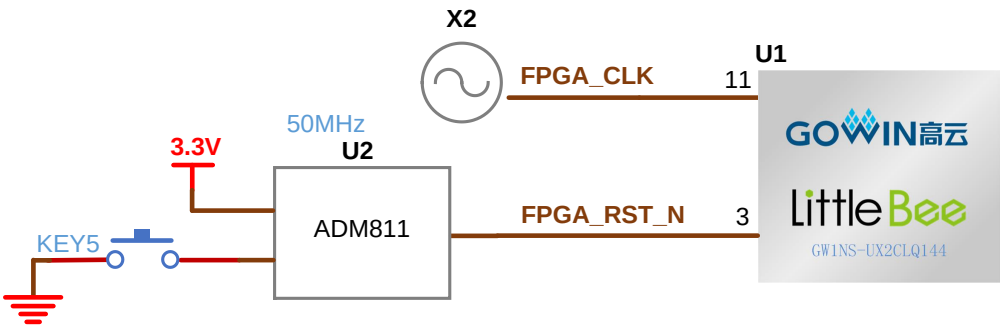
3.4 Clock, Reset

3.4.1 Overview

A 50MHz crystal oscillator is provided in the development board that connects to the PLL input pin. This can be employed as the input clock for the PLL in FPGA, and the output clock as needed via multiplication and division of the PLL frequency.

3.4.2 Clock, Reset

Figure 3-5 Clock, Reset



3.4.3 Pins Distribution

Table 3-5 FPGA Clock and Reset Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
FPGA_CLK	11	3	50MHz crystal oscillator Input	3.3V
FPGA_RST_N	3	1	Reset signal, active low	3.3V

3.5 LED

3.5.1 Overview

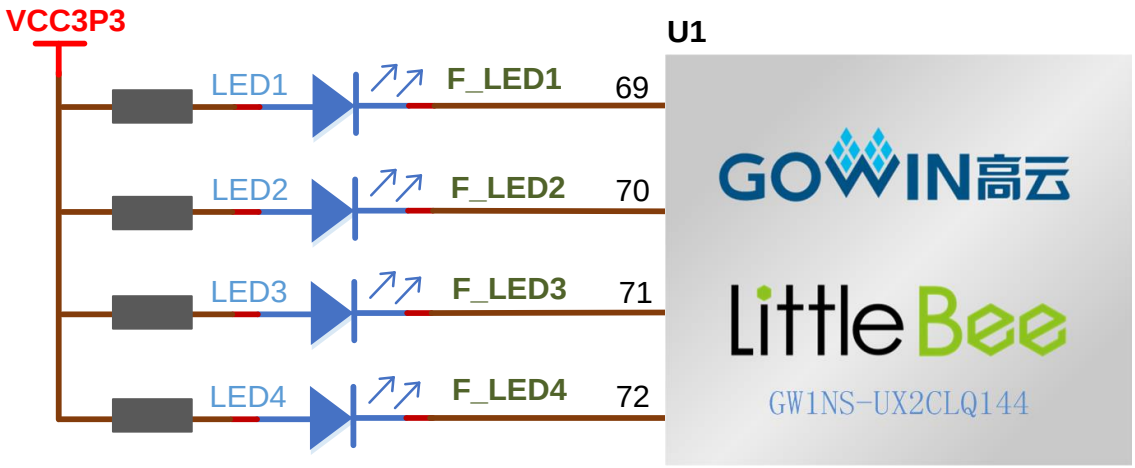
Four green LEDs are incorporated into the development board and are used to display the required status. In addition, two LEDs are reserved to signify power supply and FPGA loading status.

Users can test the LEDs in the following ways:

- If the output signal of related pins is logic low, LED is on;
- If logic is high, LED is off.

3.5.2 LED Circuit

Figure 3-6 LED Circuit



3.5.3 Pins Distribution

Table 3-6 LED Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_LED1	69	2	LED1	3.3V
F_LED2	70	2	LED2	3.3V
F_LED3	71	2	LED3	3.3V
F_LED4	72	2	JESD 4	3.3V

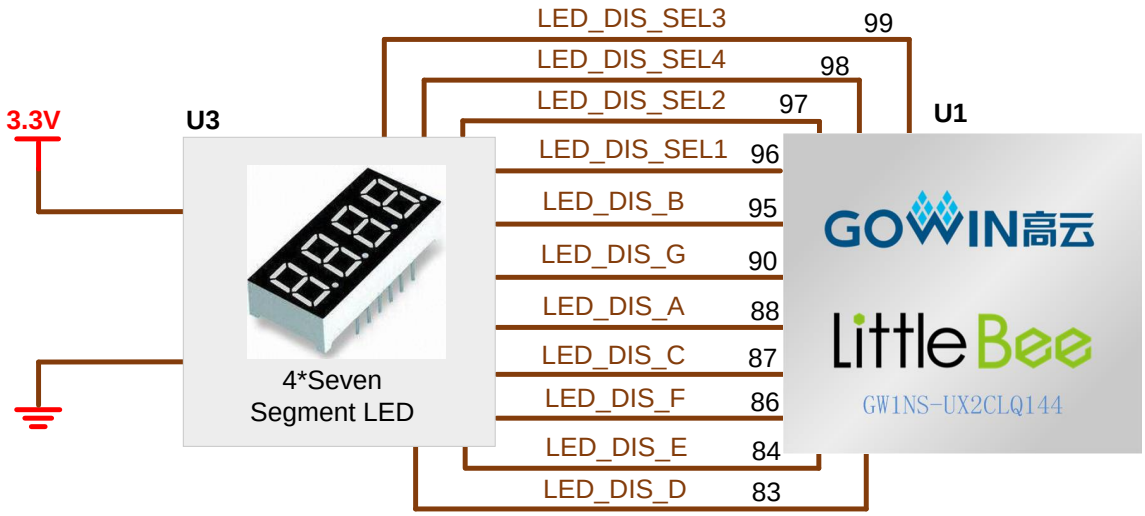
3.6 Seven-segment digital tubes

3.6.1 Overview

One seven-segment digital tube is incorporated into the development board and is used for the board's read/write test and displaying the related information on the LCD.

3.6.2 Seven-segment Digital Tube Circuit

Figure 3-7 Seven-segment Digital Tube Circuit



3.6.3 Pins Distribution

Table 3-7 LED Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
LED_DIS_SEL1	96	1	Digital tube selection signal	3.3V
LED_DIS_SEL2	97	1	Digital tube selection signal	3.3V
LED_DIS_SEL3	99	1	Digital tube selection signal	3.3V
LED_DIS_SEL4	98	1	Digital tube selection signal	3.3V
LED_DIS_A	88	1	Digital tube A signal	3.3V
LED_DIS_B	95	1	Digital tube B signal	3.3V
LED_DIS_C	87	1	Digital tube C signal	3.3V
LED_DIS_D	83	1	Digital tube D signal	3.3V
LED_DIS_E	84	1	Digital tube E signal	3.3V
LED_DIS_F	86	1	Digital tube F signal	3.3V
LED_DIS_G	90	1	Digital tube G signal	3.3V

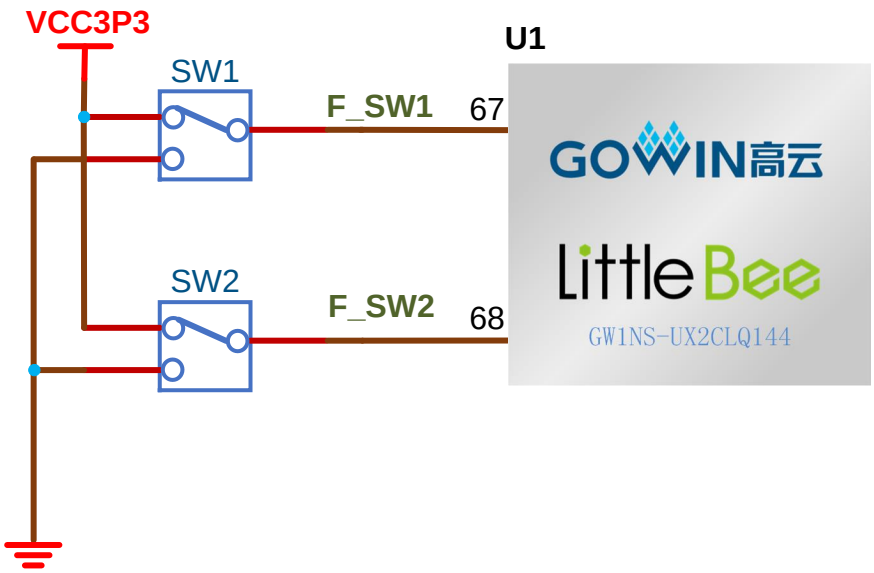
3.7 Switches

3.7.1 Overview

Two Slide switches are incorporated into the development board. These are used to control input during testing.

3.7.2 Switch Circuit

Figure 3-8 Switch Circuit



3.7.3 Pins Distribution

Table 3-8 Switch Circuit Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_SW1	67	2	Slide Switch1	2.5V
F_SW2	68	2	Slide Switch2	2.5V

3.8 Key

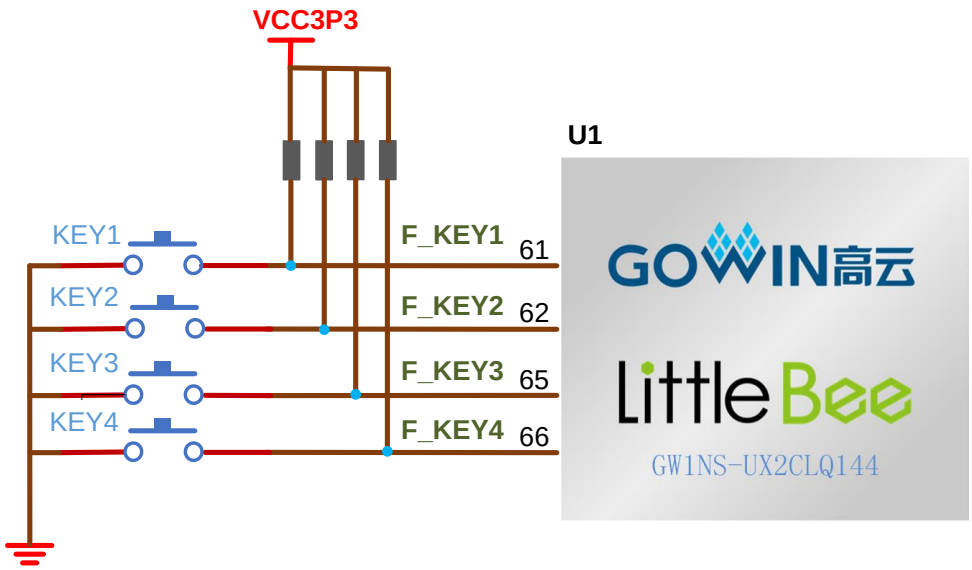
3.8.1 Overview

Four key switches are embedded in the development board. Users can manually input a low level to the corresponding FPGA pins for testing

purposes.

3.8.2 Key Circuit

Figure 3-9 Key Circuit Diagram



3.8.3 Pins Distribution

Table 3-9 Key Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_KEY1	61	2	KEY1	2.5V
F_KEY2	62	2	KEY2	2.5V
F_KEY3	65	2	KEY3	2.5V
F_KEY4	66	2	KEY4	2.5V

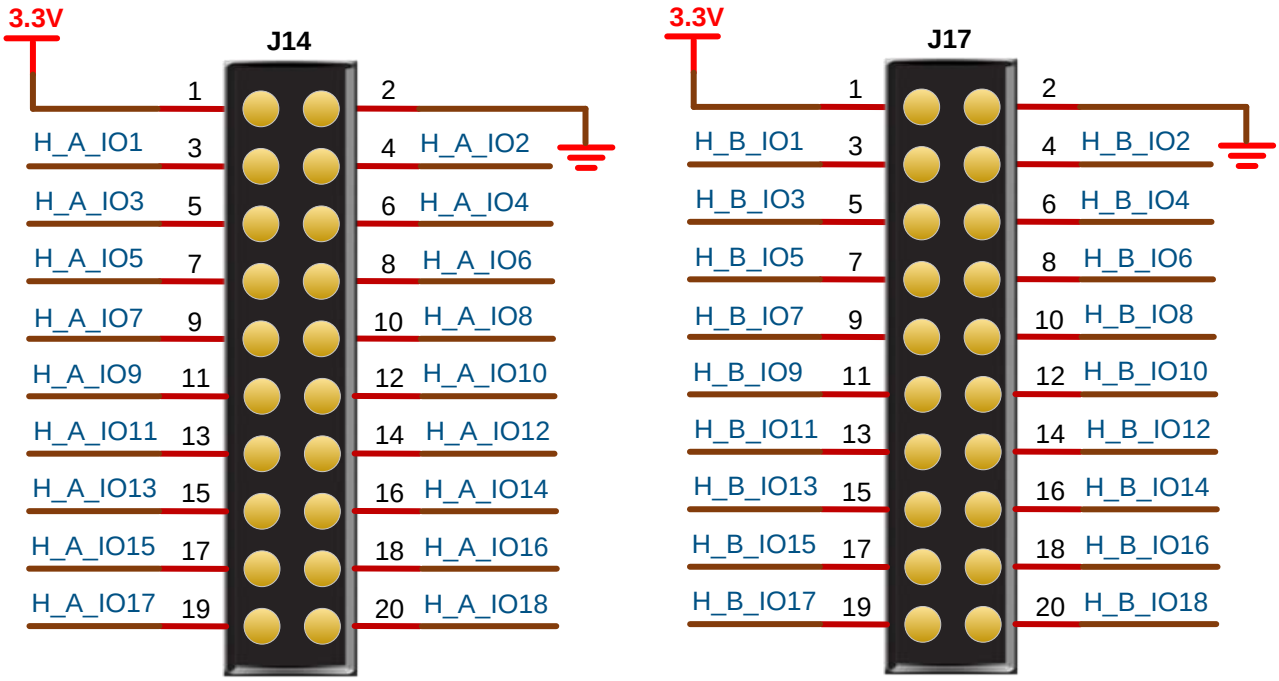
3.9 GPIO

3.9.1 Overview

Two 2.54mm DC3-20P sockets are reserved on the development board for user function extension and testing purposes.

3.9.2 GPIO Circuit

Figure3-10 GPIO Circuit



3.9.3 Pins Distribution

Table 3-10 J14 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
VCC3P3	-	1	-	-	3.3V
GND	-	2	-	-	-
H_A_IO1	132	3	0	General I/O	3.3V
H_A_IO2	131	4	0	General I/O	3.3V
H_A_IO3	130	5	0	General I/O	3.3V
H_A_IO4	129	6	0	General I/O	3.3V

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
H_A_IO5	124	7	0	General I/O	3.3V
H_A_IO6	4	8	3	General I/O	3.3V
H_A_IO7	7	9	3	General I/O	3.3V
H_A_IO8	8	10	3	General I/O	3.3V
H_A_IO9	9	11	3	General I/O	3.3V
H_A_IO10	12	12	3	General I/O	3.3V
H_A_IO11	15	13	3	General I/O	3.3V
H_A_IO12	22	14	3	General I/O	3.3V
H_A_IO13	23	15	3	General I/O	3.3V
H_A_IO14	24	16	3	General I/O	3.3V
H_A_IO15	25	17	3	General I/O	3.3V
H_A_IO16	27	18	3	General I/O	3.3V
H_A_IO17	28	19	3	General I/O	3.3V
H_A_IO18	29	20	3	General I/O	3.3V

Table3-11 J17 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
VCC3P3	-	1	-	-	3.3V
GND	-	2	-	-	-
H_B_IO1	123	3	0	General I/O	3.3V
H_B_IO2	120	4	0	General I/O	3.3V
H_B_IO3	119	5	0	General I/O	3.3V
H_B_IO4	116	6	0	General I/O	3.3V
H_B_IO5	115	7	0	General I/O	3.3V
H_B_IO6	112	8	0	General I/O	3.3V
H_B_IO7	111	9	0	General I/O	3.3V
H_B_IO8	110	10	0	General I/O	3.3V
H_B_IO9	106	11	1	General I/O	3.3V
H_B_IO10	104	12	1	General I/O	3.3V
H_B_IO11	102	13	1	General I/O	3.3V
H_B_IO12	58	14	2	General I/O	2.5V/1.2V
H_B_IO13	54	15	2	General I/O	2.5V/1.2V
H_B_IO14	45	16	2	General I/O	2.5V/1.2V
H_B_IO15	44	17	2	General I/O	2.5V/1.2V
H_B_IO16	41	18	2	General I/O	2.5V/1.2V
H_B_IO17	40	19	2	General I/O	2.5V/1.2V
H_B_IO18	30	20	3	General I/O	3.3V

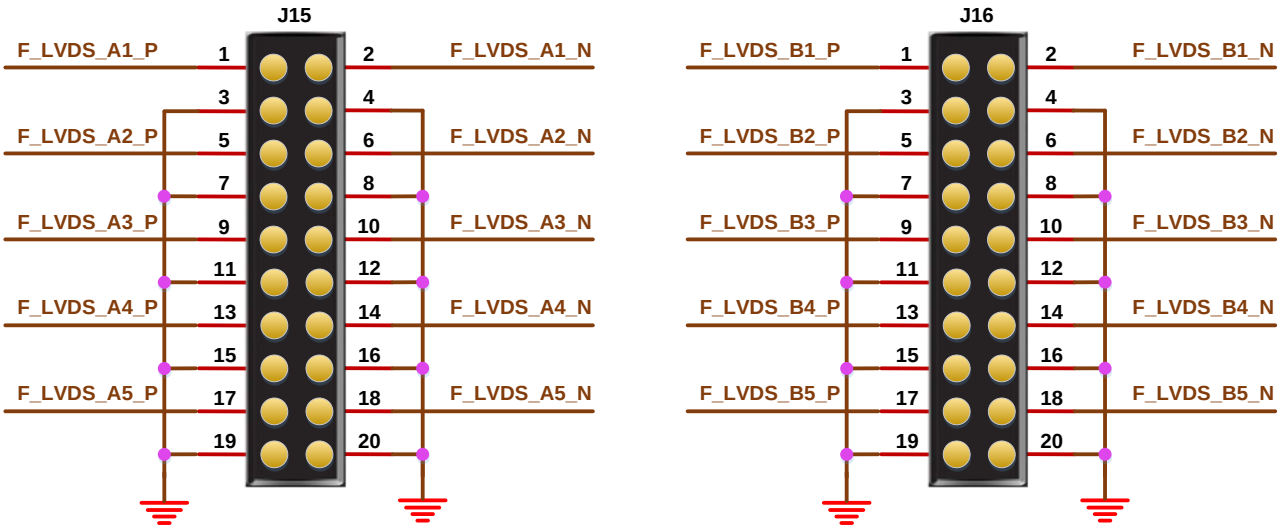
3.10 MIPI/LVDS

3.10.1 Overview

Two 2 mm DC3-20P sockets are reserved on the development board for MIPI/LVDS input/output testing and data communication.

3.10.2 MIPI/LVDS Circuit

Figure 3-11 LVDS Circuit



3.10.3 Pins Distribution

Table 3-12 J15 FPGA Pin Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
F_LVDS_A1_P	38	1	2	Differential output channel 1+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A1_N	39	2	2	Differential output channel 1-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_A2_P	42	5	2	Differential output channel 2+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A2_N	43	6	2	Differential output channel 2-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	7	-	-	
GND	-	8	-	-	
F_LVDS_A3_P	46	9	2	Differential output channel 3+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A3_N	47	10	2	Differential output channel 3-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	11	-	-	
GND	-	12	-	-	
F_LVDS_A4_P	59	13	2	Differential output channel 4+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A4_N	60	14	2	Differential output channel 4-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	15	-	-	
GND	-	16	-	-	
F_LVDS_A5_P	63	17	2	Differential output channel 5+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A5_N	64	18	2	Differential output channel 5-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	19	-	-	
GND	-	20	-	-	

Table 3-13 J16 FPGA Pin Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
F_LVDS_B1_P	136	1	0	Differential input channel 1+	3.3V
F_LVDS_B1_N	135	2	0	Differential input channel 1-	LVDS
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_B2_P	128	5	0	Differential input channel 2+	3.3V
F_LVDS_B2_N	126	6	0	Differential input channel 2-	LVDS
GND	-	7	-	-	-
GND	-	8	-	-	-
F_LVDS_B3_P	122	9	0	Differential input channel 3+	3.3V
F_LVDS_B3_N	121	10	0	Differential input channel 3-	LVDS
GND	-	11	-	-	-
GND	-	12	-	-	-
F_LVDS_B4_P	118	13	0	Differential input channel 4+	3.3V
F_LVDS_B4_N	117	14	0	Differential input channel 4-	LVDS
GND	-	15	-	-	-
GND	-	16	-	-	-
F_LVDS_B5_P	114	17	0	Differential input channel 5+	3.3V
F_LVDS_B5_N	113	18	0	Differential input channel 5-	LVDS
GND	-	19	-	-	-
GND	-	20	-	-	-

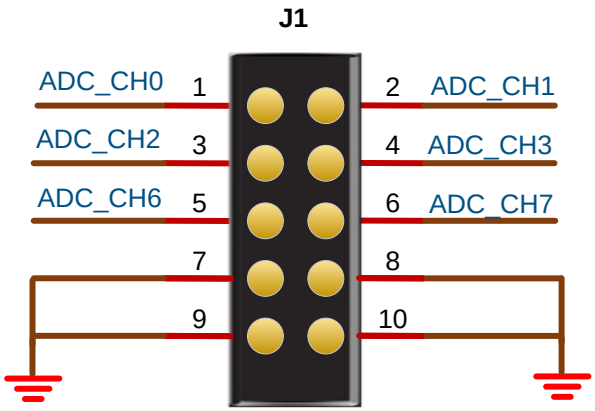
3.11 ADC

3.11.1 Overview

One 2.54mm DC3-10P socket is reserved on the development board for AD conversion. The built-in ADC can be used for up to six-channel signals.

3.11.2 ADC Circuit

Figure 3-12 ADC Circuit



3.11.3 Pins Distribution

Table 3-14 J1 ADC Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
ADC_CH0	140	1	0	General I/O	3.3V
ADC_CH1	139	2	0	General I/O	3.3V
ADC_CH2	138	3	0	General I/O	3.3V
ADC_CH3	137	4	0	General I/O	3.3V
ADC_CH6	134	5	0	General I/O	3.3V
ADC_CH7	133	6	0	General I/O	3.3V
GND	--	7	--	--	--
GND	--	8	--	--	--
GND	--	9	--	--	--
GND	--	10	--	--	--

3.12 RS232

3.12.1 Overview

One RS232 interface is reserved on the development board for the FPGA to communicate with PC or the other devices.

3.12.2 RS232 Circuit

Figure 3-13 RS232 Download Connection

3.12.3 Pins Distribution

Table 3-15 RS232 Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
UART_TXD	100	1	Serial data Sends from FPGA	3.3V
UART_RXD	101	1	Serial data Sends to FPGA	3.3V

4 Precautions

Precautions to be taken when using the development board:

1. Handle with care and pay attention to electrostatic protection;
2. Before downloading to FPGA and MCU, switch the SW3, SW4, SW5, and SW6 on the development board to the FPGA Download side;
3. Before debugging MCU, switch the SW3, SW4, SW5, and SW6 on the development board to the ARM Download side;
4. VCCO2 Bank voltage needs to be set as 2.5V when the Bank2 output differential pairs serve as LVDS output; VCCO2 Bank voltage needs to be set as 1.2V when the Bank2 output differential pairs serve as MIPI output;
5. For DK-START-GW1NS2 V2.1, the TOP layer does not support MIPI input because the Bank0 voltage stays on 3.3V;
6. GW1NSE-2C is GOWIN SecureFPGA, with the functions of Secure Mode and authentication code.
7. Gowin EDA Tool version 1.9.2 or above is required to download FPGA;
8. The "Secure Mode" mode of one-time programming is usually used for product delivery. It is not suggested to select the "Secure Mode" when downloading bitstream to Secure FPGA ;
9. Before the first use of the board, the authentication code must be read back using the Programmer tool and saved to the local PC. Each time before downloading the MCU code, it is necessary to write the authentication code first.

5 Gowin YunYuan Software

Please refer to SUG100, *Gowin Software User Guide* for details.