# DK-START-GW1NSR2 V1.1

# User Guide

**DBUG360-1.3E, 12/20/2019**

**Disclaimer**

## Revision History

| Date | Version | Description |
|---|---|---|
| 01/15/2019 | 1.0E | Initial version published. |
| 04/22/2019 | 1.1E | ● Data stream download updated;<br>● Precautions updated. |
| 11/29/2019 | 1.2E | MIPI input operating voltage modified. |
| 12/20/2019 | 1.3E | The development board version of DK-START-GW1NSR2 added. |

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# 1 About This Guide

## 1.1 Purpose

The DK-START-GW1NSR2 V1.1 user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the hardware circuits functions, circuit, and pins distribution;
3. Precautions to be taken when using the development board;
4. Introduction to the use of the FPGA development software.

## 1.2 Supported Products

The information in the guide applies to GW1NSR series of FPGA products: GW1NSR-2, GW1NSR-2C.

## 1.3 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS861, GW1NSR series of FPGA Products Data Sheet
2. UG863, GW1NSR series of FPGA Products Package and Pinout
3. UG862, GW1NSR-2&2C Pinout
4. UG290, Gowin FPGA Products Programming and Configuration User Guide
5. SUG100, Gowin YunYuan Software User Guide

# 1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

**Table 1-1 Abbreviations and Terminology**

| Abbreviations and Terminology | Full Name |
|---|---|
| FPGA | Field Programmable Gate Array |
| SoC | System On Chip |
| ARM | Advanced RISC Machines |
| AHB | Advanced High performance Bus |
| APB | Advanced Peripheral Bus |
| Timer | Timer |
| RS232 | Universal Asynchronous Receiver/Transmitter |
| NVIC | Nested Vector Interrupt Controller |
| DAP | Debug Access Port |
| Watchdog | Watchdog |
| TimeStamp | TimeStamp |
| DWT | Data Watchpoint Trace |
| ITM | Instrumentation Trace Module |
| TUIP | Trace Port Interface Unit |
| USB | Universal Serial Bus |
| PHY | Physical Layer |
| ADC | Analog to Digital Converter |
| SAR | Successive Approximation Register |
| SFDR | Spurious-free Dynamic Range |
| SINAD | Signal to Noise And Distortion |
| LSB | Least Significant Bit |
| INL | Integral Nonlinearity |
| DNL | Differential Nonlinearity |
| CFU | Configurable Function Unit |
| CLS | Configurable Logic Slice |
| CRU | Configurable Routing Unit |
| LUT4 | 4-input Look-up Tables |
| LUT5 | 5-input Look-up Tables |
| LUT6 | 6-input Look-up Tables |
| LUT7 | 7-input Look-up Tables |
| LUT8 | 8-input Look-up Tables |
| REG | Register |
| ALU | Arithmetic Logic Unit |

| Abbreviations and Terminology | Full Name |
|---|---|
| IOB | Input/Output Block |
| S-SRAM | Shadow SRAM |
| B-SRAM | Block SRAM |
| SP | Single Port |
| SDP | Semi Dual Port |
| DP | Dual Port |
| PSRAM | Pseudo static random access memory |
| DQCE | Dynamic Quadrant Clock Enable |
| DCS | Dynamic Clock Selector |
| PLL | Phase-locked Loop |
| DLL | Delay-locked Loop |
| LQ144 | LQFP144 |

## 1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

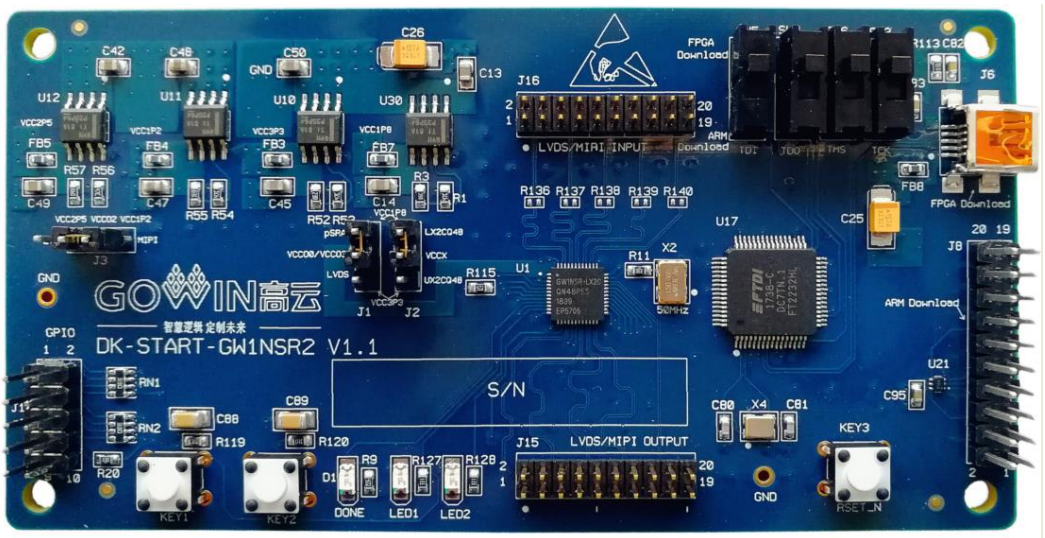
E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

# 2 Development Board Description

## 2.1 Overview

**Figure 2-1 DK-START-GW1NSR2 V1.1**




The development board adopts the GW1NSR-2 SoC FPGA. SoC FPFA is embedded with an ARM Cortex-M3 hard core processor, 32Mbit PSRAM, 1Mbit User Flash and eight-channel ADC converter, etc. When the ARM Cortex-M3 hard-core processor is employed as the core, the needs of the Min. memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits.

The development board offers abundant external interfaces, including MIPI/LVDS interfaces, GPIO interfaces, ADC interfaces, slide switches, LED, clock, reset, etc.

# 2.2 A Development Board Suite

A development board suite includes the following items:

- DK-START-GW1NSR2 V1.1
- USB cable
- Quick Start Guide

**Figure 2-2 A Development Board Suite**

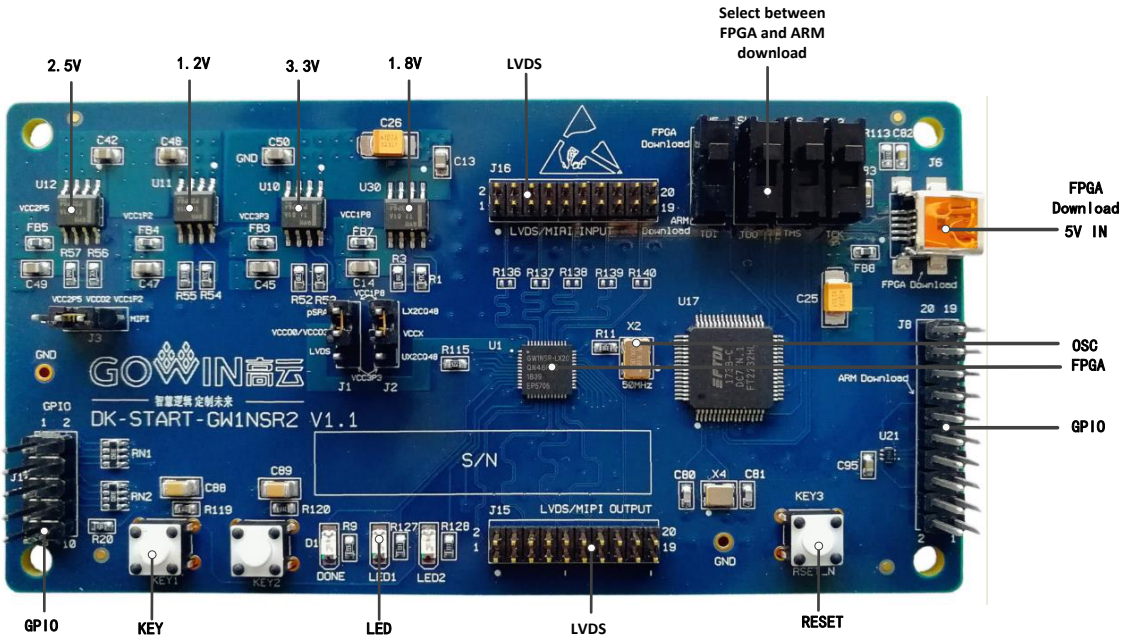

① DK-START-GW1NSR2 V1.1

② USB Cable

③ Quick Start Guide

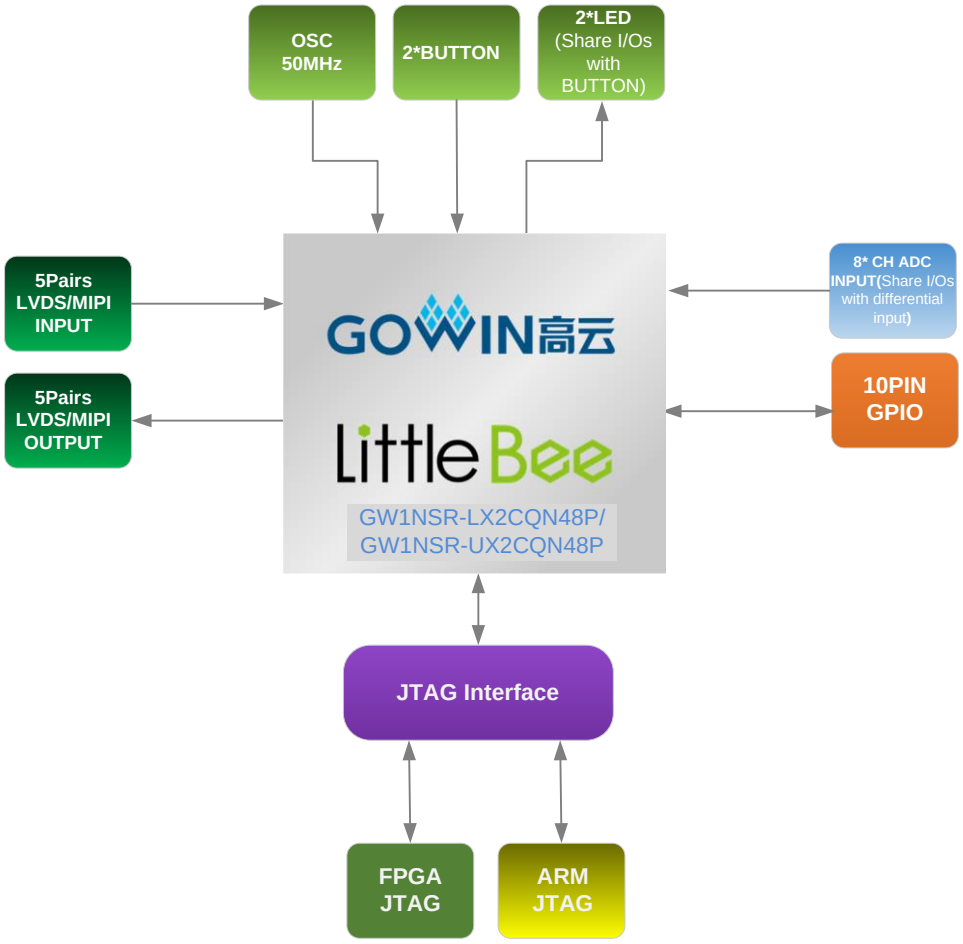
# 2.3 PCB Components

**Figure 2-3 PCB Components**



# 2.4 System Architecture

**Figure 2-4 System Architecture**



# 2.5 Features

The structure and features of the development board are as follows:

1. FPGA
   - Adopts QN48 package
   - Up to 38 user I/O
   - Embedded flash, data not easily lost if power down
   - Abundant LUT4 resources
   - Multiple modes and capacities of B-SRAM
2. FPGA Configuration Mode
   - JTAG
   - AUTO BOOT
3. Clock resource

   50MHz Clock Crystal Oscillator
4. Key switch and slide switch
   - One reset button
   - Two key switches
5. LED
   - One power indicator (green)
   - One DONE indicator (green)
   - 2 LEDs (green)
6. Memory
   - 1Mbit built-in Flash
   - 32Mbit built-in PSRAM
7. MIPI/LVDS

   5 pairs of MIPI/LVDS differential input; 5 pairs of MIPI/LVDS differential output
8. GPIO

   9 I/O expansion resources
9. LDO Power

   Support 3.3 V, 2.5V, 1.8 V, and1.2 V.

# 2.6 Development Board Specification

**Table 2-1 Development Board Specification**

| No. | Item | Functions | Technical Conditions | Remarks |
|---|---|---|---|---|
| 1 | FPGA | Core chip | – | – |
| 2 | Download | Support an USB interface; Support JTAG, AUTOBOOT | USB-JTAG module on board | – |
| 3 | Power Supply | Provide DC 5V input; 3.3 V, 2.5V,1.8V, and 1.2 V output via LDO circuit | ● Input power: 5V<br>● Provide power for FPGA, download circuit and other circuits via 5V–3.3 V circuit;<br>● Provide power for FPGA via the 5V to 2.5V circuit;<br>● Provide power for FPGA via the 5V to 1.8V circuit;<br>● Provide power to FPGA core via 5 V–1.2 V circuit. | – |
| 4 | Key Switches | Available for testing | 2 | – |
| 5 | Reset button | Reset for FPGA | 1 | – |
| 6 | LED | Test indicator, DONE indicator, Power indicator | ● Two green test indicators (share I/O resources with keys);<br>● One DONE indicator, green<br>● One Power indicator, green | – |
| 7 | Crystal Oscillator | Provide 50MHz clock for FPGA | Package5032 | – |
| 8 | Memory | Provides abundant Flash and PSRAM for designs | ● 1Mbit built-in Flash<br>● 32Mbit built-in PSRAM | – |
| 9 | GPIO | I/O, convenient for user extension and test | 9 | – |
| 10 | MIPI/LVDS | MIPI/LVDS, used for testing | 5 pairs of input, 5 pairs of output | – |
| 11 | Protection | USB interface: ESD protection;<br>Power interface: Inverse current and over current protection | ● USB interface ESD protection: ±15kV non-contact discharge, ± 8kV contact discharge;<br>● Schottky diode is connected between positive and negative anodes of power outlet; | – |

| No. | Item | Functions | Technical Conditions | Remarks |
|---|---|---|---|---|
| | | | ● 2A self-recovery fuses are connected at power inlet | |
| 12 | Voltage | – | Input Voltage: 5V | – |
| 13 | Humidity | – | 95% | – |
| 14 | Temperature | – | Operating range: –20°~70° | – |

# 3 Development Board Circuit

## 3.1 FPGA Module

### 3.1.1 Overview

The resources of GW1NSR series of FPGA products are set out in Table 3-1.

**Table 3-1 GW1NSR-2/GW1NSR-2C FPGA Resources List**

| Device | GW1NSR-2 | GW1NSR-2C |
|---|---|---|
| LUT4 | 1,728 | 1,728 |
| Flip-Flop (FF) | 1,296 | 1,296 |
| Block SRAM<br>B-SRAM (bits) | 72K | 72K |
| B-SRAM quantity<br>B-SRAM | 4 | 4 |
| User Flash (bits) | 1M | 1M |
| PSRAM(bits) | 32M | 32M |
| PLLs+DLLs | 1+2 | 1+2 |
| OSC | 1, ±5% accuracy | 1, ±5% accuracy |
| Hard core processor | - | Cortex-M3 |
| USB PHY | USB 2.0 PHY | USB 2.0 PHY |
| ADC[1] | 1 | 1 |
| Total number of I/O banks | 4 | 4 |
| Max. user I/O[1] | 38 | 38 |
| Core voltage | 1.2V | 1.2V |

**Note!**

See DS861, *GW1NSR series of FPGA Products Data Sheet* for further details.

## 3.1.2 I/O BANK Introduction

There are four I/O Banks in the GW1NSR series of FPGA products. The I/O BANK Distribution of the GW1NSR series of FPGA products is as shown in Figure 3-1.

**Figure 3-1 GW1NSR series I/O Bank Distribution**

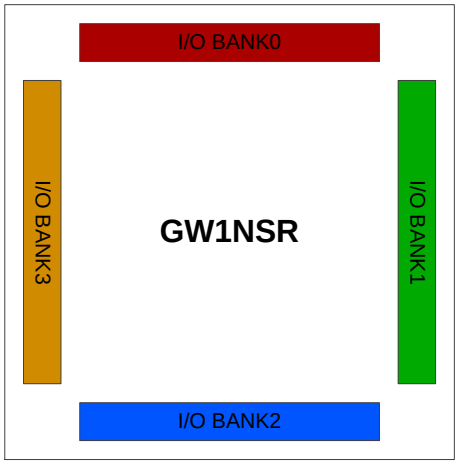



**Figure 3-2 View of GW1NSR-2 QN48 Pins Distribution (Top View)**

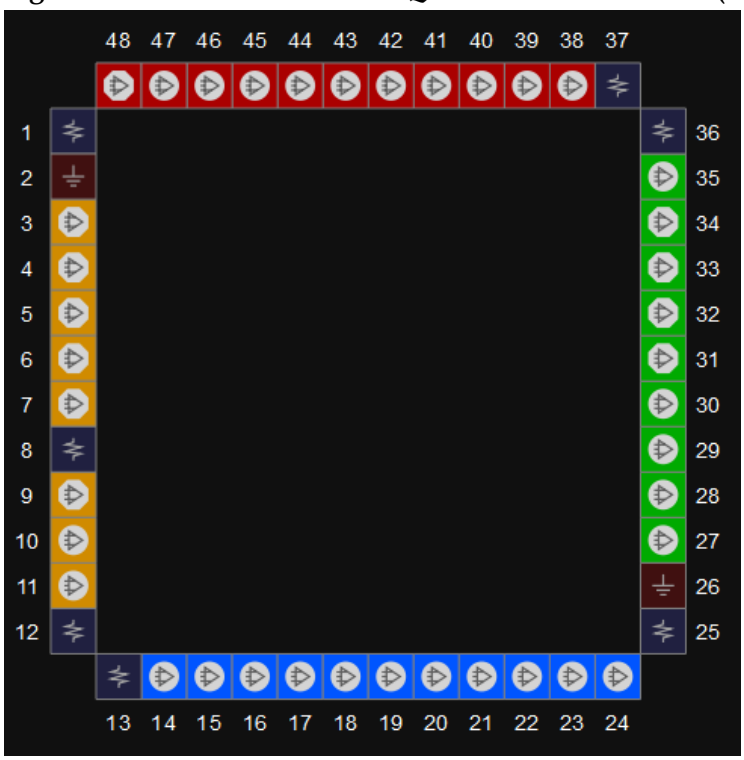


**Table 3-2 FPGA I/O Pins Distribution**

| I/O BANK No. | Modules Connected |
|---|---|
| I/O BANK0 | ● Pins used for download mode selection<br>● MIPI/LVDS differential input<br>● ADC input |
| I/O BANK1 | ● GPIO<br>● 50MHz clock input<br>● MIPI/LVDS differential output |
| I/O BANK2 | ● MIPI/LVDS differential output<br>● GPIO<br>● Reset |
| I/O BANK3 | ● GPIO<br>● LED/BUTTON<br>● JTAG Download<br>● DONE |

# 3.2 Download

## 3.2.1 Overview

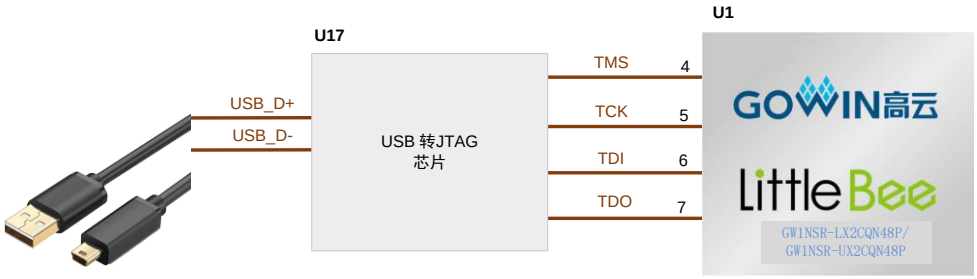
The development board provides an USB download interface. The data stream file can be downloaded to the internal SRAM, or internal flash as needed.

**Note!**

- When downloaded to SRAM, the data stream file will be lost if the device is power down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the data stream file will not be lost if the device is powered down.

## 3.2.2 USB Download Circuit

**Figure 3-3 Connection Diagram for FPGA USB Downloading**




## 3.2.3 Download Flow

1. FPGA and MCU download mode:
   Plug the USB cable to the USB interface (J6) on the development board.

   **Note!**

   Before downloading, switch the SW3, SW4, SW5, and SW6 on the development board to the FPGA Download side.
2. MCU download mode:

   Connect the J-Link ARM emulator to the ARM JTAG interface (J8).

   **Note!**

   Before debugging, switch the SW3, SW4, SW5, and SW6 on the development board to the ARM Download side.

### 3.2.4 Pins Distribution

**Table 3-3 FPGA Download and Pins Distribution**

| Signal Name | Pin No. | BANK | Description | I/O |
|---|---|---|---|---|
| TMS | 4 | 3 | JTAG Signal | 3.3V(MIPI/LVDS/ADC)/ 1.8V(PSRAM) |
| TCK | 5 | 3 | JTAG Signal | 3.3V(MIPI/LVDS/ADC)/ 1.8V(PSRAM) |
| TDI | 6 | 3 | JTAG Signal | 3.3V(MIPI/LVDS/ADC)/ 1.8V(PSRAM) |
| TDO | 7 | 3 | JTAG Signal | 3.3V(MIPI/LVDS/ADC)/ 1.8V(PSRAM) |
| MODE2 | 48 | 0 | One Mode selection pin | 3.3V(MIPI/LVDS/ADC)/ 1.8V(PSRAM) |
| DONE | 9 | 3 | One DONE indicator | 3.3V(MIPI/LVDS/ADC)/ 1.8V(PSRAM) |

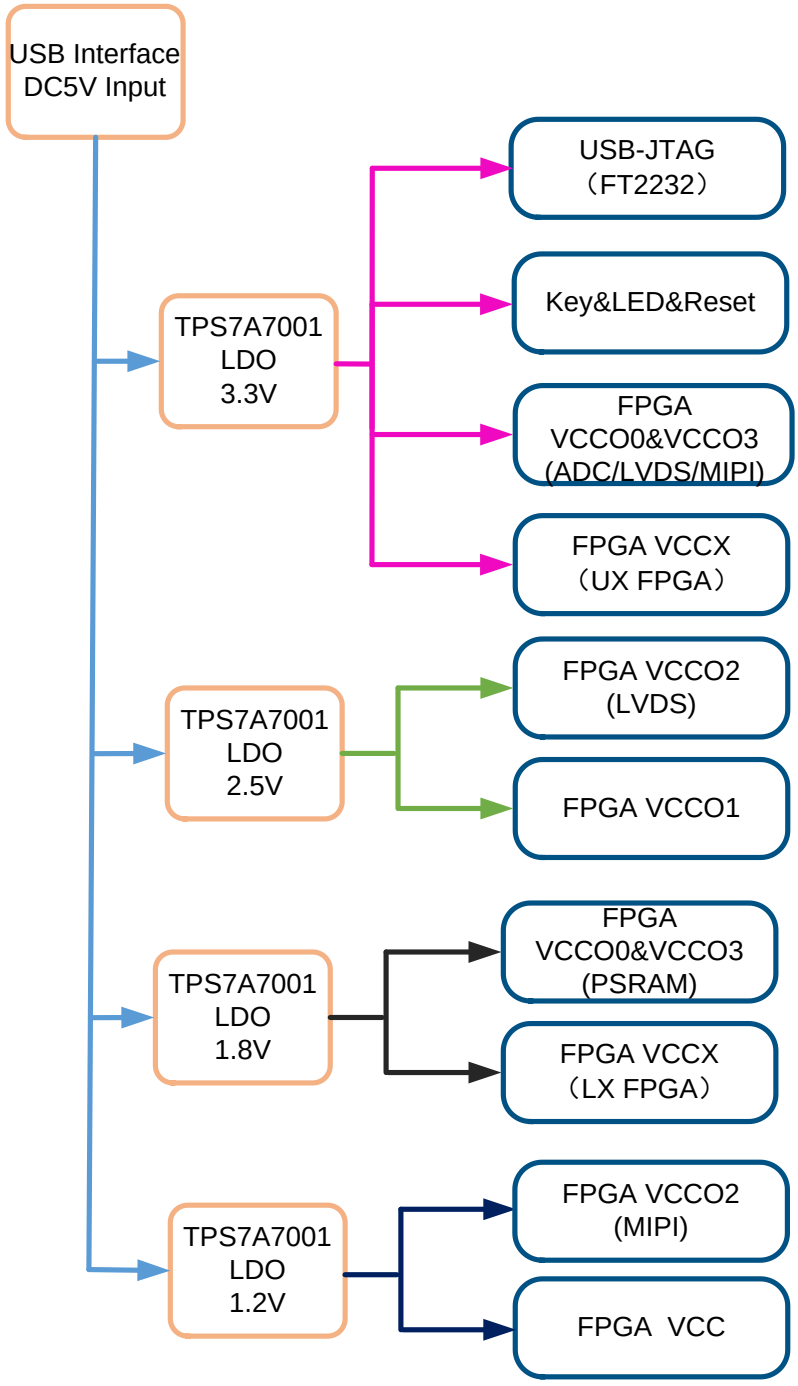
## 3.3 Power Supply

### 3.3.1 Overview

DC5V is input. The TI LDO power supply chip is used to step down voltage from 5V to 3.3V, 2.5V, 1.8V, and 1.0V, which can meet the power demand of the development board.

## 3.3.2 Power System Distribution

**Figure 3-4 Power System Distribution**



### 3.3.1 Pins Distribution

**Table 3-4 FPGA Power Pins Distribution**

| Signal Name | Pin No. | BANK | Description | I/O |
|---|---|---|---|---|
| VCCO0 | 1 | 0 | I/O Bank Power | 1.8V/3.3V |
| VCCO1 | 25 | 1 | I/O Bank Power | 2.5V |
| VCCO2 | 13 | 2 | I/O Bank Power | 1.2V/2.5V |
| VCCO3 | 1 | 3 | I/O Bank Power | 1.8V/3.3V |
| VCCX | 8, 36 | - | Auxiliary voltage | 1.8/3.3V |
| VCC | 12, 37 | - | Core voltage | 1.2V |
| VSS | 2, 26 | - | GND | - |

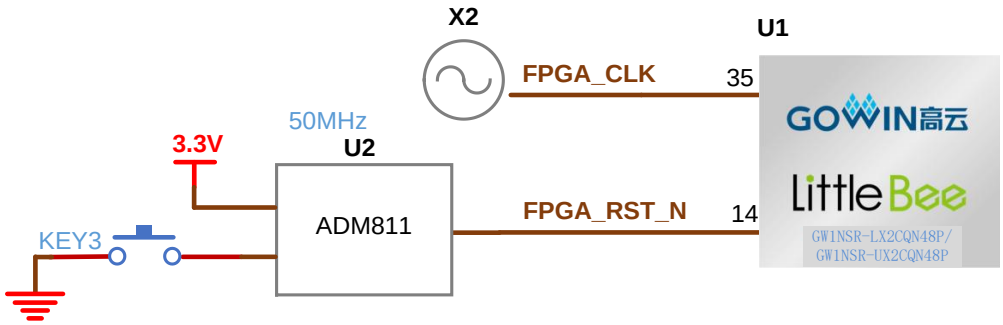
## 3.4 Clock, Reset

### 3.4.1 Overview

A 50MHz crystal oscillator is provided in the development board that connects to the PLL input pin. This can be employed as the input clock for the the PLL in FPGA, and the output clock as needed via multiplication and division of the PLL frequency.

### 3.4.2 Clock, Reset

**Figure 3-5 Clock, Reset**




### 3.4.3 Pins Distribution

**Table 3-5 FPGA Clock and Reset Pins Distribution**

| Signal Name | Pin No. | BANK | Description | I/O |
|---|---|---|---|---|
| FPGA_CLK | 35 | 1 | 50MHz crystal oscillator Input | 2.5V |
| FPGA_RST_N | 14 | 2 | Reset signal, active low | 2.5V |

# 3.5 LED

## 3.5.1 Overview

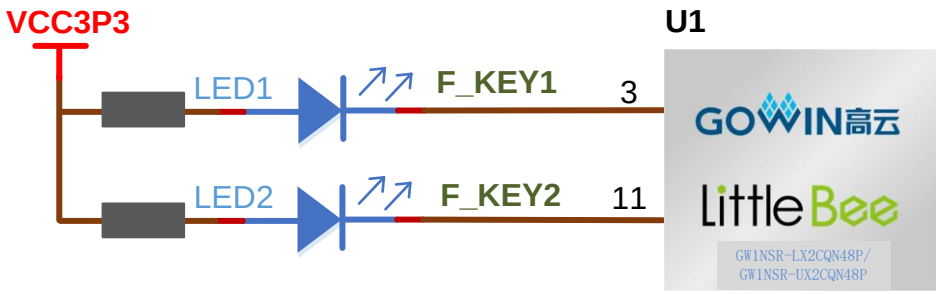
Two green LEDs (share I/O pins with keys) are incorporated into the development board and are used to display the required status. In addition, two LEDs are reserved to signify power supply and FPGA loading status.

Users can test the LEDs in the following ways:

- If the output signal of related pins is logic low, LED is on;
- If the logic is high, LED is off.

## 3.5.2 LED Circuit

**Figure 3-6 LED Circuit**




## 3.5.3 Pins Distribution

**Table 3-6 LED Pins Distribution**

| Signal Name | Pin No. | BANK | Description | I/O |
|---|---|---|---|---|
| F_KEY1 | 3 | 3 | LED1 | 1.8V/3.3V |
| F_KEY2 | 11 | 3 | LED2 | 1.8V/3.3V |

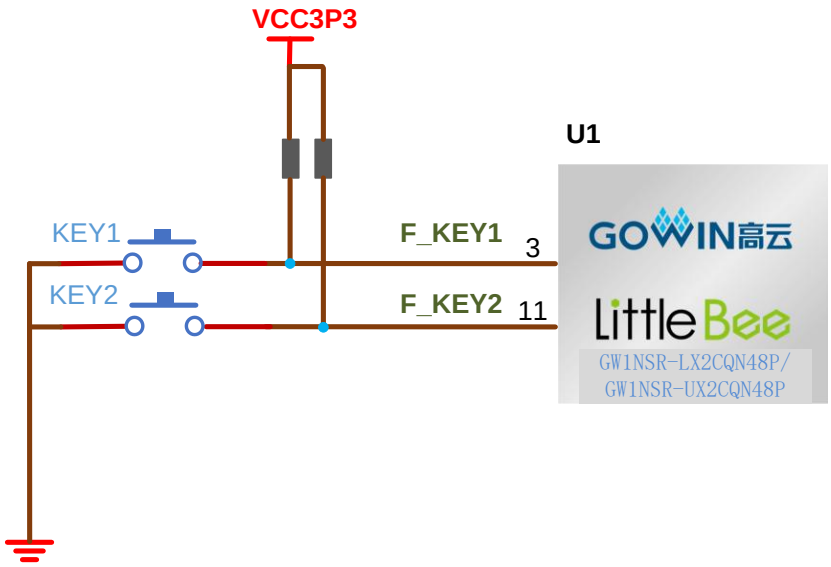
# 3.6 Key

## 3.6.1 Overview

Two key switches are embedded in the development board. Users can manually input a low level to the corresponding FPGA pins for testing purposes.

### 3.6.2 Key Circuit

**Figure 3-7 Key Circuit Diagram**




### 3.6.3 Pins Distribution

**Table 3-7 Key Pins Distribution**

| Signal Name | Pin No. | BANK | Description | I/O |
|---|---|---|---|---|
| F_KEY1 | 3 | 3 | KEY1 | 1.8V/3.3V |
| F_KEY2 | 11 | 3 | KEY2 | 1.8V/3.3V |

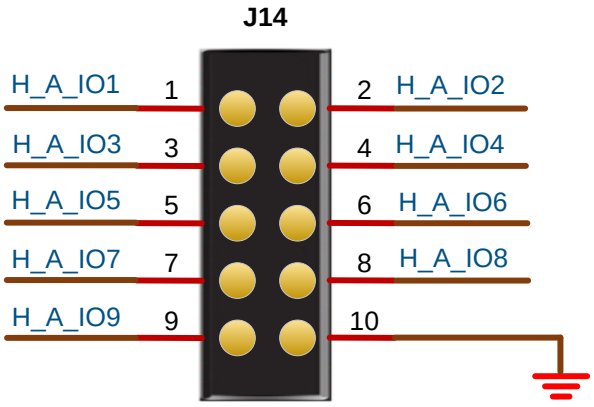
## 3.7 GPIO

### 3.7.1 Overview

One 2.54mm DC3-10P sockets are reserved on the development board for user function extension and testing purposes.

### 3.7.2 GPIO Circuit

**Figure3-8 GPIO Circuit**




### 3.7.3 Pins Distribution

**Table 3-8 J14 GPIO Pins Distribution**

| Signal Name | Pin No. | Socket Pin No. | BANK | Description | I/O |
|---|---|---|---|---|---|
| H_A_IO1 | 10 | 1 | 3 | General I/O | 1.8V/3.3V |
| H_A_IO2 | 17 | 2 | 2 | General I/O | 1.2V/2.5V |
| H_A_IO3 | 18 | 3 | 2 | General I/O | 1.2V/2.5V |
| H_A_IO4 | 27 | 4 | 1 | General I/O | 2.5V |
| H_A_IO5 | 28 | 5 | 1 | General I/O | 2.5V |
| H_A_IO6 | 29 | 6 | 1 | General I/O | 2.5V |
| H_A_IO7 | 30 | 7 | 1 | General I/O | 2.5V |
| H_A_IO8 | 31 | 8 | 1 | General I/O | 2.5V |
| H_A_IO9 | 32 | 9 | 1 | General I/O | 2.5V |
| GND | - | 10 | - | GND | - |

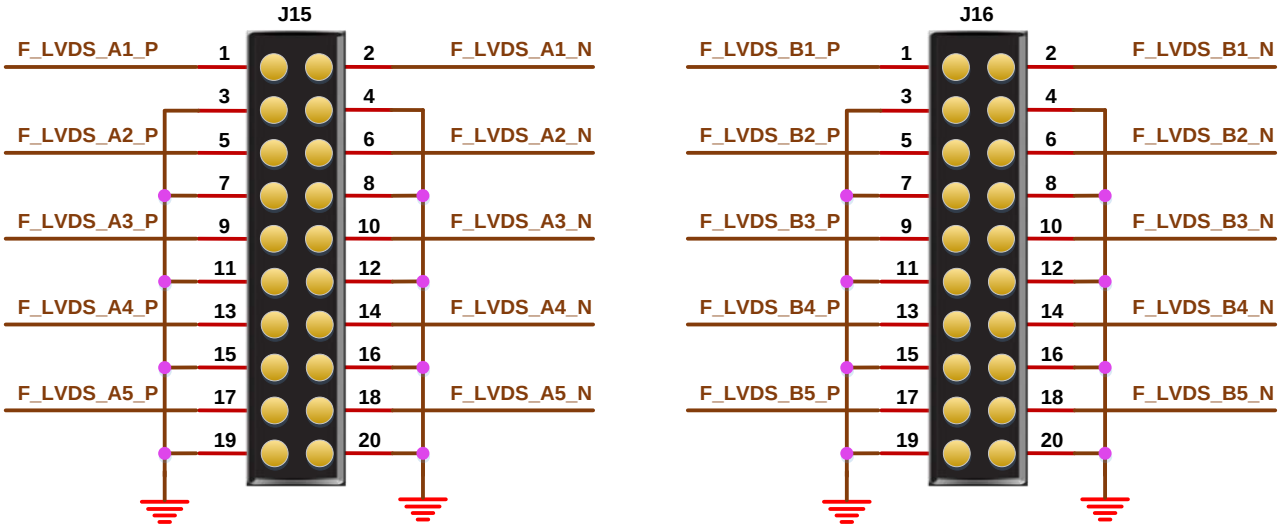
## 3.8 MIPI/LVDS

### 3.8.1 Overview

Two 2 mm DC3-20P sockets are reserved on the development board for MIPI/LVDS input/output testing and data communication.

## 3.8.2 MIPI/LVDS Circuit

Figure 3-9 LVDS Circuit



## 3.8.3 Pins Distribution

**Table 3-9 J15 FPGA Pin Distribution**

| Signal Name | Pin No. | Socket Pin No. | BANK | Description | I/O |
|---|---|---|---|---|---|
| F_LVDS_A1_P | 15 | 1 | 2 | Differential output channel 1+ | 2.5V(LVDS)/ 1.2V(MIPI) |
| F_LVDS_A1_N | 16 | 2 | 2 | Differential output channel 1- | 2.5V(LVDS)/ 1.2V(MIPI) |
| GND | - | 3 | - | - | - |
| GND | - | 4 | - | - | - |
| F_LVDS_A2_P | 19 | 5 | 2 | Differential output channel 2+ | 2.5V(LVDS)/ 1.2V(MIPI) |
| F_LVDS_A2_N | 20 | 6 | 2 | Differential output channel 2- | 2.5V(LVDS)/ 1.2V(MIPI) |
| GND | - | 7 | - | - | |
| GND | - | 8 | - | - | |
| F_LVDS_A3_P | 21 | 9 | 2 | Differential output channel 3+ | 2.5V(LVDS)/ 1.2V(MIPI) |
| F_LVDS_A3_N | 22 | 10 | 2 | Differential output channel 3- | 2.5V(LVDS)/ 1.2V(MIPI) |
| GND | - | 11 | - | - | |
| GND | - | 12 | - | - | |
| F_LVDS_A4_P | 23 | 13 | 2 | Differential output channel 4+ | 2.5V(LVDS)/ 1.2V(MIPI) |
| F_LVDS_A4_N | 24 | 14 | 2 | Differential output channel 4- | 2.5V(LVDS)/ 1.2V(MIPI) |
| GND | - | 15 | - | - | |
| GND | - | 16 | - | - | |
| F_LVDS_A5_P | 33 | 17 | 1 | Differential output channel 5+ | 2.5V(LVDS) |
| F_LVDS_A5_N | 34 | 18 | 1 | Differential output channel 5- | 2.5V(LVDS) |
| GND | - | 19 | - | - | |
| GND | - | 20 | - | - | |

**Table 3-10 J16 FPGA Pin Distribution**

| Signal Name | Pin No. | Socket Pin No. | BANK | Description | I/O |
|---|---|---|---|---|---|
| F_LVDS_B1_P | 47 | 1 | 0 | Differential input channel 1+ | 3.3V(LVDS)/ 1.8V(MIPI) |
| F_LVDS_B1_N | 46 | 2 | 0 | Differential input | 3.3V(LVDS)/ |

| Signal Name | Pin No. | Socket Pin No. | BANK | Description | I/O |
|---|---|---|---|---|---|
| | | | | channel 1- | 1.8V(MIPI) |
| GND | - | 3 | - | - | - |
| GND | - | 4 | - | - | - |
| F_LVDS_B2_P | 45 | 5 | 0 | Differential input channel 2+ | 3.3V(LVDS)/ 1.8V(MIPI) |
| F_LVDS_B2_N | 44 | 6 | 0 | Differential input channel 2- | 3.3V(LVDS)/ 1.8V(MIPI) |
| GND | - | 7 | - | - | - |
| GND | - | 8 | - | - | - |
| F_LVDS_B3_P | 43 | 9 | 0 | Differential input channel 3+ | 3.3V(LVDS)/ 1.8V(MIPI) |
| F_LVDS_B3_N | 42 | 10 | 0 | Differential input channel 3- | 3.3V(LVDS)/ 1.8V(MIPI) |
| GND | - | 11 | - | - | - |
| GND | - | 12 | - | - | - |
| F_LVDS_B4_P | 41 | 13 | 0 | Differential input channel 4+ | 3.3V(LVDS)/ 1.8V(MIPI) |
| F_LVDS_B4_N | 40 | 14 | 0 | Differential input channel 4- | 3.3V(LVDS)/ 1.8V(MIPI) |
| GND | - | 15 | - | - | - |
| GND | - | 16 | - | - | - |
| F_LVDS_B5_P | 39 | 17 | 0 | Differential input channel 5+ | 3.3V(LVDS)/ 1.8V(MIPI) |
| F_LVDS_B5_N | 38 | 18 | 0 | Differential input channel 5- | 3.3V(LVDS)/ 1.8V(MIPI) |
| GND | - | 19 | - | - | - |
| GND | - | 20 | - | - | - |

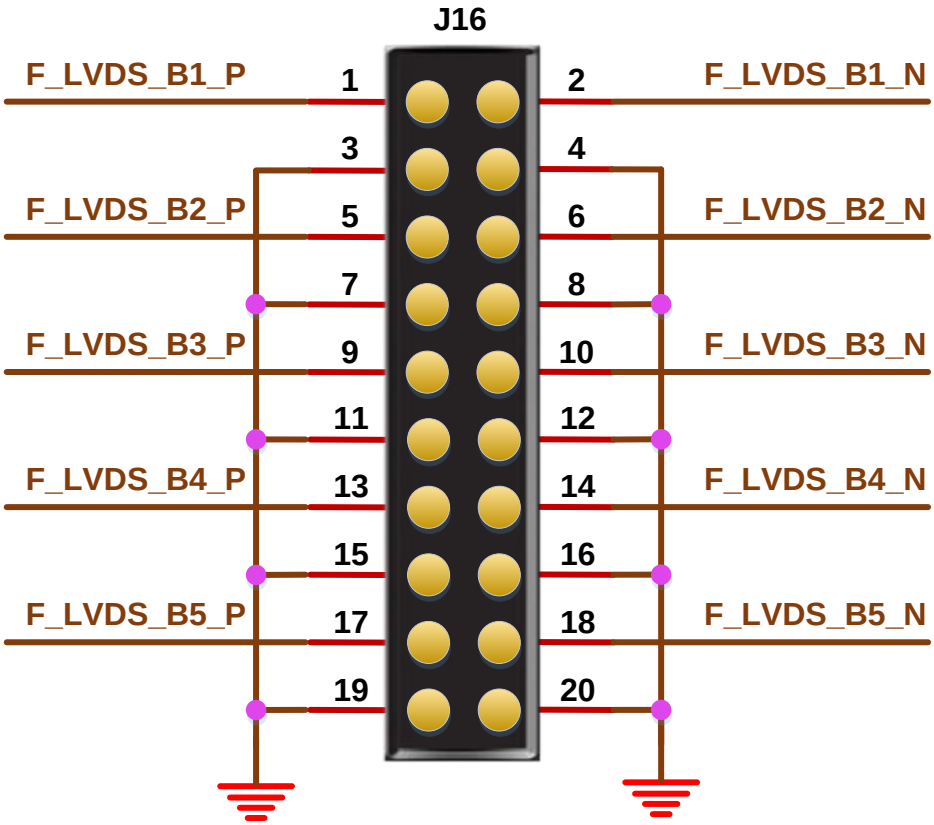
# 3.9 ADC

## 3.9.1 Overview

Up to four signals can be connected to the FPGA via the J16 socket on the development board for AD conversion by the built-in ADC.

## 3.9.2 ADC Circuit

Figure 3-10 ADC Circuit




## 3.9.3 Pins Distribution

Table 3-11 J16 ADC Pins Distribution

| Signal Name | Pin No. | Socket Pin No. | BANK | Description | I/O |
|---|---|---|---|---|---|
| F_LVDS_B1_P | 47 | 1 | 0 | ADC_CH0 | 3.3V(LVDS) |
| F_LVDS_B1_N | 46 | 2 | 0 | Ground | - |
| F_LVDS_B2_P | 45 | 3 | 0 | ADC_CH2 | 3.3V(LVDS) |
| F_LVDS_B2_N | 44 | 4 | 0 | Ground | - |
| F_LVDS_B3_P | 43 | 5 | 0 | ADC_CH4 | 3.3V(LVDS) |
| F_LVDS_B3_N | 42 | 6 | 0 | Ground | - |
| F_LVDS_B4_P | 41 | 7 | 0 | ADC_CH6 | 3.3V(LVDS) |
| F_LVDS_B4_N | 40 | 8 | 0 | Ground | - |

# 4 Precautions

Precautions to be taken when using the development board:

1. Handle with care and pay attention to electrostatic protection;
2. Programs download:
   - Before downloading to FPGA and MCU, switch the SW3, SW4, SW5, and SW6 on the development board to the FPGA Download side;
   - Before debugging MCU, switch the SW3, SW4, SW5, and SW6 on the development board to the ARM Download side;
3. Voltage selection:
   - If the development board adopts the UX device, VCCX needs to be set as 3.3V;
   - If the development board adopts the LX device, VCCX needs to be set as 1.8V;
   - VCCO2 Bank voltage needs to be set as 2.5V when the Bank2 output differential pairs serve as LVDS output;
   - VCCO2 Bank voltage needs to be set as 1.2V when the Bank2 output differential pairs serve as MIPI output.
   - VCCO0&VCCO3 Bank voltage needs to be set as 1.8V when the internal PSRAM is employed;
   - VCCO0&VCCO3 Bank voltage needs to be set as 3.3V when ADC or MIPI/LVDS input is employed.

# 5 Gowin YunYuan Software

Please refer to SUG100, *Gowin Software User Guide* for details.