DK-START-GW1N9

User Guide

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1 About This Guide

1.1 Purpose

The DK-START-GW1N9 user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the hardware circuits functions, circuit, and pins distribution;
3. Precautions to be taken when using the development board;
4. Introduction to the use of the FPGA development software.

1.2 Supported Products

The information in the guide applies to GW1N series of FPGA products: GW1N-9.

1.3 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1N series of Products Data Sheet
2. GW1N series of FPGA Products Package and Pinout
3. GW1N-6&9 Pinout
4. Gowin FPGA Products Programming and Configuration User Guide
5. Gowin YunYuan Software User Guide

1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
LED	Light Emitting Diode
LDO	Low Dropout Regulator
GPIO	General Purpose Input Output
LUT4	Four-input Look-up Table
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
PLL	Phase-locked Loop
DLL	Delay-locked Loop
DSP	Digital Signal Processing
LQ144	LQFP144

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

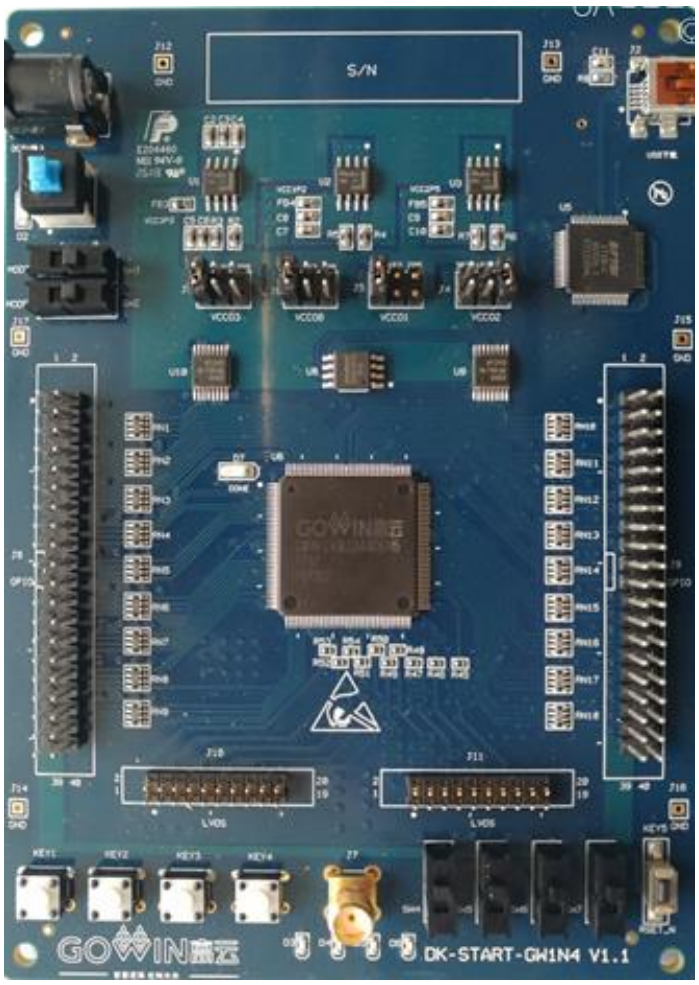
E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

2 Development Board Description

2.1 Overview

Figure 2-1 DK-START-GW1N V1.1



The Development board adopts the GW1N-LV9 LQ144 devices of the GW1N series of FPGA products. It features a range of advanced features including low power consumption, instant start-up, high security, low-cost,

and flexible extensions, all of which can effectively reduce the learning cost and help users quickly design and develop programmable logic devices.

The development board includes two GPIO ports and two LVDS ports. These provide users with a hardware evaluation and testing platform that offers a high integration level and stable performance via flexible VCCO regulation (3.3 V, 2.5 V, and 1.2 V). The development board also offers slide switches, key switches, a clock, and LEDs, all of which are useful for both developers and hobbyists alike.

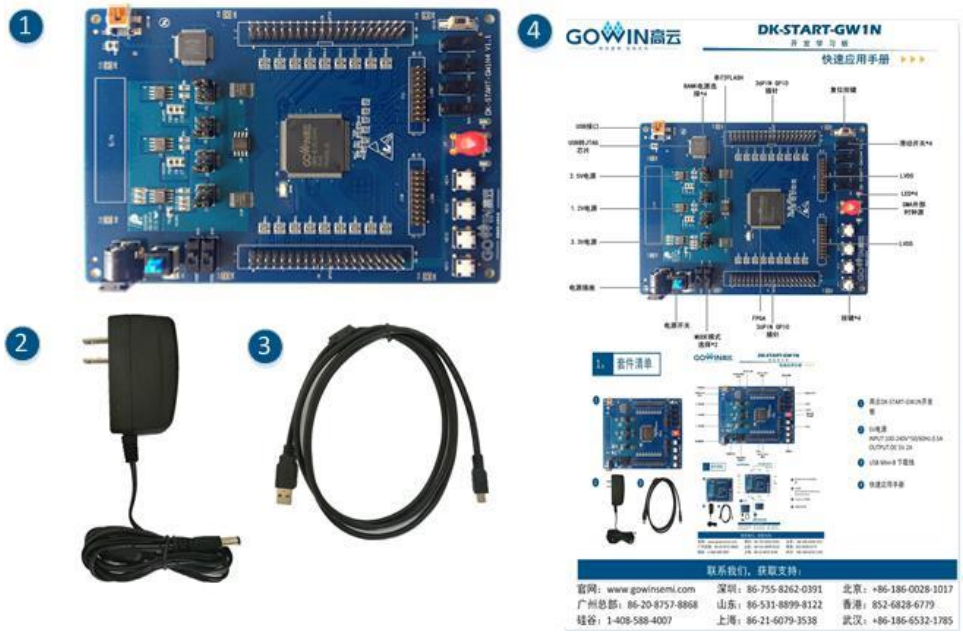
With abundant GPIO resources, the development board can be used as the main board to design an image-sampling system and the other related systems by combining video daughter boards. Motion control systems can also be designed by combining the development board with AD/DA industrial daughter boards, while human-computer interface and image processing can be realized by combining the development board with the display daughter board.

2.2 A Development Board Suite

A development board suite includes the following items:

- DK-START-GW1N9
- 5V power adapter (220V input, DC 5V 2A output)
- USB cable
- Quick Start

Figure 2-2A Development Board Suite



① DK-START-GW1N9

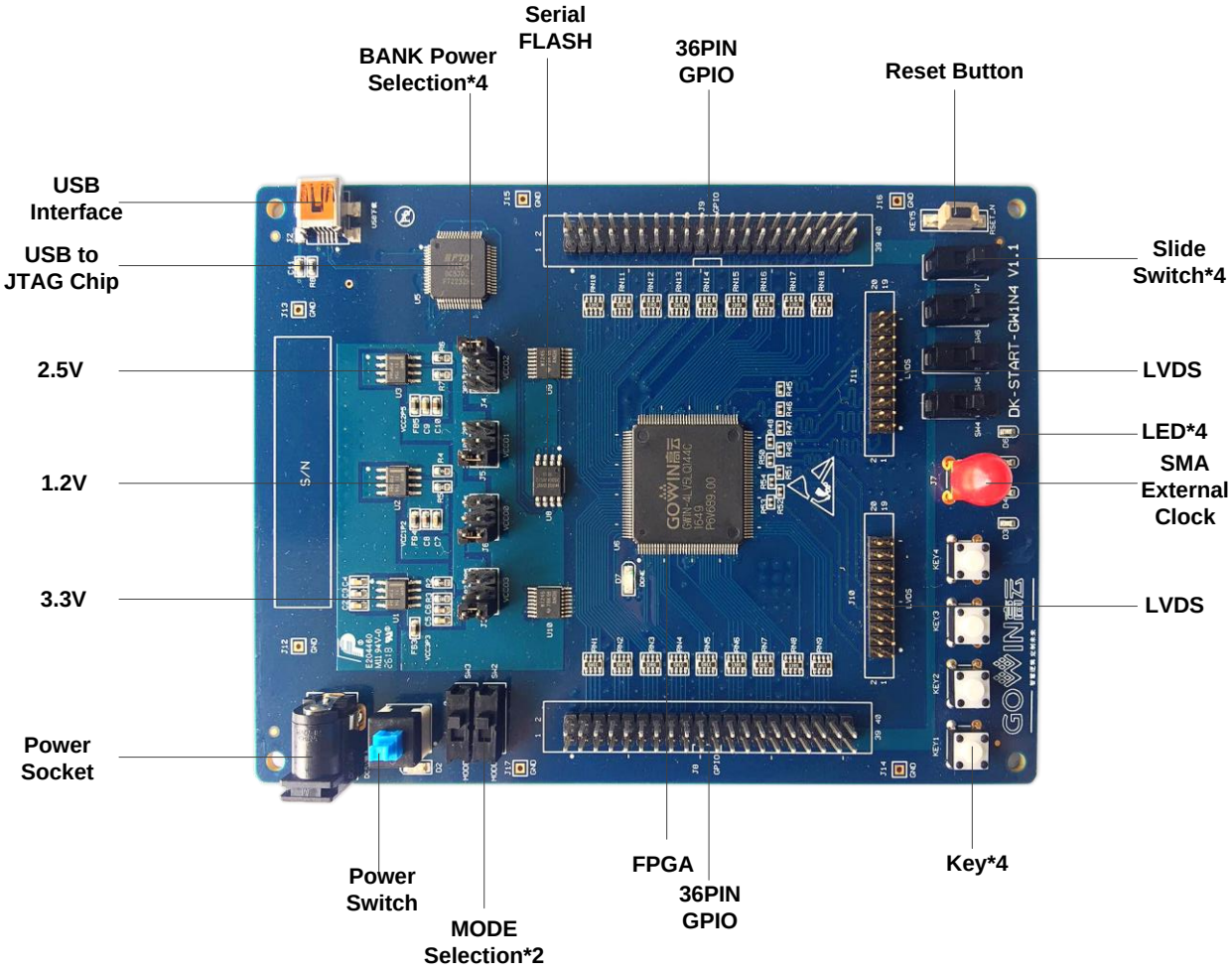
② 5V power adapter

③ USB cable

④ Quick Start

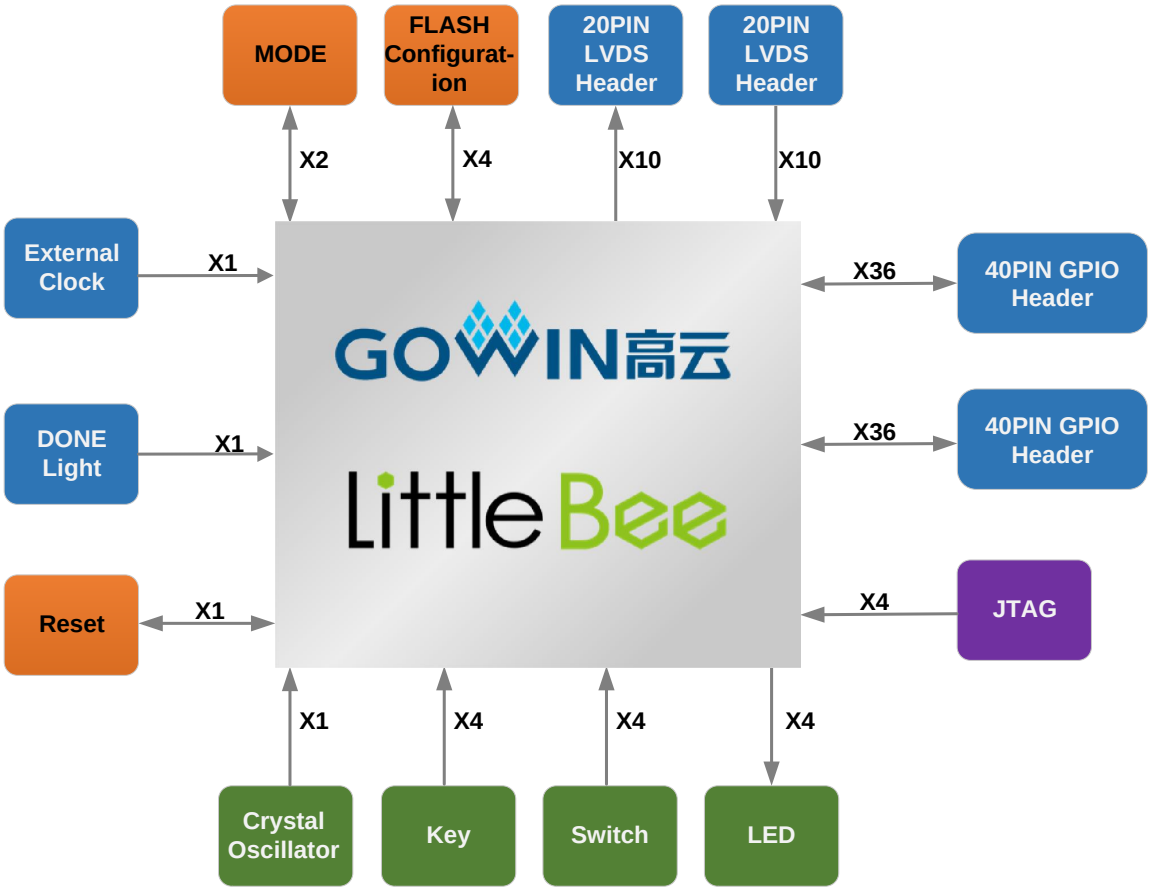
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Architecture

Figure 2-4 System Architecture



2.5 Features

The structure and features of the development board are as follows:

1. FPGA

- LQFP144 package
- Embedded flash, data not easily lost if power down
- Abundant LUT4 resources
- Multiple modes and capacities of B-SRAM
- Supports LV

2. FPGA Configuration Mode

JTAG, AUTO BOOT, MSPI

3. Clock Resources

- 50MHz clock crystal oscillator;
- SMA external clock input

4. Key switch and slide switch

- One reset button

- Four Key switches
- Four Slide switches

5. LED

- One power indicator (green)
- One DONE indicator (green)
- Four LEDs (green)

6. Memory

One 64Mbit SPI flash

7. GPIO

72 I/O Resources

8. LDO Power

- Inverse voltage protection, overcurrent protection;
- Supports 3.3 V, 2.5 V, and1.2V.

2.6 Development Board Specification

Table 2-1 Development Board Specification

No.	Item	Functional Description	Technical Conditions	Comments
1	FPGA	Core chip	–	–
2	Download Interface	Support USB interface; Support JTAG, AUTOBOOT, MSPI	USB-JTAG module on board	–
3	Power Supply	Provide DC 5V input; 3.3 V, 2.5V and 1.2 V output via LDO circuit	● Input power: 5V ● Provide power for FPGA, download circuit and other circuits via 5V–3.3 V circuit; ● Provide power for FPGA via 5V–2.5V circuit; ● Provide power to FPGA core via 3.3 V–1.2 V circuit.	–
4	Slide Switches	Available for testing	4	–
5	Key Switches	Available for testing	4	–
6	Reset button	Reset for FPGA	1	–
7	LED	Test indicator, DONE indicator, Power indicator	● Four Test indicator, green ● One DONE indicator, green ● One Power indicator, green	–
8	Crystal Oscillator	Provide 50MHz clock for FPGA	Package5032	–
9	External Clock	Input external clock frequency via SMA, used for testing		–

No.	Item	Functional Description	Technical Conditions	Comments
10	GPIO	I/O, convenient for user extension and test	76; Can be adjusted to 3.3V, 2.5V, and 1.2V IO voltage	–
11	LVDS	LVDS, used for testing	Ten pairs	–
12	Protection	USB interface: ESD protection; Power interface: Inverse current and over current protection	● USB interface ESD protection: ±15kV non-contact discharge, ± 8kV contact discharge; ● Schottky diode is connected between positive and negative anodes of power outlet; ● 2A self-recovery fuses are connected at power inlet	–
13	Voltage	–	Input range: 2.7V~5.5V	–
14	Humidity	–	95%	–
15	Temperature	–	Operating range: –20°~70°	–

3 FPGA Circuits

3.1 FPGA Module

3.1.1 Overview

The resources of GW1N series of FPGA products are set out in Table 3-1.

Table 3-1 GW1N series of FPGA Product Information List

Device	GW1N-1	GW1N-2/ GW1N-2B	GW1N-4/ GW1N-4B	GW1N-6	GW1N-9
LUT4	1,152	2,304	4,608	6,912	8,640
Flip-Flop (FF)	864	1,728	3,456	5,184	6,480
Shadow SRAM S-SRAM(bit)	0	0	0	13,824	17,280
Block SRAM Block SRAM (bit)	72K	180K	180K	468K	468K
B-SRAM quantity Block SRAM	4	10	10	26	26
User Flash (bits)	96K	256K	256K	608K	608K
18 x 18 Multiplier	0	16	16	20	20
PLL+DLL	0	2+2	2+2	2+3	2+3
Total number of I/O banks	4	4	4	4	4
Core Voltage (LV)	1.2V	1.2V	1.2V	1.2V	1.2V

Note!

See GW1N series of FPGA Products Data Sheet for further details.

3.1.2 I/O BANK Introduction

There are four I/O Banks in the GW1N series of FPGA products, as shown in Figure 3-1.Figure 3-2 is the LQ144 pins distribution view.

Figure 3-1 GW1N I/O Bank Distribution

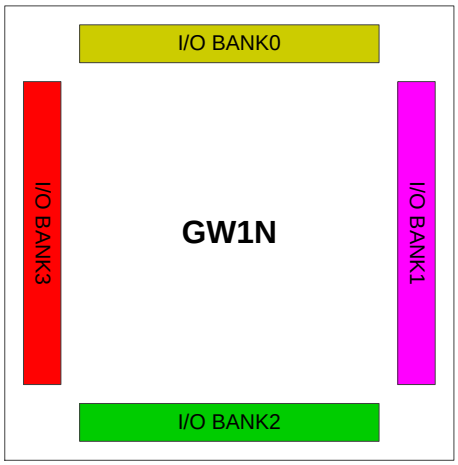


Figure 3-2 View of GW1N series LQ144 Pins Distribution (Top View)

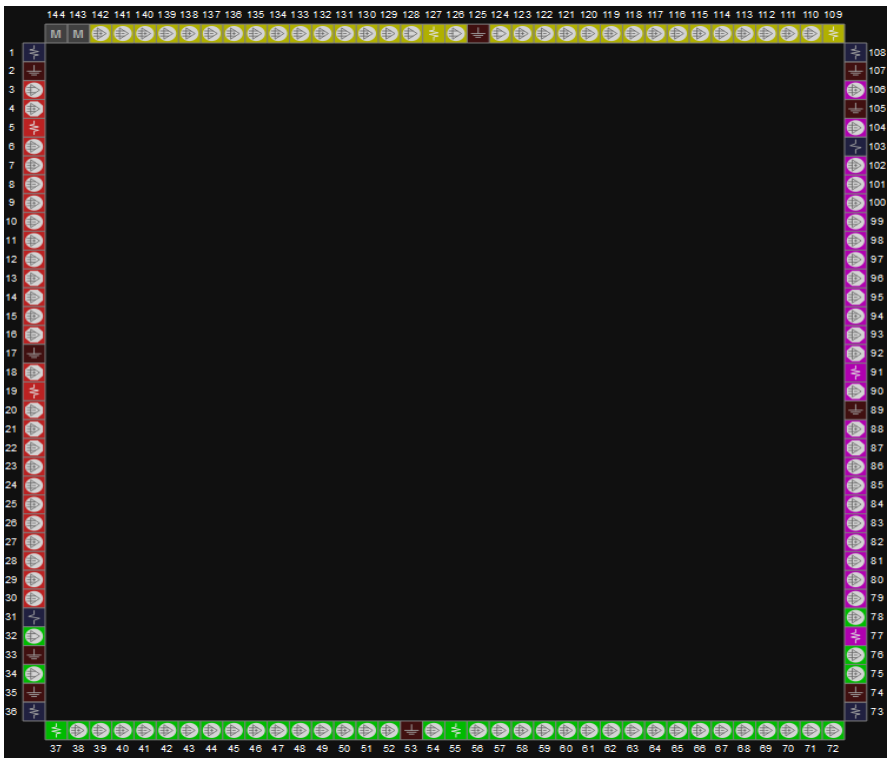


Table 3-2 FPGA I/O Pins Distribution

I/O BANK No.	Modules Connected
I/O BANK0	Pins used for download mode selection GPIO
I/O BANK1	MSPI download GPIO Reset Slide Switches
I/O BANK2	Slide Switches Key Switch GPIO LVDS LED SMA clock input
I/O BANK3	GPIO Interface JTAG download 50MHz clock input

3.2 Download Interface

3.2.1 Overview

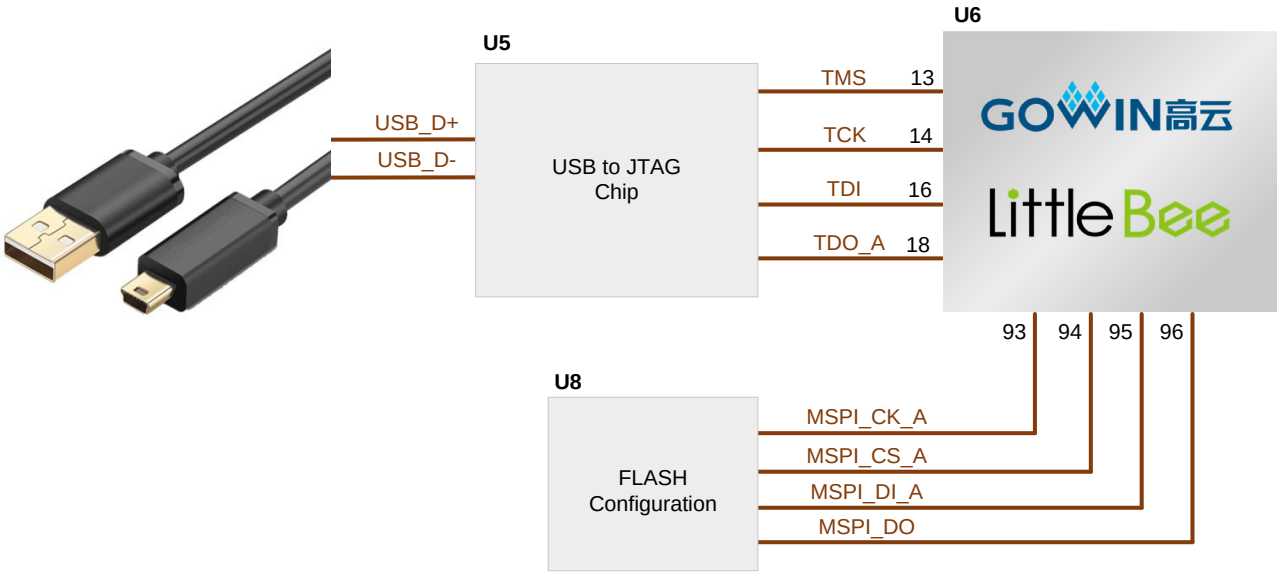
The development board provides an USB download interface. The data stream file can be downloaded to the internal SRAM, internal flash, or external flash as needed.

Note!

- When downloaded to SRAM, the data stream file will be lost if the device is power down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the data stream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure 3-3 Connection Diagram for FPGA USB Downloading and Configuration



3.2.3 Downloading the Data Stream

The data stream file can be downloaded in the following ways:

1. SRAM:

   Scan the device and download the bit file after powering the device on. The Done indicator lights up to denote that the download has been successful.

   Note!

   The mode is independent of the values of MODE0 and MODE1.

2. Internal Flash:

   Power on and download. After downloading the data stream file

successfully, power down to reset and load the bit file from the internal Flash, and when the Done indicator lights up to denote that the download has been successful.

Note!

Before downloading the bit file and the internal FLASH starts, MODE0 and MODE1 need to set to "00".

3. External Flash Configuration:

Power on and download. Power down to reset and load the bit file from the external flash. The Done indicator lights up to denote that the download has been successful.

Note!

Before downloading the bit file and the external FLASH starts, MODE0 and MODE1 need to set to "01".

3.2.4 Pins Distribution

Table 3-3 FPGA Download and Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
TMS	13	3	JTAG Signal	VCCO3
TCK	14	3	JTAG Signal	VCCO3
TDI	16	3	JTAG Signal	VCCO3
TDO_A	18	3	JTAG Signal	VCCO3
MSPI_CK_A	93	1	FLASH signals configuration	VCCO1
MSPI_CS_A	94	1	FLASH signals configuration	VCCO1
MSPI_DI_A	95	1	FLASH signals configuration	VCCO1
MSPI_DO	96	1	FLASH signals configuration	VCCO1

Note！

The VCCO1 of GW1N-9 can only be supplied with 3.3V.

3.3 Power Supply

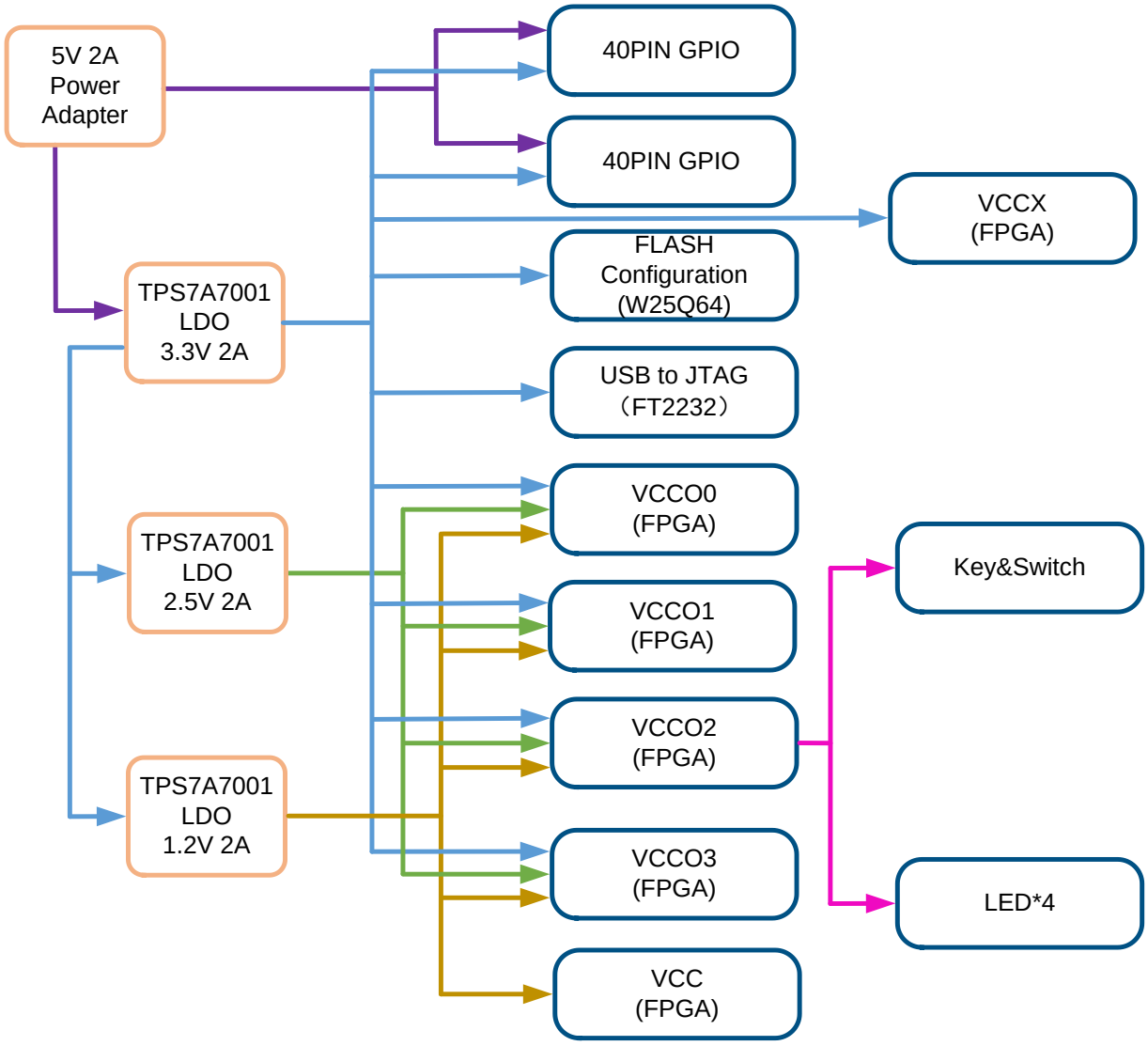
3.3.1 Overview

The DC5V input power interface has overcurrent and inverse current protection. The overcurrent limit is 2A.

The TI LDO power supply chip is used to step down voltage from 5V to 3.3V, 3.3V to 2.5V and 3.3V to 1.2V. The power supply can support up to 2A, which can meet the power demand of the development board.

3.3.2 Power System Distribution

Figure 3-4 Power System Distribution



3.3.3 Power Pins Distribution

Table 3-4 GW1N-9 FPGA Power Pins Distribution

Signal Name	FPGA Pins No.	BANK	Description	I/O Voltage
VCCO0	109,127	0	I/O Bank Voltage	3.3V/2.5V/1.2V
VCCO1	91,103	1	I/O Bank Voltage	3.3V
VCCO2	37,55	2	I/O Bank Voltage	3.3V/2.5V/1.2V
VCCO3	5,19	3	I/O Bank Voltage	3.3V/2.5V/1.2V
VCCX	31,77	-	Auxiliary Voltage	3.3V
VCC	1,36,73,108	-	Core Voltage	1.2V
VSS	2,17,33,35,53,74, 89,105,107	-	GND	-

Note!

The VCCO1 of GW1N-9 can only be supplied with 3.3V.

3.4 Clock, Reset

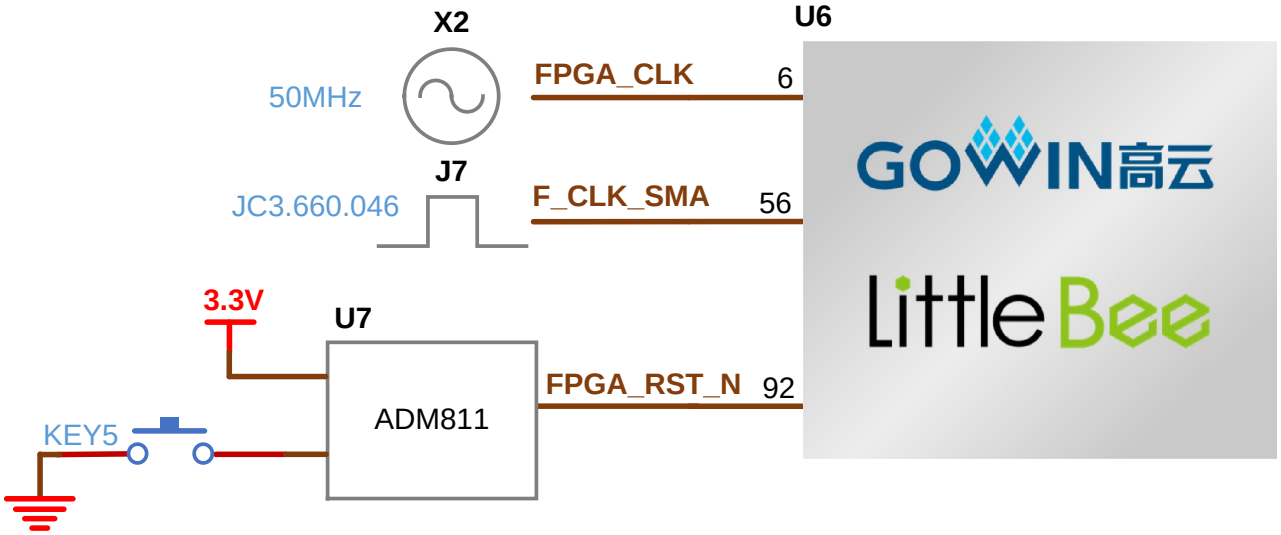
3.4.1 Overview

A 50MHz crystal oscillator is provided in the development board that connects to the PLL input pin. This can be employed as the input clock for the PLL in FPGA, and the output clock as needed via multiplication and division of the PLL frequency.

To facilitate testing, a SMA socket is reserved on the development board as the clock input interface. The clock signal is connected to the FPGA global clock pin.

3.4.2 Clock, Reset

Figure 3-5 Clock, Reset



3.4.3 Pins Distribution

Table 3-5 FPGA Clock and Reset Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
FPGA_CLK	6	3	50MHz crystal oscillator Input	3.3V, 2.5V, 1.2V
F_CLK_SMA	56	2	External clock input	3.3V, 2.5V, 1.2V
FPGA_RST_N	92	1	Reset signal, active low	3.3V, 2.5V

Note!

The VCCO1 of GW1N-9 can only be supplied with 3.3V.

3.5 LED

3.5.1 Overview

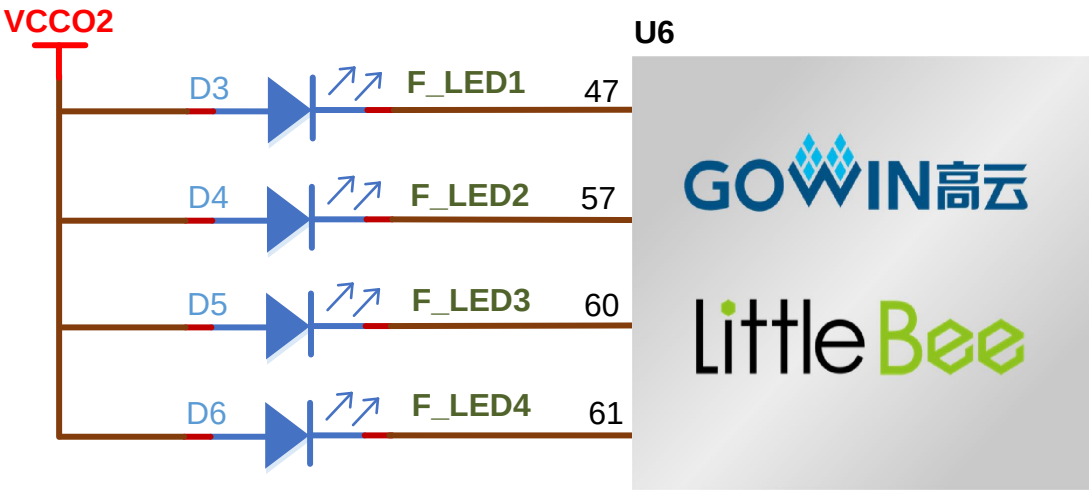
Four green LEDs are incorporated into the development board and are used to display the required status. In addition, two LEDs are reserved to signify power supply and FPGA loading status.

Users can test the LEDs in the following ways:

- If the output signal of related pins is logic low, LED is on;
- If logic is high, LED is off.

3.5.2 LED Circuit

Figure 3-6 LED Circuit



3.5.3 Pins Distribution

Table 3-6 LED Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_LED1	47	2	LED1	3.3V, 2.5V, 1.2V
F_LED2	57	2	LED2	3.3V, 2.5V, 1.2V
F_LED3	60	2	LED3	3.3V, 2.5V, 1.2V
F_LED4	61	2	LED4	3.3V, 2.5V, 1.2V

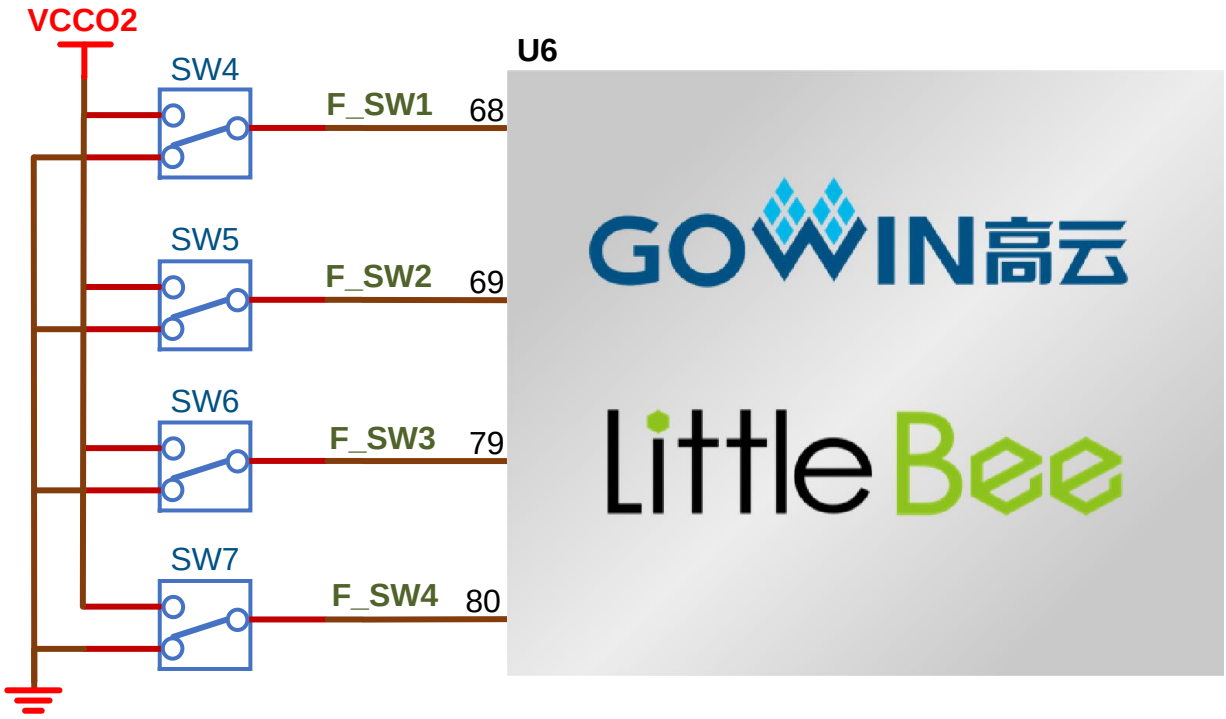
3.6 Switches

3.6.1 Overview

Four slide switches are incorporated into the development board. These are used to control input during testing.

3.6.2 Key Switch Circuit

Figure 3-7 Key Switch Circuit



3.6.3 Pins Distribution

Table 3-7 Clock Circuit Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_SW1	68	2	Slide Switch1	3.3V, 2.5V, 1.2V
F_SW2	69	2	Slide Switch2	3.3V, 2.5V, 1.2V
F_SW3	79	1	Slide Switch3	3.3V, 2.5V
F_SW4	80	1	Slide Switch4	3.3V, 2.5V

Note!

The VCCO1 of GW1N-9 can only be supplied with 3.3V.

3.7 Key

3.7.1 Overview

Four key switches are embedded in the development board. Users can manually input a low level to the corresponding FPGA pins for testing purposes.

3.7.2 Key Circuit

Figure 3-8 Key Circuit Diagram

3.7.3 Pins Distribution

Table 3-8 Key Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_KEY1	43	2	KEY1	3.3V, 2.5V, 1.2V
F_KEY2	44	2	KEY2	3.3V, 2.5V, 1.2V
F_KEY3	45	2	KEY3	3.3V, 2.5V, 1.2V
F_KEY4	46	2	KEY4	3.3V, 2.5V, 1.2V

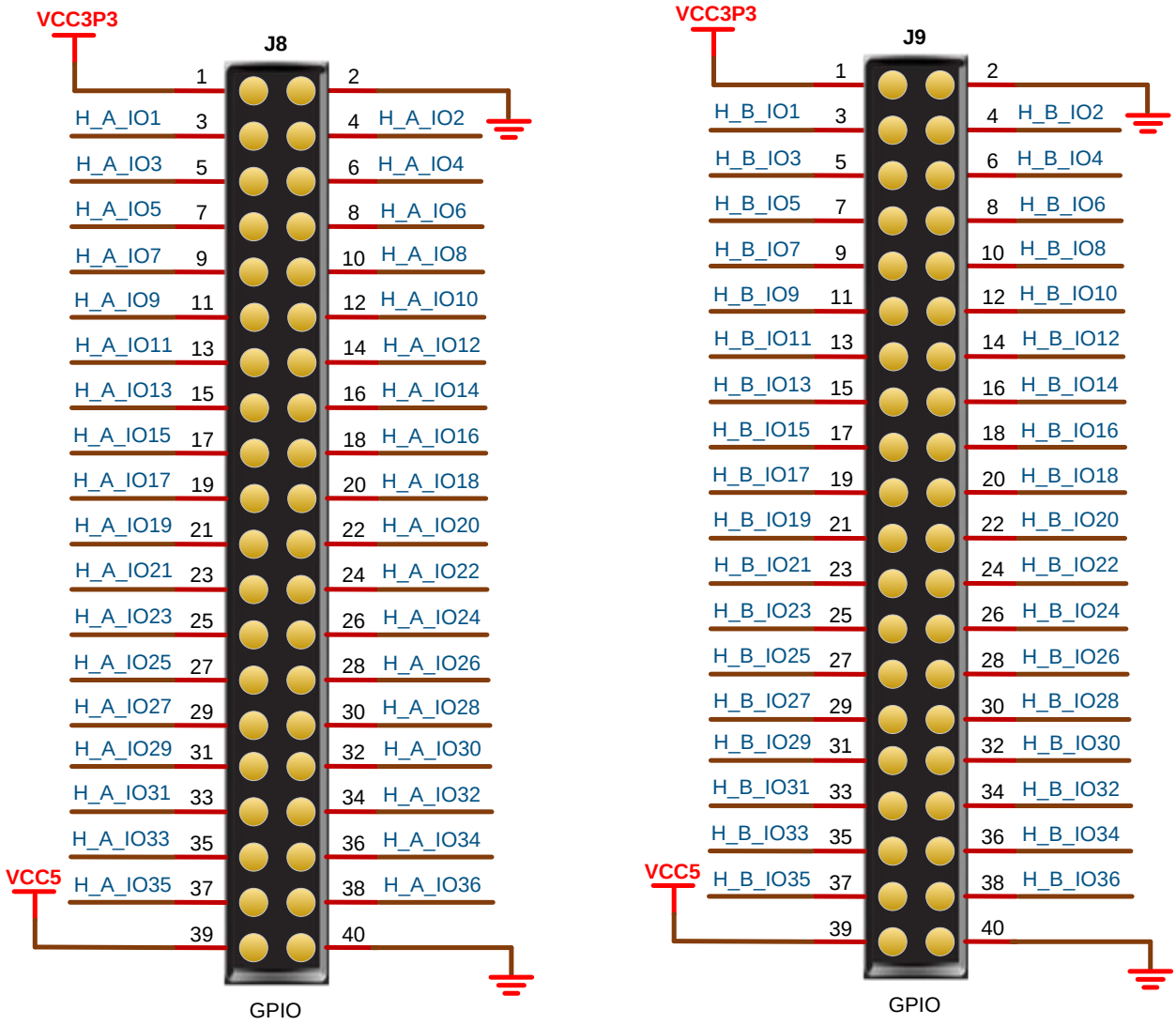
3.8 GPIO

3.8.1 Overview

Two 2.54mm DC3-40P sockets are reserved on the development board for user function extension and testing purposes.

3.8.2 GPIO Circuit

Figure 3-9 GPIO Circuit



3.8.3 Pins Distribution

The distribution of the J8 FPGA and J9 FPGA pins are presented in Table 3-9 and Table 3-10.

Table 3-9 J8 FPGA Pin Distribution

Signal Name	Pin No.	40P Socket Pin No.	BANK	Description	I/O
VCC3P3	-	1	-	-	3.3V
GND	-	2	-	-	-
H_A_IO1	131	3	0	General I/O	VCCO0
H_A_IO2	132	4	0	General I/O	VCCO0
H_A_IO3	133	5	0	General I/O	VCCO0
H_A_IO4	134	6	0	General I/O	VCCO0
H_A_IO5	135	7	0	General I/O	VCCO0
H_A_IO6	136	8	0	General I/O	VCCO0
H_A_IO7	137	9	3	General I/O	VCCO0
H_A_IO8	138	10	3	General I/O	VCCO0
H_A_IO9	139	11	3	General I/O	VCCO0
H_A_IO10	140	12	3	General I/O	VCCO0
H_A_IO11	141	13	3	General I/O	VCCO0
H_A_IO12	142	14	3	General I/O	VCCO0
H_A_IO13	3	15	3	General I/O	VCCO3
H_A_IO14	4	16	3	General I/O	VCCO3
H_A_IO15	7	17	3	General I/O	VCCO3
H_A_IO16	8	18	3	General I/O	VCCO3
H_A_IO17	9	19	3	General I/O	VCCO3
H_A_IO18	10	20	3	General I/O	VCCO3
H_A_IO19	11	21	3	General I/O	VCCO3
H_A_IO20	12	22	3	General I/O	VCCO3
H_A_IO21	15	23	3	General I/O	VCCO3
H_A_IO22	23	24	3	General I/O	VCCO3
H_A_IO23	24	25	3	General I/O	VCCO3
H_A_IO24	25	26	3	General I/O	VCCO3
H_A_IO25	26	27	3	General I/O	VCCO3
H_A_IO26	27	28	3	General I/O	VCCO3
H_A_IO27	28	29	3	General I/O	VCCO3
H_A_IO28	29	30	3	General I/O	VCCO3

Signal Name	Pin No.	40P Socket Pin No.	BANK	Description	I/O
H_A_IO29	30	31	3	General I/O	VCCO3
H_A_IO30	32	32	2	General I/O	VCCO2
H_A_IO31	34	33	2	General I/O	VCCO2
H_A_IO32	38	34	2	General I/O	VCCO2
H_A_IO33	39	35	2	General I/O	VCCO2
H_A_IO34	40	36	2	General I/O	VCCO2
H_A_IO35	41	37	2	General I/O	VCCO2
H_A_IO36	42	38	2	General I/O	VCCO2
VCC5	-	39	-	-	5V
GND	-	40	-	-	-

Table 3-10 J9 FPGA Pin Distribution

Signal Name	Pin No.	40P Socket Pin No.	BANK	Description	I/O
VCC3P3	-	1	-	-	3.3V
GND	-	2	-	-	-
H_B_IO1	130	3	0	General I/O	VCCO0
H_B_IO2	129	4	0	General I/O	VCCO0
H_B_IO3	128	5	0	General I/O	VCCO0
H_B_IO4	126	6	0	General I/O	VCCO0
H_B_IO5	124	7	0	General I/O	VCCO0
H_B_IO6	123	8	0	General I/O	VCCO0
H_B_IO7	122	9	0	General I/O	VCCO0
H_B_IO8	121	10	0	General I/O	VCCO0
H_B_IO9	120	11	0	General I/O	VCCO0
H_B_IO10	119	12	0	General I/O	VCCO0
H_B_IO11	118	13	0	General I/O	VCCO0
H_B_IO12	117	14	0	General I/O	VCCO0
H_B_IO13	116	15	0	General I/O	VCCO0
H_B_IO14	115	16	0	General I/O	VCCO0
H_B_IO15	114	17	0	General I/O	VCCO0
H_B_IO16	113	18	0	General I/O	VCCO0
H_B_IO17	112	19	0	General I/O	VCCO0
H_B_IO18	111	20	0	General I/O	VCCO0
H_B_IO19	110	21	0	General I/O	VCCO0
H_B_IO20	106	22	1	General I/O	VCCO1

Signal Name	Pin No.	40P Socket Pin No.	BANK	Description	I/O
H_B_IO21	104	23	1	General I/O	VCCO1
H_B_IO22	102	24	1	General I/O	VCCO1
H_B_IO23	101	25	1	General I/O	VCCO1
H_B_IO24	100	26	1	General I/O	VCCO1
H_B_IO25	99	27	1	General I/O	VCCO1
H_B_IO26	98	28	1	General I/O	VCCO1
H_B_IO27	97	29	1	General I/O	VCCO1
H_B_IO28	90	30	1	General I/O	VCCO1
H_B_IO29	88	31	1	General I/O	VCCO1
H_B_IO30	87	32	1	General I/O	VCCO1
H_B_IO31	86	33	1	General I/O	VCCO1
H_B_IO32	85	34	1	General I/O	VCCO1
H_B_IO33	84	35	1	General I/O	VCCO1
H_B_IO34	83	36	1	General I/O	VCCO1
H_B_IO35	82	37	1	General I/O	VCCO1
H_B_IO36	81	38	1	General I/O	VCCO1
VCC5	-	39	-	-	5V
GND	-	40	-	-	-

Note!

The VCCO1 of GW1N-9 can only be supplied with 3.3V.

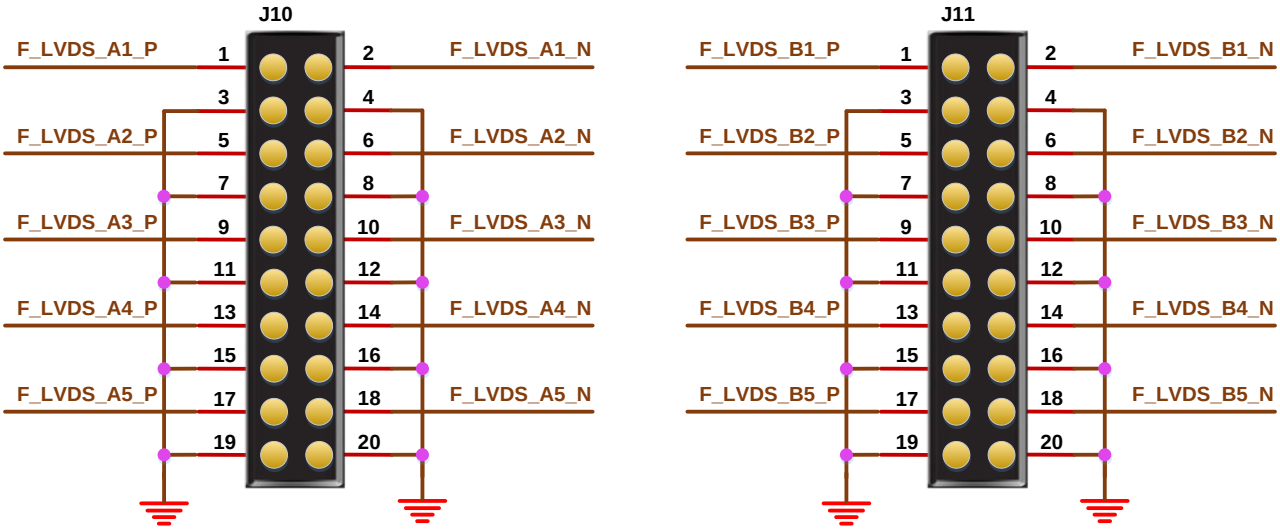
3.9 LVDS

3.9.1 Overview

Two 2 mm DC3-20P sockets are reserved on the development board for LVDS testing and data communication.

3.9.2 LVDS Circuit

Figure 3-10 LVDS Circuit



3.9.3 Pins Distribution

Table 3-11 J10 FPGA Pin Distribution

Signal Name	Pin No.	40P Socket Pin No.	BANK	Description	I/O
F_LVDS_A1_P	48	1	2	Differential Channel 1+	2.5V
F_LVDS_A1_N	49	2	2	Differential Channel 1-	2.5V
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_A2_P	50	5	2	Differential Channel 2+	2.5V
F_LVDS_A2_N	51	6	2	Differential Channel 2-	2.5V
GND	-	7	-	-	
GND	-	8	-	-	
F_LVDS_A3_P	52	9	2	Differential Channel 3+	2.5V
F_LVDS_A3_N	54	10	2	Differential Channel 3-	2.5V
GND	-	11	-	-	
GND	-	12	-	-	
F_LVDS_A4_P	58	13	2	Differential Channel 4+	2.5V
F_LVDS_A4_N	59	14	2	Differential Channel 4-	2.5V
GND	-	15	-	-	
GND	-	16	-	-	
F_LVDS_A5_P	62	17	2	Differential Channel 5+	2.5V
F_LVDS_A5_N	63	18	2	Differential Channel 5-	2.5V
GND	-	19	-	-	
GND	-	20	-	-	

Table 3-12 J10 FPGA Pin Distribution

Signal Name	Pin No.	40P Socket Pin No.	BANK	Description	I/O
F_LVDS_B1_P	64	1	2	Differential Channel 1+	2.5V
F_LVDS_B1_N	65	2	2	Differential Channel 1-	2.5V
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_B2_P	66	5	2	Differential Channel 2+	2.5V
F_LVDS_B2_N	67	6	2	Differential Channel 2-	2.5V
GND	-	7	-	-	-
GND	-	8	-	-	-
F_LVDS_B3_P	70	9	2	Differential Channel 3+	2.5V

Signal Name	Pin No.	40P Socket Pin No.	BANK	Description	I/O
F_LVDS_B3_N	71	10	2	Differential Channel 3-	2.5V
GND	-	11	-	-	-
GND	-	12	-	-	-
F_LVDS_B4_P	72	13	2	Differential Channel 4+	2.5V
F_LVDS_B4_N	75	14	2	Differential Channel 4-	2.5V
GND	-	15	-	-	-
GND	-	16	-	-	-
F_LVDS_B5_P	76	17	2	Differential Channel 5+	2.5V
F_LVDS_B5_N	78	18	2	Differential Channel 5-	2.5V
GND	-	19	-	-	-
GND	-	20	-	-	-

Note!

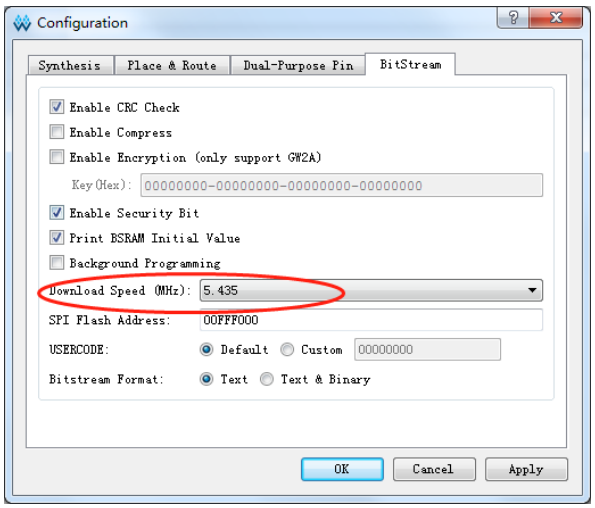
The pin 72 and pin 75 of GW1N-9 are the none-TLVDS differential output pins.

4 Precautions

Precautions to be taken when using the development board:

1. Handle with care and pay attention to electrostatic protection.
   2. When downloading bitstream files to internal flash or external flash, set the MODE pin state to the correct configuration value, please refer to UG290, *Gowin FPGA products Programming and Configuration User Guide* for details;
   3. 100 ohm terminating resistors are welded into the LVDS Port. As the output port, the corresponding terminating resistors are removed in the LVDS interface.
   4. Input DC5V power supply via USB download interface or power socket. Input via the power socket if the SW1 switch is pressed; input via the USB download interface if the SW1 switch pops up.
   5. The value of download speed configured in Project should be no less than 5MHz, as shown in below.

Figure 4-1 LVDS Circuit



6. VCCO of four FPGA Banks can select the voltage between 3.3V, 2.5V, and 1.2V through J3 to J6 pins using jumpers.

GW1N-9

- VCCO1 is 3V, i.e., J5 jumper should be set as 3.3V.
- VCCO0, VCCO2 and VCCO3 can be set as 3.3V, 2.5V and 1.2V using jumpers.

5 Gowin YunYuan Software

Please refer to SUG100, *Gowin YunYuan Software User Guide* for details.