19-6312; Rev 6/12

DS1321
Flexible Nonvolatile Controller with Lithium Battery Monitor

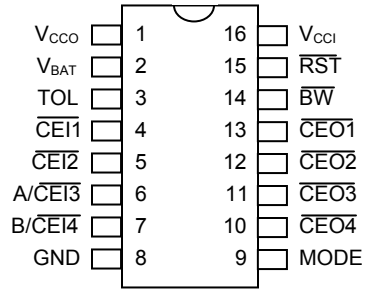
FEATURES

- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects SRAM when V_{CC} is out of tolerance
- Automatically switches to battery backup supply when V_{CC} power failure occurs
- Flexible memory organization
  - Mode 0: 4 banks with 1 SRAM each
  - Mode 1: 2 banks with 2 SRAMs each
  - Mode 2: 1 bank with 4 SRAMs each
- Monitors voltage of a lithium cell and provides advanced warning of impending battery failure
- Signals low-battery condition on active low Battery Warning output signal
- Resets processor when power failure occurs and holds processor in reset during system power-up
- Optional 5% or 10% power-fail detection
- 16-pin PDIP, 16-pin SO and 20-pin TSSOP packages
- Industrial temperature range of -40°C to +85°C

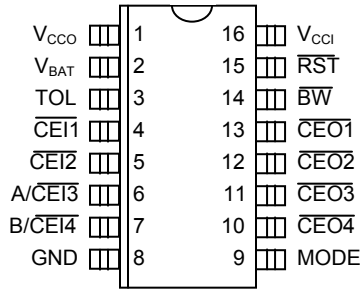
PIN DESCRIPTION

V_{CCI}	- +5V Power Supply Input
V_{CCO}	- SRAM Power Supply Output
V_{BAT}	- Backup Battery Input
A, B	- Address Inputs
$\overline{CEI1}$ - $\overline{CEI4}$	- Chip Enable Inputs
$\overline{CEO1}$ - $\overline{CEO4}$	- Chip Enable Outputs
TOL	- V_{CC} Tolerance Select
$\overline{BW}$	- Battery Warning Output (Open Drain)
$\overline{RST}$	- Reset Output (Open Drain)
MODE	- Mode Input
GND	- Ground
NC	- No Connection

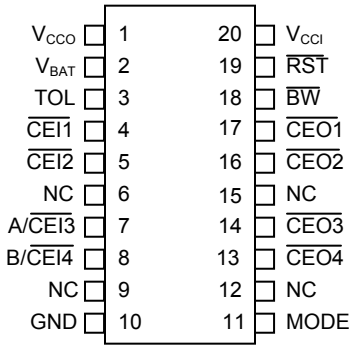
PIN ASSIGNMENT



DS1321 16-Pin PDIP
(300 mils)



DS1321S 16-Pin SO
(150 mils)



DS1321E 20-Pin TSSOP

DESCRIPTION

The DS1321 Flexible Nonvolatile Controller with Lithium Battery Monitor is a CMOS circuit which solves the application problem of converting CMOS SRAMs into nonvolatile memory. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply the SRAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. One DS1321 can support as many as four SRAMs arranged in any of three memory configurations.

In addition to battery-backup support, the DS1321 performs the important function of monitoring the remaining capacity of the lithium battery and providing a warning before the battery reaches end-of-life. Because the open-circuit voltage of a lithium backup battery remains relatively constant over the majority of its life, accurate battery monitoring requires loaded-battery voltage measurement. The DS1321 performs such measurement by periodically comparing the voltage of the battery as it supports an internal resistive load with a carefully selected reference voltage. If the battery voltage falls below the reference voltage under such conditions, the battery will soon reach end-of-life. As a result, the Battery Warning pin is activated to signal the need for battery replacement.

MEMORY BACKUP

The DS1321 performs all the circuit functions required to provide battery-backup for as many as four SRAMs. First, the device provides a switch to direct power from the battery or the system power supply (V_{CCI}). Whenever V_{CCI} is less than the V_{CCTP} trip point and V_{CCI} is less than the battery voltage V_{BAT}, the battery is switched in to provide backup power to the SRAM. This switch has voltage drop of less than 0.2 volts.

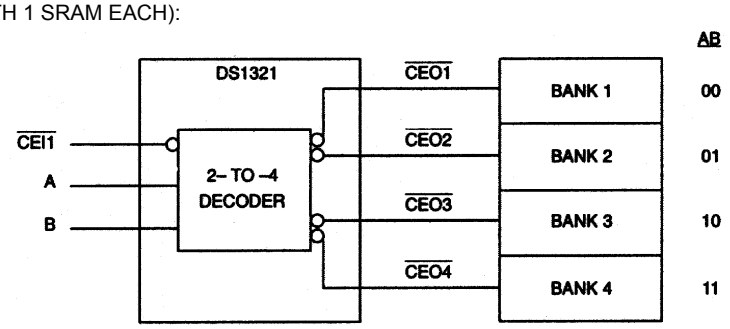
Second, the DS1321 handles power failure detection and SRAM write-protection. V_{CCI} is constantly monitored, and when the supply goes out of tolerance, a precision comparator detects power failure and inhibits the four chip enable outputs in order to write-protect the SRAMs. This is accomplished by holding $\overline{CEO1}$ through $\overline{CEO4}$ to within 0.2 volts of V_{CCO} when V_{CCI} is out of tolerance. If any $\overline{CEI}$ is active (low) at the time that power failure is detected, the corresponding $\overline{CEO}$ signal is kept low until the $\overline{CEI}$ signal is brought high again. Once the $\overline{CEI}$ signal is brought high, the $\overline{CEO}$ signal is taken high and held high until after V_{CCI} has returned to its nominal voltage level. If the $\overline{CEI}$ signal is not brought high by 1.5 µs after power failure is detected, the corresponding $\overline{CEO}$ is forced high at that time. This specific scheme for delaying write protection for up to 1.5 µs guarantees that any memory access in progress when power failure occurs will complete properly. Power failure detection occurs in the range of 4.75 to 4.5 volts (5% tolerance) when the TOL pin is wired to GND or in the range of 4.5 to 4.25 volts (10% tolerance) when TOL is connected to V_{CCO}.

MEMORY CONFIGURATIONS

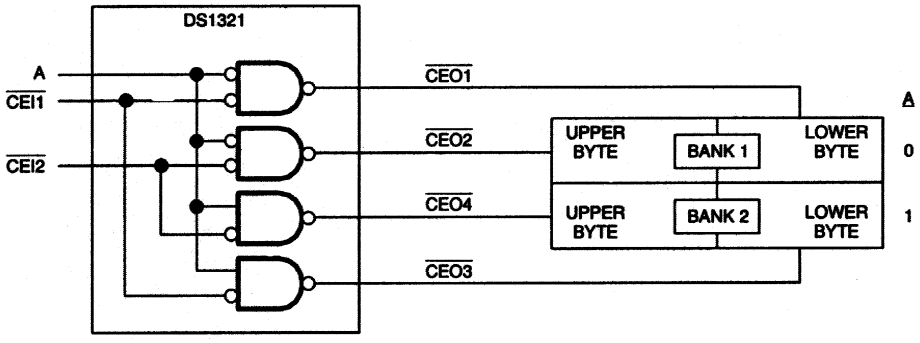
The DS1321 can be configured via the MODE pin for three different arrangements of the four attached SRAMs. The state of the MODE pin is latched at $V_{CCI} = V_{CCTP}$ on power up. See Figure 1 for details.

MEMORY CONFIGURATIONS Figure 1

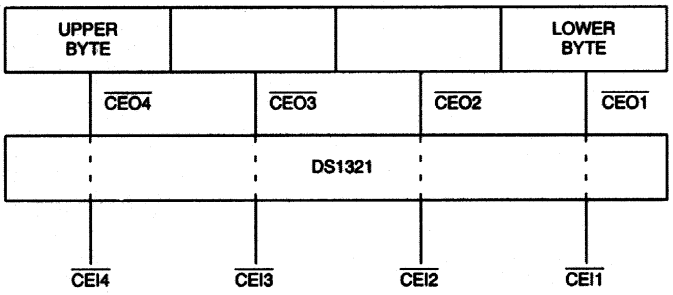
MODE = GND (4 BANKS WITH 1 SRAM EACH):



MODE = V_{CCO} (2 BANKS WITH 2 SRAM EACH):



MODE FLOATING (1 BANK WITH 4 SRAMs):



BATTERY VOLTAGE MONITORING

The DS1321 automatically performs periodic battery voltage monitoring at a factory-programmed time interval of 24 hours. Such monitoring begins within t_{REC} after V_{CCI} rises above V_{CCTP} and is suspended when power failure occurs.

After each 24-hour period (t_{BTCN}) has elapsed, the DS1321 connects V_{BAT} to an internal 1 MΩ test resistor (R_{INT}) for one second (t_{BTPW}). During this one second, if V_{BAT} falls below the factory-programmed battery voltage trip point (V_{BTP}), the battery warning output $\overline{BW}$ is asserted. While $\overline{BW}$ is active, battery testing will be performed with period t_{BTCW} to detect battery removal and replacement. Once asserted, $\overline{BW}$ remains active until the battery is physically removed and replaced by a fresh cell. The battery is still retested after each V_{CC} power-up, however, even if $\overline{BW}$ was active on power-down. If the battery is found to be higher than V_{BTP} during such testing, $\overline{BW}$ is deasserted and regular 24-hour testing resumes. $\overline{BW}$ has an open-drain output driver.

Battery replacement following $\overline{BW}$ activation is normally done with V_{CCI} nominal so that SRAM data is not lost. During battery replacement, the minimum time duration between old battery detachment and new battery attachment (t_{BDBA}) must be met or $\overline{BW}$ will not deactivate following attachment of the new battery. Should $\overline{BW}$ not deactivate for this reason, the new battery can be detached for t_{BDBA} and then re-attached to clear $\overline{BW}$.

NOTE: The DS1321 cannot constantly monitor an attached battery because such monitoring would drastically reduce the life of the battery. As a result, the DS1321 only tests the battery for one second out of every 24 hours and does not monitor the battery in any way between tests. If a good battery (one that has not been previously flagged with $\overline{BW}$) is removed between battery tests, the DS1321 may not immediately sense the removal and may not activate $\overline{BW}$ until the next scheduled battery test. If a battery is then reattached to the DS1321, the battery may not be tested until the next scheduled test.

NOTE: Battery monitoring is only a useful technique when testing can be done regularly over the entire life of a lithium battery. Because the DS1321 only performs battery monitoring when V_{CC} is nominal, systems which are powered-down for excessively long periods can completely drain their lithium cells without receiving any advanced warning. To prevent such an occurrence, systems using the DS1321 battery monitoring feature should be powered-up periodically (at least once every few months) in order to perform battery testing. Furthermore, anytime $\overline{BW}$ is activated on the first battery test after a power-up, data integrity should be checked via checksum or other technique.

POWER MONITORING

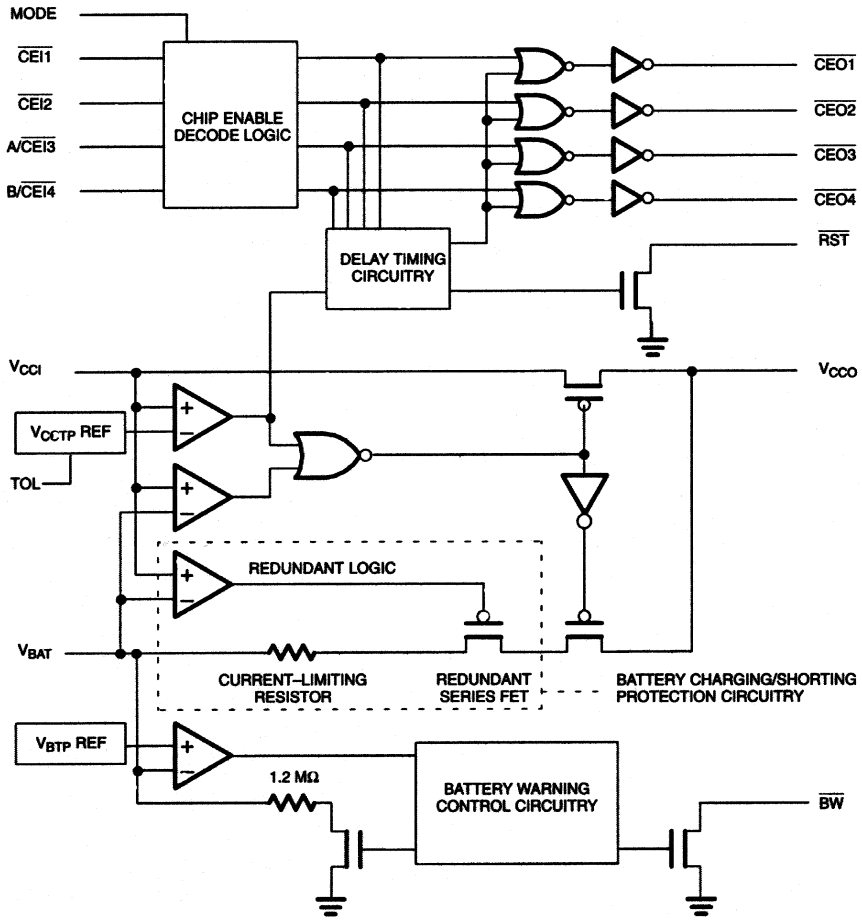
The DS1321 automatically detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CCI} falls below the trip point level defined by the TOL pin (V_{CCTP}), the V_{CCI} comparator activates the reset signal $\overline{RST}$. Reset occurs in the range of 4.75 to 4.5 volts (5% tolerance) when the TOL pin is connected to GND or in the range of 4.5 to 4.25 volts (10% tolerance) when TOL is connected to V_{CCO}.

$\overline{RST}$ also serves as a power-on reset during power-up. After V_{CCI} exceeds V_{CCTP}, $\overline{RST}$ will be held active for 200 ms nominal (t_{RPU}). This reset period is sufficiently long to prevent system operation during power-on transients and to allow t_{REC} to expire. $\overline{RST}$ has an open-drain output driver.

FRESHNESS SEAL MODE

When the battery is first attached to the DS1321 without V_{CC} power applied, the device does not immediately provide battery-backup power on V_{CCO}. Only after V_{CCI} exceeds V_{CCTP} will the DS1321 leave Freshness Seal Mode. This mode allows a battery to be attached during manufacturing but not used until after the system has been activated for the first time. As a result, no battery energy is drained during storage and shipping.

FUNCTIONAL BLOCK DIAGRAM Figure 2



ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature (reflow, SO or TSSOP)	+260°C
Lead Temperature (soldering, 10s)	+300°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

PDIP

Junction-to-Ambient Thermal Resistance (θ_{JA})……...…….....95°C/W

Junction-to-Case Thermal Resistance (θ_{JC})……35°C/W

SO

Junction-to-Ambient Thermal Resistance (θ_{JA})……...…….....75°C/W

Junction-to-Case Thermal Resistance (θ_{JC})……24°C/W

TSSOP

Junction-to-Ambient Thermal Resistance (θ_{JA})……..73.8°C/W

Junction-to-Case Thermal Resistance (θ_{JC})……20°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board for the SMT packages. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

RECOMMENDED OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage TOL=GND	V_{CCI}	4.75	5.0	5.5	V	2
Supply Voltage TOL=V_{CCO}	V_{CCI}	4.5	5.0	5.5	V	2
Battery Supply Voltage	V_{BAT}	2.0	3.0	6.0	V	2
Logic 1 Input	V_{IH}	2.0		V_{CCI}+0.3	V	2. 13
Logic 0 Input	V_{IL}	-0.3		+0.8	V	2, 13

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; $V_{CCI} \geq V_{CCTP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current (TTL inputs)	I_{CC1}		1	1.5	mA	3
Operating Current (CMOS inputs)	I_{CC2}		100	150	µA	3, 6
RAM Supply Voltage	V_{CCO}	V_{CC1} -0.2			V	2
RAM Supply Current ($V_{CCO} \geq V_{CCI}$ -0.2V)	I_{CCO1}			185	mA	4
Supply Current ($V_{CCO} \geq V_{CCI}$ -0.3V)	I_{CCO2}			260	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.75	V	2
V_{CC} Trip Point (TOL=V_{CCO})	V_{CCTP}	4.25	4.37	4.50	V	2
V_{BAT} Trip Point	V_{BTP}	2.50	2.6	2.70	V	2
Output Current @ 2.2V	I_{OH}	-1			mA	8, 11
Output Current @ 0.4V	I_{OL}			4	mA	8, 11

Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Battery Monitoring Test Load	R_{INT}	0.8	1.2	1.5	MΩ	

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; $V_{CCI} < V_{BAT}$; $V_{CCI} < V_{CCTP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Current	I_{BAT}			100	nA	3
Battery Backup Current	I_{CCO3}			500	µA	7
Supply Voltage	V_{CCO}	V_{BAT}-0.2			V	2
$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	2, 9

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance ($\overline{CEI}$*, TOL, MODE)	C_{IN}			7	pF	
Output Capacitance ($\overline{CEO}$*, $\overline{BW}$, $\overline{RST}$)	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; $V_{CCI} \geq V_{CCTP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEI}$ to $\overline{CEO}$ Propagation Delay	t_{PD}		12	20	ns	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	12
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	10
V_{CC} Valid to $\overline{CEI}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to $\overline{RST}$ Inactive	t_{RPU}	150	200	350	ms	11
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	11

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; $V_{CCI} < V_{CCTP}$)

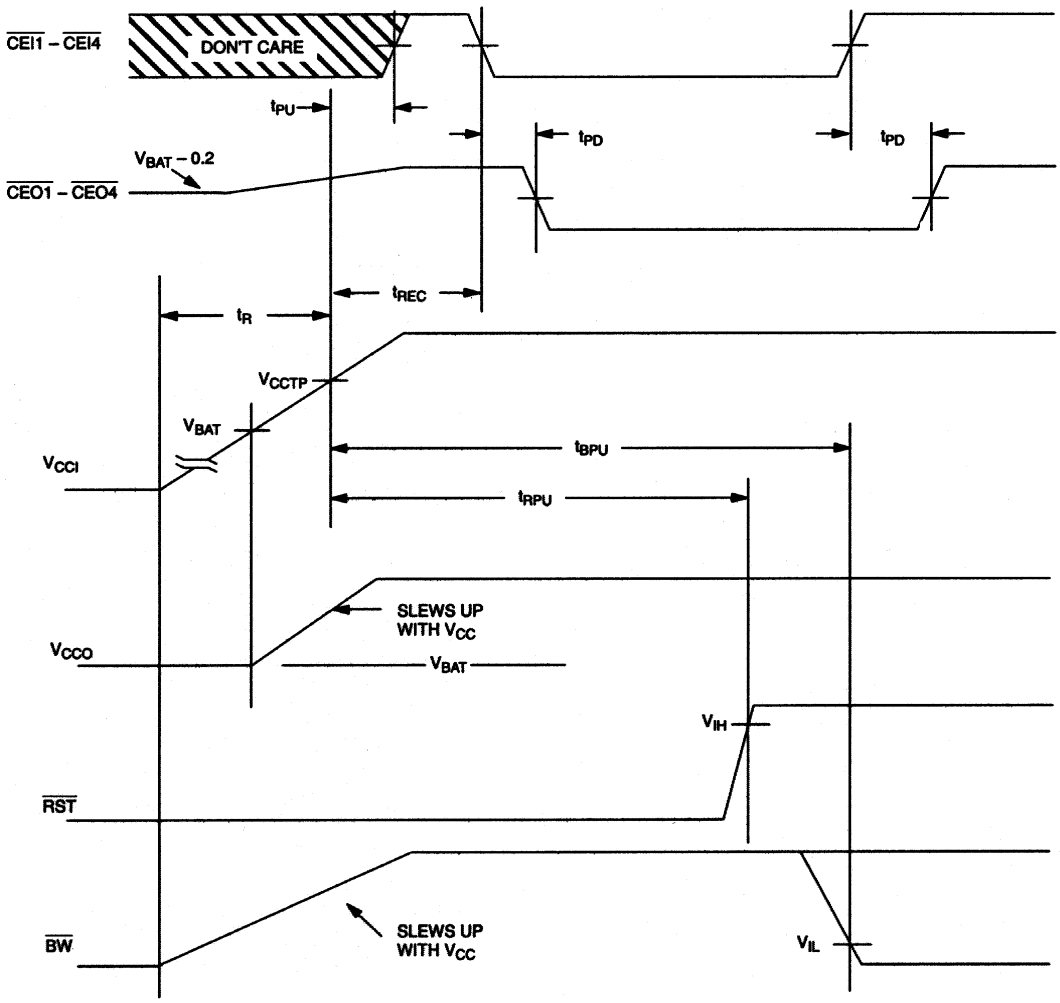
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Slew Rate	t_F	150			µs	
V_{CC} Fail Detect to $\overline{RST}$ Active	t_{RPD}			15	µs	11
V_{CC} Slew Rate	t_R	15			µs	

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; $V_{CCI} \geq V_{CCTP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test to $\overline{BW}$ Active	t_{BW}			1	s	11
Battery Test Cycle-Normal	t_{BTCN}		24		hr	
Battery Test Cycle-Warning	t_{BTCW}		5		s	
Battery Test Pulse Width	t_{BTPW}			1	s	
Battery Detach to Battery Attach	t_{BDBA}	7			s	
Battery Attach to $\overline{BW}$ Inactive	t_{BABW}			1	s	11

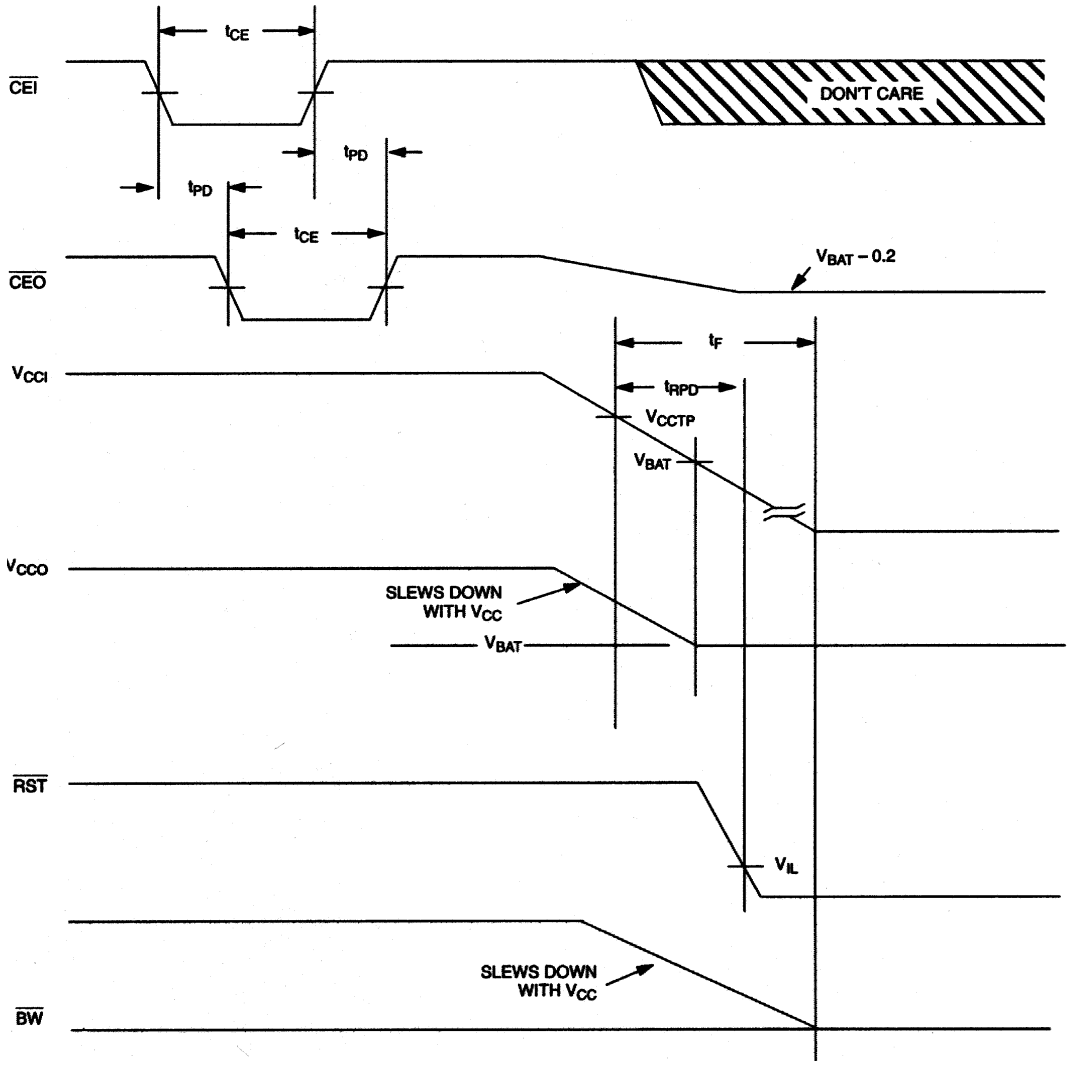
TIMING DIAGRAM: POWER-UP



NOTE:

If $V_{BAT} > V_{CCTP}$, V_{CCO} will begin to slew with V_{CCI} when $V_{CCI} = V_{CCTP}$.

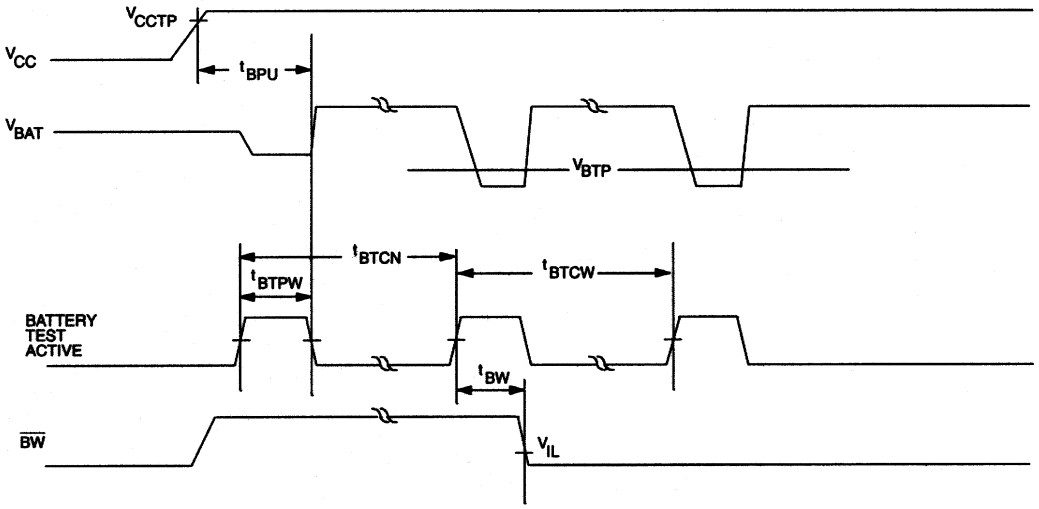
TIMING DIAGRAM: POWER-DOWN



NOTES:

If $V_{BAT} > V_{CCTP}$, V_{CCO} will slew down with V_{CCI} until $V_{CCI} = V_{CCTP}$.

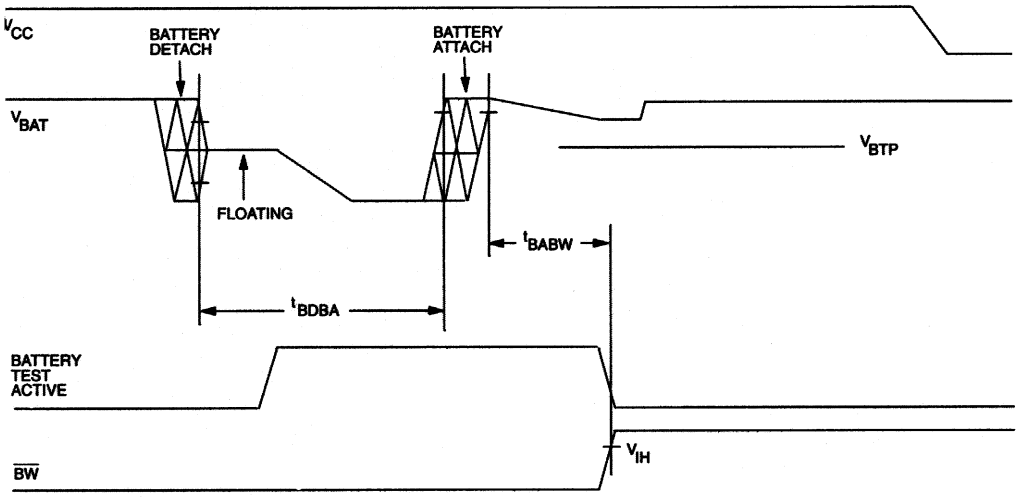
TIMING DIAGRAM: BATTERY WARNING DETECTION



NOTE:

t_{BW} is measured from the expiration of the internal timer to the activation of the battery warning output $\overline{BW}$.

TIMING DIAGRAM: BATTERY REPLACEMENT



NOTES:

2. All voltages referenced to ground.

3. Measured with outputs open circuited.

4. I_{CCO1} is the maximum average load which the DS1321 can supply to attached memories at $V_{CCO} \geq V_{CCI}$ -0.2V.

5. I_{CCO2} is the maximum average load which the DS1321 can supply to attached memories at $V_{CCO} \geq V_{CCI}$ -0.3V.

6. All inputs within 0.3V of ground or V_{CCI}.

7. I_{CCO3} is the maximum average load current which the DS1321 can supply to the memories in the battery backup mode at $V_{CCO} \geq V_{BAT}$ -0.2V.

8. Measured with a load as shown in Figure 1.

9. Chip Enable Outputs $\overline{CEO1}$ - $\overline{CEO4}$ can only sustain leakage current in the battery backup mode.

10. $\overline{CEO1}$ through $\overline{CEO4}$ will be held high for a time equal to t_{REC} after V_{CCI} crosses V_{CCTP} on power-up.

11. $\overline{BW}$ and $\overline{RST}$ are open drain outputs and, as such, cannot source current. External pullup resistors should be connected to these pins for proper operation. Both $\overline{BW}$ and $\overline{RST}$ can sink 10 mA.

12. t_{CE} maximum must be met to ensure data integrity on power down.

13. In battery backup mode, inputs must never be below ground or above V_{CCO}.

14. The DS1321 is recognized by Underwriters Laboratories (UL) under file E99151.

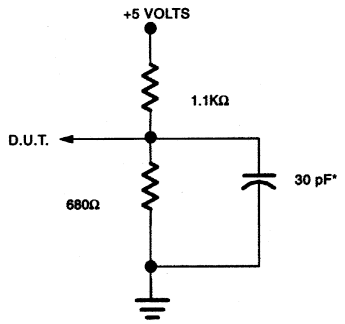
DC TEST CONDITIONS

Outputs Open
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: See below
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

OUTPUT LOAD Figure 3



*INCLUDING SCOPE AND JIG CAPACITANCE

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS1321+	-40°C to +85°C	16 PDIP
DS1321S+	-40°C to +85°C	16 SO
DS1321E+	-40°C to +85°C	20 TSSOP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 PDIP	P16+1	**21-0043**	—
16 SO	S16+1	**21-0041**	**90-0097**
20 TSSOP	U20+1	**21-0066**	**90-0116**