DS1806
Digital Sextet Potentiometer

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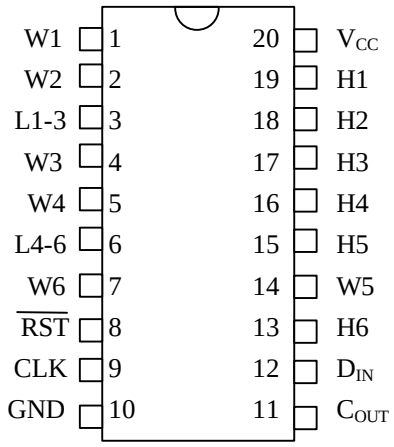
FEATURES

- Six digitally controlled 64-position potentiometers
- 3-wire serial port provides for reading and setting each potentiometer
- Devices can be cascaded for single processor multi-device control
- Standard resistance values:
  - DS1806-010 10 kΩ
  - DS1806-050 50 kΩ
  - DS1806-100 100 kΩ
- Operating Temperature Range:
  - Industrial temperature: -40°C to +85°C

PIN ASSIGNMENT



DS1806 20-Pin DIP (300-mil)
DS1806S 20-Pin SOIC (300-mil)
DS1806E 20-Pin TSSOP (173-mil)
See Mech. Drawings Section

PIN DESCIPTION

V_{CC}	-	3V or 5V Supply
$\overline{RST}$	-	Serial Port Reset Input
D_{IN}	-	Serial Port Data Input
CLK	-	Serial Port Clock Input
C_{OUT}	-	Cascade Data Output
H1 - H6	-	High End terminal of Pot
W1 - W6	-	Wiper Terminal of Pot
GND	-	Ground
L1-3	-	Low Terminal Pots 1 through 3
L4-6	-	Low Terminal Pots 4 through 6

DESCRIPTION

The DS1806 Digital Sextet Potentiometer is a six-channel, digitally controlled, solid-state linear potentiometer. Each potentiometer is comprised of 63 equiresistive sections as illustrated in the block diagram of Figure 1. Each potentiometer has three terminals accessible to the user. These include the high side terminals, H_X, the wiper terminals, W_X, and the low-end terminals, L1-3 and L4-6. Potentiometers 1 through 3 share the same low-end terminal L1-3; likewise, potentiometers 4 through 6 share the low-end terminal L4-6.

Each wiper's position is selected via an 8-bit register value. Communication and control of the device is accomplished via a 3-wire serial port interface. This interface in conjunction with a cascade output allows the value of the device wiper settings to be read.

For multiple device and single processor environments, the DS1806 can be cascaded or daisy-chained. This feature allows a single processor to control multiple devices.

The DS1806 is available in 10, 50 and 100-kohm versions and is specified over the industrial temperature range. Packages for the device include 20-lead DIPs, SOICs, and TSSOPs.

OPERATION

A block diagram of the device is provided in Figure 1. As shown, the DS1806 contains six 64-position potentiometers whose wiper positions are set by an 8-bit value. The DS1806 contains a 48-bit I/O shift register which is used to store the respective wiper position data for each of the six potentiometers.

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Control of the DS1806 is accomplished via a 3-wire serial communication interface which allows the user to set the wiper position value for each potentiometer. The 3-wire serial interface consists of the control signals $\overline{RST}$, D_{IN}, and CLK. On power-up, the wiper positions of each potentiometer are set to the low-end terminal L_X (00000000).

The $\overline{RST}$ control signal is used to enable 3-wire serial port operation. The $\overline{RST}$ signal (3-wire serial port) is active when in a high state. Any communication intended to change wiper settings must begin with the transition of the $\overline{RST}$ from the low state to the high state.

The CLK signal input is used to provide timing synchronization for data input and output. Wiper position data is loaded into the DS1806 through the D_{IN} input terminal. This data is shifted one bit at a time into the 48-bit I/O shift register of the part, LSB first. Figure 3 provides an illustration of the 48-bit shift register.

Figure 4 provides 3-wire serial port protocol and timing diagrams. As shown, the 3-wire port is inactive when the $\overline{RST}$ signal input is low. Once $\overline{RST}$ has transitioned from the low to the high state, the serial port becomes active. When active, data is loaded into the I/O shift register on the low-to-high transition of the CLK.

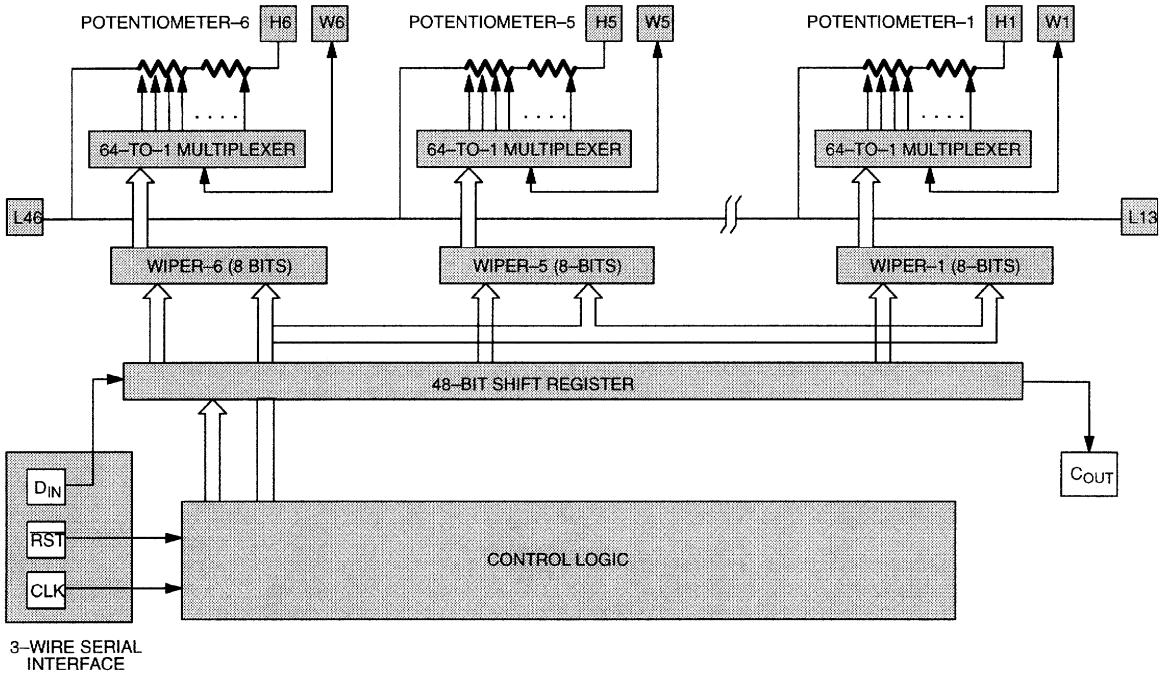
Data is transmitted in order of LSB first. Potentiometers are designated from 1 through 6 and the value for potentiometer-1 will be the first data entered into the shift register, followed by that of potentiometer-2 and so forth.

Each wiper has an 8-bit register which is used for setting the position of the wiper on the resistor array. Because the DS1806 is a 64-position potentiometer, only six bits of information are needed to set wiper position. The remaining two bits of information are used to provide a “don’t change” feature. Wiper position is controlled by bit positions 0 through 5 of each register. The “don’t change” feature is controlled by bits 6 and 7 of each register. When bits 6 and 7 have value “11 xxxxxx,” wiper position will not change regardless of the states of bits 0 through 5. If bits 6 and 7 are set to any other value, bits 0 through 5 will be used as the new wiper position. The “don’t change” feature allows the user to change the value of any potentiometer of the DS1806 without affecting or having to remember the remaining positions of the potentiometer wipers. Figure 2 provides the format for a wiper’s register.

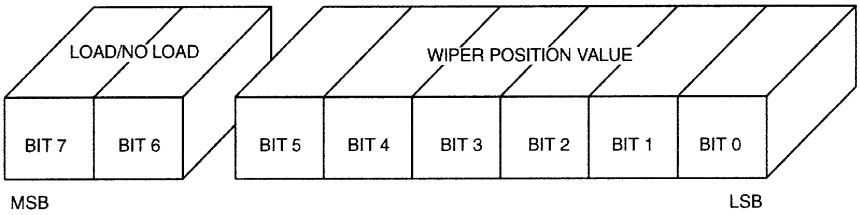
Wiper placement for each potentiometer is such that position-63 corresponds to the H_X terminal of the device while position-0 corresponds to the ground terminal. For example, to set a potentiometer's wiper position to 15 (decimal), the binary value shifted into the wiper register should be 00001111. This will place the wiper tap at the 15th step above the low-end terminal, L_X.

All communication transactions should provide the total 48 bits of information when writing or reading from the part. This is especially true for applications using all six potentiometers. If a complete set of 48 bits is not transmitted to the part, undesired wiper position settings may occur.

DS1806 BLOCK DIAGRAM Figure 1



WIPER REGISTER CONFIGURATION Figure 2



Bits 6 and 7 Functionality

11 – Do not load wiper value
10 – Load wiper value
01 – Load wiper value
00 – Load wiper value

48-BIT I/O SHIFT REGISTER Figure 3

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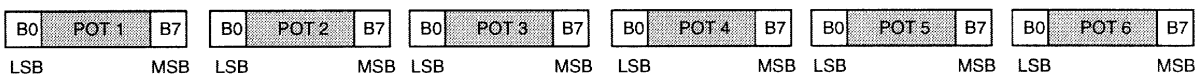
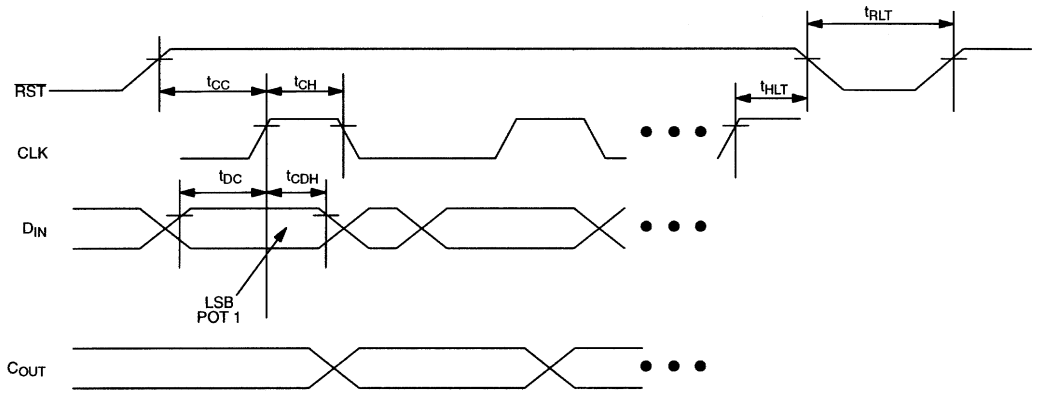


Data entered LSB first, starting with potentiometer–1.

3-WIRE SERIAL PORT TIMING Figure 4



CASCADE OPERATION

A feature of the DS1806 is the ability to control multiple devices from a single processor. Multiple DS1806s can be linked or daisy chained as shown in Figure 5. As a data bit is entered into the I/O shift register of the DS1806, a bit will appear at the C_{OUT} terminal before a maximum delay of 50 nanoseconds. The LSB of potentiometer-1 will always be the first out of the part at the beginning of a transaction. Additionally, the C_{OUT} terminal is always active regardless of the state $\overline{RST}$. However, D_{IN} and CLK inputs are ignored when $\overline{RST}$ is in the low state.

The C_{OUT} output of the DS1806 can be used to drive the D_{IN} input of another DS1806. When cascading multiple devices, the total number of bits transmitted is always 48 multiplied by the total number of DS1806s being cascaded.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1806 D_{IN} input, which allows the controlling processor to read as well as write data or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 1 kΩ to 10 kΩ.

To read data, the reading device configures itself as an input and monitors the state of the D_{IN} line, which is driven by C_{OUT} through the isolation resistor. When $\overline{RST}$ is driven high, bit 48 is present on the C_{OUT} pin, which is fed back to the input D_{IN} pin through the isolation resistor. When the CLK input transitions low to high, bit 48 is loaded into the first position of the I/O shift register and bit 47 becomes present on C_{OUT} and D_{IN} of the next device. After 48 bits (or 48 times the number of the DS1806s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded in the shift register.

ABSOLUTE AND RELATIVE LINEARITY

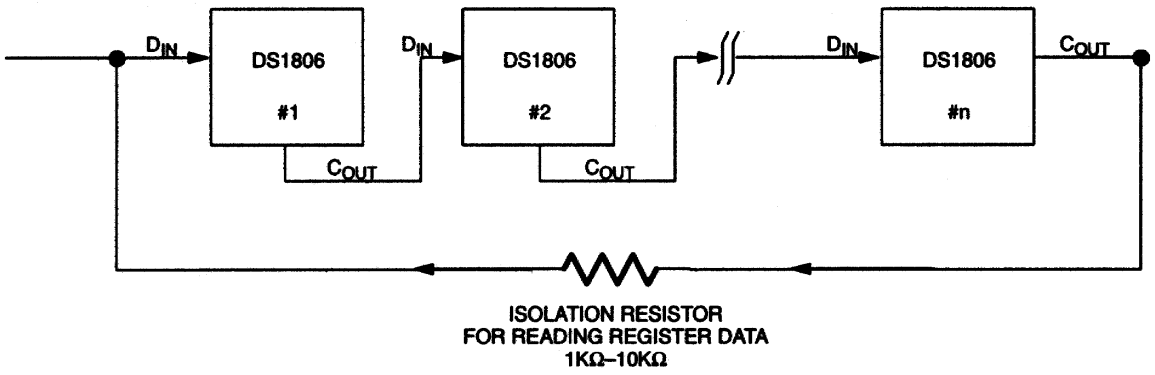
Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. The DS1806 is specified to have an absolute linearity of ±0.50 LSB.

Relative linearity is a measure of error between two adjacent wiper position points. The DS1806 is specified to have a relative linearity of ±0.25 LSB.

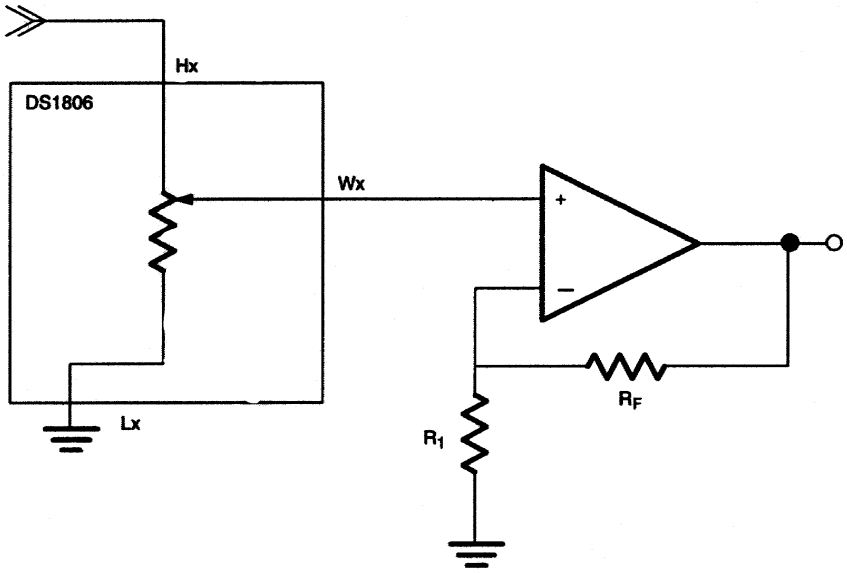
TYPICAL APPLICATION CONFIGURATIONS

Figure 6 shows the typical application configuration of the DS1806 as a fixed gain attenuator. In this configuration, the DS1806 adjusts the attenuation level of the incoming signal. Variations in wiper resistance are minimized by connecting the wiper terminal of the part to a high impedance load. Depending on voltage across the wiper, its resistance may vary from 400 ohms to 1000 ohms. Note that the resistance R1 in Figure 6 should be chosen to be much greater than the wiper resistance R_W.

CASCADING MULTIPLE DEVICES Figure 5



FIXED GAIN ATTENUATOR Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C; industrial
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1

DC ELECTRICAL CONDITIONS (-40°C to +85°C; V_{CC}=2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}		1.3	2	mA	
Input Leakage	I_{IL}	-1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8 +0.6	V	1,6
Logic 1 Output @ 2.4 volts	I_{OH}	-1			mA	
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	6
Standby Current 3 Volts 5 Volts	I_{STBY}		12 20	 40	µA µA	9
Resistor Inputs	H_X, L_X, W_X	GND-0.5		V_{CC}+0.5	µA	2

ANALOG RESISTOR CHARACTERISTICS (-40°C to +85°C;V_{CC}=2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistor Tolerance		-20		+20	%	10
Absolute Linearity		-0.5		+0.5	LSB	7
Relative Linearity		-0.25		+0.25	LSB	8
-3 dB Cutoff Frequency	I_{CUTOFF}				Hz	4
Temperature Coefficient			750		ppm/°C	

CAPACITANCE (t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C;V_{CC}=2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLK}	DC		10	MHz	5
Width of CLK Pulse	t_{CH}	50			ns	5
Data Setup Time	t_{DC}	30			ns	5
Data Hold Time	t_{CDH}	0			ns	5
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	5
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	5
$\overline{RST}$ Low to Clock Input High	t_{HLT}	50			ns	5
$\overline{RST}$ Inactive	t_{RLT}	125			ns	5
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	5

NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot go below GND by more than 0.5 volts or above V_{CC} by 0.5 volts in the positive direction.
3. Capacitance values apply at 25°C.