19-4539; Rev 1; 2/12

Fast Sample-and-Hold Circuit

General Description

The DS1843 is a sample-and-hold circuit useful for capturing fast signals where board space is constrained. It includes a differential, high-speed switched capacitor input sample stage, offset nulling circuitry, and an output buffer. The DS1843 is optimized for use in optical line transmission (OLT) systems for burst-mode RSSI measurement in conjunction with an external sense resistor.

Features

- **Fast Sample Time < 300ns**
- **Hold Time > 100µs**
- **Low Input Offset**
- **Buffered Output**
- **Small, 8-Pin µDFN (2mm x 2mm) Pb-Free Package**

Applications

Gigabit Passive Optical Network (GPON) OLT

Gigabit Ethernet Passive Optical Network (GEPON) OLT

GPON Optical Network Unit

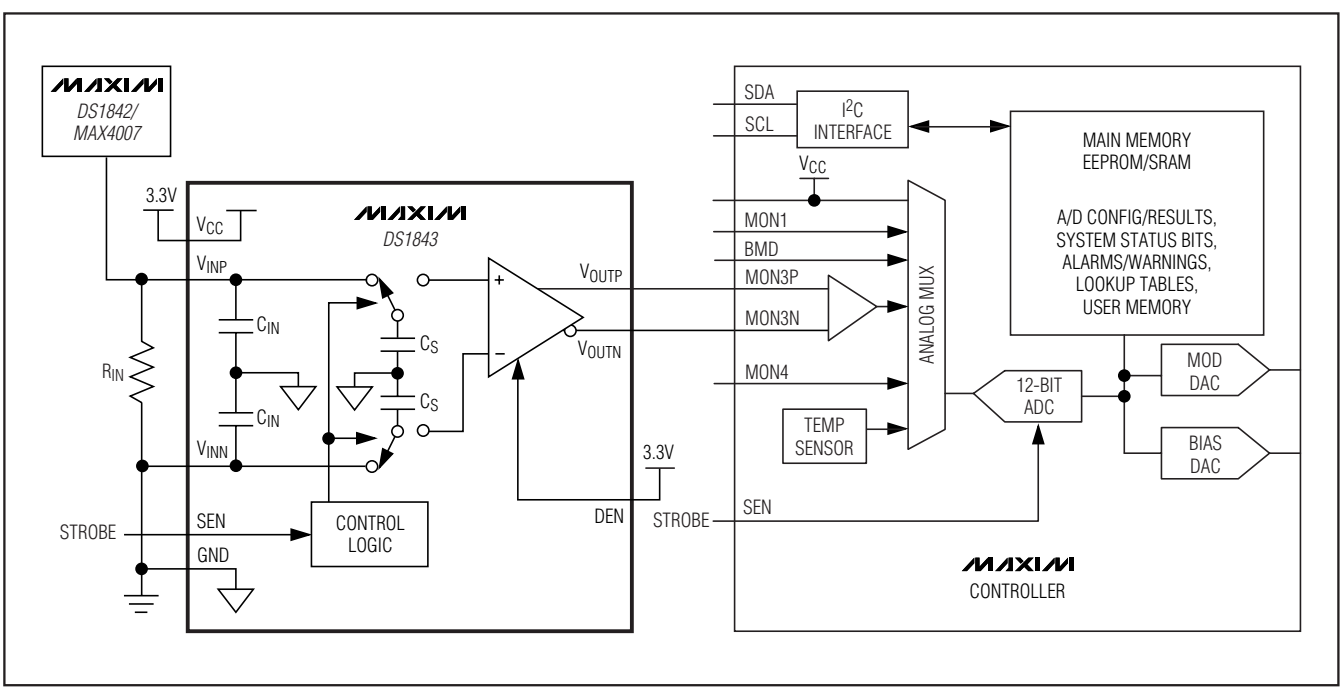
Sample and Hold

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1843D+	-40°C to +85°C	8 µDFN
DS1843D+TRL	-40°C to +85°C	8 µDFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
TRL = Tape and reel.

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

Fast Sample-and-Hold Circuit

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} .....-0.5V to +6V
Voltage Range on V_{OUTP}, V_{OUTN}, V_{INP}, V_{INN}, SEN, DEN .....-0.5V to (V_{CC} + 0.5V)*
Continuous Power Dissipation (T_A = +70°C)
µDFN (derate 4.8mW/°C above +70°C).....380.6mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**Subject to not exceeding +6V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.97		+5.5	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 1)		5.7	9	mA
Input Capacitance	C_{IN}	All pins (Note 2)			7	pF
Sample Capacitance	C_S	V_{INN} and V_{INP} (Note 2)		5		pF
Logic-Input Low	V_{IL}	SEN and DEN inputs			0.3 x V_{CC}	V
Logic-Input High	V_{IH}	SEN and DEN inputs	0.7 x V_{CC}			V
Input Leakage	I_{IN}	V_{INN} or V_{INP}, SEN = 0			1	µA
Input Voltage	V_{IN}	V_{IN} = V_{INP} - V_{INN}	0		1.0	V
Output Voltage	V_{OUT}	V_{OUT} = V_{OUTP} - V_{OUTN}; 100kΩ load on each output pin	0		1.0	V
Output Impedance	R_{OUTMAX}	(Note 2)		1	1.3	kΩ
Output Capacitive Load	C_{OUT}	Capacitance for stable operation			50	pF
Total Input Referenced Voltage Offset: Differential	$V_{OS-DIFF}$	V_{CC} = 2.9V, 1µs sample time, V_{IN} = 6mV		3.6	6.1	mV
		Voltco (V_{CC} = 2.9V to 5.5V)			1	mV/V
Total Input Referenced Voltage Offset: Single-Ended	V_{OS-SE}	V_{CC} = 2.9V, 1µs sample time, V_{IN} = 6mV		3.4	8	mV
		Voltco (V_{CC} = 2.9V to 5.5V)			1	mV/V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (See the *Timing Diagram*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Time Minimum	t_S	V_{OUT} is within 0.4dB (Note 3)	300			ns
Delay Time Minimum	t_{DEL}	(Note 4)	10			ns
Output Time	t_{OUT}	Delay from SEN falling edge until valid output at V_{OUT} to 1% accuracy			2	µs
Hold Time	t_{HOLD}	(Note 5)	t_{OUT}		100	µs
Output Step Recovery Time (Note 6)	t_{REC}	1V step, DEN = high			2	µs
		3V step, DEN = high or low			3.5	

Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive and currents exiting the IC are negative.

Note 2: Guaranteed by design.

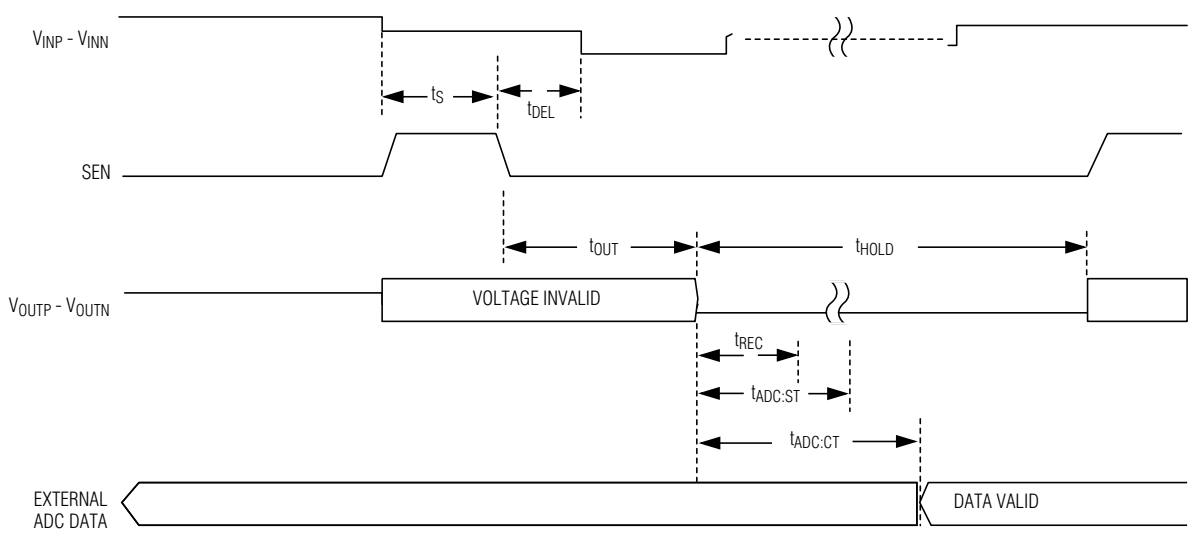
Note 3: V_{OUT} at the end of the 10µs hold time is within specified level of V_{IN} during the sample window; a 50Ω resistor connected in series to both V_{INP} and V_{INN} (V_{INP} - V_{INN} = 1V). External capacitance to ground for both V_{INP} and V_{INN} is approximately 10pF.

Note 4: The sampling capacitor must be removed from the input signal before the input signal changes. Therefore, the SEN pin must be low for a short period of time, t_{DEL}, before the input changes.

Note 5: V_{OUT} at the end of the hold time is within 1% of V_{IN} during the sample window (V_{INP} - V_{INN} = 1V).

Note 6: Voltage step applied across V_{OUTP} to V_{OUTN} through a 5pF capacitor connected to each pin. This models the load presented by an ADC while it is sampling the DS1843's output. See the *Output Buffer* section. Settled within 1% of initial voltage.

Timing Diagram



$t_{ADC:ST}$ = EXTERNAL ADC SAMPLING TIME.

$t_{ADC:CT}$ = EXTERNAL ADC CONVERSION TIME.

DEN IS CONNECTED TO V_{CC} FOR DIFFERENTIAL OUTPUT.

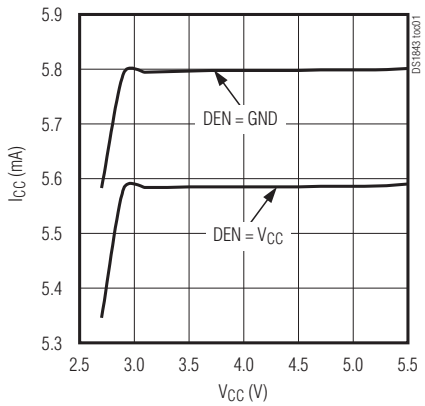
NOTE: THIS TIMING DIAGRAM IS APPLICABLE FOR SINGLE-ENDED AND DIFFERENTIAL OUTPUT CONFIGURATIONS.

Fast Sample-and-Hold Circuit

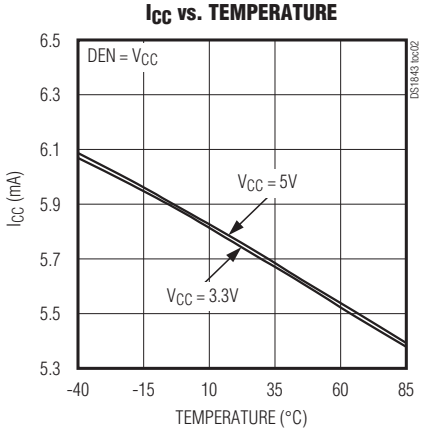
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

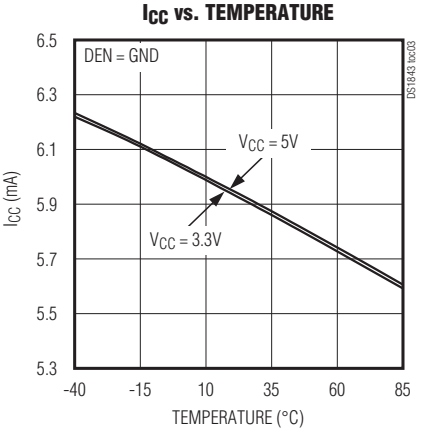
I_{CC} vs. V_{CC}



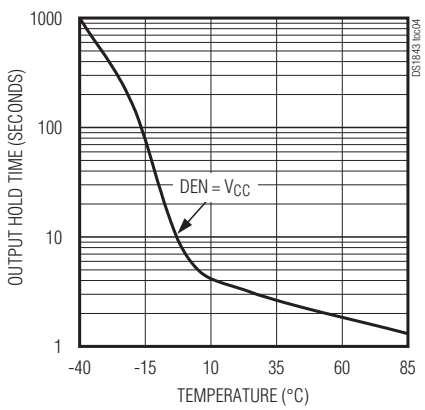
I_{CC} vs. TEMPERATURE



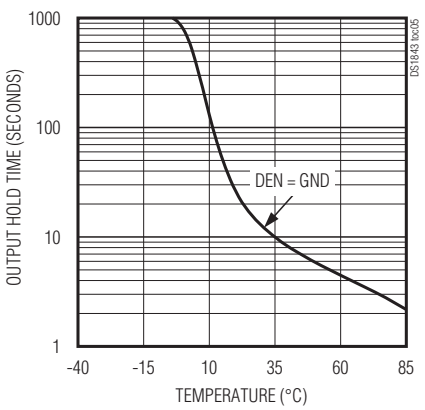
I_{CC} vs. TEMPERATURE



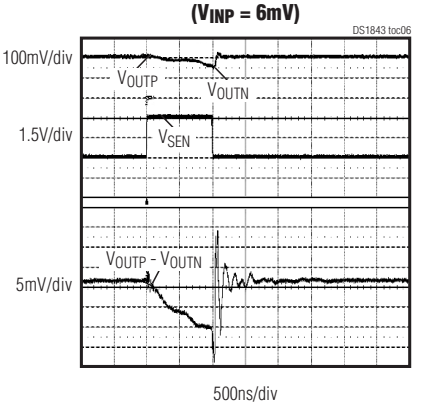
OUTPUT HOLD TIME vs. TEMPERATURE



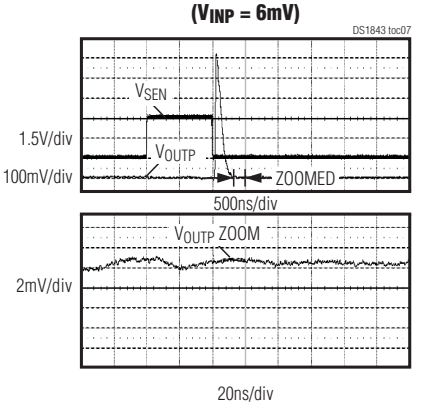
OUTPUT HOLD TIME vs. TEMPERATURE



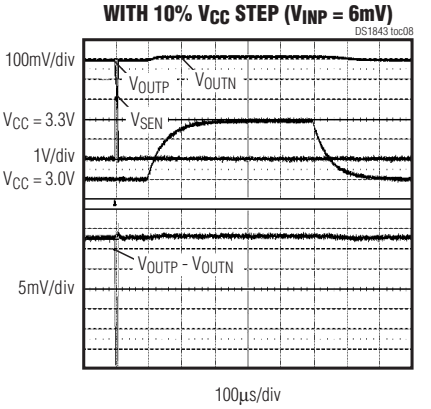
DIFFERENTIAL OUTPUT DURING SAMPLING (V_{INP} = 6mV)



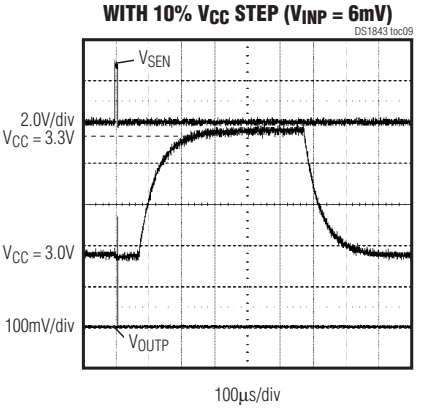
SINGLE-ENDED OUTPUT DURING SAMPLING (V_{INP} = 6mV)



DIFFERENTIAL OUTPUT, TRANSIENT WITH 10% V_{CC} STEP (V_{INP} = 6mV)



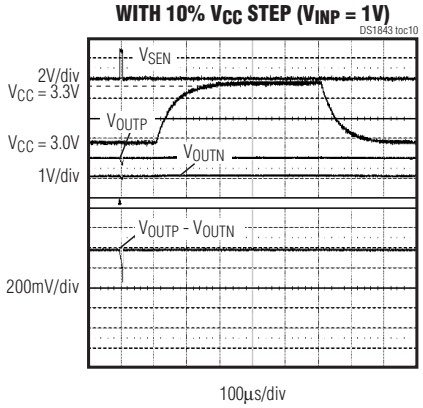
SINGLE-ENDED OUTPUT, TRANSIENT WITH 10% V_{CC} STEP (V_{INP} = 6mV)



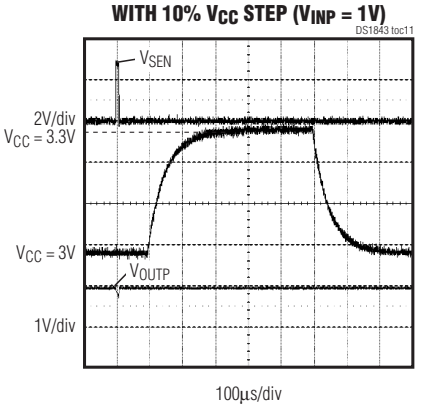
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

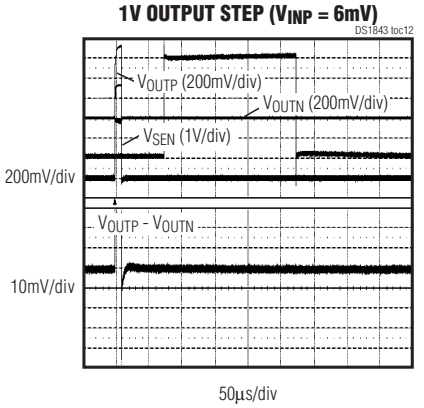
DIFFERENTIAL OUTPUT, TRANSIENT WITH 10% V_{CC} STEP (V_{INP} = 1V)



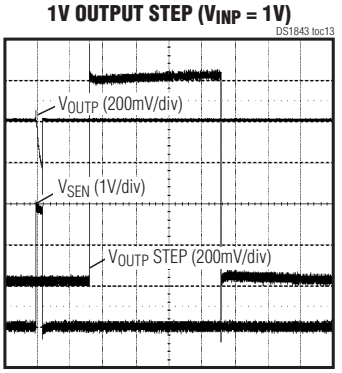
SINGLE-ENDED OUTPUT, TRANSIENT WITH 10% V_{CC} STEP (V_{INP} = 1V)



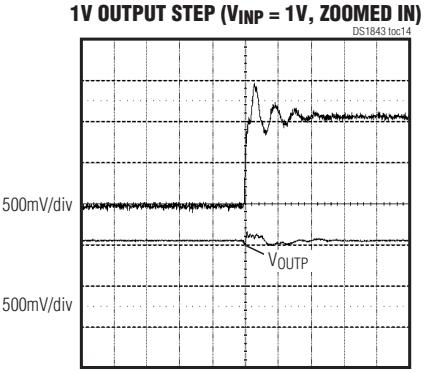
DIFFERENTIAL OUTPUT STEP RECOVERY, 1V OUTPUT STEP (V_{INP} = 6mV)



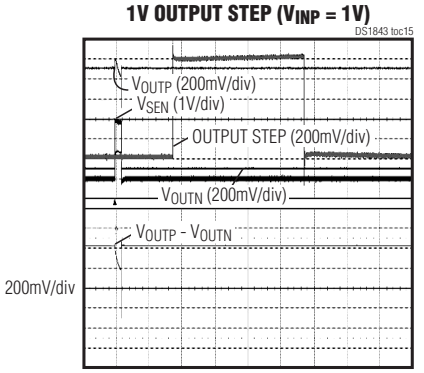
SINGLE-ENDED STEP RECOVERY, 1V OUTPUT STEP (V_{INP} = 1V)



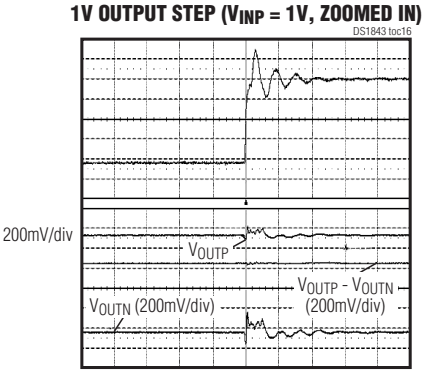
SINGLE-ENDED OUTPUT, STEP RECOVERY, 1V OUTPUT STEP (V_{INP} = 1V, ZOOMED IN)



DIFFERENTIAL OUTPUT STEP RECOVERY, 1V OUTPUT STEP (V_{INP} = 1V)



DIFFERENTIAL OUTPUT STEP RECOVERY, 1V OUTPUT STEP (V_{INP} = 1V, ZOOMED IN)

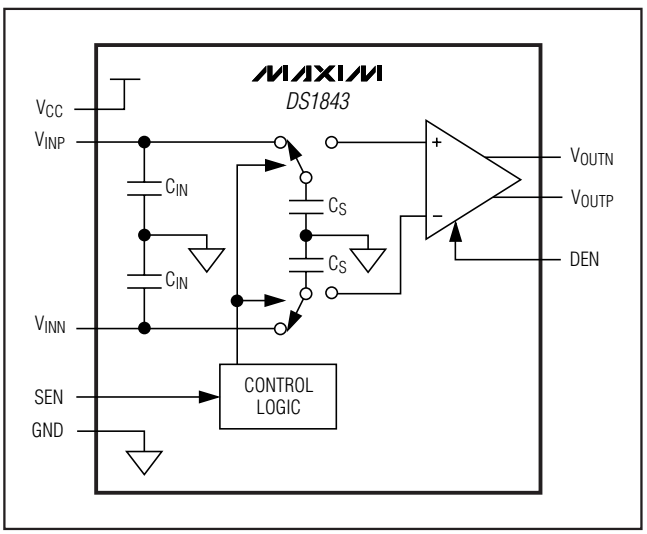


Fast Sample-and-Hold Circuit

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Power-Supply Input
2	V_{INP}	Positive Voltage Input. Input to sample circuit.
3	V_{INN}	Negative Voltage Input. Input to sample circuit.
4	DEN	Differential Output Enable. Connect to V_{CC} for differential output or GND for single-ended output.
5	GND	Ground Terminal
6	V_{OUTN}	Sampled Voltage Negative Output. Buffered output of the hold capacitor. Keep unconnected or connect to GND for single-ended output mode.
7	V_{OUTP}	Sampled Voltage Positive Output and Single-Ended Output. Buffered output of the hold capacitor.
8	SEN	Sample Enable. Enables input sampling. This input is pulsed.

Block Diagram



Detailed Description

The DS1843 consists of a fully differential sampling capacitor, switches, and a differential output buffer. It is designed to operate in fiber optic burst-mode systems; however, it can be used in other applications requiring a fast sample-and-hold circuit. The output can be configured for single-ended operations.

Input Sampling Capacitor

The input voltage is sampled using a 5pF capacitor on the positive input and another on the negative input. The capacitors are connected to the input when SEN is high. In addition to the sampling capacitors, the inputs also have parasitic capacitance (C_{IN}). These capacitors must fully charge before SEN is switched to low in order to ensure accurate sampling. An RC time constant is created by the resistance of the voltage source connected to the DS1843's input and the capacitances on this node. See the *Applications Information* section for details.

Output Buffer

After sampling is complete, the sampling capacitor is switched to the output buffer. This buffer requires a small amount of time to settle, t_{OUT}. When an ADC is used to measure the DS1843's output, a step occurs at the ADC's input caused by the ADC's internal sampling capacitor. The DS1843's recovery time, t_{REC}, is dependent on the size of the ADC's sampling capacitor and the voltage applied across the ADC. To maximize accuracy, the ADC's sampling speed (ADC clock frequency) should be reduced until the ADC's conversion window ($t_{ADC:ST}$, as shown in the *Timing Diagram*) is larger than the DS1843's recovery time. Refer to the ADC's documentation for $t_{ADC:ST}$.

Sampling Time and Output Error

As the sampling time (t_S) is decreased, the output error increases. The output error is largely dependent on the settling time of the sampling capacitor and, to a lesser degree, the output buffer's gain error and offset voltage. Settling time can be reduced by driving the DS1843 with a lower impedance. In a typical fiber optic application, a current is applied across a 5kΩ resistor. By using a stronger current source, the resistance and the settling time can be reduced (see the *Applications Information* section for details).

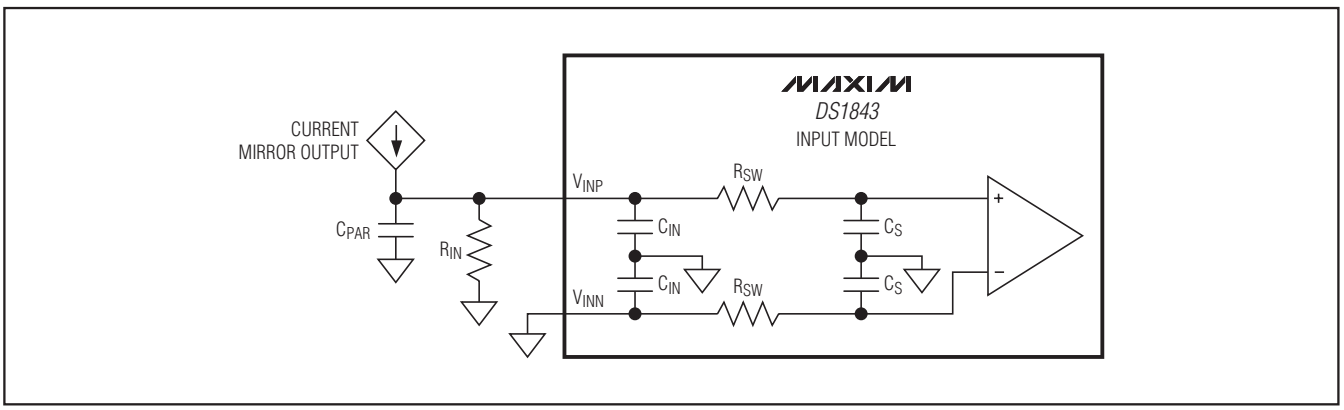


Figure 1. Input Impedances for Settling Time Calculations Diagram

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS1843, decouple the power-supply pin, V_{CC}, with a 0.01µF or 0.1µF capacitor. Use a high-quality X7R or equivalent ceramic surface-mount capacitor.

DS1843 Estimated Settling Time

The settling time is dependent on the gain ratio of the current mirror used at the input of the DS1843. For example, the MAX4007 includes a 10:1 ratio current mirror. This requires a 5kΩ resistor to create a 1V full-scale output with 2mA current input to the MAX4007. This resistor can be decreased to 2.5kΩ by using the DS1842, which has a 5:1 ratio current mirror.

Variable Definitions:

R_{IN}: Input resistor. The current mirror creates a voltage across this resistor.

R_{SW}: Resistance of series switch that connects internal circuitry to input pins after t_{IST} time.

C_{IN}: 7pF parasitic (ESD) capacitor.

C_{PAR}: External parasitic capacitance. A current mirror's output and typical trace capacitance are less than 10pF.

C_S: 5pF sample capacitor.

t_{IST}: Internal settling time based on t_S from the AC electrical specification. The minimum t_S includes one time constant. t_{IST} removes this time constant.

t_{RC}: RC settling time of the input.

Figure 1 shows the simplified diagram of input impedances for settling time calculations. Sample time is divided into two parts:

1) t_{IST}: Internal settling time (max 250ns). During this time, voltage V_{IN} (V_{INP} - V_{INN}) rises with a time constant of:

$$R_{IN} \times (C_{IN} + C_{PAR})$$

2) t_{RC}: During this period two things happen:

   a. Input V_{IN} keeps increasing from its value at t_{IST} to its final value with a new time constant of:

$$\sqrt{\left\{\left(R_{IN} \times \left(C_{IN} + C_{PAR}\right)\right)^2 + \left(R_{SW} \times C_S\right)^2\right\}}$$

   b. R_{SW} and C_S track this V_{IN} (input) with a time constant of R_{SW} x C_S, which is 12.5ns (worst case).

Example:

Approximate accuracy calculations can be done for an input voltage based on the above impedance values. These calculations can be divided into three parts.

1) Accuracy of input at t_{IST} (250ns):

$$\text{Accuracy} = 1 - e^{\frac{-t_1}{\left[R_{IN} \times \left(C_{IN} + C_{PAR}\right)\right]}}$$

   where $t_1 = t_{IST} = 250ns$.

   At t_{IST} the internal circuit tags input impedance. This causes charge redistribution to occur, which causes a dip in the input voltage. The worst-case value of the input voltage at t_{IST} is:

$$V_{IN@t_{IST}} = \left[1 - \frac{C_S}{\left(C_{IN} + C_{PAR} + C_S\right)}\right] \times \left[1 - e^{\frac{-t_{IST}}{\left[R_{IN} \times \left(C_{IN} + C_{PAR}\right)\right]}}\right] \times V_{IN}$$