DS1845
Dual NV Potentiometer and Memory

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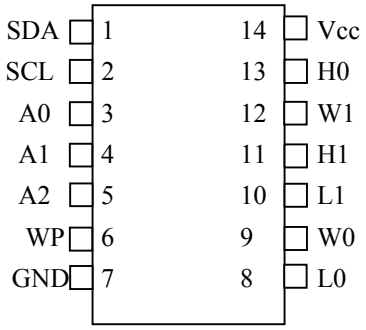
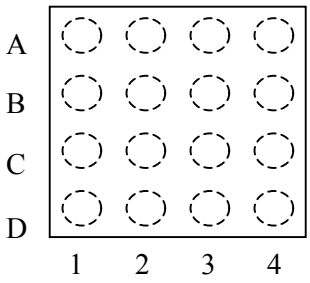
FEATURES

- Two linear taper potentiometers
  - DS1845-010 one 10k, 100 position & one 10k, 256 position
  - DS1845-050 one 10k, 100 position & one 50k, 256 postition
  - DS1845-100 one 10k, 100 position & one 100k, 256 position
- 256 bytes of EEPROM memory
- Access to data and potentiometer control via an I^2C compatible 2-wire interface
- External Write Enable pin to protect data and potentiometer settings
- Nonvolatile wiper storage
- Operates from 3V or 5V supplies
- Packaging: Flip Chip Package, 16-ball CSBGA, 14-pin TSSOP
- Industrial operating temperature: -40ºC to +85ºC



14-Pin TSSOP (173 mil)

Top View



16-Ball CSBGA (4mm x 4mm)

14-Pin Flip Chip (100-mil x 100-mil) (*Not Shown)*

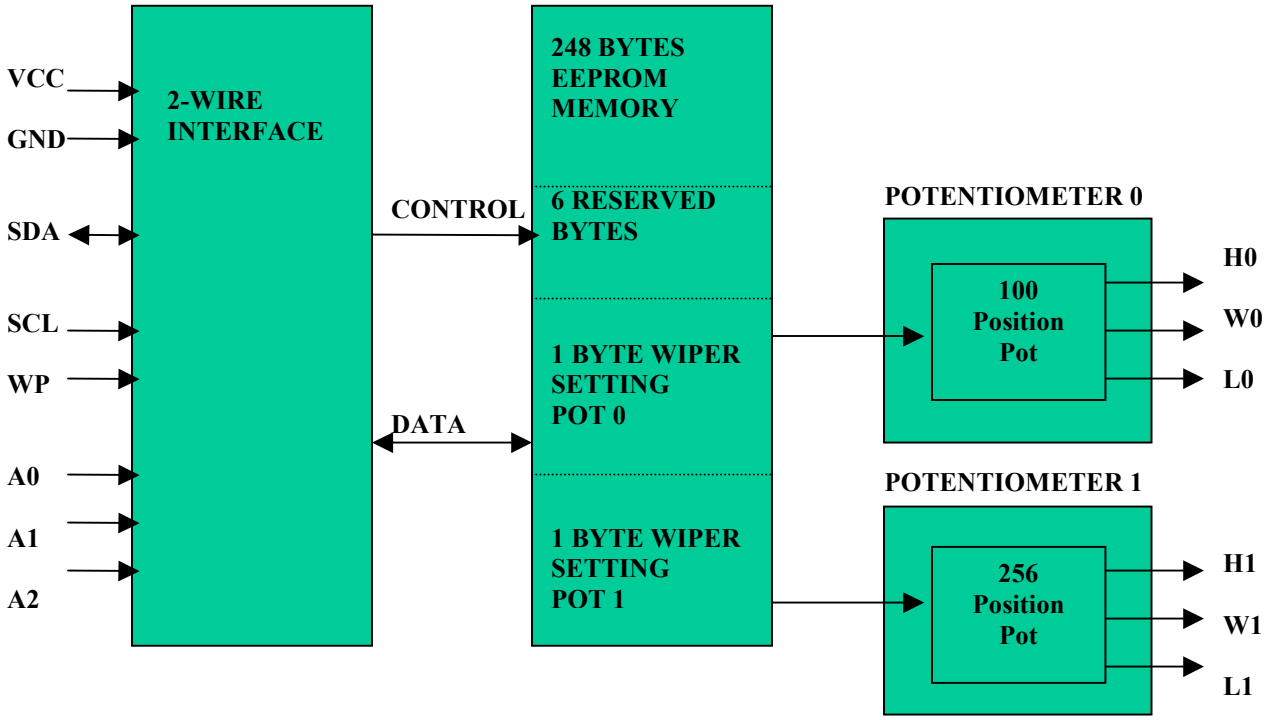
DESCRIPTION

The DS1845 Dual NV Potentiometer and Memory consists of one 100-position linear taper potentiometer, one 256-position linear taper potentiometer, 256 bytes of EEPROM memory, and a 2-wire interface. The device provides an ideal method for setting bias voltages and currents in control applications using a minimum of circuitry. The EEPROM memory allows a user to store configuration or calibration data for a specific system or device as well as provide control of the potentiometer wiper settings. Any type of user information may reside in the first 248 bytes of this memory. The next two addresses of EEPROM memory are for potentiometer settings. Access to this EEPROM is via an industry standard 2-wire bus. The wiper position of the DS1845, as well as EEPROM data, can be hardware write-protected using the Write Protect (WP) input pin. Up to eight DS1845s can be installed on a single 2-wire bus. Access to an individual device is achieved by using a device address that is determined by the logic levels of address pins A0 though A2. Additionally, the DS1845 will operate from 3 volt or 5 volt supplies. Three package options are available: Flip Chip Package, 16-ball CSBGA and 14-pin TSSOP.

PIN DESCRIPTIONS

Name	TSSOP	BGA	Description
V_{CC}	14	A3	**Power Supply Terminal.** The DS1845 will support supply voltages ranging from +2.7V to +5.5V.
GND	7	D1	**Ground Terminal.**
SDA	1	B2	**2-Wire serial data interface.** The serial data pin is for serial data transfer to and from the DS1845. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces.
SCL	2	A2	**2-Wire Serial Clock Input.** The serial clock input is used to clock data into the DS1845 on rising edges and clock data out on falling edges.
WP	6	C1	**Write Protect Input.** If set to logic 0, the data in memory and the potentiometer wiper setting may be changed. If set to logic 1, both the memory and the potentiometer wiper settings will be write protected. The WP pin is pulled high internally.
A0	3	A1	**Address Input.** Pins A0, A1, and A2 are used to specify the address of each DS1845 when used in a multi-dropped configuration. Up to eight DS1845s may be addressed on a single 2-wire bus.
A1	4	B1	**Address Input.**
A2	5	C2	**Address Input.**
H0	13	A4	**High terminal of Potentiometer 0.** For both potentiometers, it is not required that the high terminal be connected to a potential greater than the low terminal. Voltage applied to the high terminal of each potentiometer cannot exceed V_{CC} or go below ground.
H1	11	B3	**High terminal of Potentiometer 1.**
L0	8	D3	**Low terminal of Potentiometer 0.** For both potentiometers, it is not required that the low terminal be connected to a potential less than the high terminal. Voltage applied to the low terminal of each potentiometer cannot exceed V_{CC} or go below ground.
L1	10	C4	**Low terminal of Potentiometer 1.**
W0	9	D4	**Wiper terminal of Pot 0.** The wiper position of Potentiometer 0 is determined by the byte at EEPROM memory location F9h. Voltage applied to the wiper terminal of each potentiometer cannot exceed the power supply voltage, V_{CC}, or go below ground.
W1	12	B4	**Wiper terminal of Pot 1.** The wiper position of Potentiometer 1 is determined by the byte at EEPROM memory location F8h.
NC		C3	**No Connect.**
NC		D2	**No Connect.**

DS1845 BLOCK DIAGRAM Figure 1



MEMORY ORGANIZATION

The DS1845's serial EEPROM is internally organized with 256 words of 1 byte each. Each word requires an 8-bit address for random word addressing. The byte at address F9h determines the wiper setting for potentiometer 0, which contains 100 positions. Writing values above 63h to this address sets the wiper to its uppermost position. The byte at address F8h determines the wiper setting for potentiometer 1, which contains 256 positions (00h to FFh). The factory default wiper position for both potentiometers is FFh. Memory locations 00h to F7h are factory programmed to 00h. Address locations FAh though FFh are reserved and should not be written.

DEVICE OPERATION

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL low time periods. Data changes during SCL high periods will indicate a start or stop conditions depending on the conditions discussed below. Refer to the timing diagram Fig 2 for further details.

Start Condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command. Refer to the timing diagram Fig 2 for further details.

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command places the DS1845 into a low-power mode. Refer to the timing diagram Fig 2 for further details.

Acknowledge: All address and data byte are transmitted via a serial protocol. The DS1845 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.
Standby Mode: The DS1845 features a low-power mode that is automatically enabled after power-on, after a stop command, and after the completion of all internal operations.

2-Wire Interface Reset: After any interruption in protocol, power loss, or system reset, the following steps reset the DS1845.

1. Clock up to nine cycles.

2. Look for SDA high in each cycle while SCL is high.

3. Create a start condition while SDA is high.

Device Addressing: The DS1845 must receive an 8-bit device address word following a start condition to enable a specific device for a read or write operation. The address word is clocked into the DS1845 MSB to LSB. The address word consists of Ah (1010) followed by A2, A1, and A0 then the R/W (READ/WRITE) bit. If the R/W bit is high, a read operation is initiated. The R/W is low, a write operation is initiated. For a device to become active, the values of A2, A1 and A0 must be the same as the hard-wired address pins on the DS1845. Upon a match of written and hard-wired addresses, the DS1845 will output a zero for one clock cycle as an acknowledge. If the address does not match the DS1845 returns to a low-power mode.

Write Operations: After receiving a matching address byte with the R/W bit set low, the device goes into the write mode of operation. The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After the reception of this byte, the DS1845 will transmit a zero for one clock cycle to acknowledge the receipt of the address. The master must then transmit an 8-bit data word to be written into this address. The DS1845 will again transmit a zero for one clock cycle to acknowledge the receipt of the data. At this point the master must terminate the write operation with a stop condition. The DS1845 then enters an internally timed write process t_w to the EEPROM memory. All inputs are disabled during this byte write cycle.

The DS1845 is capable of an 8-byte page write. A page write is initiated the same way as a byte write, but the master does not send a stop condition after the 1st byte. Instead, after the slave acknowledges receipt of the data byte, the master can send up to seven more bytes using the same nine-clock sequence. The master must terminate the write cycle with a stop condition or the data clocked into the DS1845 will not be latched into permanent memory.

Acknowledge Polling: Once the internally-timed write has started and the DS1845 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a start condition followed by the device address. The R/W bit signifies the type of operation that is desired. The read or write sequence will only be allowed to proceed if the internal write cycle has completed and the DS1845 responds with a zero.

Read Operations: After receiving a matching address byte with the R/W bit set high, the device goes into the read mode of operation. There are three read operations: current address read, random read and sequential address read.

CURRENT ADDRESS READ

The DS1845 has an internal address register that maintains the address used during the last read or write operation, incremented by one. This data is maintained as long as V_{CC} is valid. If the most recent address was the last byte in memory, then the register resets to the first address. This address stays valid between operations as long as power is available.

Once the device address is clocked in and acknowledged by the DS1845 with the R/W bit set to high, the current address data word is clocked out. The master does not respond with a zero, but does generate a stop condition afterwards.

RANDOM READ

A random read requires a dummy byte write sequence to load in the data word address. Once the device and data address bytes are clocked in by the master, and acknowledged by the DS1845, the master must generate another start condition. The master now initiates a current address read by sending the device address with the read/write bit set high. The DS1845 will acknowledge the device address and serially clocks out the data byte.

SEQUENTIAL ADDRESS READ

Sequential reads are initiated by either a current address read or a random address read. After the master receives the first data byte, the master responds with an acknowledge. As long as the DS1845 receives this acknowledge after a byte is read, the master may clock out additional data words from the DS1845. After reaching address FFh, it resets to address 00h.

The sequential read operation is terminated when the master initiates a stop condition. The master does not respond with a zero.

For a more detailed description of 2-wire theory of operation, refer to the following section.

2-WIRE SERIAL PORT OPERATION

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1845 operates as a slave on the two-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA, SCL, A0, A1, A2. Timing diagrams for the 2-wire serial port can be found in Figures 2 and 3. Timing information for the 2-wire serial port is provided in the AC Electrical Characteristics table for 2-wire serial communications.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

Stop data transfer: A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figures 2 and 3 detail how data transfer is accomplished on the two-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a 9th bit.

Within the bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1845 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The 1st byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The master transmits the 1st byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a ‘not acknowledge’ can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1845 may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCL respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.

2. Slave transmitter mode: The 1st byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1845 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Address: command/control byte is the 1st byte received following the START condition from the master device. The command/control byte consists of a 4-bit control code. For the DS1845, this is set as ***1010*** binary for read/write operations. The next 3 bits of the command/ control byte are the device select bits or slave address (A2, A1, A0). They are used by the master device to select which of eight devices is to be accessed. When reading or writing the DS1845, the device-select bits must match the device-select pins (A2, A1, A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1 a read operation is selected, and when set to a 0 a write operation is selected.

Following the START condition, the DS1845 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the ***1010*** control code, the appropriate device address bits, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

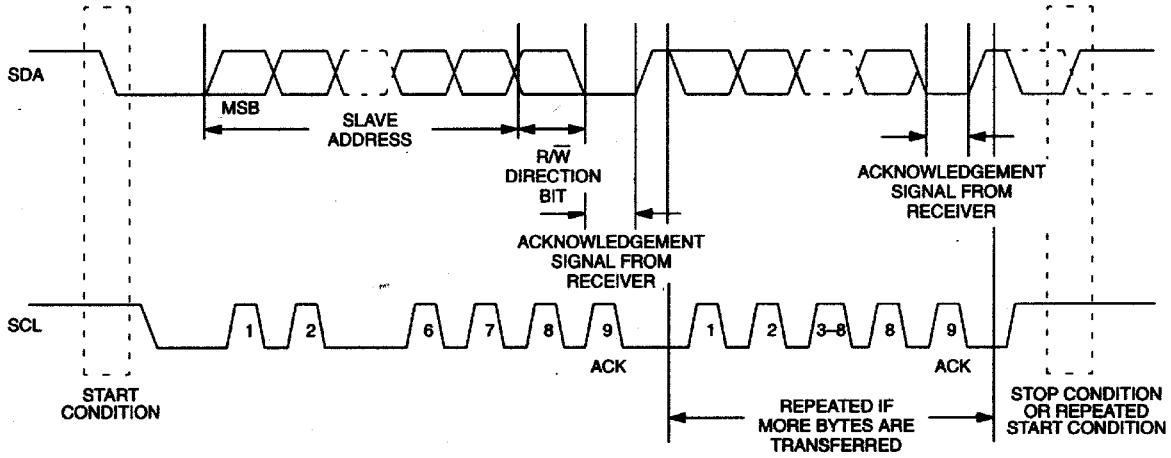
WRITE PROTECT

An external pin WP (write protect) protects EEPROM data and potentiometer position from alteration in an application. This pin must be open or tied high to protect data from alteration.

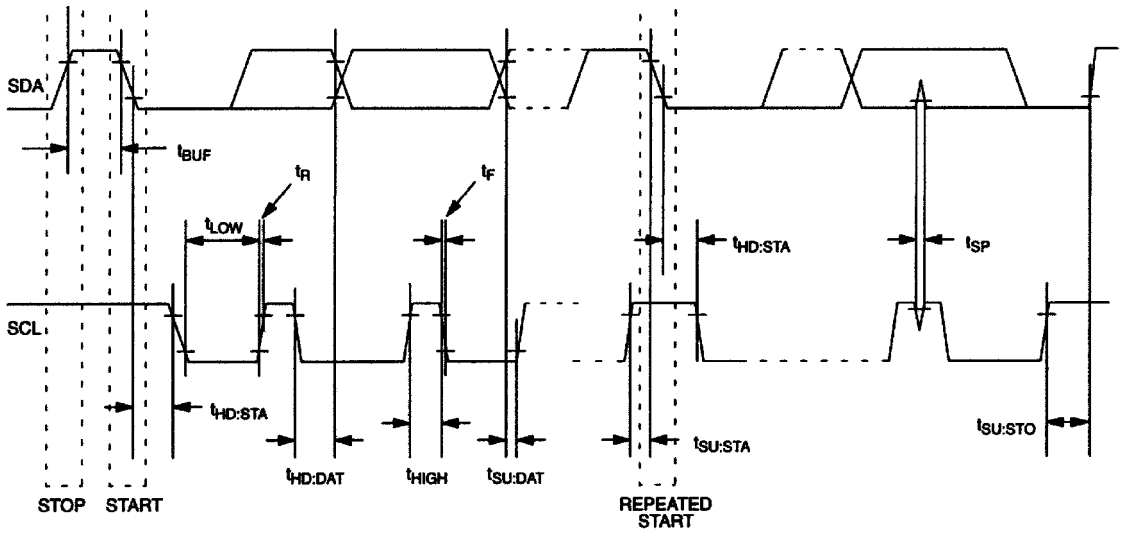
READING AND WRITING THE POTENTIOMETER VALUES

Reading from and writing to the potentiometers consists of a standard read or write to EEPROM memory at the addresses F8h and F9h. The 8-bit value at address F9h controls the wiper setting for potentiometer 0, which has 100 positions. The 8-bit value at address F8h controls the wiper setting of potentiometer 1, which has 256 positions. Potentiometer 1 may be set to any value between 00h and FFh. 00h sets the wiper of potentiometer 1 to its lowest value and FFh sets the wiper to its highest. Potentiometer 0 may be set to any value between 00h and 63h. A value of 00h sets the wiper of potentiometer 0 to its lowest position and 63h sets the wiper to its highest position. Any hexadecimal value is a valid address. Setting a value greater than the upper limit of the potentiometer's range, 64h or greater for potentiometer 0, will result in setting the wiper to its highest position, but the MSB will be ignored.

2- WIRE PROTOCOL DATA TRANSFER PROTOCOL Figure 2



2-WIRE AC CHARACTERISTICS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature	-40°C to +85°C; Industrial
Programming Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020 specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Input Logic 1	V_{IH}	.7 V_{CC}		V_{CC}+0.5	V	1,3
Input Logic 0	V_{IL}	-0.5		.3 V_{CC}	V	1,3
Resistor Inputs	L,H,W	-0.5		V_{CC}+0.5	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} =2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}				0.5	mA	12,13
Input Leakage	I_{LI}		-1		+1	µA	
Wiper Resistance 3V 5V	R_W			 500 250	 1000 600	 Ω	
Wiper Current	I_W				2	mA	
Input Logic levels A0, A1, A2		Input Logic 1 Input Logic 0	0.7 V_{CC} -0.5		V_{CC}+0.5 0.3 V_{CC}	V	
Input Current each I/O pin		0.4<$V_{I/O}$ <0.9V_{DD}	-10		+10	µA	
Standby Current 3V 5V	I_{STBY}			 20 30	 40 60	 µA	2
Low Level Output Voltage (SDA)	V_{OL1}	3 mA sink current	0.0		0.4	V	
	V_{OL2}	6 mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/O}$				10	pF	
WP Internal Pull Up Resistance, R_{wp}	R_{wp}		40	65	100	kΩ	

ANALOG RESISTOR CHARACTERISTICS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistance		25°C	-20		+20	%	
Absolute Linearity		10kΩ/100 pos. 10kΩ/256 pos. 20kΩ/256 pos. 50kΩ/256 pos. 100kΩ/256 pos.	-0.75 -0.75 -1.0 -1.5 -2.25		+0.75 +0.75 +1.0 +1.5 +2.25	LSB	9
Relative Linearity		10kΩ/100 pos. all other pots	-0.25 -0.5		+0.25 +0.5	LSB	10
-3dB Cutoff freq.	f_{CUTOFF}	DS1845-010		1		MHz	
End-to-End Temp. Coefficient				750		ppm/°C	11

AC ELECTRICAL CHARACTERISTICS (-40°C to 85°C , Vcc=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL clock frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	kHz	4
Bus free time between STOP and START condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	
Hold time (repeated) START condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	5
Low period of SCL clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	
High period of SCL clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	
Data hold time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	6
Data set-up time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	
Start set-up time	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	
Rise time of both SDA and SCL signals	t_R	Fast Mode Standard Mode	20 + 0.1C_B		300 1000	ns	7
Fall time of both SDA and SCL signals	t_F	Fast Mode Standard Mode	20 + 0.1C_B		300 300	ns	7
Set-up time for STOP condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive load for each bus line	C_B				400	pF	7
EEPROM write time	t_W			5		ms	8

NOTES:

1. All voltages are referenced to ground.

2. I_{STBY} specified with V_{CC} equal 3.0V and 5.0V and control port logic pins are driven to the appropriate logic levels. Appropriate logic levels specify that logic inputs are within a 0.5V of ground or V_{CC} for the corresponding inactive state.

3. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.

4. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.

5. After this period, the first clock pulse is generated.

6. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

7. C_B - total capacitance of one bus line in picofarads. Timing referenced to $0.9V_{CC}$ and $0.1V_{CC}$.

8. EEPROM write begins after a stop condition occurs.

9. Absolute linearity is used to measure expected wiper voltage as determined by wiper position.

10. Relative linearity is used to determine the change of wiper voltage between two adjacent wiper positions.

11. When used as a rheostat or variable resister the temperature coefficient applies: 750 ppm/°C. When used as a voltage divider or potentiometer, the effective temperature coefficient approaches 30 ppm/°C.

12. I_{CC} specified with SDA pin open.

13. Maximum Icc is dependent on clock rates.