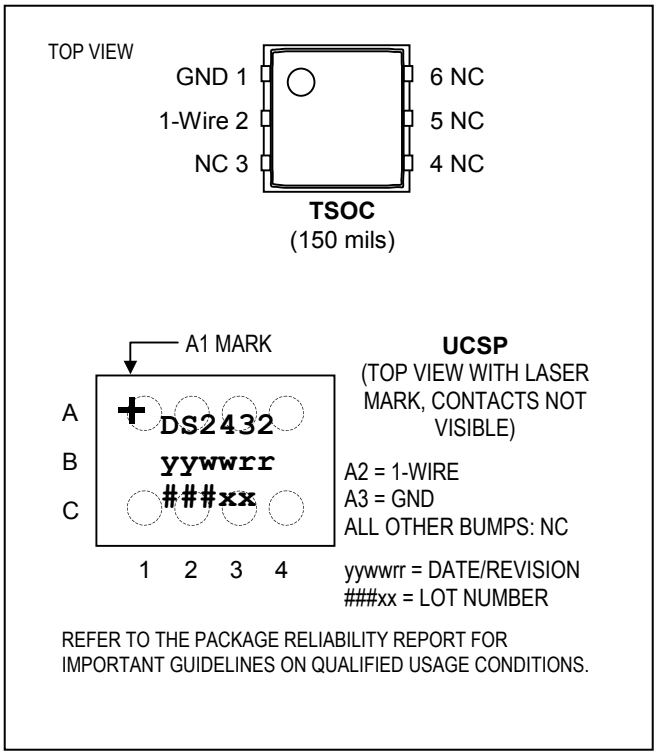
ABRIDGED DATA SHEET

DS2432
1Kb Protected 1-Wire EEPROM with SHA-1 Engine

FEATURES

- 1128 Bits of 5V EEPROM Memory Partitioned Into Four Pages of 256 Bits, a 64-Bit Write-Only Secret, and Up to Five General-Purpose Read/Write Registers
- On-Chip 512-Bit ISO/IEC 10118-3 SHA-1 Engine to Compute 160-Bit Message Authentication Codes (MACs) and to Generate Secrets
- Write Access Requires Knowledge of the Secret and the Capability of Computing and Transmitting a 160-Bit MAC as Authorization
- Secret and Data Memory Can Be Write Protected (All or Page 0 Only) or Put in EPROM-Emulation Mode ("Write to 0", Page 1)
- Unique, Factory-Lasered and Tested 64-Bit Registration Number Assures Absolute Traceability Because No Two Parts Are Alike
- Built-In Multidrop Controller Ensures Compatibility with Other 1-Wire® Net Products
- Reduces Control, Address, Data, and Power to a Single Data Pin
- Directly Connects to a Single Port Pin of a Microprocessor and Communicates at Up to 15.3kbps
- Overdrive Mode Boosts Communication Speed to 90.9kbps
- Low-Cost 6-Lead TSOC Surface-Mount Package or Solder-Bumped UCSP™ Package
- Reads and Writes Over a Wide Voltage Range of 2.8V to 5.25V from -40°C to +85°C

PIN CONFIGURATIONS



ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2432P+	-40°C to +85°C	6 TSOC
DS2432P+T&R	-40°C to +85°C	6 TSOC
DS2432X-S+	-40°C to +85°C	8 UCSP (2.5k pcs, T&R)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

Request Full Data Sheet at:
www.maximintegrated.com/DS2432

1-Wire is a registered trademark and UCSP is a trademark of Maxim Integrated Products, Inc.

219-0003; Rev 9/12

DESCRIPTION

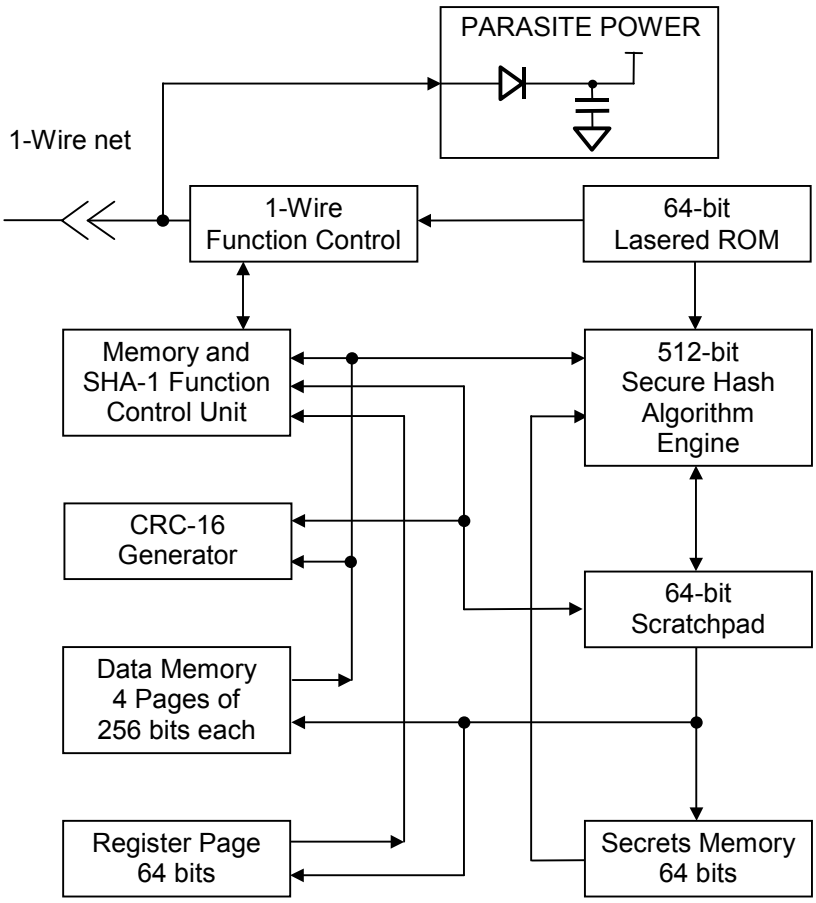
The DS2432 combines 1024 bits of EEPROM, a 64-bit secret, an 8-byte register/control page with up to five user read/write bytes, a 512-bit SHA-1 engine, and a fully-featured 1-Wire interface in a single chip. Each DS2432 has its own 64-bit ROM registration number that is factory lasered into the chip to provide a guaranteed unique identity for absolute traceability. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return. The DS2432 has an additional memory area called the scratchpad that acts as a buffer when writing to the main memory, the register page or when installing a new secret. Data is first written to the scratchpad from where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to its final memory location, provided that the DS2432 receives a matching 160-Bit MAC. The computation of the MAC involves the secret and additional data stored in the DS2432 including the device's registration number. Only a new secret can be loaded without providing a MAC. The SHA-1 engine can also be activated to compute 160-bit message authentication codes (MAC) when reading a memory page or to compute a new secret, instead of loading it. Applications of the DS2432 include intellectual property security, after-market management of consumables, and tamper-proof data carriers.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2432. The DS2432 has five main data components: 1) 64-bit lasered ROM, 2) 64-bit scratchpad, 3) four 32-byte pages of EEPROM, 4) 64-bit register page, 5) 64-bit Secrets Memory, and 6) a 512-bit SHA-1 Engine (SHA = Secure Hash Algorithm). The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Resume Communication, 6) Overdrive-Skip ROM or 7) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at regular speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory and SHA-1 functions become accessible and the master may provide any one of the seven memory function commands. The protocol for these memory function commands is described in Figure 7*. **All data is read and written least significant bit first.**

* For Figure 7, refer to the full version of the data sheet.

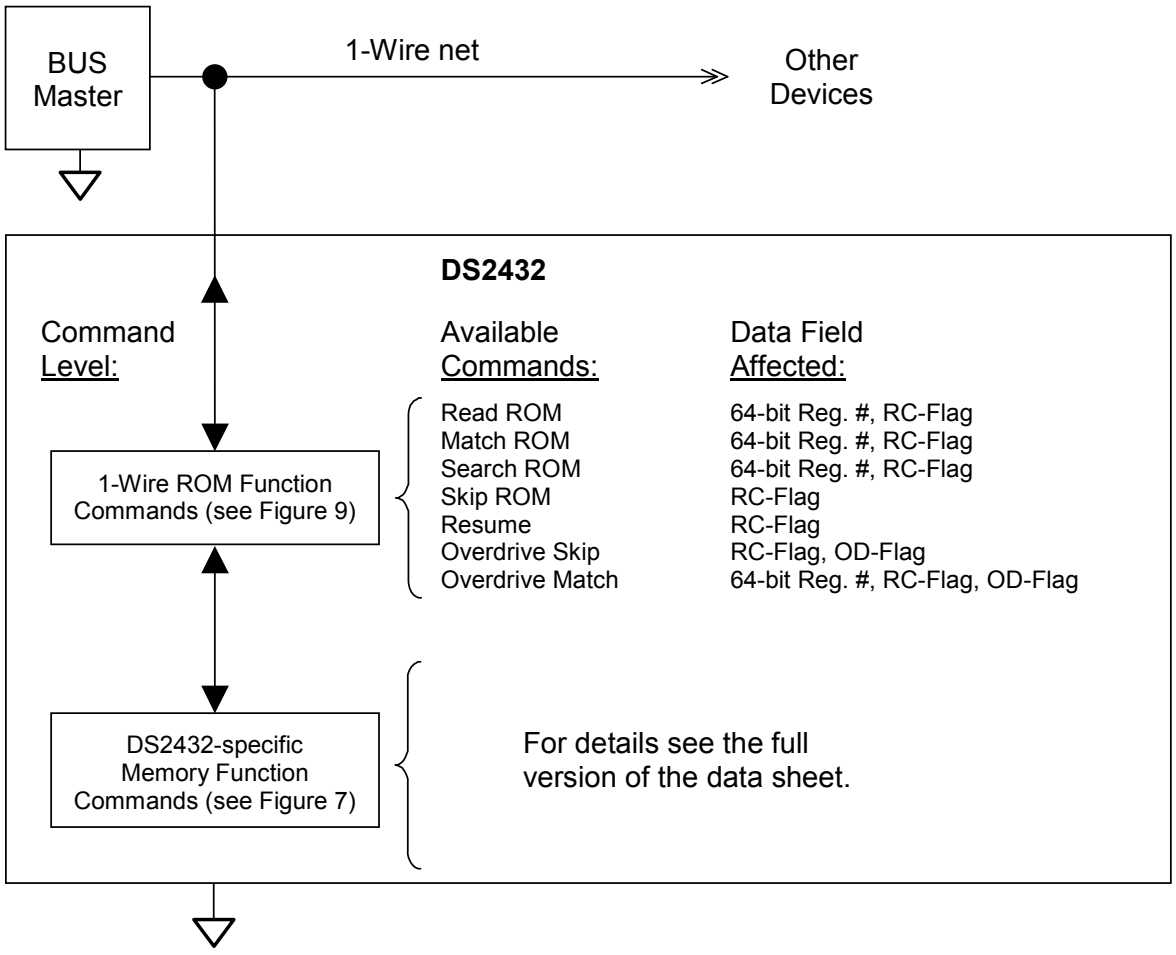
DS2432 BLOCK DIAGRAM Figure 1



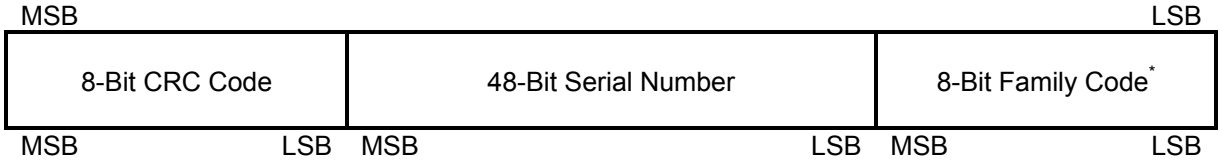
64-BIT LASERED ROM

Each DS2432 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire Cyclic Redundancy Check is available in Application Note 27. The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

HIERARCHCAL STRUCTURE FOR 1-Wire PROTOCOL Figure 2

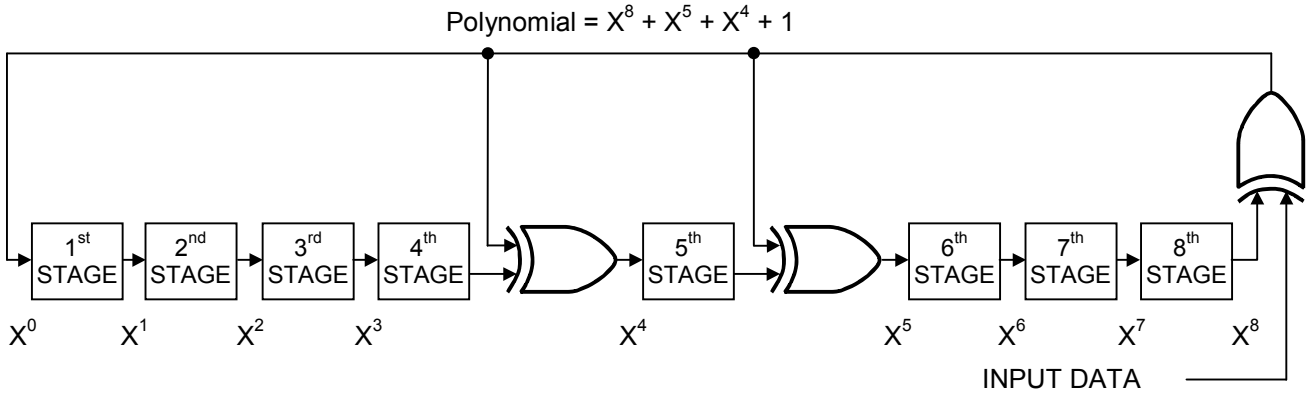


64-BIT LASERED ROM Figure 3



*For the actual Family Code value, refer to the full version of the data sheet.

1-Wire CRC GENERATOR Figure 4



MEMORY MAP

The DS2432 has four memory areas: data memory, secrets memory, register page with special function registers and user-bytes, and a scratchpad. The data memory is organized in pages of 32 bytes. Secret, register page and scratchpad are 8 bytes each. The scratchpad acts as a buffer when writing to the data memory, loading the initial secret or when writing to the register page. For further details (including Figure 5) refer to the full version of the data sheet.

ADDRESS REGISTERS AND TRANSFER STATUS

The DS2432 employs three address registers: TA1, TA2 and E/S (Figure 6). These registers are common to many other 1-Wire devices but operate slightly differently with the DS2432. Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be read. Register E/S is a read-only transfer-status register, used to verify data integrity with write commands. Since the scratchpad of the DS2432 is designed to accept data in blocks of eight bytes only, the lower three bits of TA1 will be forced to 0 and the lower three bits of the E/S register (Ending Offset) will always read 1. This indicates that all the data in the scratchpad will be used for a subsequent copying into main memory or secret. Bit 5 of the E/S register, called PF or "partial byte flag", is a logic-1 if the number of data bits sent by the master is not an integer multiple of 8 or if the data in the scratchpad is not valid due to a loss of power. A valid write to the scratchpad will clear the PF bit. Bits 3, 4 and 6 have no function; they always read 1. The Partial Flag supports the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA or Authorization Accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

ADDRESS REGISTERS Figure 6

Bit #	7	6	5	4	3	2	1	0
Target Address (TA1)	T7	T6	T5	T4	T3	T2 (0)	T1 (0)	T0 (0)
Target Address (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
Ending Address with Data Status (E/S) (Read Only)	AA	1	PF	1	1	E2 (1)	E1 (1)	E0 (1)

WRITING WITH VERIFICATION

To write data to the DS2432, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Note that writes to data memory must be performed on 8-byte boundaries with the 3 LSBs of the target address (T2..T0) equal to 000b. If T2..T0 are sent with non-zero values, the device will set these bits to zero and will write to the modified address upon completion of the command sequence. In addition, the entire 8-byte scratchpad will be copied to memory when commanded, therefore eight bytes of data should be written into the scratchpad to ensure that the data to be copied is known. Under certain conditions (see the Write Scratchpad command) the master will receive an inverted CRC-16 of the command, address (actual address sent) and data at the end of the write scratchpad command sequence. Note that the CRC is calculated based on the actual target address sent and not the modified address in the case of a non-zero T2..T0. Knowing this CRC value, the master can compare it to the value it has calculated itself to decide if the communication was successful and proceed to the Copy Scratchpad command. If the master could not receive the CRC-16, it should send the Read Scratchpad command to verify data integrity. As preamble to the scratchpad data, the DS2432 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad or there was a loss of power since data was last written to the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the device did not recognize the Write command. If everything went correctly, both flags are cleared. Now the master can continue reading and verifying every data byte. After the master has verified the data, it can send the Copy Scratchpad command, for example. This command must be followed exactly by the data of the three address registers TA1, TA2 and E/S. The master should obtain the contents of these registers by reading the scratchpad.

MEMORY AND SHA-1 FUNCTION COMMANDS

This section describes the commands and flow charts to use the memory and SHA-1 engine of the device. It includes Tables 1 to 4 and Figure 7. Please refer to the full version of the data sheet.

SHA-1 COMPUTATION ALGORITHM

The SHA-1 computation is adapted from the Secure Hash Standard SHA-1 document as it can be downloaded from the NIST website (http://www.itl.nist.gov/fipspubs/fip180-1.htm). Further details are found in the full version of the data sheet.

1-Wire BUS SYSTEM

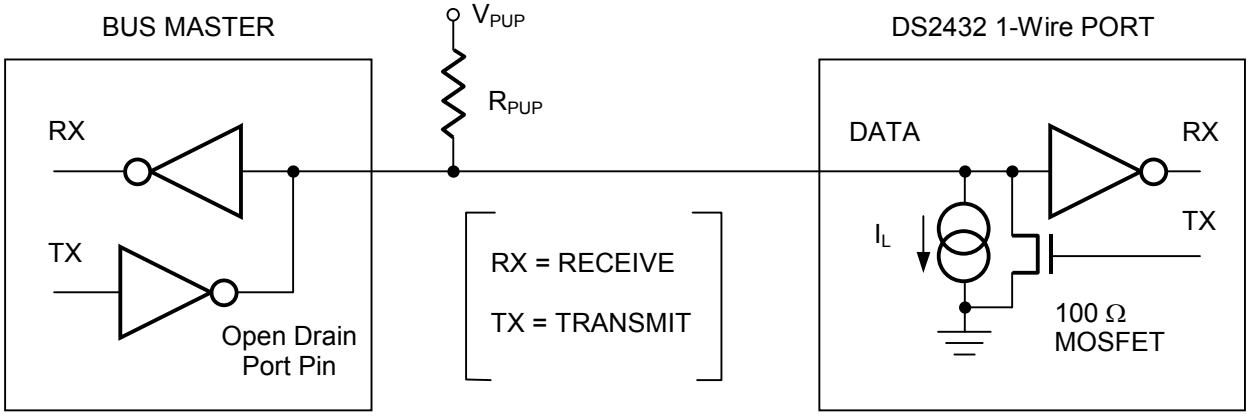
The 1-Wire bus is a system, which has a single bus master and one or more slaves. In all instances the DS2432 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2432 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 15.3kbps. The speed can be boosted to 90.9kbps by activating the Overdrive Mode. The DS2432 requires a 1-Wire pullup resistor of maximum 2.2 kΩ for executing any of its memory and SHA-1 function commands at any speed. When communicating with several DS2432 simultaneously, e.g., to install the same secret in several devices, the resistor should be bypassed by a low-impedance pullup to V_{PUP} while the device transfers data from the scratchpad to the EEPROM.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 µs (Overdrive Speed) or more than 120 µs (regular speed), one or more devices on the bus may be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS2432 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory or SHA-1 Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2432 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS2432 supports. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33h]

This command allows the bus master to read the DS2432's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command should only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number read by the master will be invalid.

Match ROM [55h]

The match ROM command, followed by a 64-bit registration number, allows the bus master to address a specific DS2432 on a multidrop bus. Only the DS2432 that exactly matches the 64-bit registration number will respond to the following memory function command. All other slaves will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit registration numbers. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit numbers of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this 3-step routine on each bit of the registration number. After one complete pass, the bus master knows the 64-bit number of one device. Additional passes will identify the registration numbers of the remaining devices. Refer to Application Note 187 for a detailed discussion of a search ROM, including an actual example.

Skip ROM [CCh]

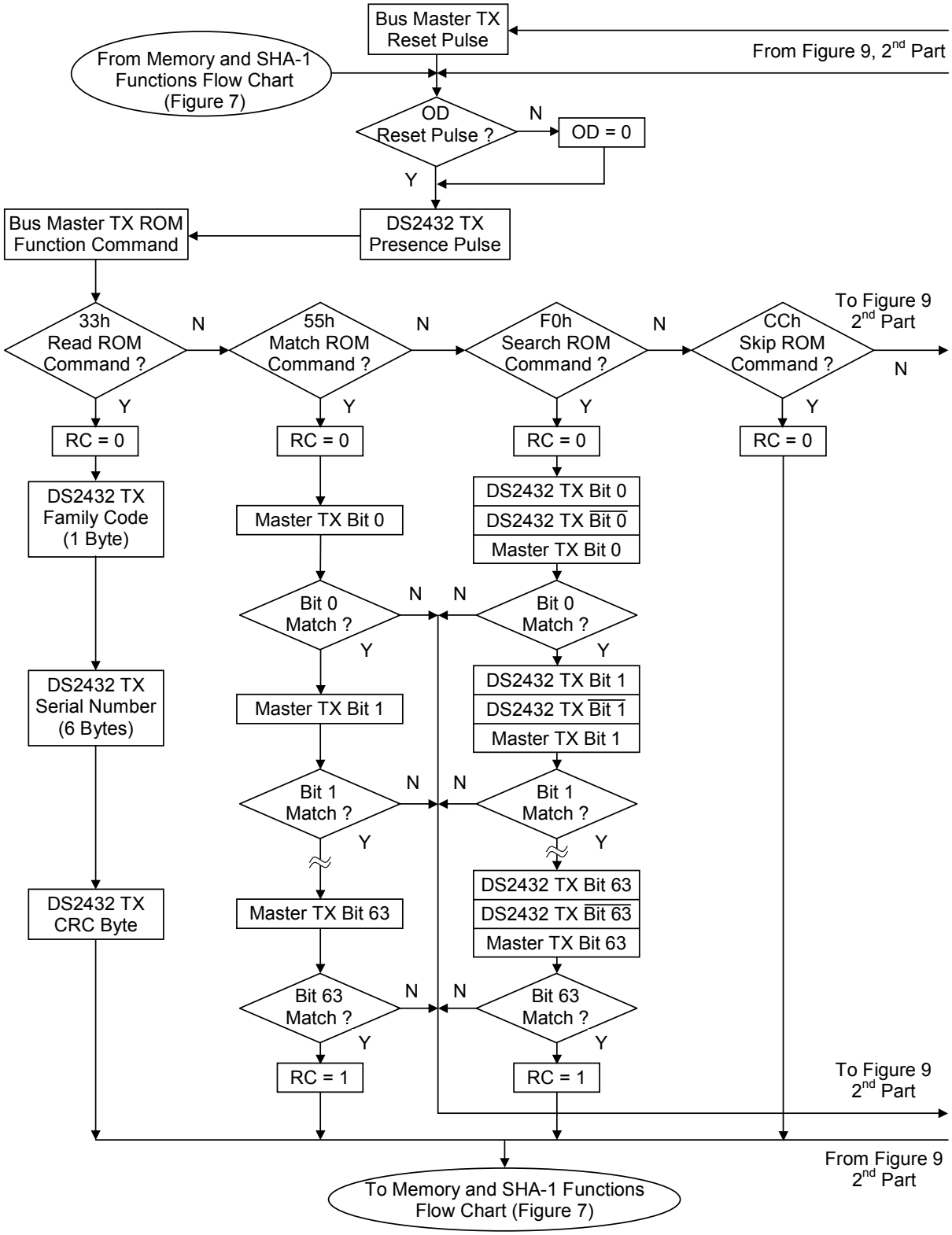
This command can save time in a single drop bus system by allowing the bus master to access the memory and SHA-1 functions without providing the 64-bit registration number. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open-drain pulldowns will produce a wired-AND result).

Overdrive Skip ROM [3Ch]

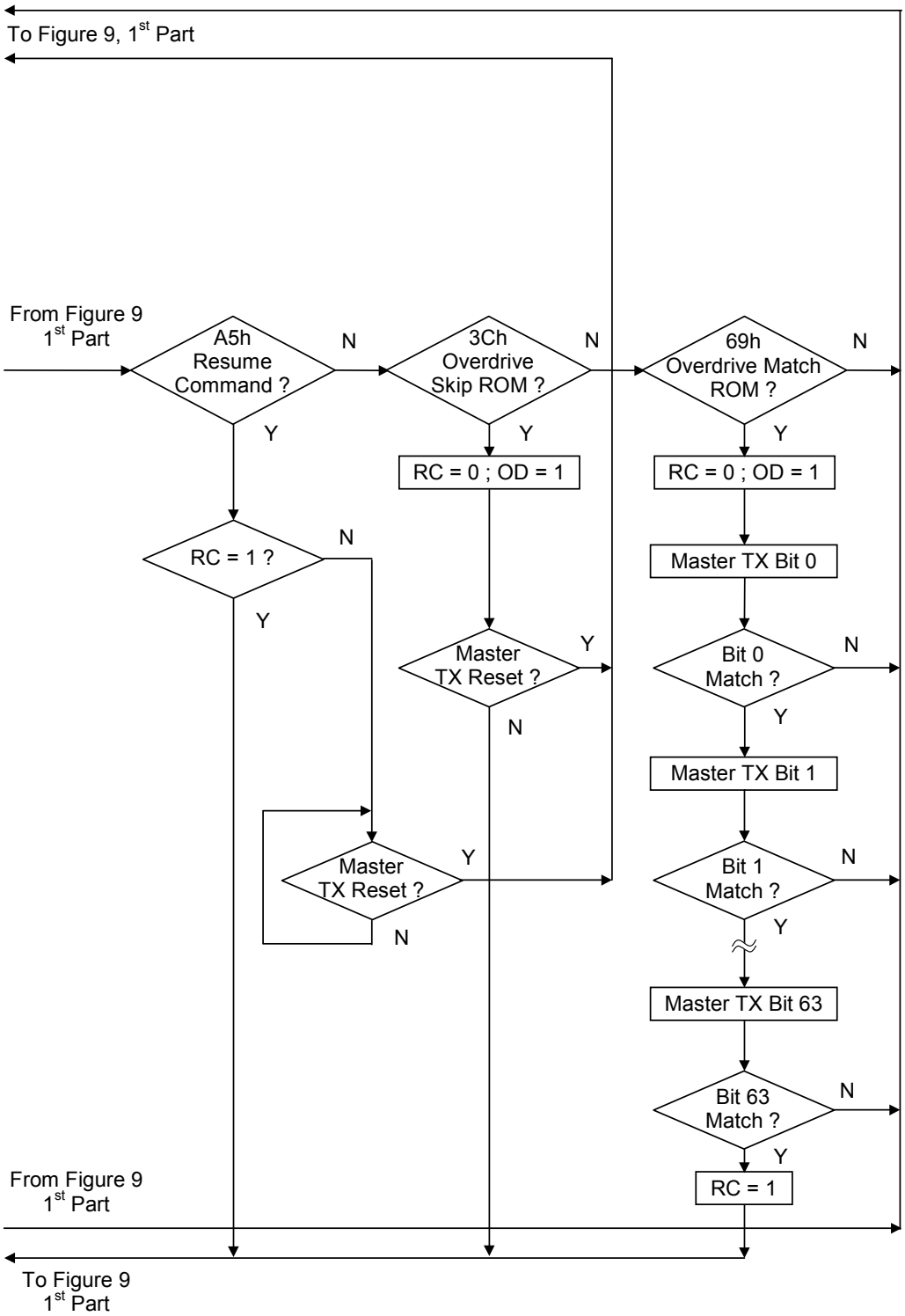
On a single-drop bus this command can save time by allowing the bus master to access the memory and SHA-1 functions without providing the 64-bit registration number. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS2432 in the Overdrive Mode (OD = 1). All communication following this command code has to occur at Overdrive Speed until a reset pulse of minimum 480 µs duration resets all devices on the bus to regular speed (OD = 0).

When issued on a multidrop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the search process. If more than one Overdrive-supporting slave is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

ROM FUNCTIONS FLOW CHART Figure 9



ROM FUNCTIONS FLOW CHART (continued) Figure 9



Overdrive Match ROM [69h]

The Overdrive Match ROM command, followed by a 64-bit registration number transmitted at Overdrive Speed, allows the bus master to address a specific DS2432 on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS2432 that exactly matches the 64-bit number will respond to the subsequent memory or SHA-1 function command. Slaves already in Overdrive mode from a previous Overdrive Skip or a successful Overdrive Match command will remain in Overdrive mode. All Overdrive-capable slaves will return to regular speed at the next Reset Pulse of minimum 480 µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

Resume Command [A5h]

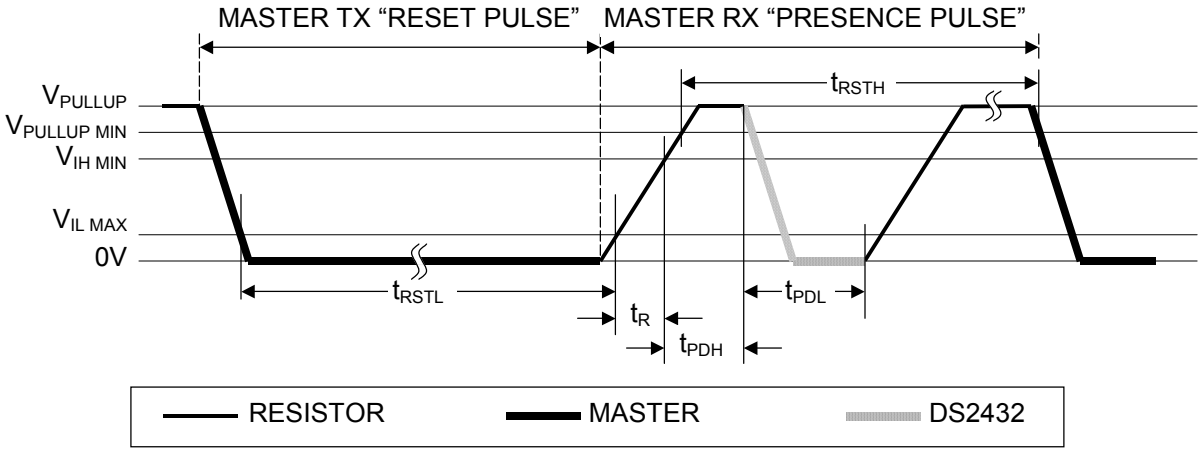
In a typical application the DS2432 needs to be accessed several times to write a full 32-byte page. In a multidrop environment this means that the 64-bit registration number of a Match ROM command has to be repeated for every access. To maximize the data throughput in a multidrop environment the Resume Command function was implemented. This function checks the status of the RC bit and, if it is set, directly transfers control to the Memory and SHA-1 functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM or Overdrive Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume Command function. Accessing another device on the bus will clear the RC bit, preventing two or more devices from simultaneously responding to the Resume Command function.

1-Wire SIGNALING

The DS2432 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. Except for the presence pulse the bus master initiates all these signals. The DS2432 can communicate at two different speeds, regular speed and Overdrive Speed. If not explicitly set into the Overdrive mode, the DS2432 will communicate at regular speed. While in Overdrive Mode the fast timing applies to all waveforms.

The initialization sequence required to begin any communication with the DS2432 is shown in Figure 10. A Reset Pulse followed by a Presence Pulse indicates the DS2432 is ready to send or receive data. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs at regular speed, 48 µs at Overdrive Speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS2432 waits (t_{PDH}, 15-60 µs at regular speed, 2-6 µs at Overdrive speed) and then transmits the Presence Pulse (t_{PDL}, 60-240 µs at regular speed, 8-24 µs at Overdrive Speed). A Reset Pulse of 480 µs or longer will exit the Overdrive Mode returning the device to regular speed. If the DS2432 is in Overdrive Mode and the Reset Pulse is no longer than 80 µs the device will remain in Overdrive Mode.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10

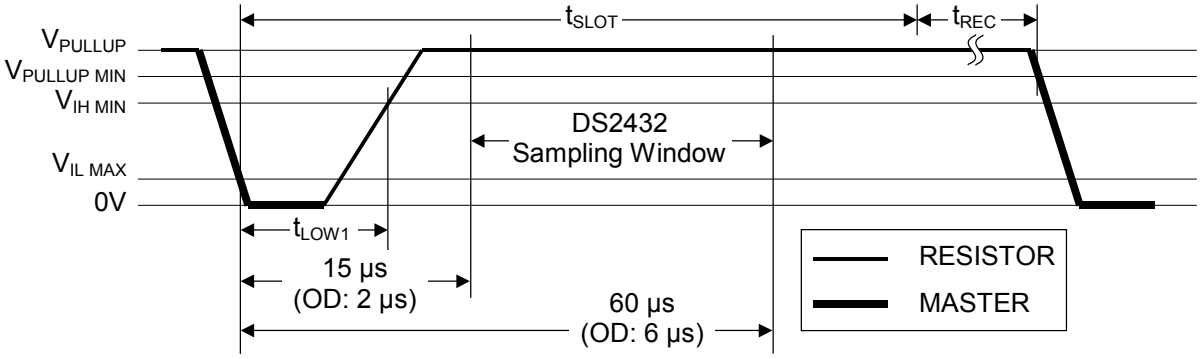


Read/Write Time Slots

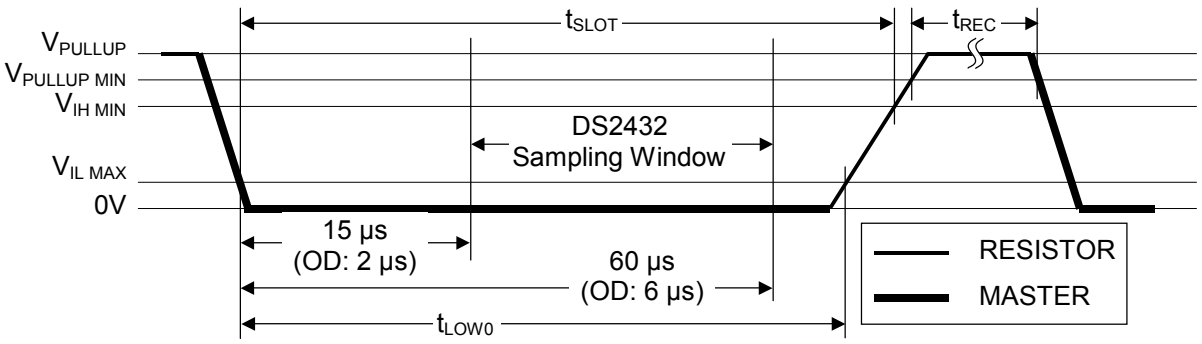
The definitions of write and read time slots are illustrated in Figure 11. The master initiates all time slots by driving the data line low. The falling edge of the data line synchronizes the DS2432 to the master by triggering an internal delay circuit. During write time slots, the delay circuit determines when the DS2432 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2432 will hold the data line low. If the data bit is a "1", the DS2432 will not hold the data line low at all.

READ/WRITE TIMING DIAGRAM Figure 11

Write-one Time Slot

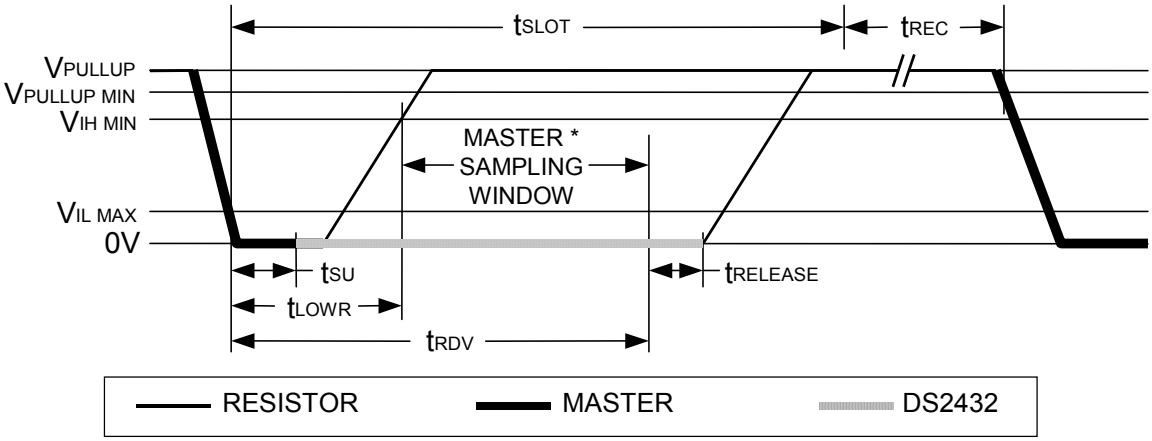


Write-zero Time Slot



READ/WRITE TIMING DIAGRAM Figure 11 (continued)

Read-data Time Slot



*The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pullup resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device releases the line ($t_{RELEASE} = 0$).

CRC GENERATION

With the DS2432 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8-bit type. It is computed at the factory and lasered into the most significant byte of the 64-bit ROM. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. To determine whether the ROM data has been read without error the bus master can compute the CRC value from the first 56 bits of the 64-bit ROM and compare it to the value read from the DS2432. This 8-bit CRC is received in the true form (non-inverted) when reading the ROM.

The other CRC is a 16-bit type, which is used for error detection with Memory and SHA-1 function commands. For details (including Figure 12), refer to the full version of the data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.5V to +5.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (TSOC only; soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Pullup Voltage	V_{PUP}	2.8		5.25	V	1, 2
1-Wire Input High	V_{IH}	2.2			V	1, 3
1-Wire Input Low	V_{IL}	-0.3		0.3	V	1
1-Wire Output Low at 4mA	V_{OL}			0.4	V	1
Input Load Current	I_L		5		µA	4
Programming Current	I_{LPROG}		500		µA	5, 6
SHA-1 Computation Current	I_{CSHA}	Refer to the full version of data sheet.				

CAPACITANCE

(T_A = +25°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire I/O	$C_{IN/OUT}$		100	800	pF	7

EEPROM

(V_{PUP} = 5.0V, T_A = +25°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write/Erase Cycles	N_{CYCLE}	50k			—	
Data Retention (at 85°C)	t_{DRET}	10			years	

AC ELECTRICAL CHARACTERISTICS: REGULAR SPEED

(V_{PUP} = 2.8V to 5.25V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	
Read Data Valid	t_{RDV}		15		µs	8
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	9
Recovery Time	t_{REC}	5			µs	10
Reset High Time	t_{RSTH}	480			µs	
Reset Low Time	t_{RSTL}	480			µs	11
Presence Detect High	t_{PDHIGH}	15		60	µs	12
Presence Detect Low	t_{PDLOW}	60		240	µs	12
Programming Time	t_{PROG}			10	ms	
SHA-1 Computation Time	t_{CSHA}	Refer to the full version of data sheet.				

AC ELECTRICAL CHARACTERISTICS: OVERDRIVE SPEED

(V_{PUP} = 2.8V to 5.25V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Low Time	t_{LOWR}	1		2	µs	
Read Data Valid	t_{RDV}		2		µs	8
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	9
Recovery Time	t_{REC}	5			µs	10
Reset High Time	t_{RSTH}	48			µs	
Reset Low Time	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDHIGH}	2		6	µs	
Presence Detect Low	t_{PDLOW}	8		24	µs	
Programming Time	t_{PROG}			10	ms	
SHA-1 Computation Time	t_{CSHA}	Refer to the full version of data sheet.				

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pullup voltage, see Figure 8.
3. V_{IH} is a function of the external pullup resistor and V_{PUP}.
4. Input load is to ground.
5. During write operations to the EEPROM the voltage on the 1-Wire bus must not fall below 2.8V.
6. Guaranteed by design, not production tested.
7. Capacitance on the data pin could be 800 pF when power is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
8. The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pullup resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device releases the line ($t_{RELEASE}$ = 0).
9. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.
10. Applies to a single device attached to a 1-Wire line and a pullup resistor of maximum 2.2kΩ.
11. The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.
12. The first presence pulse after power-up could be outside the $t_{PDHIGHmax}$ to ($t_{PDHIGHmin}$ + $t_{PDLOWmin}$) interval, but will be complete within 2ms after power-up.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 TSOC	D6+1	21-0382	90-0321
8 UCSP	BR823+1	21-0373	Refer to Application Note 1891