Rev 0; 6/02

DALLAS SEMICONDUCTOR MAXIM

Triple 128-Position Nonvolatile Digital Potentiometer

General Description

The DS3903 contains three nonvolatile (NV) low temperature coefficient digital potentiometers, which can be accessed through a 2-wire bus. It operates in both 3V and 5V systems, and it features a write-protect pin that can lock the positions of the potentiometers. An address pin allows two DS3903s to be placed on the same 2-wire bus.

Applications

Power-Supply Calibration

Mobile Phones and PDAs

Fiber Optics Transceiver Modules

Portable Electronics

A Small, Low-Cost Replacement for Mechanical Potentiometers

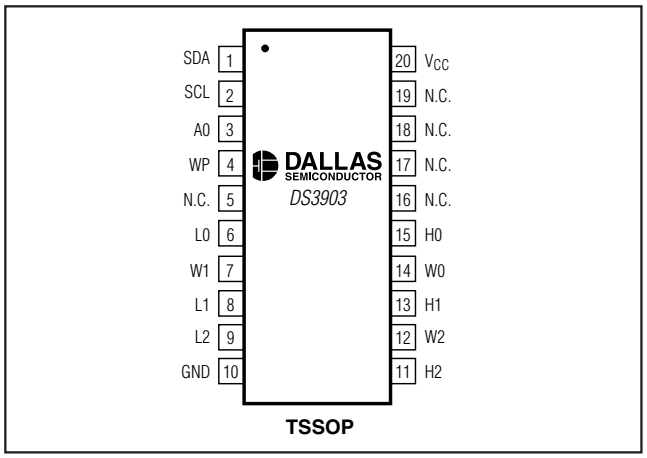
Features

- **Three 128-Position Linear Potentiometers (Two 10kΩ, One 90kΩ)**
- **NV Wiper Storage**
- **0 to 5.5V on Any Potentiometer Terminal Independent of V_{CC}**
- **Low End-to-End Temperature Coefficient**
- **Operates on an Industry-Standard 2-Wire Bus**
- **Write-Protect Pin**
- **Supply Voltage: 3V or 5V**
- **Operating Temperature Range: -40°C to +85°C**
- **Packaging: 20-Pin TSSOP**

Ordering Information

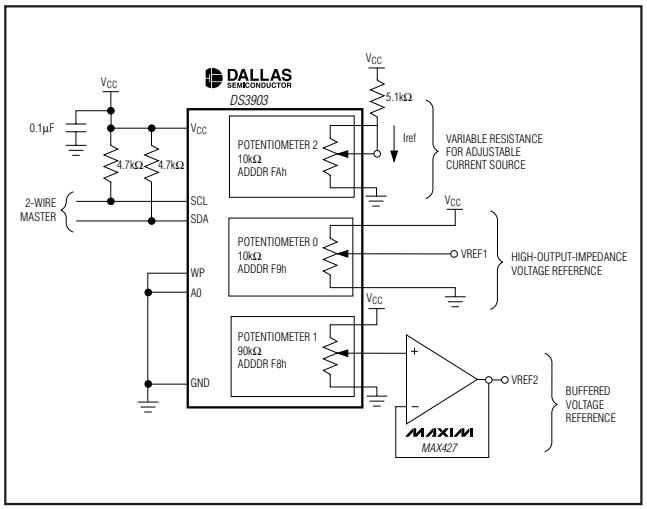
PART	TEMP RANGE	PIN-PACKAGE
DS3903E-020	-40°C to +85°C	20 TSSOP
DS3903E-020/T&R	-40°C to +85°C	20 TSSOP (Tape-and-Reel)

Pin Configuration



TSSOP

Typical Operating Circuit



Triple 128-Position Nonvolatile Digital Potentiometer

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Pin Relative to Ground.....-0.5V to +6.0V
Voltage on SDA, SCL, A0, and WP Relative to Ground.....-0.5V to V_{CC} + 0.5V
Voltage on L0, L1, L2, W0, W1, W2, H0, H1, and H2 Relative to Ground.....-0.5V to +6.0V
Current Through W0, W1, and W2.....±4mA
Operating Temperature Range .....-40°C to +85°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40° to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.7		+5.5	V
Input Logic 1	V_{IH}	(Notes 2, 3)	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}	(Notes 2, 3)	-0.3		0.3 x V_{CC}	V
Wiper Current	I_W		-3		+3	mA
Resistor Terminals L0, L1, L2, W0, W1, W2, H0, H1, H2		V_{CC} = +2.7V to +5.5V	-0.3		+5.5	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_L		-1		+1	µA
Standby Supply Current	I_{stby}	V_{CC} = 3V (Note 2)		100	200	µA
		V_{CC} = 5V (Note 2)		150	250	
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	V
I/O Capacitance	$C_{I/O}$				10	pF
WP Internal Pullup Resistance	R_{WP}		35	65	110	kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode (Note 4)	0		400	kHz
		Standard mode (Note 4)	0		100	
Bus Free Time Between Stop and Start Conditions	t_{BUF}	Fast mode (Note 4)	1.3			µs
		Standard mode (Note 4)	4.7			
Hold Time (Repeated) Start Condition	$t_{HD:STA}$	Fast mode (Notes 4, 5)	0.6			µs
		Standard mode (Notes 4, 5)	4.0			
Low Period of SCL Clock	t_{LOW}	Fast mode (Note 4)	1.3			µs
		Standard mode (Note 4)	4.7			
High Period of SCL Clock	t_{HIGH}	Fast mode (Note 4)	0.6			µs
		Standard mode (Note 4)	4.0			
Data Hold Time	$t_{HD:DAT}$	Fast mode (Notes 4, 6, 7)	0		0.9	µs
		Standard mode (Notes 4, 6, 7)	0		0.9	
Data Set-Up Time	$t_{SU:DAT}$	Fast mode (Note 4)	100			ns
		Standard mode (Note 4)	250			
Start Set-Up Time	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals	t_R	Fast mode (Note 8)	$20 + 0.1C_B$		300	ns
		Standard mode (Note 8)	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals	t_F	Fast mode (Note 8)	$20 + 0.1C_B$		300	ns
		Standard mode (Note 8)	$20 + 0.1C_B$		300	
Set-Up Time for Stop Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.7			
Capacitive Load for Each Bus	C_B	(Note 8)			400	pF
EEPROM Write Time	t_W	(Note 9)		10		ms
Startup Time	t_{ST}				2	ms

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-to-End Resistance Tolerance		+25°C	-20		+20	%
End-to-End Resistance		10kΩ Pot		10.5		kΩ
		90kΩ Pot		90		
Factory-Default Wiper Setting		Position 127 (max resistance)				
Wiper Resistance	R_W			250	500	Ω
Absolute Linearity		(Note 10)	-1.0		+1.0	LSB
Relative Linearity		(Note 11)	-0.25		+0.25	LSB
End-to-End Temperature Coefficient			-300	0	+300	ppm/°C
Ratiometric Temperature Coefficient				±30		ppm/°C

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Note 1: All voltages are referenced to ground.

Note 2: I_{STBY} specified for V_{CC} equal to 3.0V and 5.0V while control port logic pins are driven to the appropriate logic levels. Appropriate logic levels specify that logic inputs are within a 0.5V of ground or V_{CC} for the corresponding inactive state. WP must be disconnected or connected high.

Note 3: I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 4: A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.

Note 5: After this period, the first clock pulse is generated.

Note 6: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 7: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IN\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

Note 8: C_B—total capacitance of one bus line in picofarads, timing referenced to 0.9 x V_{CC} and 0.1 x V_{CC}.

Note 9: EEPROM write begins after a stop condition occurs.

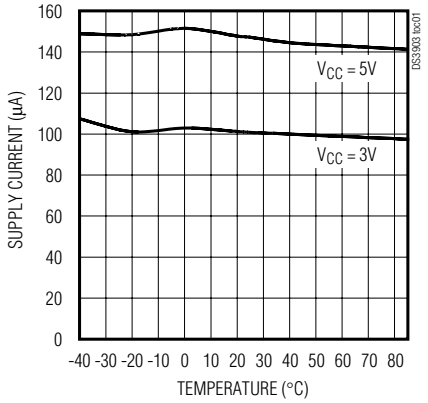
Note 10: Absolute linearity is used to measure expected wiper voltage as determined by wiper position in a voltage-divider configuration.

Note 11: Relative linearity is used to determine the change of wiper voltage between two adjacent wiper positions in a voltage-divider configuration.

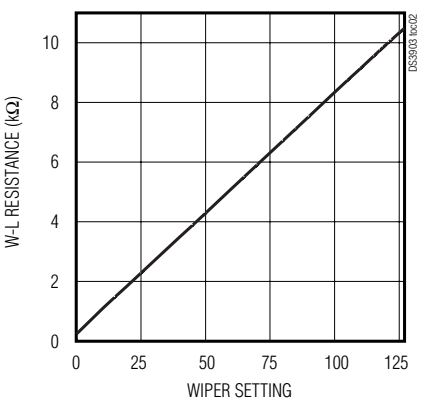
Typical Operating Characteristics

(V_{CC} = 5.0V, 10kΩ plots apply to both pot0 and pot2, T_A = +25°C unless otherwise noted.)

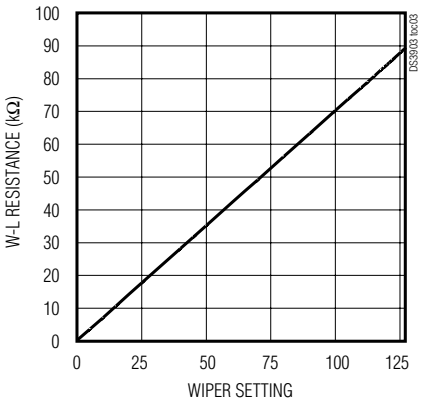
STANDBY SUPPLY CURRENT vs. TEMPERATURE



W-L RESISTANCE vs. WIPER SETTING (10kΩ)



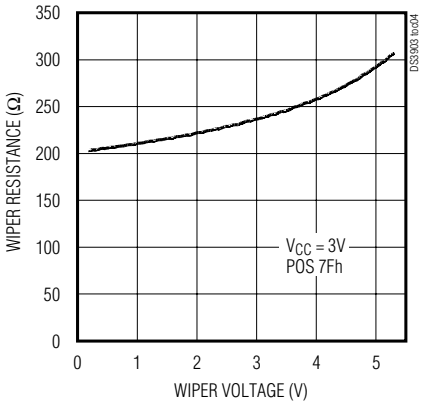
W-L RESISTANCE vs. WIPER SETTING (90kΩ)



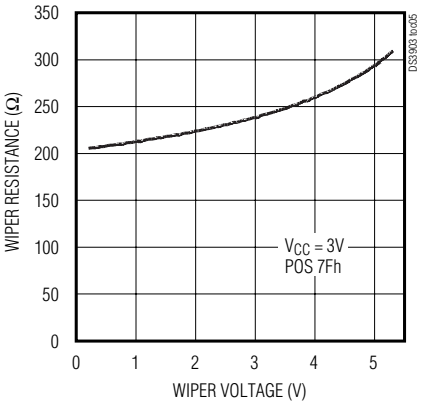
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, 10kΩ plots apply to both pot0 and pot2, T_A = +25°C unless otherwise noted.)

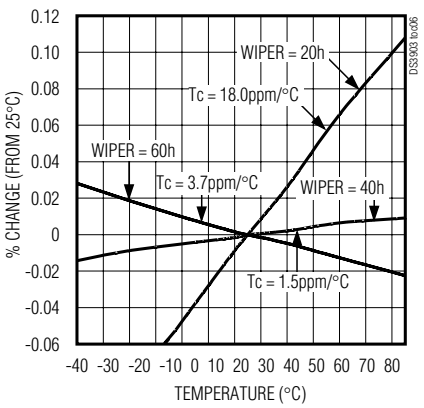
WIPER RESISTANCE vs. WIPER VOLTAGE (10kΩ)



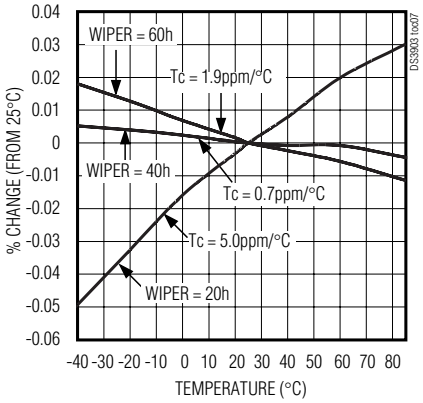
WIPER RESISTANCE vs. WIPER VOLTAGE (90kΩ)



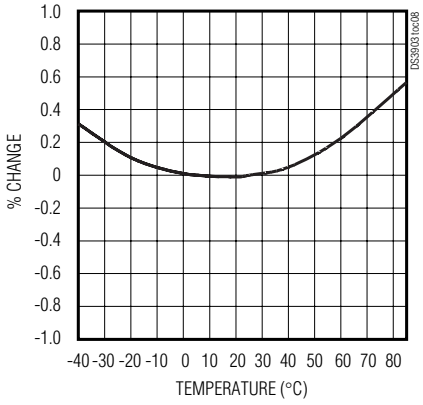
VOLTAGE-DIVIDER PERCENT CHANGE FROM 25°C vs. TEMPERATURE (10kΩ)



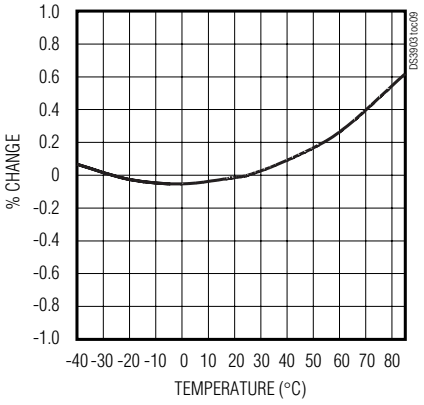
VOLTAGE-DIVIDER PERCENT CHANGE FROM 25°C vs. TEMPERATURE (10kΩ)



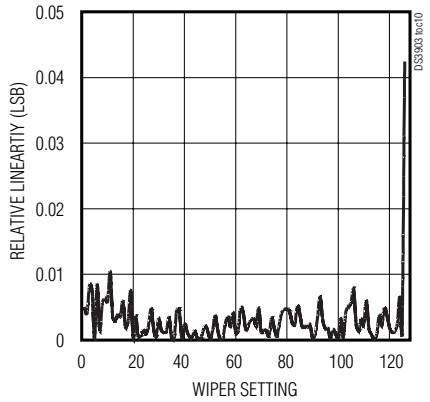
END-TO-END RESISTANCE PERCENT CHANGE FROM 25°C vs. TEMPERATURE (10kΩ)



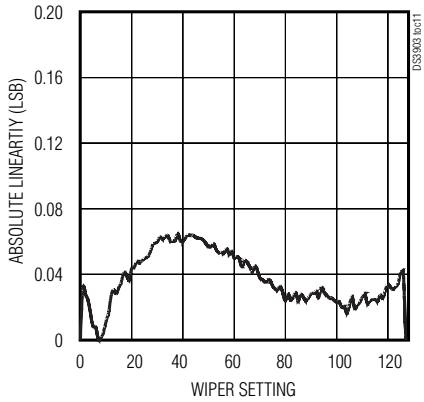
END-TO-END RESISTANCE PERCENT CHANGE FROM 25°C vs. TEMPERATURE (90kΩ)



VOLTAGE-DIVIDER RELATIVE LINEARITY vs. WIPER SETTING (10kΩ)



VOLTAGE-DIVIDER ABSOLUTE LINEARITY vs. WIPER SETTING (10kΩ)

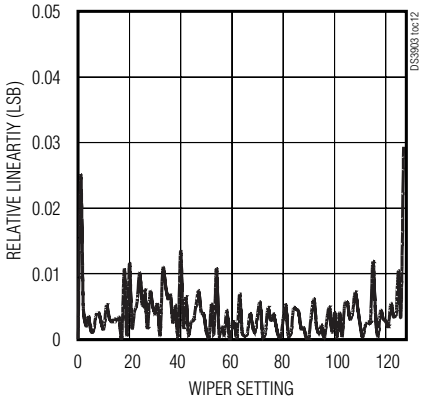


Triple 128-Position Nonvolatile Digital Potentiometer

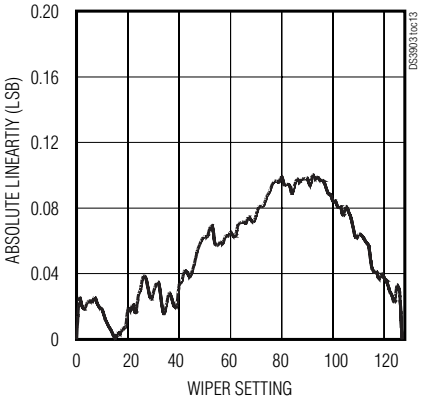
Typical Operating Characteristics (continued)

(VCC = 5.0V, 10kΩ plots apply to both pot0 and pot2, TA = +25°C unless otherwise noted.)

VOLTAGE-DIVIDER RELATIVE LINEARITY vs. WIPER SETTING (90kΩ)



VOLTAGE-DIVIDER ABSOLUTE LINEARITY vs. WIPER SETTING (90kΩ)



Pin Description

PIN	NAME	FUNCTION
1	SDA	2-Wire Serial Data. Input/output for 2-wire data.
2	SCL	2-Wire Serial Clock. Input for 2-wire clock.
3	A0	Address-Select Input. Determines device 2-wire address.
4	WP	Write-Protect Input. Must be grounded to write to the potentiometer registers. An internal pullup locks the potentiometer positions if this pin is not connected.
5, 16, 17 18, 19	N.C.	No Connection
6, 8, 9	L0, L1, L2	Potentiometer Low Terminals. Voltages on these pins should remain between GND and +5.5V while V_{CC} is above +2.7V. Low terminals can be at potentials above the wiper or high terminals.
7, 12, 14	W1, W2, W0	Potentiometer Wiper Terminal. Voltages on these pins should remain between GND and +5.5V while V_{CC} is above +2.7V.
10	GND	Ground Terminal
11, 13, 15	H2, H1, H0	Potentiometer High Terminals. Voltages on these pins should remain between GND and +5.5V while V_{CC} is above +2.7V. High terminals can be at potentials below the low terminals.
20	V_{CC}	Supply Voltage Terminal

Triple 128-Position Nonvolatile Digital Potentiometer

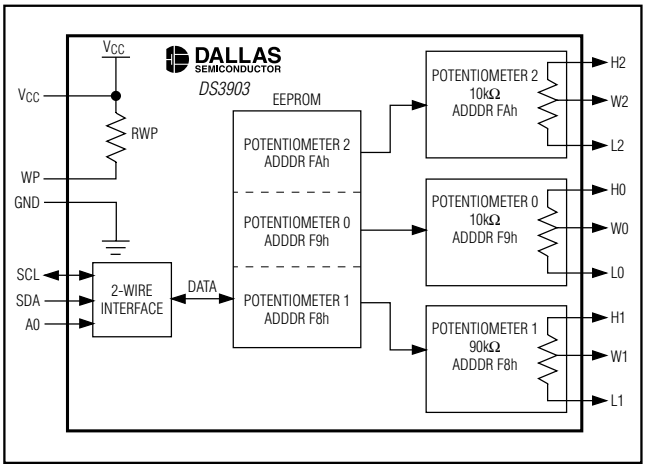


Figure 1. DS3903 Block Diagram

Detailed Description

The DS3903 contains three NV, low-temperature coefficient digital potentiometers. It is accessible through a 2-wire bus, and it serves as a small, low-cost replacement for designs using mechanical potentiometers. The low end-to-end resistance temperature coefficient is especially beneficial for designs using a digital potentiometer as a 2-terminal variable resistor.

It operates in both 3V and 5V systems, and it features a write-protect pin that can lock the positions of the potentiometers. The address pin allows two DS3903s to be placed on the same 2-wire bus.

With its low cost and small board space, the DS3903 is well tailored to replace larger mechanical potentiometers. This allows the automation of calibration in many instances because the 2-wire interface can easily be adjusted by test hardware. Once the system is calibrated, the write-protect pin can be disconnected and the potentiometers retain their settings.

Potentiometer Memory Organization

The potentiometers of the DS3903 are addressed by communicating with the registers in Table 1.

Device Operation

Clock and Data Transitions

The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin can only change during SCL low time periods. Data changes during SCL high periods indicates a start or stop condition depending on the conditions discussed below. See the timing diagrams for further details (Figures 2 and 3).

Start Condition

A high-to-low transition of SDA with SCL high is a start condition, which must precede any other command. See the timing diagrams for further details (Figures 2 and 3).

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command places the DS3903 into a low-power mode. See the timing diagrams for further details (Figures 2 and 3).

Acknowledge

All address and data bytes are transmitted through a serial protocol. The DS3903 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.

Standby Mode

The DS3903 features a low-power mode that is automatically enabled after power-on, after a stop command, and after the completion of all internal operations.

Memory Reset

After any interruption in protocol, power loss, or system reset, the following steps reset the DS3903:

1) Clock up to nine cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a start condition while SDA is high.

Device Addressing

The DS3903 must receive an 8-bit device address word following a start condition to enable a specific device for a read or write operation. The address word is clocked into the DS3903 MSB to LSB. The address

Table 1. Potentiometer Registers

ADDRESS	POTENTIOMETER	END-TO-END RESISTANCE	NUMBER OF POSITIONS
F8h	Pot 1	90kΩ	*128 (00h to 7Fh)
F9h	Pot 0	10kΩ	*128 (00h to 7Fh)
FAh	Pot 2	10kΩ	*128 (00h to 7Fh)

**The most significant bit of each potentiometer position value is ignored. Writing a value greater than 7Fh to any of the potentiometer registers results in a valid 7-bit position, without regard to the value of the most significant bit. Example: position 0x82 is the same as position 0x02.*

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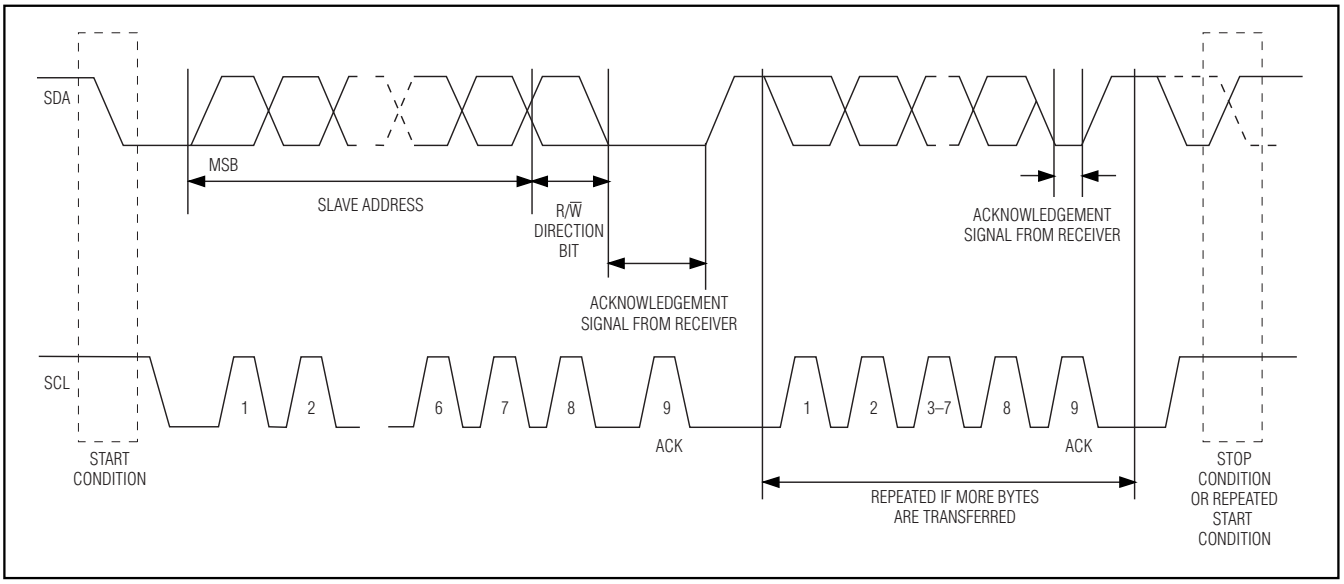

Figure 2. 2-Wire Data Transfer Protocol

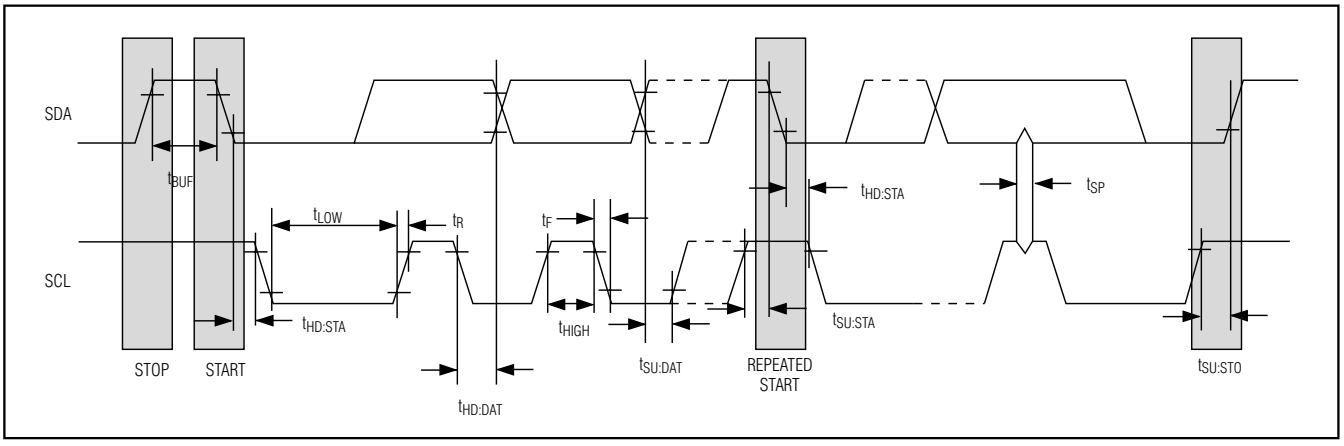

Figure 3. 2-Wire AC Characteristics

word consists of 101000 binary followed by A0 then the R/W bit. If the R/W bit is high, a read operation is initiated. If the R/W bit is low, a write operation is initiated. For a device to become active, the value of A0 must be the same as the hard-wired address pins on the DS3903. Upon a match of written and hard-wired addresses, the DS3903 outputs a zero for one clock cycle as an acknowledge. If the address does not match, the DS3903 returns to a low-power mode.

Write Operations

After receiving a matching device address byte with the R/W bit set low, the device goes into the write mode of operation. The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After the byte has been received, the DS3903 transmits a zero for one clock cycle to acknowledge the memory address has been received. The master must then transmit an 8-bit data word to be written into this memory address. The DS3903 again transmits a zero for one clock cycle to acknowledge the receipt of the data byte. At this point, the master must terminate the write operation with a stop condition. The DS3903 then enters an internally timed

write process t_W to the EEPROM memory. All inputs are disabled during this write cycle.

The DS3903 is capable of an 8-byte page write. A page write is initiated the same way as a byte write, but the master does not send a stop condition after the first data byte. Instead, after the slave acknowledges the data byte has been received, the master can send up to seven more data bytes using the same nine-clock sequence. After a write to the last byte in the page, the address returns to the beginning of the same page. The master must then terminate the write cycle with a stop condition or the data clocked into the DS3903 is not latched into EEPROM. Note that in order for eight bytes to be stored sequentially (and to prevent looping around), the address byte must be set to the beginning of the desired page (three LSBs of the address are 0). For detailed information concerning page operations, see the *Potentiometer Memory Organization* section.

Acknowledge Polling

Once the internally timed write has started and the DS3903 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a start condition followed by the device address. The R/W bit signifies the type of operation that is desired. The read or write sequence is only allowed to proceed if the internal write cycle has completed and the DS3903 responds with a zero.

Read Operations

After receiving a matching address byte with the R/W bit set high, the device goes into the read mode of operation. There are three read operations: current address read, random read, and sequential address read.

Current Address Read

The DS3903 has an internal address register that maintains the address used during the last read or write operation, incremented by one. This data is maintained as long as V_{CC} is valid. If the most recent address was the last byte in memory, then the register resets to the first address. This address stays valid between operations as long as power is available.

Once the device address is clocked in and acknowledged by the DS3903 with the R/W bit set to high, the current address data word is clocked out. The master does not respond with a zero, but does generate a stop condition afterwards.

Random Address Read

A random read requires a dummy byte write sequence to load in the data word address. Once the device address and data address bytes are clocked in by the master, and acknowledged by the DS3903, the master must generate another start condition. The master now initiates a current address read by sending the device address with the R/W bit set high. The DS3903 acknowledges the device address and serially clocks out the data byte.

Sequential Address Read

Sequential reads are initiated by either a current address read or a random address read. After the master receives the first data byte, the master responds with an acknowledge. As long as the DS3903 receives this acknowledge after a byte is read, the master can clock out additional data words from the DS3903. After reaching address FFh, it resets to address 00h.

The sequential read operation is terminated when the master initiates a stop condition. The master does not respond with a zero.

For a more detailed description of 2-wire theory of operation, see the following section.

2-Wire Serial Port Operation

The 2-wire serial port interface supports a bidirectional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions. The DS3903 operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA, SCL, and A0. Timing diagrams for the 2-wire serial port can be found in Figures 2 and 3. Timing information for the 2-wire serial port is provided in the *AC Electrical Characteristics* table for 2-wire serial communications.

The following bus protocol has been defined:

Data transfer can be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain high.

Start Data Transfer: A change in the state of the data line from high to low while the clock is high defines a start condition.

Stop Data Transfer: A change in the state of the data line from low to high while the clock line is high defines the stop condition.

Data Valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figures 2 and 3 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between start and stop conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications, a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS3903 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the stop condition.

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge can be returned.

The master device generates all serial clock pulses and the start and stop conditions. A transfer is ended with a stop condition or with a repeated start condition. Since a repeated start condition is also the beginning of the next serial transfer, the bus is not released.

The DS3903 can operate in the following three modes:

1) **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL, respectively. After each byte is received, an acknowledge bit is transmitted. Start and stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after the slave (device) address and direction bit has been received.
2) **Slave Transmitter Mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS3903 while the serial clock is input on SCL. Start and stop conditions are recognized as the beginning and end of a serial transfer.
3) **Slave Address:** Command/control byte is the first byte received following the start condition from the master device. The command/control byte consists of a 6-bit control code. For the DS3903, this is set as 101000 binary for read/write operations. The next bit of the command/control byte is the device select bit or slave address (A0). It is used by the master device to select which of two devices is to be accessed. When reading or writing the DS3903, the device-select bits must match the device-select pin (A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a '1', a read operation is selected, and when set to a '0', a write operation is selected.

Following the start condition, the DS3903 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 101000 control code,