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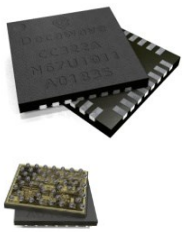
Product Overview



The DW3000 IC family is a fully integrated single chip Ultra Wideband (UWB) low-power low-cost transceiver IC compliant to IEEE802.15.4-2015 and IEEE802.15.4z (BPRF mode). It can be used in 2-way ranging, TDoA and PDoA systems to locate assets to an accuracy of 10 cm.

Key Features

- IEEE802.15.4-2015 UWB IEEE802.15.4z (BPRF mode)
- Supports channels 5 & 9 (6489.6 MHz & 7987.2 MHz)
- Supports 2-way ranging, TDoA and PDoA location schemes
- Low external component count
- Supports enhanced Time-of-Flight security modes
- Integrated HW AES 256
- Worldwide UWB Radio Regulatory compliance
- Low power consumption
- Data rates of 850 kbps and 6.8 Mbps
- Packet length up to 1023 bytes
- Integrated MAC support features
- Up to 38 MHz SPI interface
- QFN40 (5mm x 5 mm) and WLCSP52 (3.1mm x 3.5mm) package options

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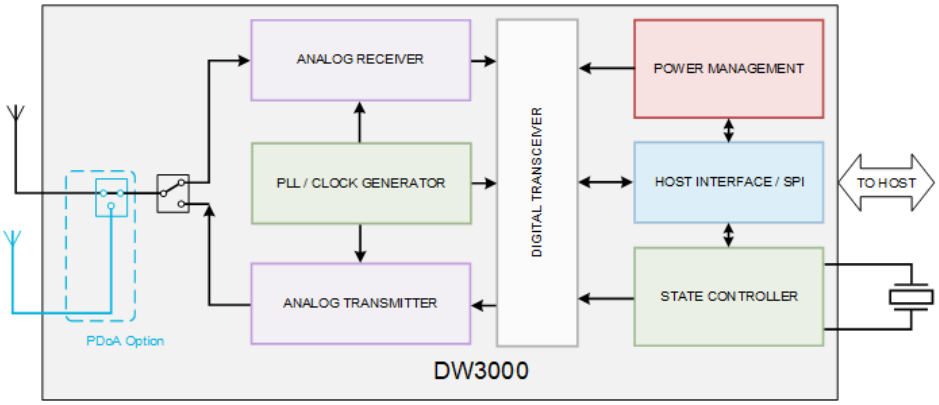
Key Benefits

- Provides precision location and data transfer simultaneously
- Asset location to an accuracy of 10 cm
- High multipath fading immunity
- Secure ranging/distance measurement
- Supports high tag densities in RTLS
- Low cost precision location
- Suitable for coin cell applications

Applications

- Precision real time location systems (RTLS) using two-way ranging, TDoA or PDoA schemes in a variety of markets:
  - Healthcare
  - Consumer
  - Industrial
  - Automotive
- Presence detection for secure entry and secure payment
- Location aware wireless sensor networks



High Level Functional Diagram

DW3000 *UWB Transceiver*

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DOCUMENT INFORMATION

Disclaimer

Decawave reserves the right to change product specifications without notice. As far as possible changes to functionality and specifications will be issued in product specific errata sheets or in new versions of this document. Customers are advised to check with Decawave for the most recent updates on this product.

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Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

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The DW3000, as supplied from Decawave, has not been certified for use in any particular geographic region by the appropriate regulatory body governing radio emissions in that region although it is capable of such certification depending on the region and the manner in which it is used.

All products developed by the user incorporating the DW3000 must be approved by the relevant authority governing radio emissions in any given jurisdiction prior to the marketing or sale of such products in that jurisdiction and user bears all responsibility for obtaining such approval as needed from the appropriate authorities.

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1 IC DESCRIPTION

DW3000 is a fully integrated low-power, single chip CMOS RF 6.5GHz-8GHz IR-UWB transceiver IC compliant with the IEEE 802.15.4-2015 (HRP UWB PHY), IEEE 802.15.4z and IEEE 802.15.8 standards.

DW3000 consists of an analog front end containing a receiver and a transmitter and a digital back end that interfaces to an off-chip host processor. A TX/RX switch is used to connect the receiver or transmitter to the antenna port. Temperature and voltage monitors are provided on-chip.

The receiver consists of an RF front end which amplifies the received signal in a low-noise amplifier before down-converting it directly to baseband. The receiver is optimized for wide bandwidth, high linearity and low noise figure. This allows each of the supported IEEE802.15.4-2015 UWB channels to be down converted with minimum additional noise and distortion. The baseband signal is demodulated and the resulting received data is made available to the host controller via SPI.

The transmit pulse train is generated by applying digitally encoded transmit data to the analog pulse generator. The pulse train is up-converted to a carrier generated by the synthesizer and centred on one of the permitted IEEE802.15.4-2015 UWB channels. The modulated RF waveform is amplified before transmission from the external antenna.

A variant of the IC is available which has two RF antenna ports and is used for Phase Difference of Arrival (PDoA) applications. In this variant the receiver switches between antenna ports to enable a PDoA measurement.

The IC has an on-chip One-Time Programmable (OTP) memory. This memory can be used to store calibration data such as TX power level and crystal initial frequency error adjustment.

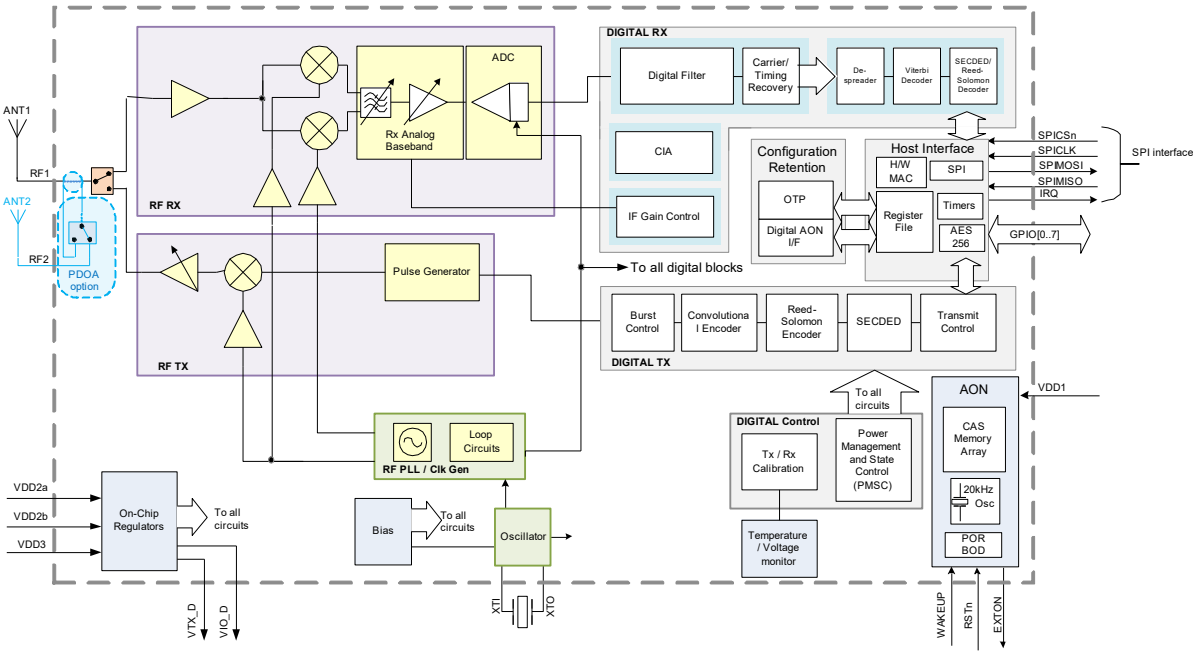


Figure 1: IC Block Diagram

The Always-On (AON) memory is 256 bytes and can be used to retain DW3000 configuration data during the lowest power operational states. The AON can operate directly from battery. This data is downloaded during crystal start up automatically.

DW3000 contains a phase-locked-loop (PLL) with integrated loop filters. This PLL provides the RF local oscillator signals for the Rx Mixer and the Tx RF frequency carrier to the Tx mixer. The channel information signal defines the output channel frequency as follows; channel 5 = 6489.6 MHz, channel 9 = 7987.2 MHz

The DW3000 has various debug and test options (RF loopback, event counters. test modes and more) and gives access to internal signals for on-the-bench debugging and to simplify production test.

The DW3000 incorporates Time Stamp system security features to prevent all known hacking type attacks such as ‘imposter’, ‘cicada’, ‘parasite’ ‘record & replay’ attacks etc.

The host interface includes a peripheral-only SPI for device communications and configuration. Several MAC features are implemented including CRC generation, CRC checking and receive frame filtering.

1.1 DW3000 Variants

The following DW3000 variants exists:

Table 1: DW3000 variants

IC Variant	Type of package	Number of balls/pads	PDoA support	Operating Temperature
DW3110	WLCSP	52	No	-40℃ to +85℃
DW3120	WLCSP	52	Yes	
DW3210	QFN	40	No	
DW3220	QFN	40	Yes	

1.2 DW3000 Backwards compatibility with DW1000

DW3000 is backward compatible with DW1000 on channel 5 and for data rates of 6.8 Mb/s and 850 kb/s.

2 PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

The DW3000 chip can be supplied in two packages, QFN (40 pads) or WLSCP (52 balls). The pin assignments for packages is illustrated on Figure 2 and Figure 3 and the description is given in the Table 2 below.

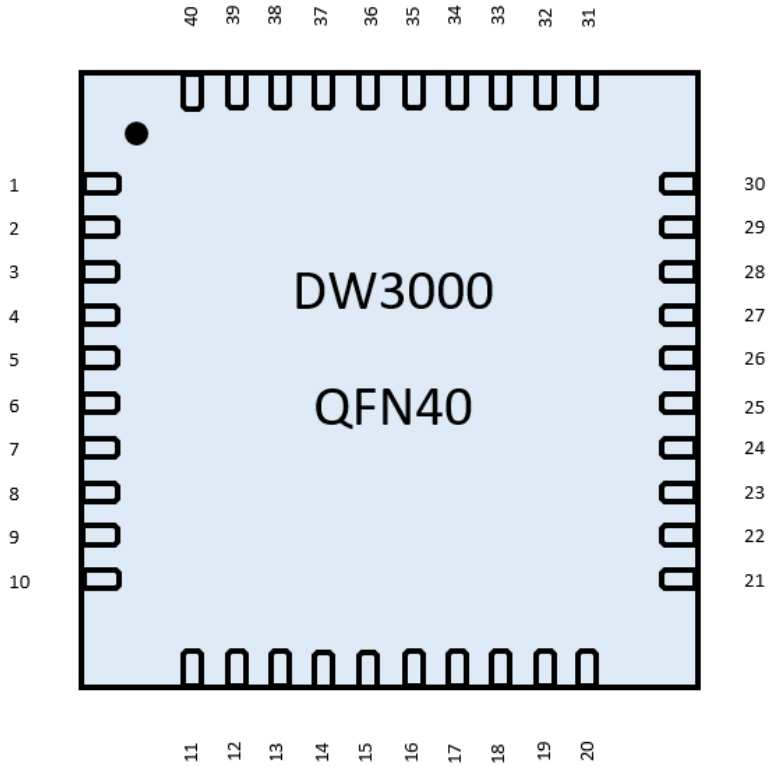


Figure 2: The QFN Top view pin assignments

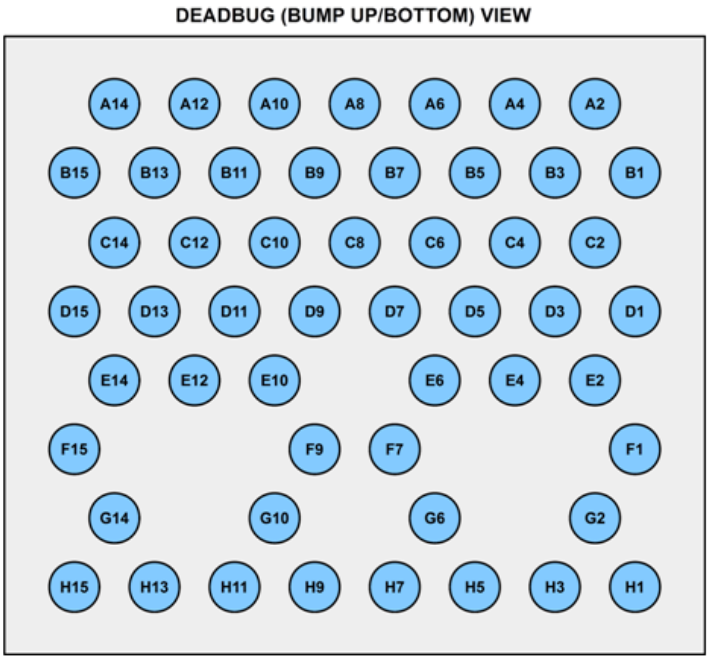


Figure 3: The WLCSP pin assignments

Table 2: DW3000 QFN & WLCSP Pin functions

Signal Name	QFN Pin #	WLCSP Ball #	I/O Type (default)	DESCRIPTION
IRQ	1	B-1	DIO (O-L)	Interrupt request output from the DW3000 to the host processor. By default IRQ is an active-high output but may be configured to be active low if required. For correct operation in SLEEP and DEEPSLEEP modes it should be configured for active high operation. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts on the host unless pulled low externally (100kΩ recommended). When the IRQ functionality is not being used the pin may be reconfigured as a general purpose I/O line[2], GPIO8.
GPIO6 / EXTRXE / SPIPHA	2	C-4	DIO (I)	General purpose I/O pin[2]. On power-up it acts as the SPIPHA (SPI phase selection) pin for configuring the SPI mode of operation. It may be configured for use as EXTRXE (External Receiver Enable). This pin goes high when the DW3000 is in receive mode. After power-up, the pin will default to a General Purpose I/O pin.
GPIO0/ RXOKLED	3	C-2	DIO (I)	General purpose I/O pin[2]. It may be configured for use as a RXOKLED driving pin that can be used to light a LED on reception of a good frame.
GPIO1/ SFDLED	4	D-3	DIO (I)	General purpose I/O pin[2]. It may be configured for use as a SFDLED driving pin that can be used to light a LED when SFD (Start Frame Delimiter) is found by the receiver.
GPIO5 / EXTTXE / SPIPOL	5	D-1	DIO (I)	General purpose I/O pin[2]. On power-up it acts as the SPIPOL (SPI polarity selection) pin for configuring the SPI operation mode. After power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as EXTTXE (External Transmit Enable). This pin goes high when the DW3000 is in transmit mode.
GPIO2 / RXLED	6	E-4	DIO (I)	General purpose I/O pin[2]. It may be configured for use as a RXLED driving pin that can be used to light a LED during receive mode.
GPIO3 / TXLED	7	E-2	DIO (I)	General purpose I/O pin[2]. It may be configured for use as a TXLED driving pin that can be used to light a LED following a transmission.
GPIO4/ EXTPA	8	F-1	DIO (I)	General purpose I/O pin[2]. It may be configured for use as EXTPA (External Power Amplifier). This pin can enable an external Power Amplifier.
GPIO7/ SYNC	9	G-2	DIO (I)	The SYNC input pin is used for external synchronisation. When the SYNC input functionality is not being used this pin may be reconfigured as a general purpose I/O pin[2], GPIO7. This pin is internally pulled down.
GND	10 11 12	E-6 E-10 E-12 F7	G	RF ground pin[1].
RF2	13	H-5	AIO	RF port for antenna 2 (50 Ω single ended RF connection). When in use for PDoA, a series 2pF is required on the pin. In non PDoA chip variants, a 2pF is **not** required, but it should be grounded with 50 Ω. A 50 Ω PCB trace from the RF2 port to the termination resistor is also required in this case.
GND	14 15 16 17	F-9 G-6 G-10 H-1 H-3	G	RF ground pin[1].
RF1	18	H-11	AIO	RF port for antenna 1 (50 Ω single ended connection). A 2pF is required on the pin.

Signal Name	QFN Pin #	WLCSP Ball #	I/O Type (default)	DESCRIPTION
GND	19 20	H-7 H-9 H-13	G	RF ground pin[1].
XTI	21	H-15	AI	Reference crystal input or external reference overdrive pin.
XTO	22	G-14	AI	Reference crystal output.
VDD2a	28	F-15	P	Voltage Supply (2.4V to 3.6V)[1]. F-15 requires isolation with a ferrite from B-15.
VDD2b	23	B-15	P	Voltage Supply (2.4V to 3.6V)[1].
VSS2	24	D-11 E-14	G	Ground return for VDD2.
VSS3	25	C-12 D-13	G	Ground return for VDD3.
VDD3	26	D-15	P	Voltage Supply (1.5V to 3.6V)[1].
VTX_D	27	C-14	PD	TX supply decoupling. Requires external capacitor to ground[1].
VDD1	29	B-13	P	Main power supply (1.62V – 3.6V). This pin also supplies the device I/O's and Always-On domain[1]. The following I/Os are supplied by this pin: WAKEUP, EXTON, RSTn, SPICLK, SPICSn, SPICDI and SPICDO.
VSS1	30	A-14 B-11 C-8 C-10 D-9	G	Ground return for VDD1.
EXTON	31	A-12	DO (O-L)	External device enable. Asserted during wake up process and held active until device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode so as to minimise power consumption.
WAKEUP	32	B-9	DI	When asserted into its active high state, the WAKEUP pin brings the DW3000 out of SLEEP or DEEPSLEEP states into operational mode. This should be connected to ground if not used.
RSTn	33	A-10	DIO (O-H)	Reset pin. Active Low Output. May be pulled low by external open drain driver to reset the DW3000. Must not be pulled high by external source.
SPICLK	34	A-8	DI	SPI peripheral clock input.
SPICDI (SPIMOSI)	35	B-7	DI	SPI peripheral data input.
SPICDO (SPIMISO)	36	A-6	D0 (O-L)	SPI peripheral data output.
SPICSn	37	B-5	DI	SPI chip select. This is an active low enable input. The high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also act as a wake-up signal to bring DW3000 out of either SLEEP or DEEPSLEEP states.
VIO_D	38	A-4	PD	IO supply decoupling. Internally connected to the VDD1 with switch to allow disconnect from VDD1 for ultra-low power consumption mode.
VSS	39 40	A-2 B-3 C-6 D-5 D-7	G	Ground return for internal digital supply[1].

[1] Reference to the schematics and the layout
[2] GPIO pins are not suitable to drive LEDs directly. See Table 5 for details of the maximum current limit.

Table 3: Abbreviations

ABBREVIATION	EXPLANATION
AI	Analog Input.
AIO	Analog Input / Output.
AO	Analog Output.
DI	Digital Input.
DIO	Digital Input / Output.
DO	Digital Output.
G	Ground.
P	Power Supply.
PD	Power Decoupling.
NC	No Connect.
O-L	Defaults to output, low level after reset.
O-H	Defaults to output, high level after reset.
I	Defaults to input.
Note: Any signal with the suffix 'n' indicates an active low signal.	

3 ELECTRICAL SPECIFICATIONS

3.1 Nominal Operating Conditions

Table 4: Nominal Operating Conditions

Parameter	Min	Typ.	Max	Units	Condition/Note
Operating temperature	-40		85	˚C	
Storage temperature	-65		150	˚C	
Supply voltage VDD1	1.62	3.0	3.6	V	
Supply voltage VDD2a and VDD2b	2.4	3.0	3.6	V	
Supply voltage VDD3	1.5	3.0	3.6	V	
Voltage on GPIO0-5, WAKEUP, RSTn, SPICSn, SPIMOSI, SPICLK			3.6	V	Note that 3.6 V is the max voltage that should be applied to these pins.

Note: Unit operation is guaranteed by design when operating within these ranges. Sufficient headroom for any power supply voltage ripple should be considered in system designs.

3.2 DC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V

Table 5: DC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Supply current DEEP SLEEP mode		260		nA	
Supply current SLEEP mode		850			
Supply current IDLE mode channel 5		18		mA	
Supply current IDLE mode channel 9		32			
Supply current IDLE-RC mode		8			
Supply current OSC start-up		1.5			
Current single frame Tx/Rx with 47uF capacitor					
TX CH5		14		mA	Refer to section 6.4.1 for details of single TX frame configuration.
TX CH9		17			
RX CH5		16			Refer to section 6.4.3 for details of single RX frame configuration.
RX CH9		19			
Peak current continuous Tx/Rx					
TX CH5 (nominal power @ -41.3dBm/MHz) VDD2		23		mA	Continuous TX mode is only used as test mode. In normal device operation the TX is powered up for a frame transmission and then powered down.
TX CH5 (nominal power @ -41.3dBm/MHz) VDD3		25			
TX CH5 (maximum power @ -32dBm/MHz). VDD2		29			
TX CH5 (maximum power @ -32dBm/MHz). VDD3		25			
TX CH9 (nominal power @ -41.3dBm/MHz). VDD2		24			
TX CH9 (nominal power @ -41.3dBm/MHz). VDD3		35			
TX CH9 (maximum power @ -32dBm/MHz). VDD2		29			
TX CH9 (maximum power @ -32dBm/MHz). VDD3		35			
RX CH5		72			
RX CH9		88			
Digital input voltage high	0.7 * VDD1			V	

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Digital input voltage low			0.3 * VDD1		
Digital output voltage high	0.7 * VDD1				Assumes 500 Ω load.
Digital output voltage low			0.3* VDD1		
Digital output drive current					
GPIOx, IRQ			0.8	mA	While these IO can drive higher currents than specified, this value should be considered a maximum for continuously loaded operation.
SPICDO	8	10			
EXTON	3	4			

Note: Peak supply currents quoted can be significantly reduced if VDD3 is supplied from a high efficiency SMPS at 1.6V for example.

3.3 Receiver AC Characteristics

Table 6: Receiver AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Centre Frequency Channel 5		6489.6		MHz	
Centre Frequency Channel 9		7987.2		MHz	
Channel bandwidths		499.2		MHz	Programmable.
Input P1dB compression point. Channel 5		-25		dBm	Measured at IC input.
Input P1dB compression point. Channel 9		-32		dBm	Measured at IC input.
In-band blocking level		-80		dBm	Chip referred (power at the pin) to give 1% PER with 3dB desense.
Out-of-band blocking level		-17		dBm	Chip referred (power at the pin) to give 1% PER with 3dB desense (see figure 8 and 9).
Relative velocity between Receiver & Transmitter	0		500	m/s	64 preamble 6.8 Mbps, 12 bytes.

3.4 Receiver Sensitivity Characteristics

The receiver sensitivity measured at the 1% Packet Error Rate (PER).

Table 7 Test conditions of the Rx sensitivity measurements

Parameter	Value
Ambient Temperature	25 ˚C
Supply voltage	3.0V
PHR rate (of data packets)	850Kbps
Payload length (of data packets)	20 bytes
Preamble Code	9
SFD Type for Preamble for frames length 1024	Decawave-defined 16-symbol SFD
SFD Type for Preamble for frames length 64	IEEE 802.15.4z defined 8-symbol SFD
Carrier frequency offset	±10 ppm

Table 8: Rx Sensitivity Characteristics (Channel 5)

Typical Receiver Sensitivity (dBm/500MHz)	Data Rate	Preamble length (symbols)	STS length (symbols)	Conditions
-100	850 Kbps	1024	n/a	See Table 7
-94.3	6.8 Mbps	64	64	See Table 7
-98.6	6.8 Mbps	64	64	No data packets mode. See Table 7

Table 9: Rx Sensitivity Characteristics (Channel 9)

Typical Receiver Sensitivity (dBm/500MHz)	Data Rate	Preamble length (symbols)	STS length (symbols)	Conditions
-99.3	850 Kbps	1024	n/a	See Table 7
-93.2	6.8 Mbps	64	64	See Table 7
-98.0	6.8 Mbps	64	64	No data packets mode. See Table 7

Note: The above typical receiver sensitivities are for DW3110 and DW3210 variants. For PDoA variants (DW3120, DW3220) the RX sensitivity level is approximately 1.4 dB lower (i.e. less sensitive) due to the additional internal PDoA switch.

Reference Clock AC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V

Table 10: Reference Clock AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Crystal oscillator reference frequency		38.4		MHz	A 38.4 MHz signal can be provided from an external reference in place of a crystal if desired.
External Crystal Specifications					
Load capacitance	0		35	pF	Depends on crystal used and PCB parasitics.
Shunt capacitance	0		4	pF	
Drive level			200	µW	Depends on crystal & load capacitance used.
Equivalent Series Resistance (ESR)			60	Ω	
Frequency tolerance			±20	ppm	DW3000 includes circuitry to trim the crystal oscillator to reduce the initial frequency offset.
Crystal trimming range	-20		+20	ppm	Trimming range provided by on-chip circuitry. Depends on the crystal used and PCB design.
External Reference (For example a TCXO)					
Amplitude	0.8		VDD2	Vpp	Must be AC coupled. A coupling capacitor value of 2200 pF is recommended.
SSB phase noise power density			-132	dBc/Hz	@1 kHz offset.
SSB phase noise power density			-145	dBc/Hz	@10 kHz offset.
Duty Cycle	40		60	%	
Internal Fast and Slow Oscillators					
Slow RC Oscillator		23		kHz	User programmable [1]
Fast RC Oscillator		125		MHz	Internally calibrated.

[1]Note: Chip start-up time depends on this clock. The typical frequency of Slow LP OCS reflected the chip start-up time of 913us. With the time, required to download the AON after wake-up, the overall start-up time is ~1000us. It is possible to trim the LP OSC to the higher frequency in software, which would decrease the start-up time to ~770us.

3.5 Transmitter AC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V

Table 11: Transmitter AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Centre Frequency Channel 5		6489.6		MHz	
Centre Frequency Channel 9		7987.2			
Channel Bandwidths		499.2			Programmable.
Output power spectral density (programmable)			-31	dBm/MHz	Using DW3110[1]
Load impedance		50		Ω	Single ended.
Power level range		30		dB	
Power level step		0.5			See figure 6 and figure 7.
Output power variation with temperature		0.02		dB/^{O}C	Channel 5.
		0.01			Channel 9.
Output power variation with voltage		0		dB/V	Internally regulated.
Transmit bandwidth variation with temperature		0.06		MHz/^{O}C	With internal calibration enabled.

[1] The TX power quoted is for the DW3110 (CSP) variant, measured as a mean power in a 1MHz bandwidth. Typically the QFN package variants (DW3210, DW3220) output 2 dB less maximum TX power. For the PDoA variants (DW3120, DW3220) the TX power is reduced by an additional ~1 dB due to insertion loss associated with the internal PDoA switch.

3.6 Link Budget

Using the receiver sensitivity above, expected transmission link budgets can be estimated with the following assumptions:

1. Receiver sensitivities as per Table 11 below.
2. Transmitter and receiver antennas have 0 dBi gain.
3. No losses between the antenna and DW3000 RF pins.
4. The transmitter is operating at an EIRP of -41.3 dBm/MHz (widely used regulatory limit).

Table 12: Typical Link Budget for DW3110

Typical Link Budget (dB)		Data Rate	Preamble length (symbols)	STS length (symbols)	Condition/Note
CH5	CH9				
86	85	850 Kbps	1024	n/a	
91	90		128	n/a	With 12 bytes data → 5 dB gating gain.
89	88	6.8 Mbps	64	64	With 12 bytes data → 9 dB gating gain.
98	97		64	64	No data mode → 9 dB gating gain.

3.7 Temperature and Voltage Monitor Characteristics

Table 13: Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units
Voltage Monitor Range	1.62		3.8	V
Voltage Monitor Accuracy		5		%
Temperature Monitor Range	-40		105	°C
Temperature Monitor Accuracy	-3		3	%

3.8 Location functionality Characteristics

Table 14: Location Accuracy Characteristics

Parameter	Typ.	Units	Condition/Note
Ranging accuracy[1]	+/- 6	cm	In line of sight conditions.
Ranging standard deviation[2]	1.5	cm	
PDoA accuracy[3][4]	+/- 10	deg	
PDoA standard deviation	5	deg	

[1] After calibration is applied. Approximately +/-15cm without calibration.
[2] Ranging standard deviation is measured at -85 dBm power level.
[3] Note: in a typical PDoA based system the computed angle of arrival (AoA) accuracy is better than the PDoA accuracy by a factor of approximately two i.e. if PDoA accuracy is ±10° then AoA accuracy is ±5°.
[4] For optimal PDoA performance a crystal offset of greater than |5| ppm is required between devices.

3.9 Absolute Maximum Ratings

Table 15: Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply voltage	-0.3	4.0	V
Receiver power		14	dBm
Storage temperature	-65	+150	˚C
Operating temperature (Industrial)	-40	+85	˚C
MSL (Moisture sensitivity level) for WLCSP package [1]	1	1	Level
MSL (Moisture sensitivity level) for QFN packages [1]	3	3	Level
ESD (Human Body Model)		2000	V

[1] Note: Tested according JEDEC-JSTD-020 spec.

3.10 Typical performance

3.10.1 Transmit Spectrum

The typical transmit spectrums for channel 5 and channel 9 are on the pictures below.

The UWB configuration is:

- PRF = 64 MHz
- Preamble length = 64 symbols
- STS length = 64 symbols
- Data length = 20 bytes

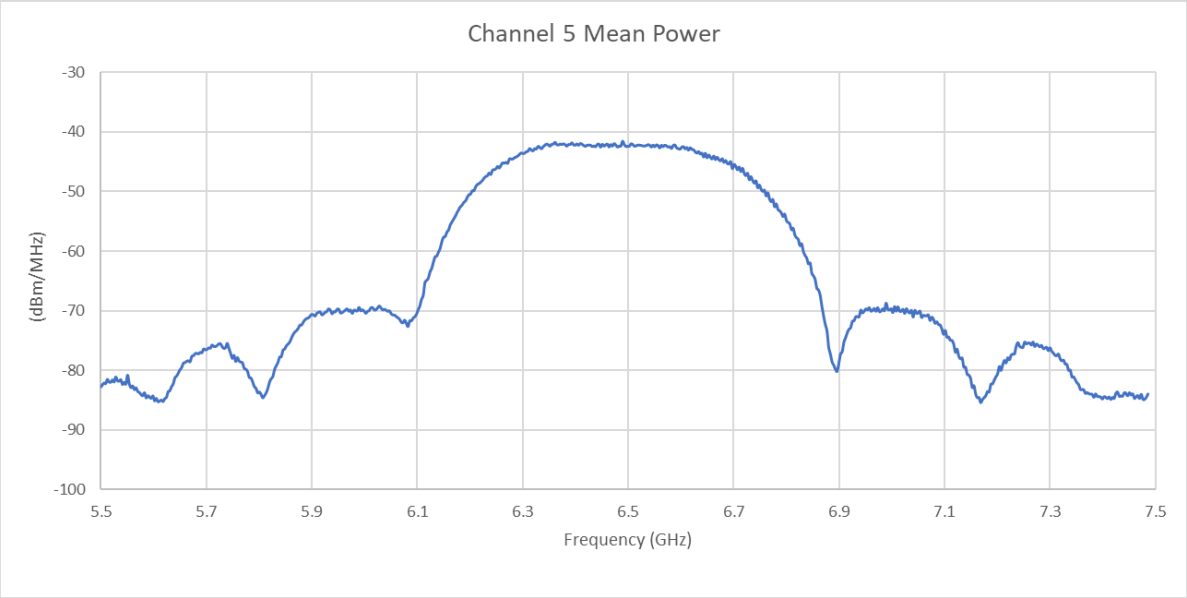


Figure 4: Typical Transmit Spectrum Channel 5

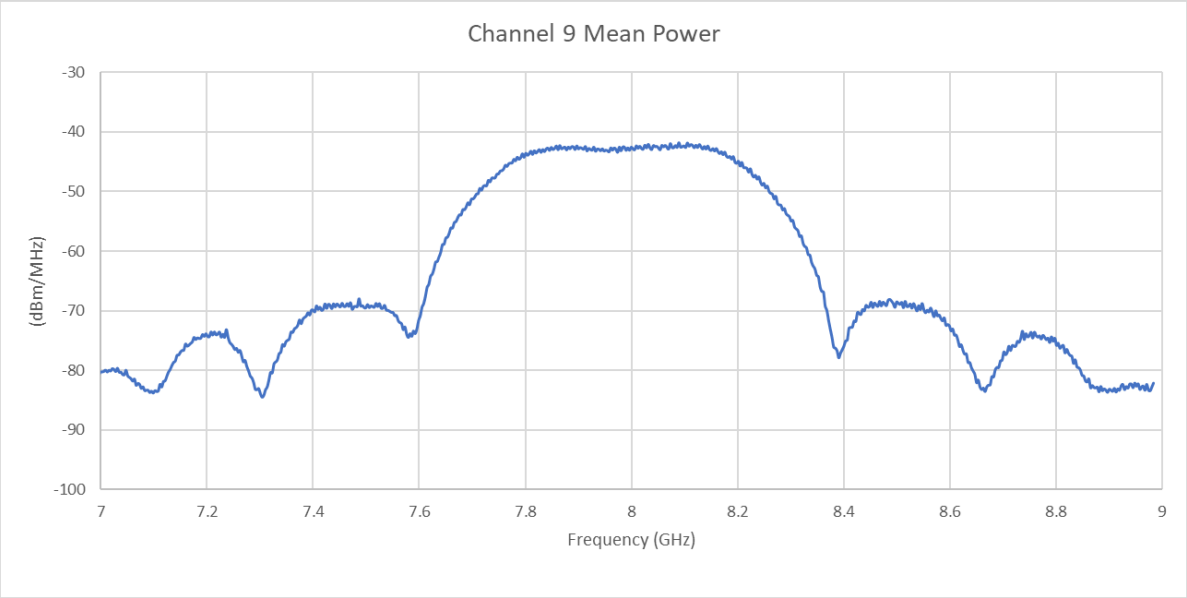


Figure 5: Typical Transmit Spectrum Channel 9

3.10.2 Transmit Power Adjustment

DW3000 has a coarse TX power adjustment and a fine TX power adjustment. The plots below show the relationship between these adjustments for each channel. The y-axis, Power(dB), is the output power in dB below the maximum.

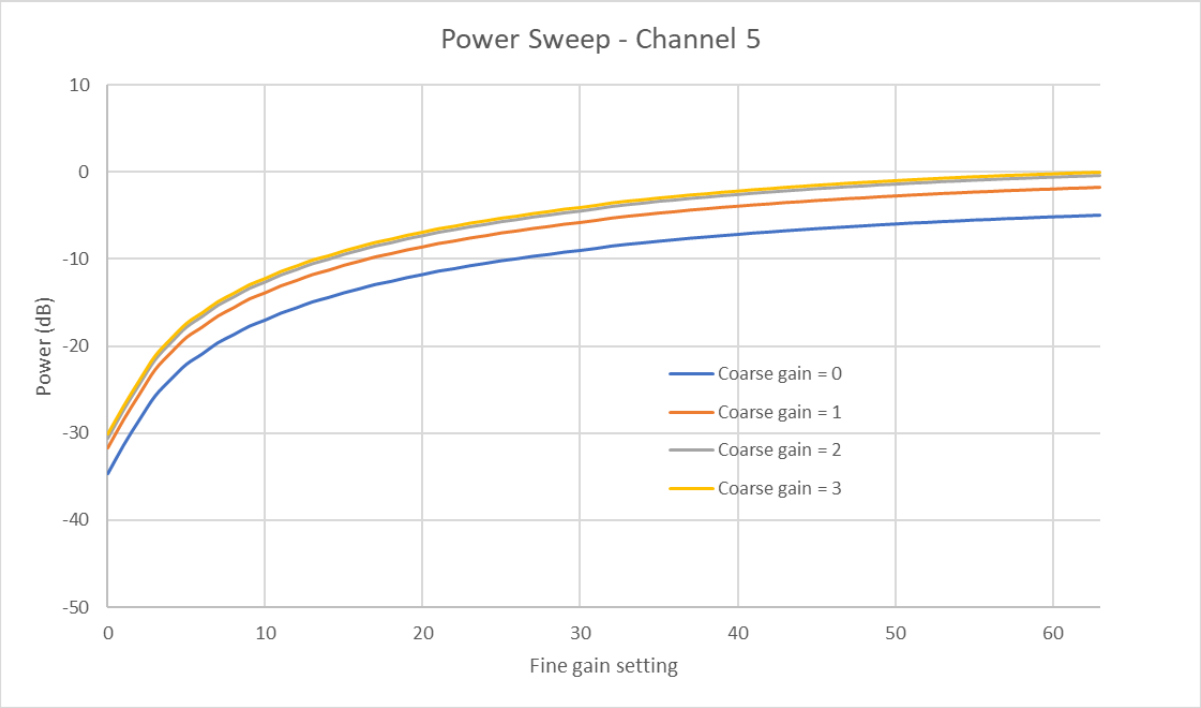


Figure 6 Tx power coarse and fine gain settings Channel 5

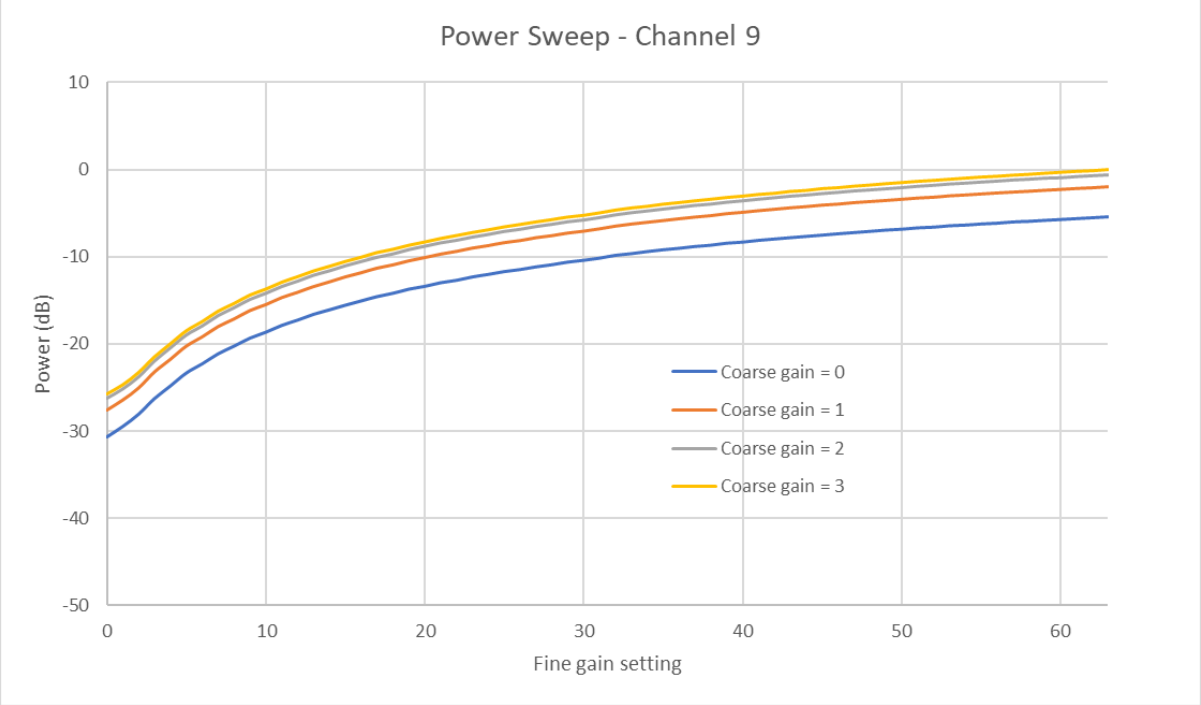


Figure 7 Tx power coarse and fine gain settings Channel 9

3.10.3 Receiver Blocking

The following plots show typical blocking levels to give 1% UWB PER at 3 dB back off from the sensitivity point. The UWB configuration is:

- PRF = 64 MHz
- Preamble length = 64 symbols
- STS length = 64 symbols

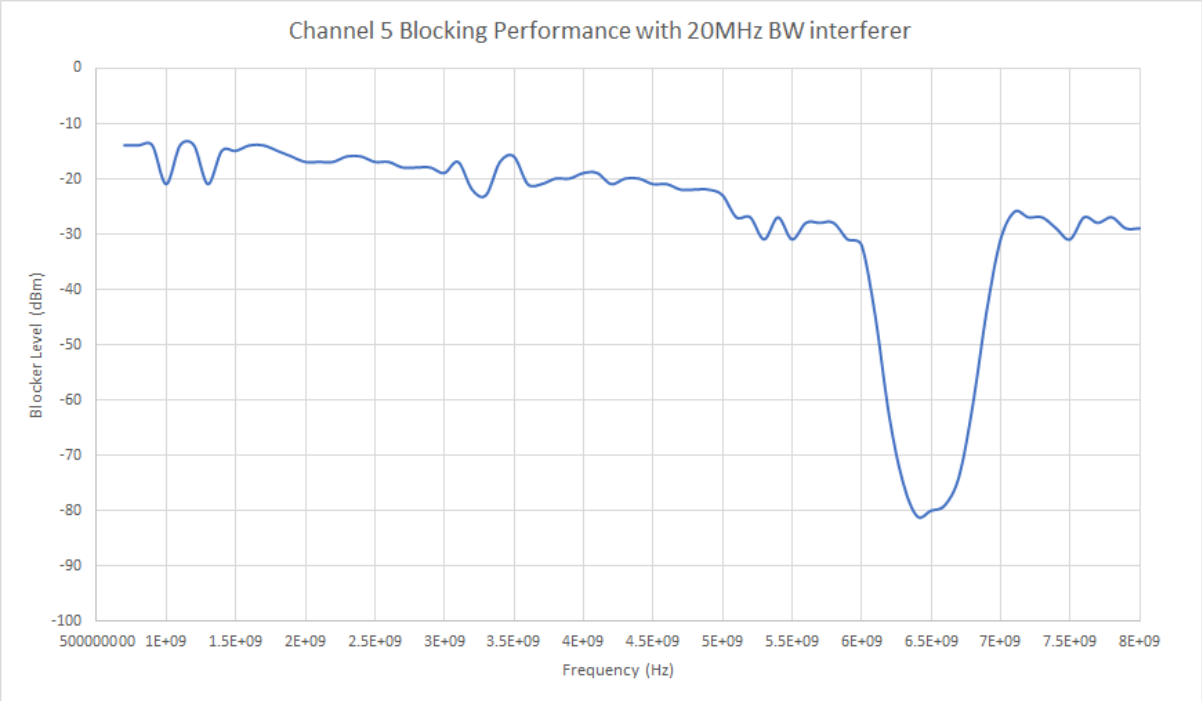


Figure 8 Blocking performance channel 5

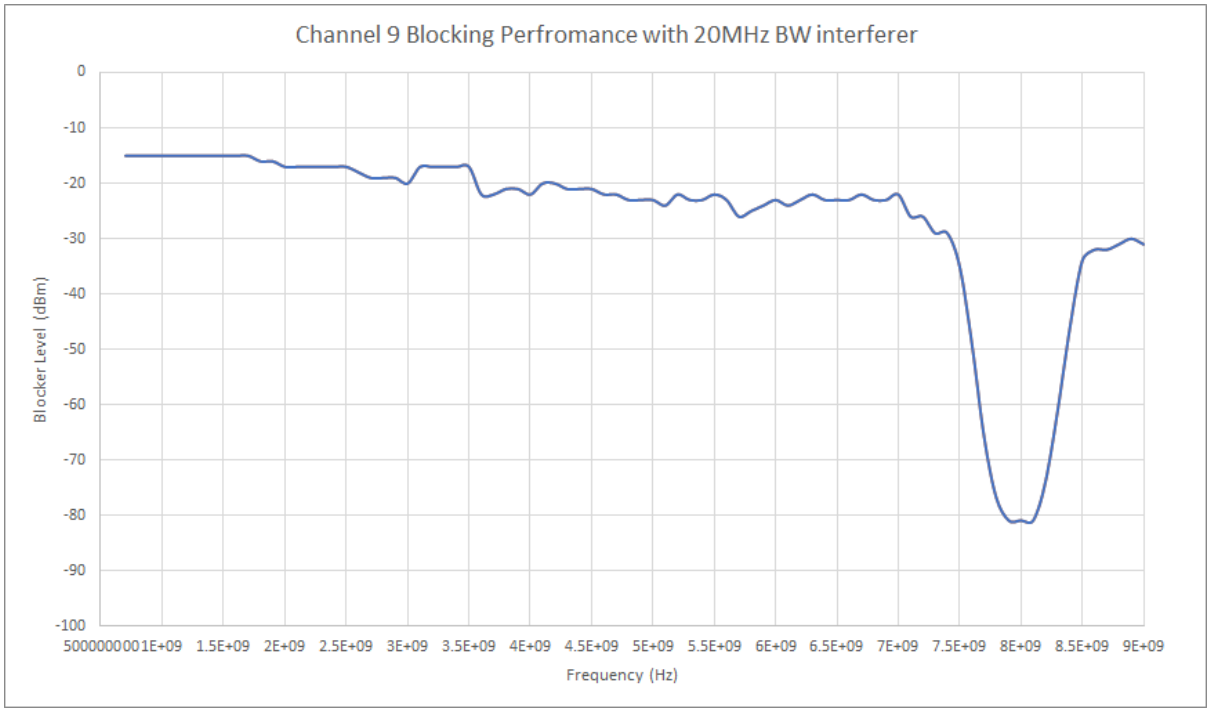


Figure 9 Blocking performance channel 9

3.10.4 Ranging

Typical measured distribution of double sided two-way ranging (DSR) performance.

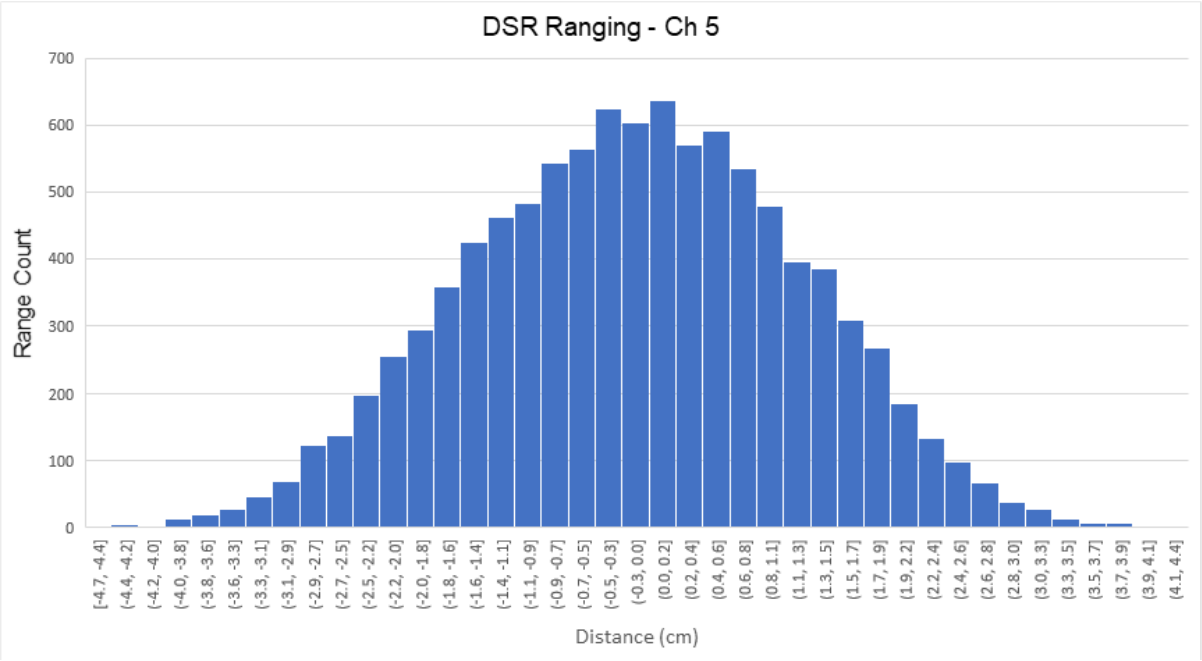


Figure 10 Ranging performance channel 5

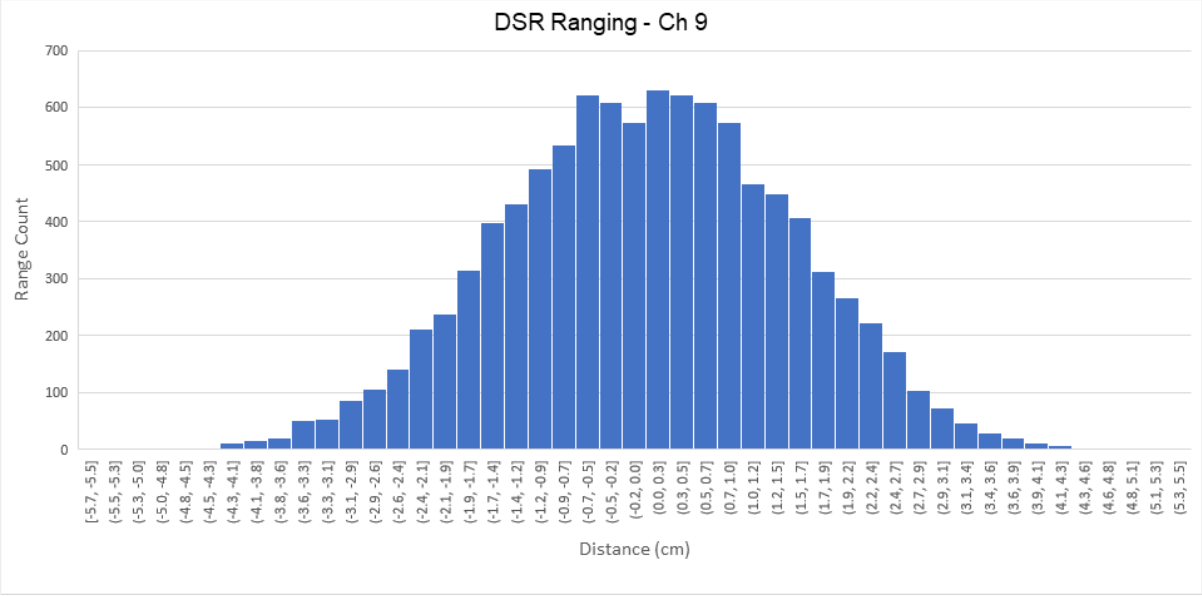


Figure 11 Ranging performance channel 9

4 FUNCTIONAL DESCRIPTION

4.1 Physical Layer Modes

Please refer to IEEE802.15.4-2015 and IEEE802.15.4z for the PHY specification.

4.2 Supported Channels and Bandwidths

The DW3000 supports the following IEEE802.15.4-2015 and IEEE802.15.4z UWB channels:

Table 16 UWB Channels supported

UWB Channel Number	Centre Frequency (MHz)	Bandwidth (MHz)
5	6489.6	499.2
9	7987.2	499.2

4.3 Supported Bit Rates and Pulse Repetition Frequencies (PRF)

The DW3000 supports IEEE802.15.4-2011, IEEE802.15.4-2015 UWB standard bit rates 850 kbps and 6.81 Mbps and nominal PRF values of 16 MHz and 64 MHz. The Base PRF (BPRF) mode of a newly defined draft standard IEEE802.15.4z is also supported.

Table 17 PRF and data rates supported

PRF (MHz)	Data Rate (Mbps)
16[1]	0,85
16[1]	6.81
64[2]	0.85
64[2]	6.81

Actual PRF mean values are slightly higher for SHR as opposed to the other portions of a frame. Mean PRF values are 16.1/15.6 MHz and 62.89/62.4 MHz, nominally referred to as 16 MHz and 64 MHz in this document. Refer to [1], [2] (UWB PHY rate-dependent and timing-related parameters) for full details of peak and mean PRFs.

[1] Backward-compatible for 802.15.4-2011 UWB devices
[2] Base PRF (BPRF) mode of 802.15.4z(draft) and 802.15.4-2011

In general, lower data rates give increased receiver sensitivity, increased link margin and longer range but due to longer frame lengths for a given number of data bytes they result in increased air occupancy per frame and a reduction in the number of individual transmissions that can take place per unit time.
16MHz PRF gives a marginal reduction in transmitter power consumption over 64 MHz PRF (BPRF).

4.4 Symbol timings

Timing durations in IEEE802.15.4 are expressed in an integer number of symbols. This convention is adopted in DW3000 documentation. Symbol times vary depending on the data rate and PRF configuration of the device and the part of the frame. DW3000 can transmit PHR on the 0.85 and 6.81 Mbps data rates. See the table below for symbol timings supported by DW3000.

Table 18 DW3000 Symbol Timings Duration

PRF (MHz)	Data Rate (Mbps)	SHR (ns)	PHR 0.85 Mbps (ns)	PHR 6.81 Mbps (ns)	Data (ns)
16	0.85	993.59	1025.64	-	1025.64
16	6.81	993.59	1025.64	128.21	128.21
64	0.85	1017.63	1025.64	-	1025.64
64	6.81	1017.63	1025.64	128.21	128.21

4.5 Frame Format IEEE802.15.4-2011, IEEE802.15.4-2015

IEEE802.15.4-2011, IEEE802.15.4-2015 frames are structured as shown in Figure 12. Detailed descriptions of the frame format are given in the standard. The frame consists of a synchronisation header (SHR) which includes the preamble symbols and start frame delimiter (SFD), followed by the PHY header (PHR) and data. The data frame is usually specified in number of bytes and the frame format will include 48 Reed-Solomon parity bits following each block of 330 data bits (or less).

While zero length payloads and zero length PHR is supported the maximum frame length is 1023 bytes, including the 2-byte FCS.

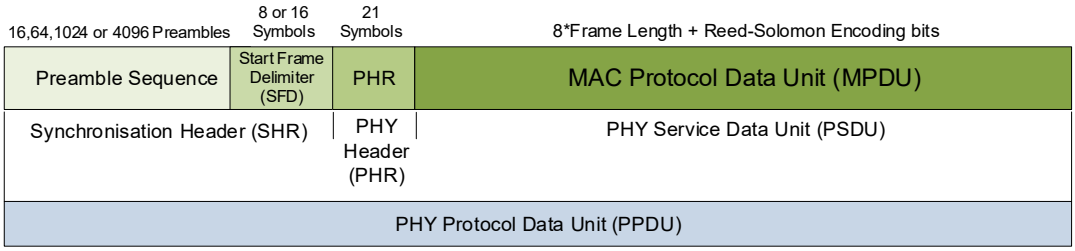


Figure 12: IEEE802.15.4-2011 PPDU Structure

4.6 Packet Formats of IEEE Std 802.15.4z™

The 4z amendment added new packet formats to HRP UWB PHY incorporating a Scrambled Timestamp Sequence (STS) into the packet structure, defining four STS Packet Configurations as shown in Figure 7 below.

The STS is a random sequence of positive and negative pulses generated using an AES-128 based deterministic random bit generator (DRBG). Only valid transmitters and receivers have the correct seed (i.e., the key and IV) to generate the sequence for transmission and to validly cross correlate in the receiver to determine the receive timestamp. The STS provides for secure receive timestamping and secure ranging.

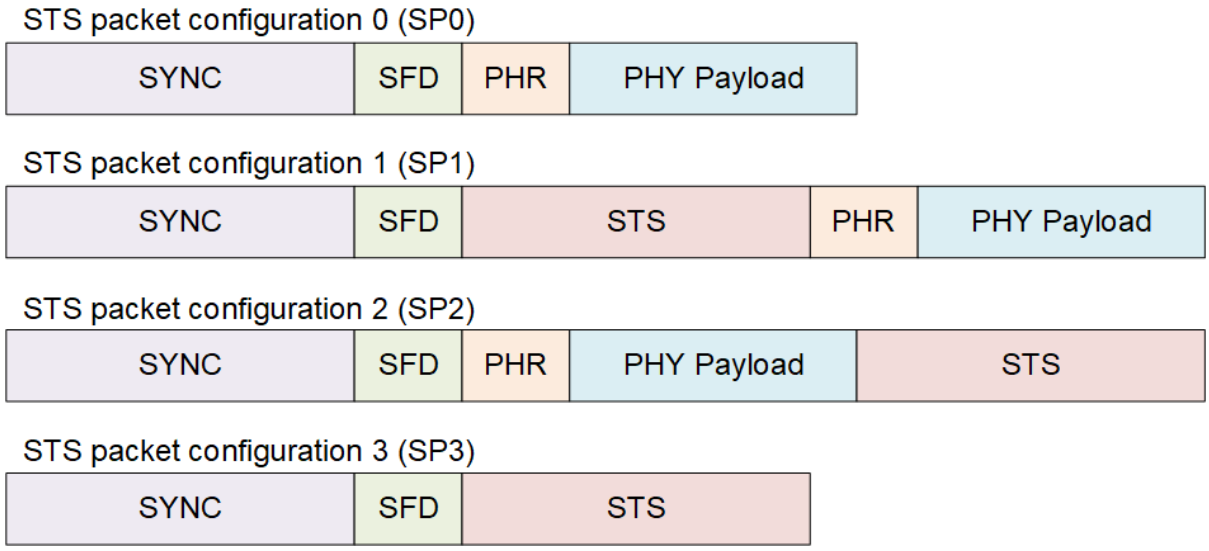


Figure 7: IEEE 802.15.4z HRP UWB PHY PPDU formats

4.7 Proprietary long frames

The DW3000 offers a proprietary long frame mode where frames of up to 1023 bytes may be transferred. Refer to the DW3000 user manual for full details.

4.8 No Data frames

The DW3000 offers zero length payloads and zero length PHR (SP3). This is for use cases where an alternative method of data communications is available.

4.9 Host Controller Interface

The primary interface DW3000 is via a 4 wire SPI interface. DW3000 will act a SPI peripheral device, in non-daisy-chain mode and operate at SPI clock frequencies up to 36MHz.

4.9.1 SPI Functional Description

The host interface to DW3000 is a 4-wire SPI-compatible peripheral. The assertion of SPICSn low by the SPI controller (host) indicates the beginning of a transaction.
The SPI interface is used to read and write registers in the DW3000 device. All data and address transfer on the SPI is most significant bit first. All address bytes are transmitted with MSB first, and all data is transmitted commencing with lowest addressed byte.

- Assertion low of SPICSn initialises transaction.
- De-assertion high of SPICSn ends the SPI transaction.
- The device supports direct and per-byte sub-addressing access to the full register space.
- Efficient block data reading/writing is allowed. Continuous, long transactions can be carried out while the addressed location is auto-incremented on the DW3000 side.

The SPICDO (ex. SPIMISO) I/O of DW3000 is going open-drain when SPICSn is de-asserted, to allow interoperation with other peripherals on the SPI bus.

SPI daisy chaining is not supported. This is the mode where the CDO (ex. SPIMISO), CDI (ex. SPIMOSI) lines are passed through a device when it is not chip selected.

4.9.2 SPI Timing Parameters

The SPI peripheral complies with the Motorola SPI protocol within the constraints of the timing parameters listed in Table 19 and illustrated in Figure 13 and Figure 14.

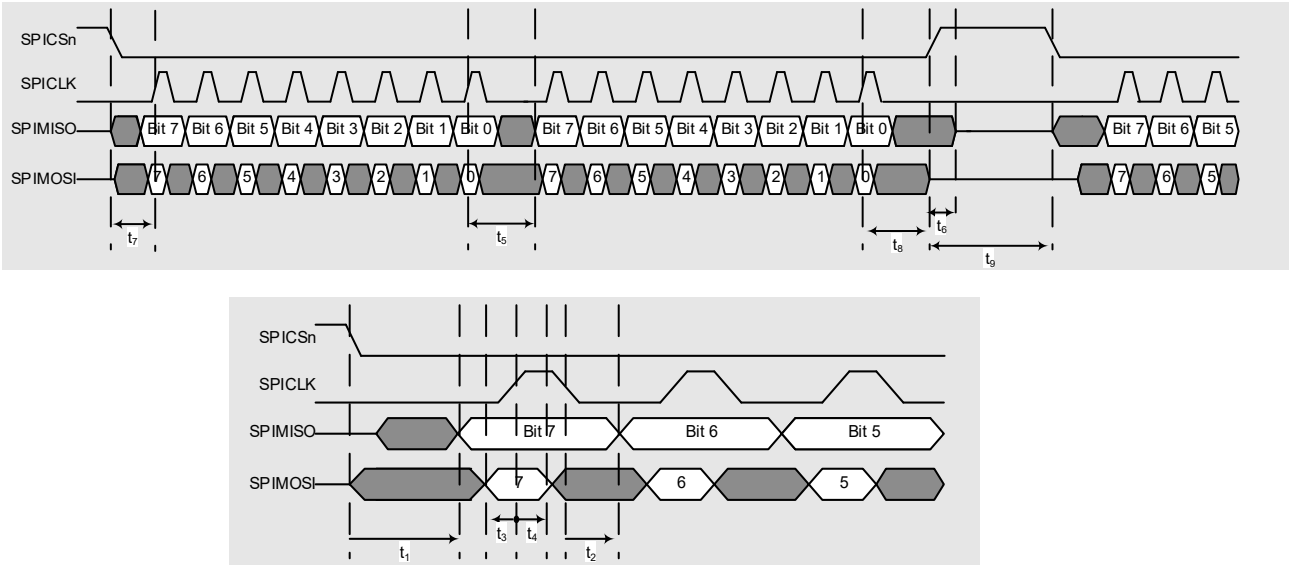


Figure 13: SPI Timing Diagram

Table 19 SPI Timing Parameters

Parameter	Min	Max	Unit	Description
t_1		3	ns	SPICSn asserted low to valid peripheral (DW3000) output data
t_2		8.5	ns	SPICLK low to valid peripheral (DW3000) output data.
t_3	14		ns	Controller data setup time.
t_4	2		ns	Controller data hold time.
t_5	27		ns	LSB last byte to MSB next byte.
t_6		45	ns	SPICSn deasserted high to CDO tristate.
t_7	23		ns	Start time; time from select asserted to first SPICLK.
t_8	24		ns	Last SPICLK to SPICSn deasserted.
t_9	40		ns	Idle time between consecutive accesses.
t_{10}		36[1]	MHz	SPICLK SPI mode 0

[1]Note: SPICLK frequency in CRC mode is 20MHz.

4.9.3 SPI Operating Modes

The SPI interface supports both clock polarities (SPIPOL=0/1) and phases (SPIPHA=0/1), as defined in the Motorola SPI protocol. The DW3000 transfer protocols for each SPIPOL and SPIPHA setting are given in Figure 14 and Figure 15. These modes are selected using GPIO 5 & 6 as follows:

Table 20 SPI Mode Configuration

GPIO 5 (SPIPOL)	GPIO 6 (SPIPHA)	SPI Mode
0	0	0
0	1	1
1	0	2
1	1	3

GPIO 5 and 6 pins are sampled as shown on the Figure 21 and Figure 22 to determine the SPI mode. They are internally pulled low to configure a default SPI mode 0. If mode other than 0 is required, then they should be pulled up using an external resistor of value no greater than 10 kΩ to the VIO_D supply.

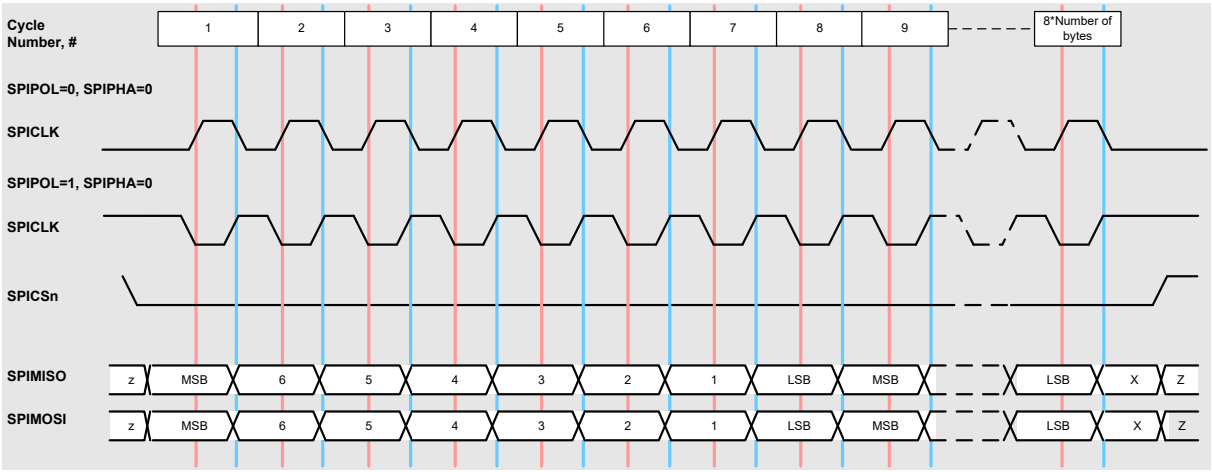


Figure 14: DW3000 SPIPHA=0 Transfer Protocol

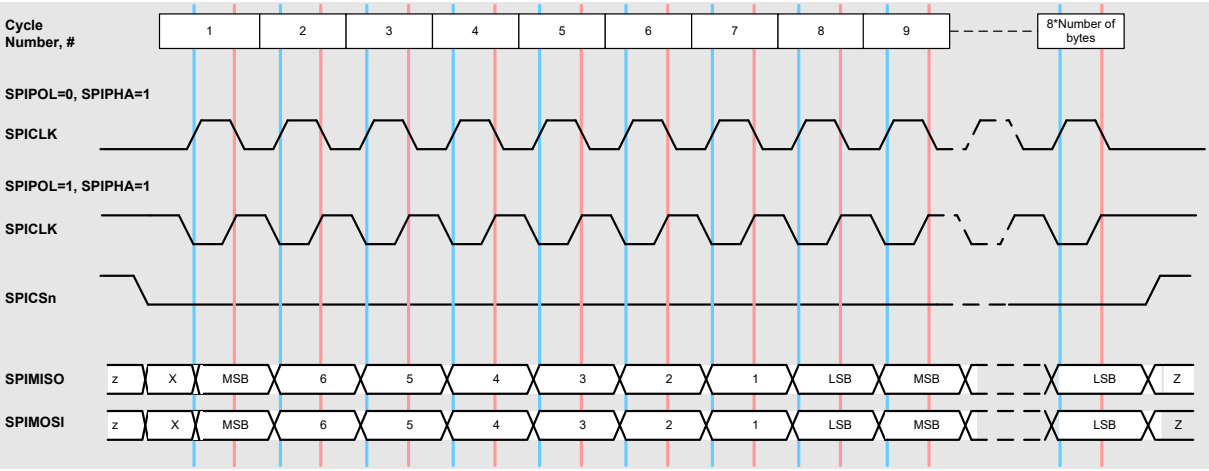


Figure 15: DW3000 SPIPHA=1 Transfer Protocol

4.9.4 SPI Transaction Formatting

The SPI command structure allows for 4 different types of SPI command:

1. Fast, single byte commands. Up to 32 unique commands such as “TX now”, “TX/RX Off”.
2. Fast addressed mode. Allowing for read and write addressing to 32 addresses. This command structure is padded by a trailing bit to allow the SPI address decoder time to fetch any read data. The length of the read is determined by the length of the SPI transaction.
3. Full addressed mode. Allowing for read and write addressing to 32 addresses and up to 128 byte offset addressing. This command structure is padded by a trailing bit to allow the SPI address decoder time to fetch any read data. The length of the read or write is determined by the length of the SPI transaction.
4. Masked write transaction. These are intended to simplify read-modify-write operations by allowing the host to write to an address and apply a set, clear or toggle mask to 1, 2, or 4 bytes. The SPI command decoder then carries out the required read-modify-write instructions internally.

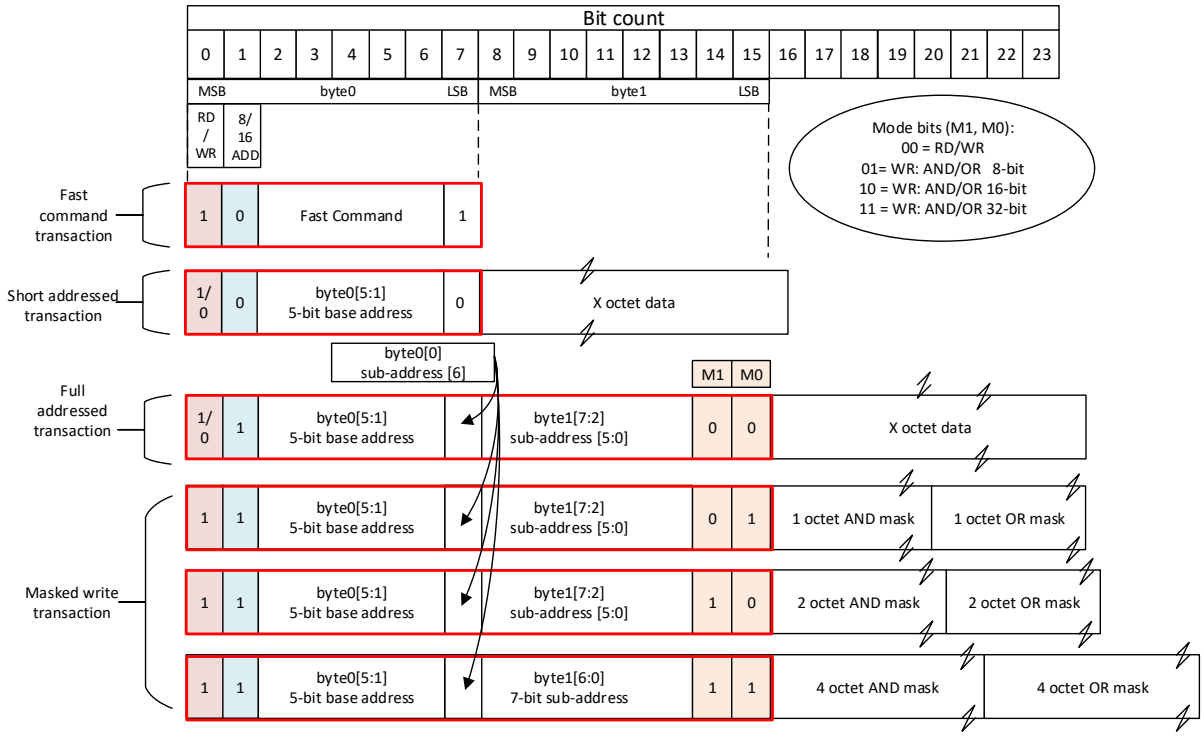


Figure 16: SPI Command Formatting

4.9.5 GPIO and SPI I/O internal pull up/down

All of the GPIO pins have a software controllable internal pull down resistor except for SPICSn, which has a pull up, to ensure safe operation when input pins are not driven. The value of the internal resistors can vary with the VDD1 supply voltage over a range from 10 kΩ (VDD1 is 1.8V) to 30 kΩ (VDD1 is 3.6V).

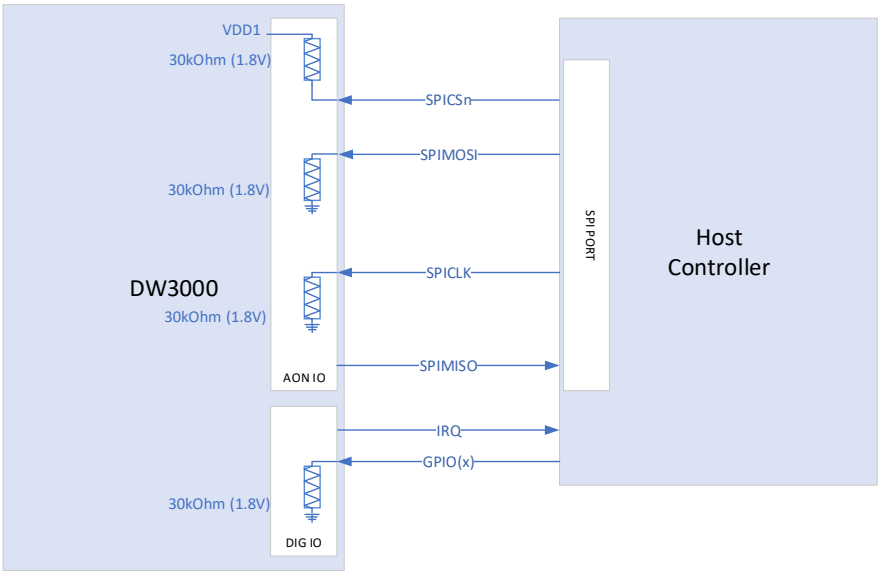


Figure 17: SPI and GPIO pull up/down

4.10 Reference Crystal Oscillator

With the addition of an external 38.4 MHz crystal and appropriate loading capacitors, the on-chip crystal oscillator generates the reference frequency for the integrated frequency synthesizer's RFPLL.
The DW3000 crystal oscillator is used to provide the reference clock to the internal PLL and provides a direct clock source to the digital core when operating in the lower power INIT_RC mode. The oscillator operates at a frequency of 38.4 MHz. A trim facility is provided which can be used to trim out crystal initial frequency error. Typically, a trimming range of ± 20 ppm is possible using a 6-bit trim range. This trimming in 0.125pF steps provides for up to 8 pF additional capacitance on the XTI and XTO crystal connections.

4.10.1 Calculation of external capacitor values for frequency trim

Ideally the value of external loading capacitors (Cext) should be calculated to give an equal trim range about the center trim value. To do this, one needs to estimate the parasitic capacitance (Cpar) between the crystal pads XTI/XTO and the crystal pads. A good starting estimate is usually about 5 pF however some trial and error maybe required initially. The values of Cm, Lm, Rm and Co obtained from the crystal manufacturer are also required.

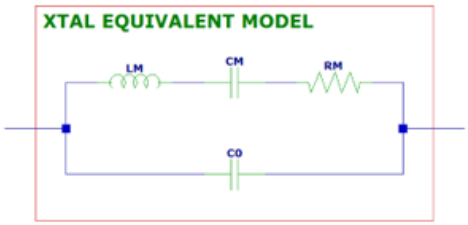


Figure 18 Crystal Model

Using the following formulae, the required Cext and trim range can be estimated where:

fs = series frequency
fp = parallel frequency
Fl = loaded (desired) frequency

]

$$f_S = \frac{1}{2\pi\sqrt{C_M L_M}}$$

$$f_P = f_S\left(\sqrt{1+\frac{C_M}{C_0}}\right)$$

$$f_L = f_S\left(\sqrt{1+\frac{C_M}{C_L}}\right)$$

$$C_L = C_0+\frac{1}{2}\left(C_{TRIM}+C_{PAR}+C_{EXT}\right)$$

$$\Delta f_{ppm} = 10^6 \times \frac{f_L - f_{L_{NOM}}}{f_{L_{NOM}}}$$

A typical crystal trimming plot is shown below:

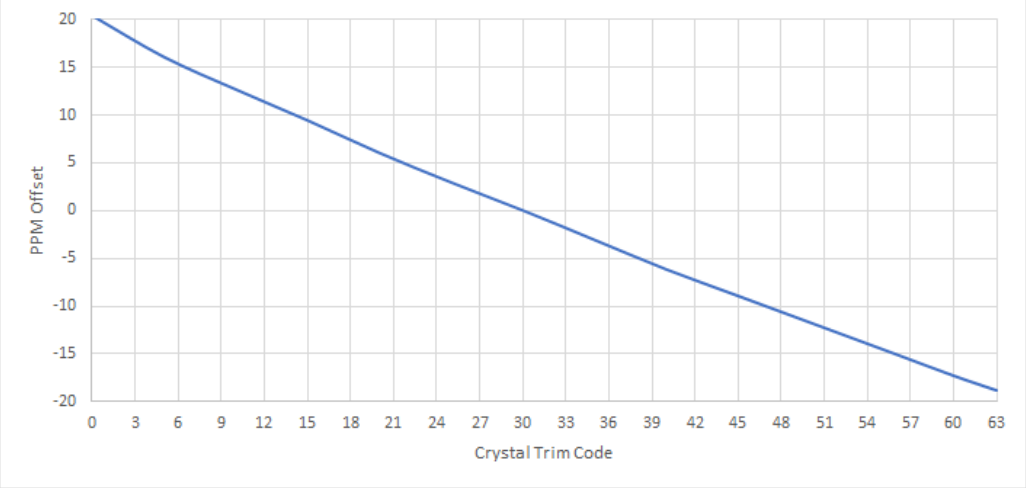


Figure 19 Crystal Trim plot

5 OPERATIONAL STATES

5.1 Overview

DW3000 has a number of basic operations states as described in Table 21.

Table 21: Operating States

State	Description
OFF	Digital core is powered off, digital LDO is disabled. Reset is held low.
INIT_RC	System is clocked from 30MHz RC Osc, SPI comms @ 7MHz. AON download is performed. Automatically goes to IDLE_RC on completion.
IDLE_RC	System is clocked at ~120MHz to allow full speed SPI comms.
IDLE_PLL	System is clocked from the PLL at 124.8MHz.
TX_WAIT	TX blocks are sequenced on as required. Includes DELAYED_TX mode.
TX	Active TX state. Automatically reverts to IDLE_PLL after transmission.
RX_WAIT	RX blocks are sequenced on as required. Includes DELAYED RX mode.
RX	Active RX state. Can revert to IDLE_PLL if packet received or timeout triggers.
SLEEP	Low power state. Sleep counter is clocked from slow RC Osc at ~20kHz.
DEEPSLEEP	Low power state. All clocks off. Wakeup via IO event on WAKEUP or SPICSn, or by resetting the device (RSTn).

5.2 Operating State Transitions

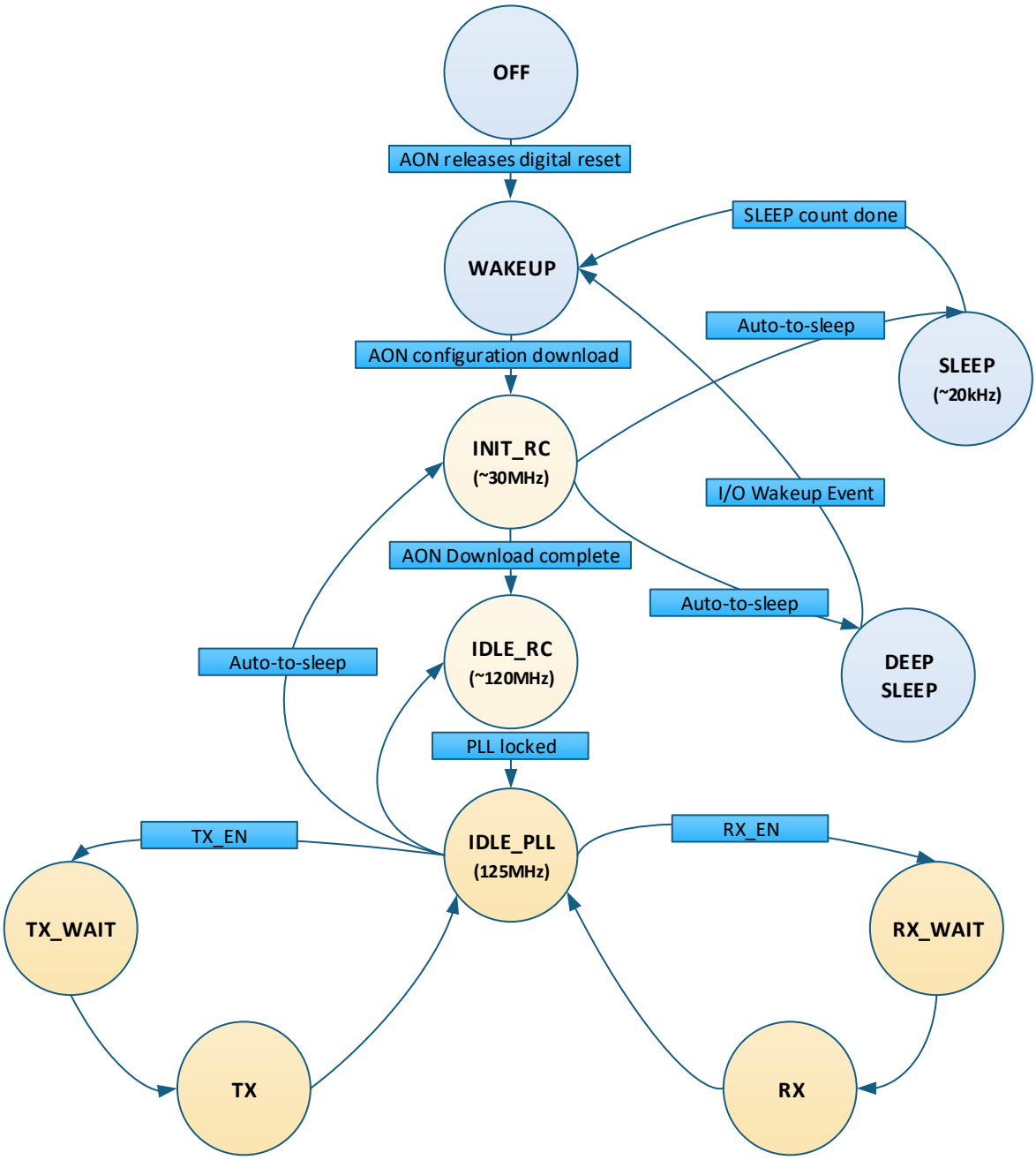


Figure 20: Operating State Transitions

6 POWERING DW3000

DW3000 is designed such that it can be powered in a number of different configurations depending on the application. These options are described below. Figure 21: Timing diagram for cold start POR details the power up sequence when external power sources are applied. The power supply design should ensure that VDD2a/b and VDD3 are stable less than 10ms after VDD1 (3.3V) comes up, otherwise a device reset is required.

When the external power source is applied to the DW3000 for the first time (cold power up), the internal Power On Reset (POR) circuit compares the externally applied supply voltage (VDD1) to an internal power-on threshold (approximately 1.5V), and once this threshold is passed the AON block is released from reset and the external device enable pin EXTON is asserted.

Then the VDD2a and VDD3 supplies are monitored and once they are above the required voltage as specified in the Datasheet (2.2V and 1.4V respectively), the fast RC oscillator (FAST_RC) and crystal (XTAL Oscillator) will come on within 500 µs and 1 ms respectively.

The DW3000 digital core will be held in reset until the crystal oscillator is stable. Once the digital reset is de-asserted the digital core wakes up and enters the INIT_RC state, (see Figure 21 and Figure 22). Then once the configurations stored in AON and OTP have been restored (into the configuration registers) the device will enter IDLE_RC. Then the host can set the AINIT2IDLE configuration bit in SEQ_CTRL and the IC will enable the CLKPLL and wait for it to lock before entering the IDLE_PLL state.

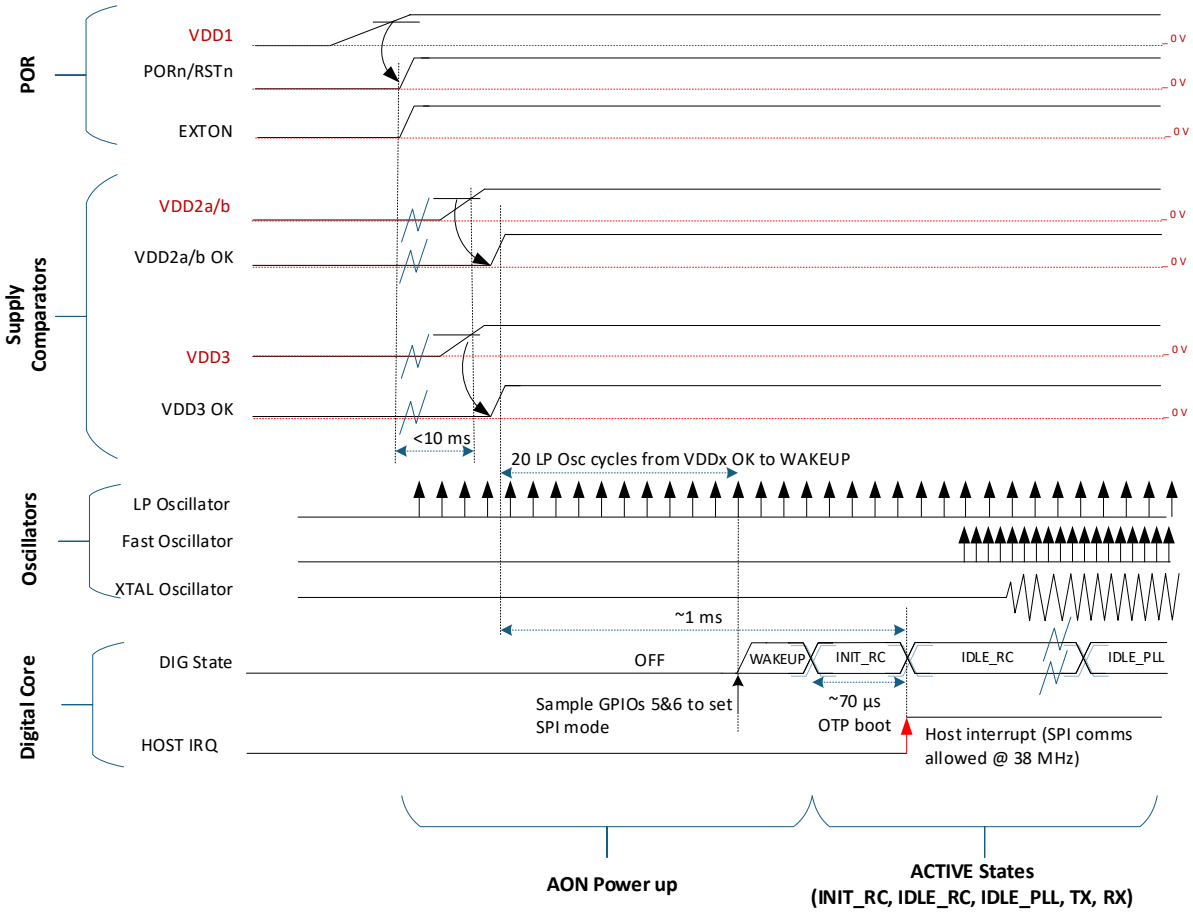


Figure 21: Timing diagram for cold start POR

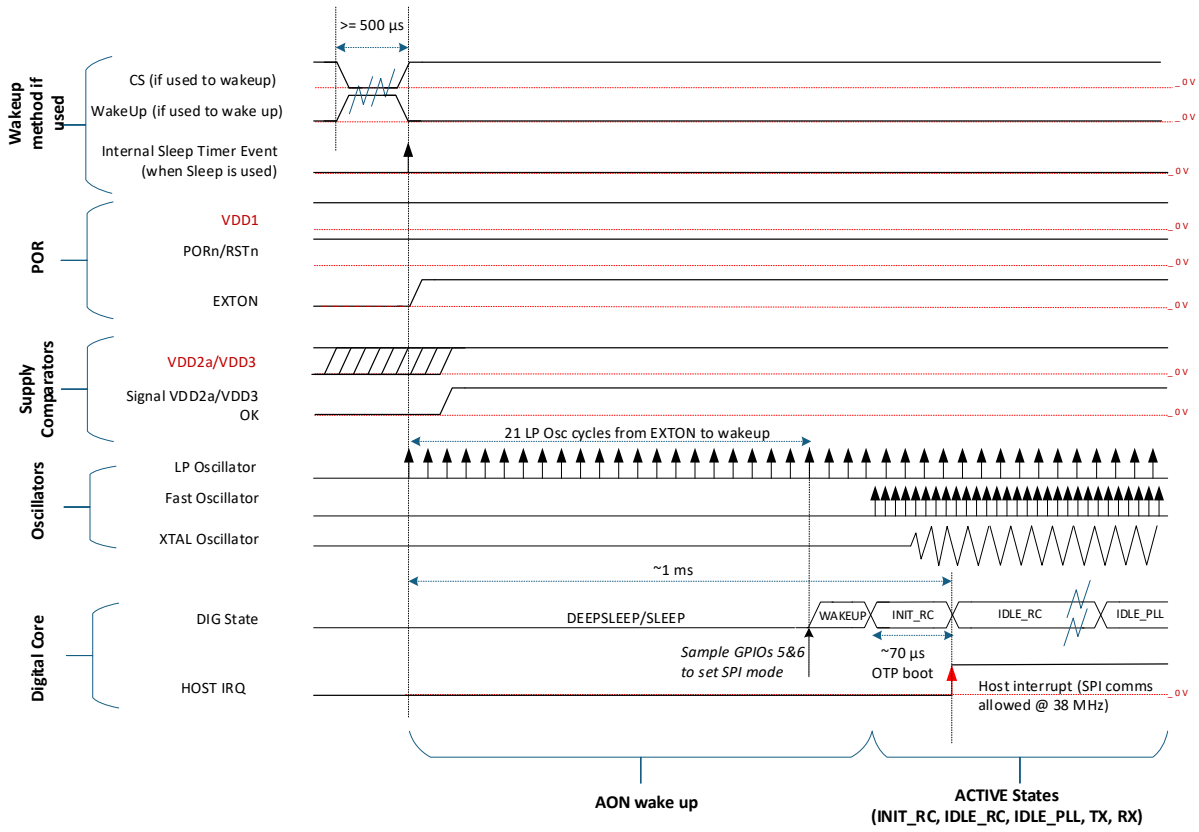


Figure 22 Timing diagram for warm start

6.1 Lowest Bill of Materials (BOM) powering scheme

In the following configuration the DW3000 is powered directly from a coin-cell battery. This is for applications that require the minimal BOM. The bulk capacitor required to store energy. The value of capacitor depends on the time the transceiver is in the active Tx/Rx state, typically 47uF.

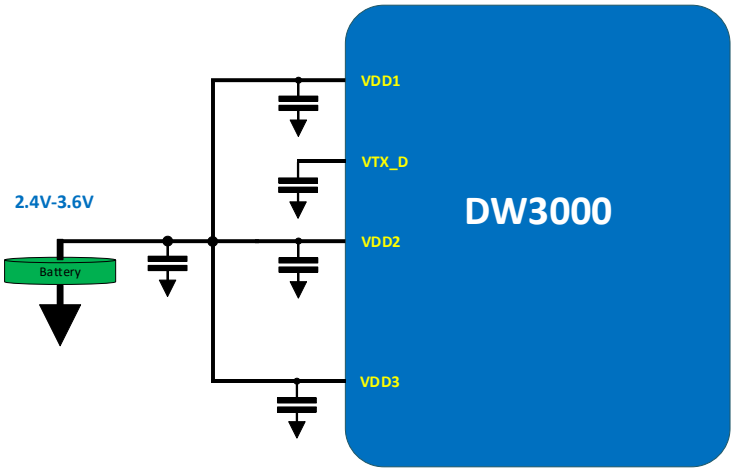


Figure 23: Lowest BOM powering option

6.2 Highest Efficiency powering scheme

In the following configuration the external Buck SMPS regulator is used. This is for applications that require the longest battery lifetimes. Depending on the use-case either the EXTON output or MCU can be used to control the Buck DC-DC.

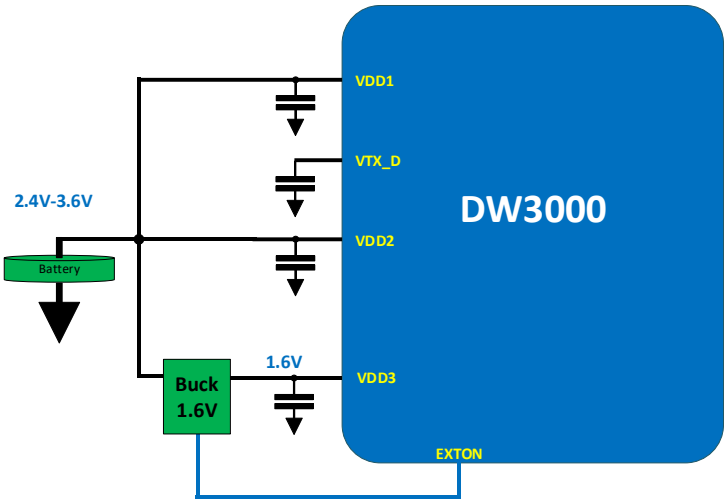


Figure 24: Single O/P Buck SMPS option

6.3 Mobile powering scheme

In the following configuration the external PMIC circuit is used to provide all the power rails to the chip. The VDD1 is used to power Always-On memory and IO rail only, the current consumption for powering AON is negligible.

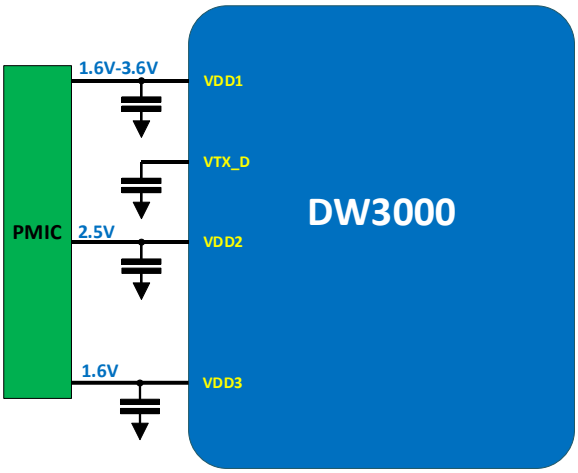


Figure 25: Mobile Option

6.4 Typical power profiles

The current drawn during operation with DW3000 will vary depending on supplies voltage used, batteries used, use case etc. Figure 26 shows the current drawn from a battery with typical TX frames transmitted, Figure 28 shows the current drawn for the reception of the frame by the receiver.

6.4.1 TX current profile for the minimal BOM

Figure 26 below shows the current profiles during of frame transmission without secure preamble and 6.8Mbps TDoA tag frame. This mode is compatible to a DW1000 TDoA tag blink. All supplies are connected to the battery assumed to at 3.0V, i.e. the lowest BOM option, see section 6.1.

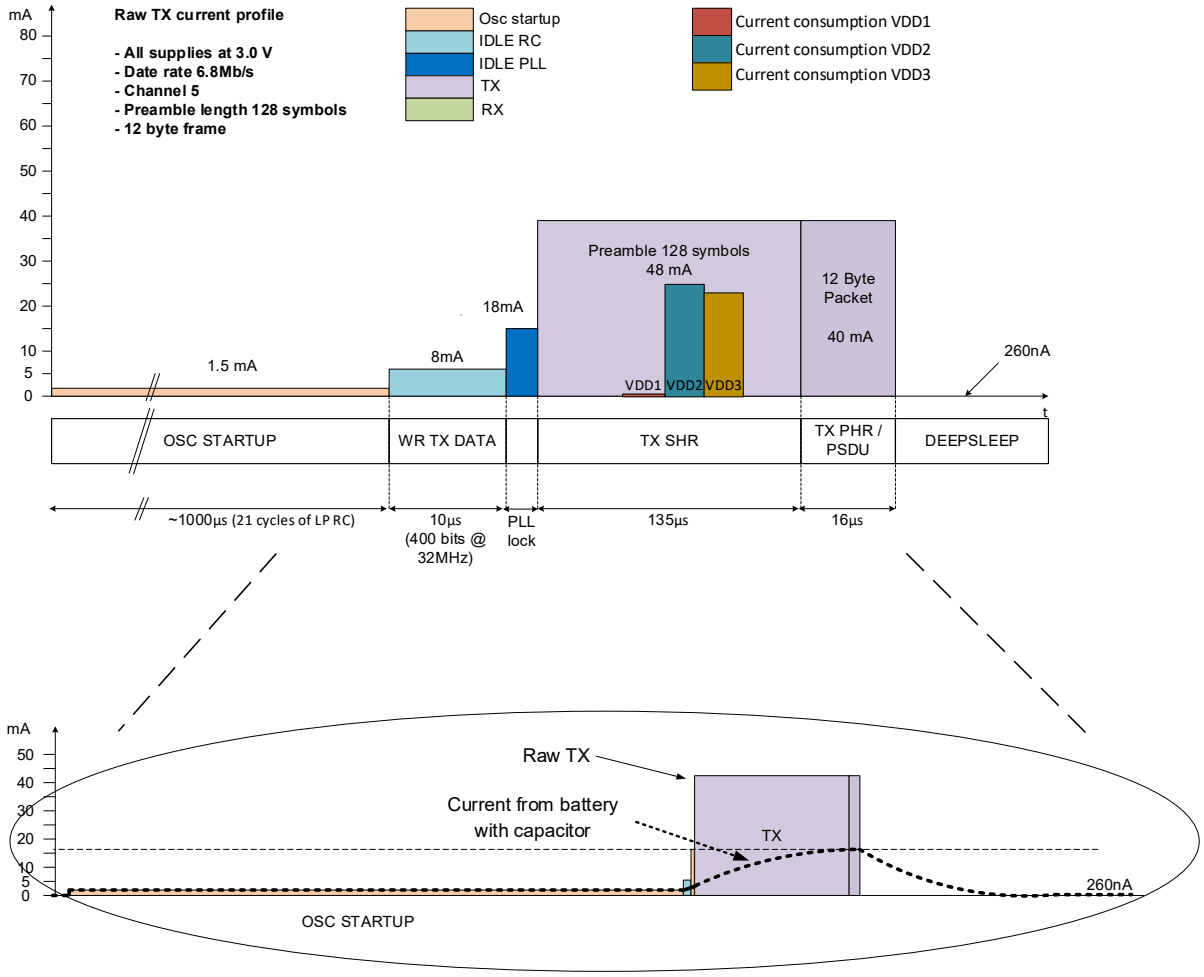


Figure 26: Current profile when transmitting a frame (6.8Mbps) in lowest BOM use case

6.4.2 TX current profile for high efficiency modes

In the high efficiency modes, i.e. when an external DC-DC/PMIC is used, the current consumption from VDD3 (1.6V) and VDD2a and VDD2b (2.5V) are different, therefore more efficient current consumption can be achieved using alternative powering schemes, illustrated in section 6.2 and 6.3. The VDD1 is used to power AON memory and IO rail only, the current consumption for powering AON is negligible.

For high efficiency schemes, the overall power consumption depends on the efficiency of external DC-DC and/or PMIC. For DW3000 device, the power consumption during different phases of operation as illustrated below.

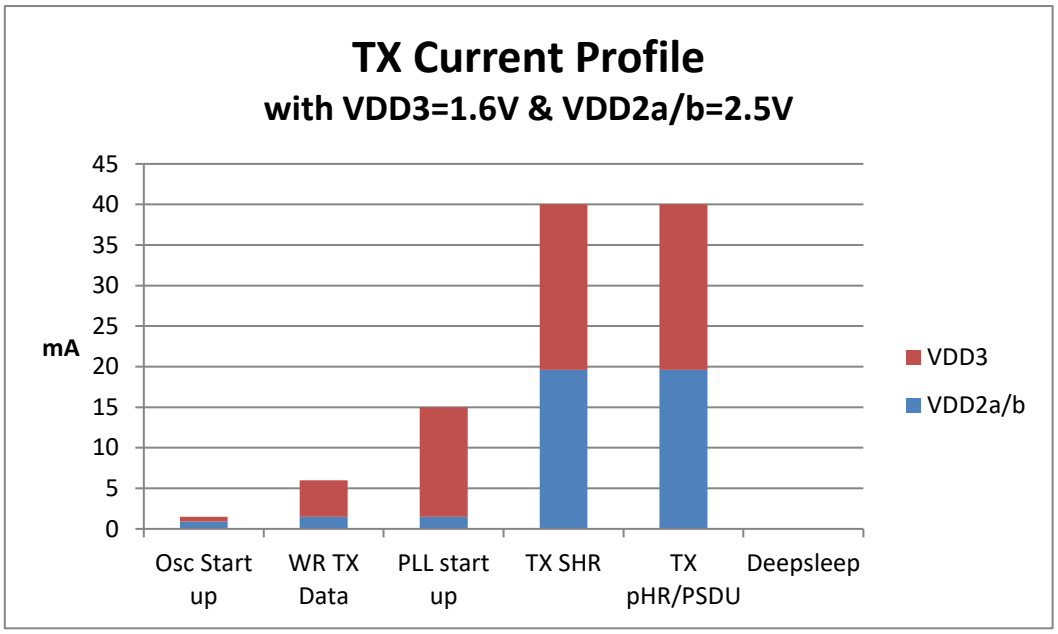


Figure 27: Current consumption during TX for high efficiency powering modes

6.4.3 RX current profile

Figure 28 illustrates the current profiles during the reception of a single frame. All supplies are connected to the battery assumed to at 3.0V, i.e. the lowest BOM option, see 6.1.

The example given for a case where a variable part of Preamble Hunt is ~30us. The preamble hunt can be minimized to 0 (zero) when using Delayed RX in the optimized Two Way Ranging (TWR) protocol (not illustrated), however with a Delayed RX the IDLE PLL should be maintained in between end of the transmission and start of the reception.

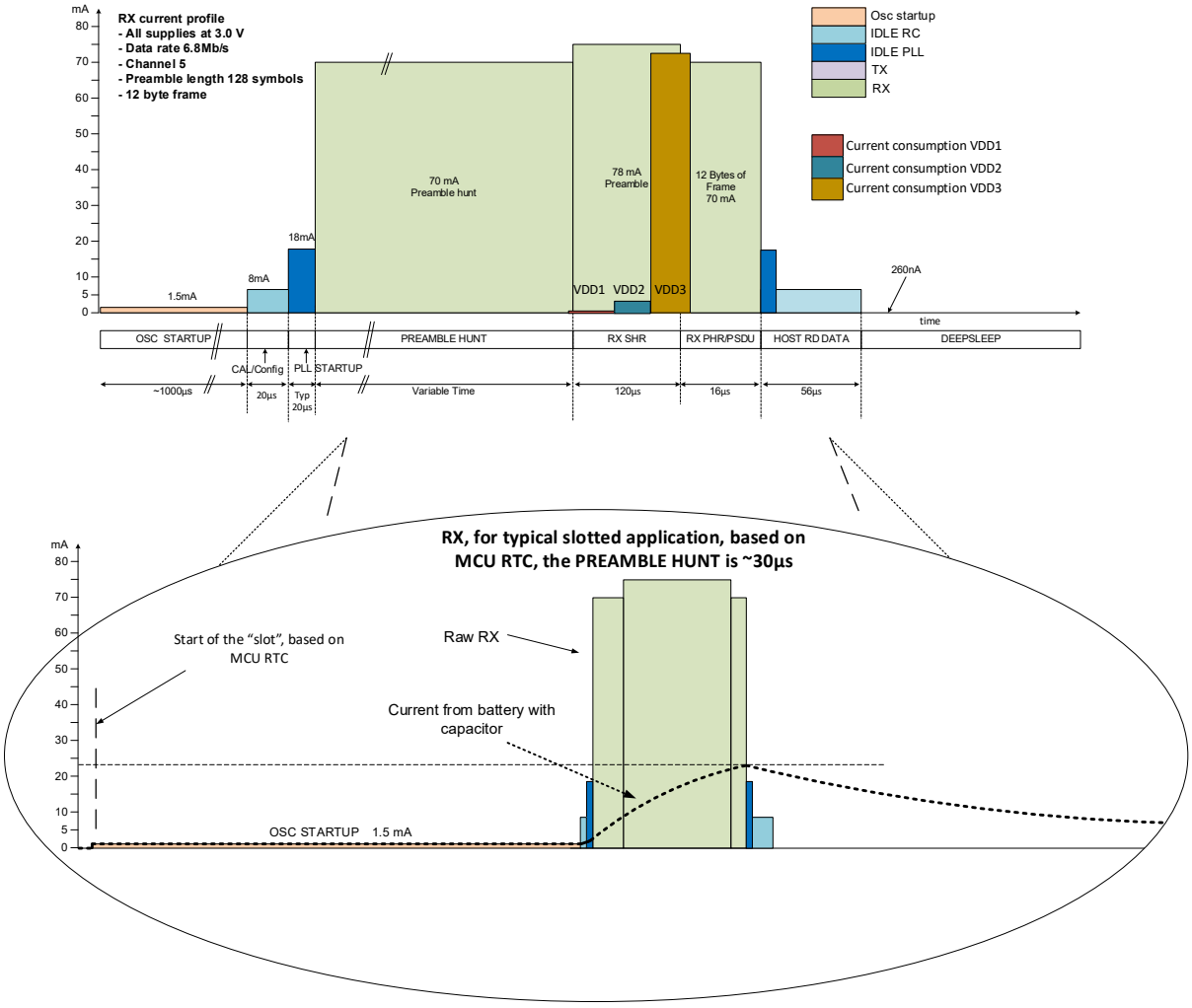


Figure 28: Current profile for receiving a frame

6.4.4 RX current profile for high efficiency BOMs

In the high efficiency modes, i.e. when an external DC-DC/PMIC is used, the current consumption from VDD2 (2.5V) and VDD3 (1.6V) are different, therefore more efficient current consumption can be achieved using alternative powering schemes, illustrated in section 6.2 and 6.3. The VDD1 is used to power AON memory and IO only, the current consumption for powering AON is negligible.

For high efficiency schemes, the overall power consumption depends on the efficiency of external the DC-DC and/or PMIC. For the DW3000 device, the power consumption during different phases of operation as illustrated below.

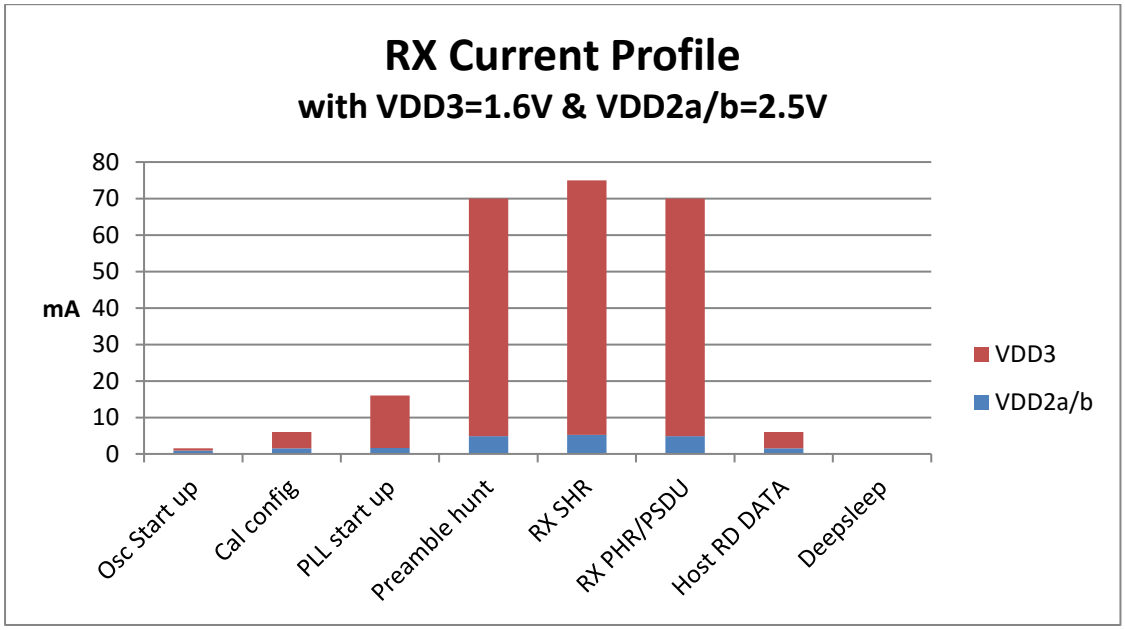


Figure 29: Current consumption during RX for high efficiency powering modes

6.4.5 Typical TWR current profile

Figure 30 illustrates the current profiles of the Initiator device during the typical optimized Double Sided TWR scheme. All supplies are connected to the battery assumed to at 3.0V, i.e. the lowest BOM option, see 6.1.

The example given for a case with Delayed RX and TX are used in the optimized TWR protocol. It should be noted, that IDLE PLL should be maintained in between TX and RX frames that chip clock domain is stable during the Two Way Ranging. If chip is used for protocols, where its precise clock is not needed (for example for application with Data transfer), then IDLE RC can be used to save power between TX and RX states. In this case the PLL Lock time should be considered before start of TX and RX.

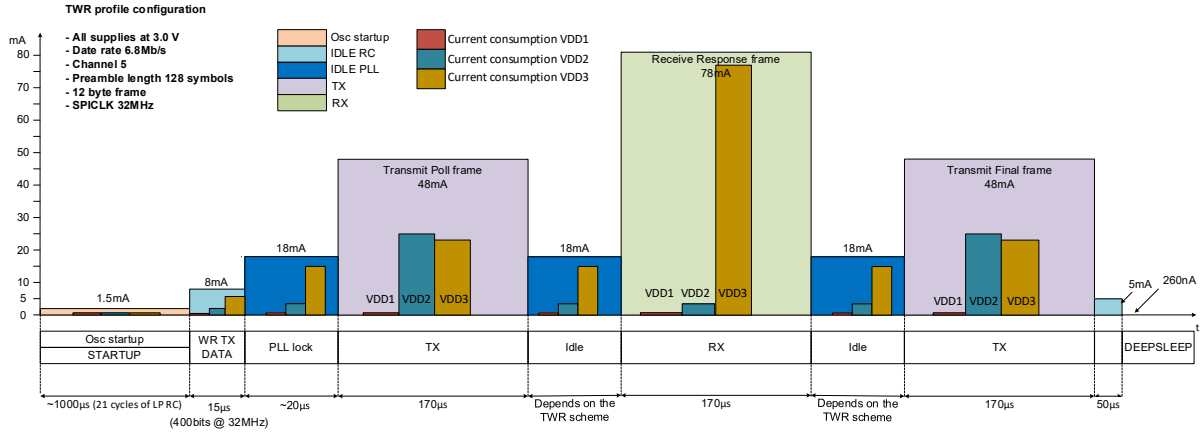


Figure 30 Current profile of Initiator in the DS-TWR with embedded data to frames

6.5 Internal Power supply distribution

The block diagram shows the power distribution within the DW3000 device.

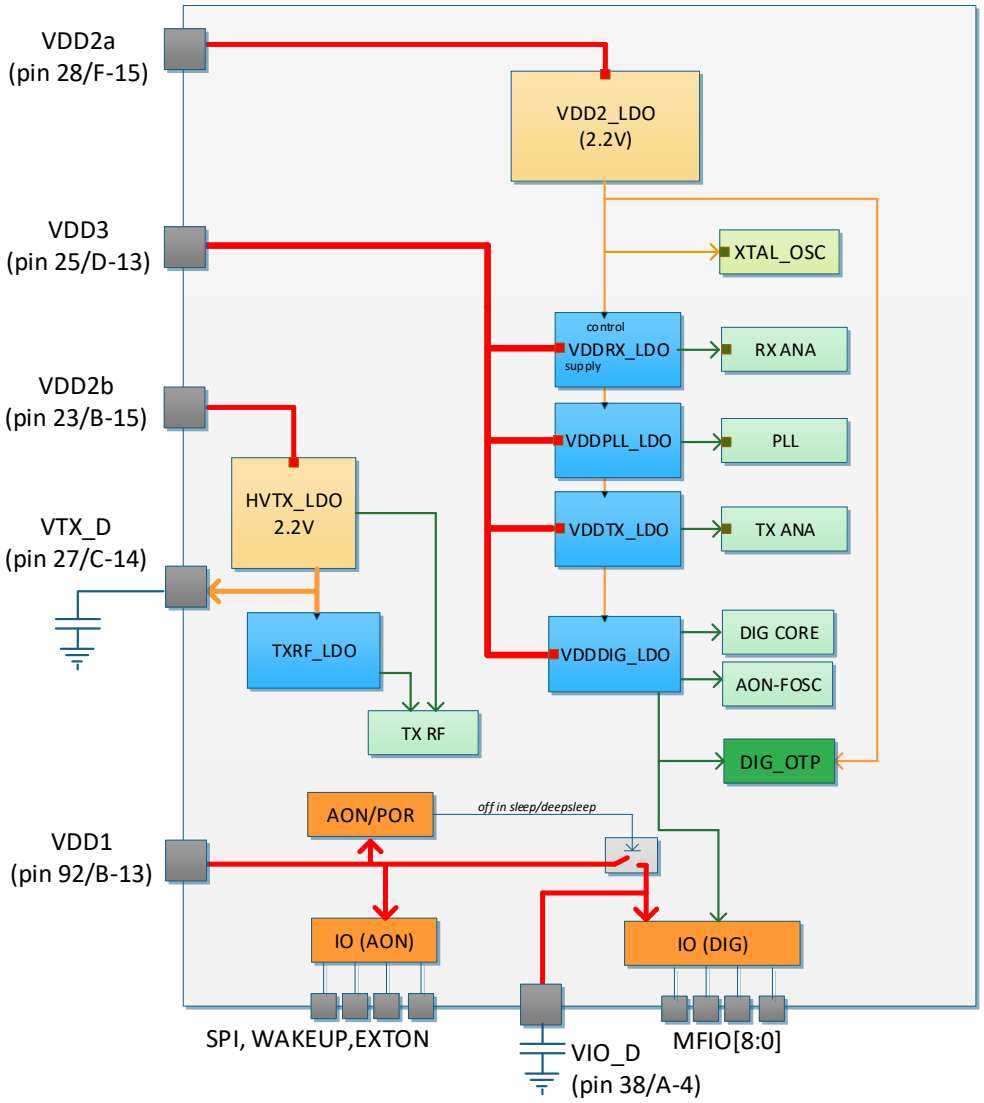


Figure 31: Internal power distribution

7 APPLICATION INFORMATION

7.1 Application Circuit Diagram (lowest BOM powering scheme)

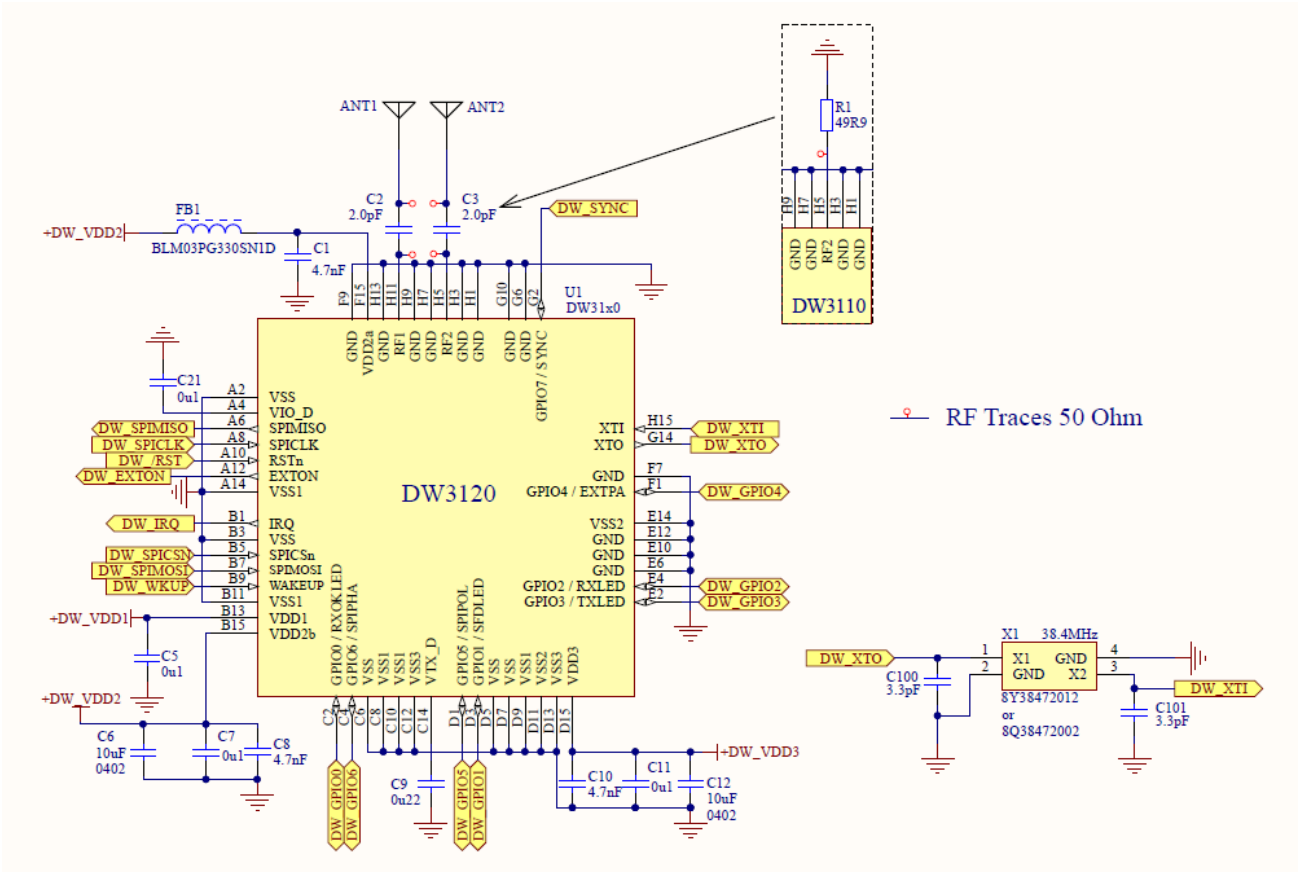


Figure 32: DW3000 WLCSP Application Circuit

Note, the suggested crystal loading will vary depending on board layout and actual crystal used. C2 and C3 are not only a DC blocking capacitor, these capacitors are a part of the RF transmission line, this line was simulated in design and this capacitance value was chosen as the result of the simulation.
BPF on RF1/2 pins may be required for certification in some regions that mandate conducted testing.

7.2 Boost Circuit Diagram

To power DW3000 from a low-capacity battery, it is recommended to use the boost circuit shown on the picture below.

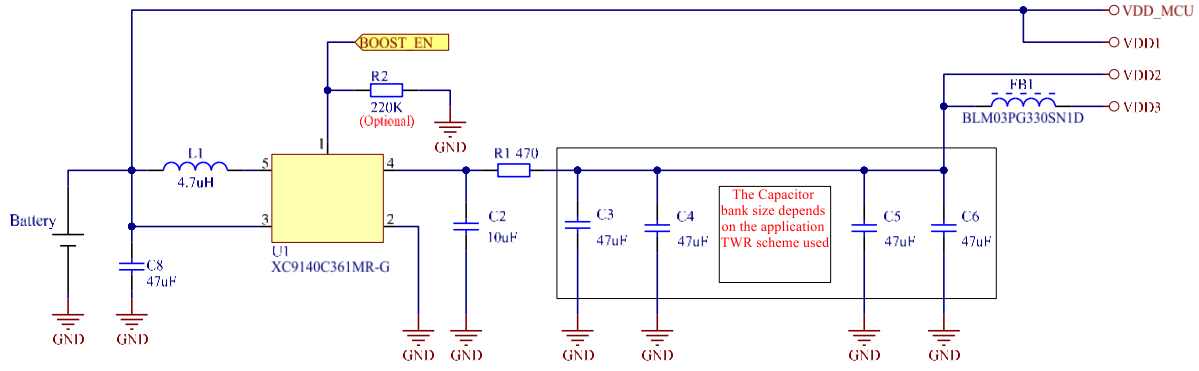


Figure 33 Boost Circuit

7.3 Recommended chip layout and Stack-up

The recommendation for the chip layout:

- Keep all the traces as short as possible.
- Avoid mixing Analog (RF1, RF2, XIN, XOUT), Power (VDD1, VDD2a/b, VDD3, VDD decoupling) and Digital (SPI etc) groups together.
- Place all the decoupling capacitors as close to the corresponding chip pads as possible, the smaller capacitor should be closer to the pad. Connect ground pad of each capacitor to the good ground plane directly to minimize ESR and ESL of the return current path.
- RF1 and RF2 lines should be 50 Ohm impedance-controlled lines. The DC-blocking 2pF capacitor pads should be embedded into the track (have the same width) to remove any possible discontinuities.
- The ground copper should be removed from under the chip in the areas shown in the picture (Top layer and Inner Layer 1). The first solid ground copper should be on the Inner Layer 2. If different stack-up will be used – this first solid copper layer should be at least 0.45mm away from the Top Layer, any inner layers close to the Top Layer should have the ground removed in the same manner as in Inner Layer 1 above.

7.3.1 WLCSP variant Stack-up

The DW31x0 WLCSP stack-up recommendation is shown below.

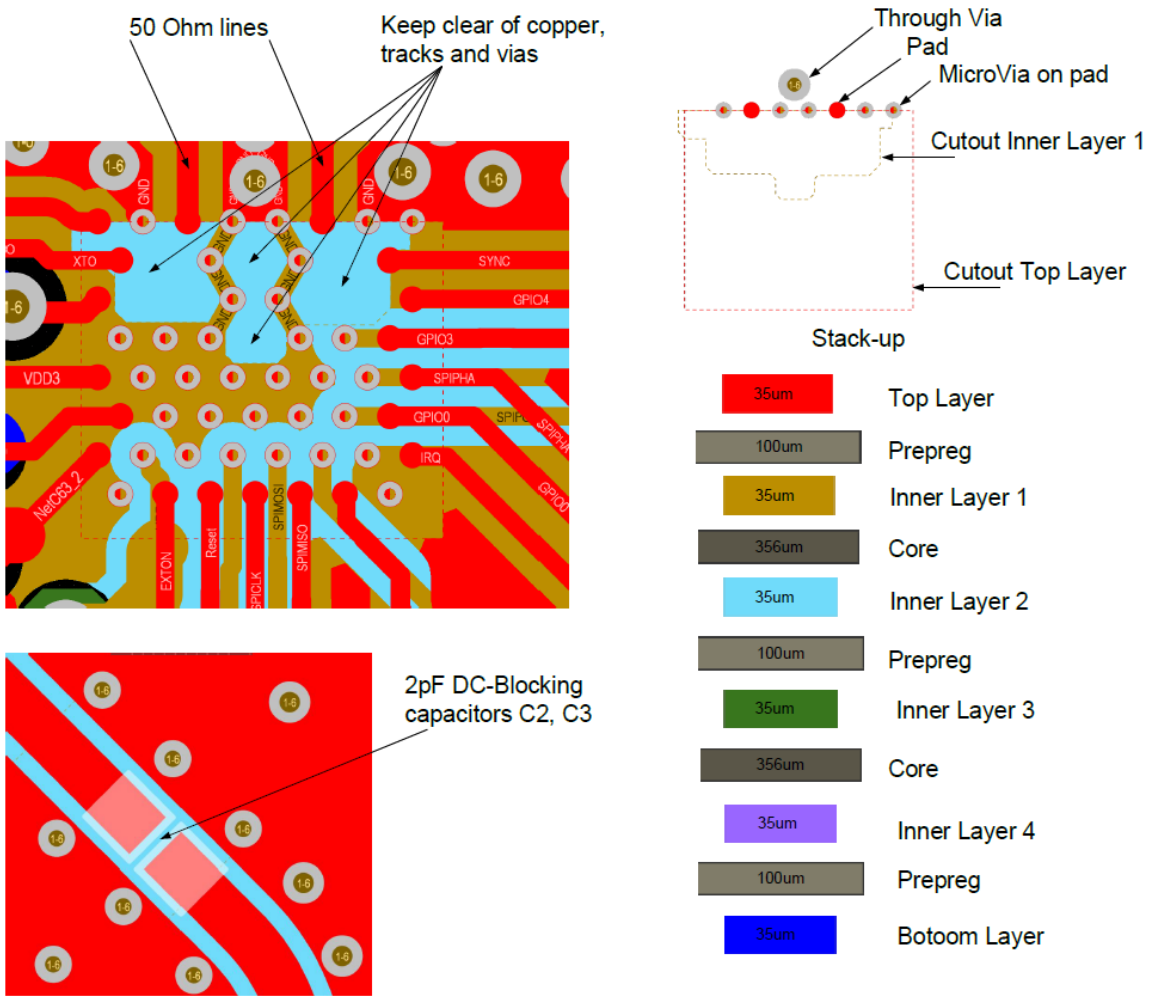


Figure 34 Recommended WLCSP Stack-up

7.3.2 QFN variant Stack-up

The DW32x0 QFN stack-up recommendation is shown below.

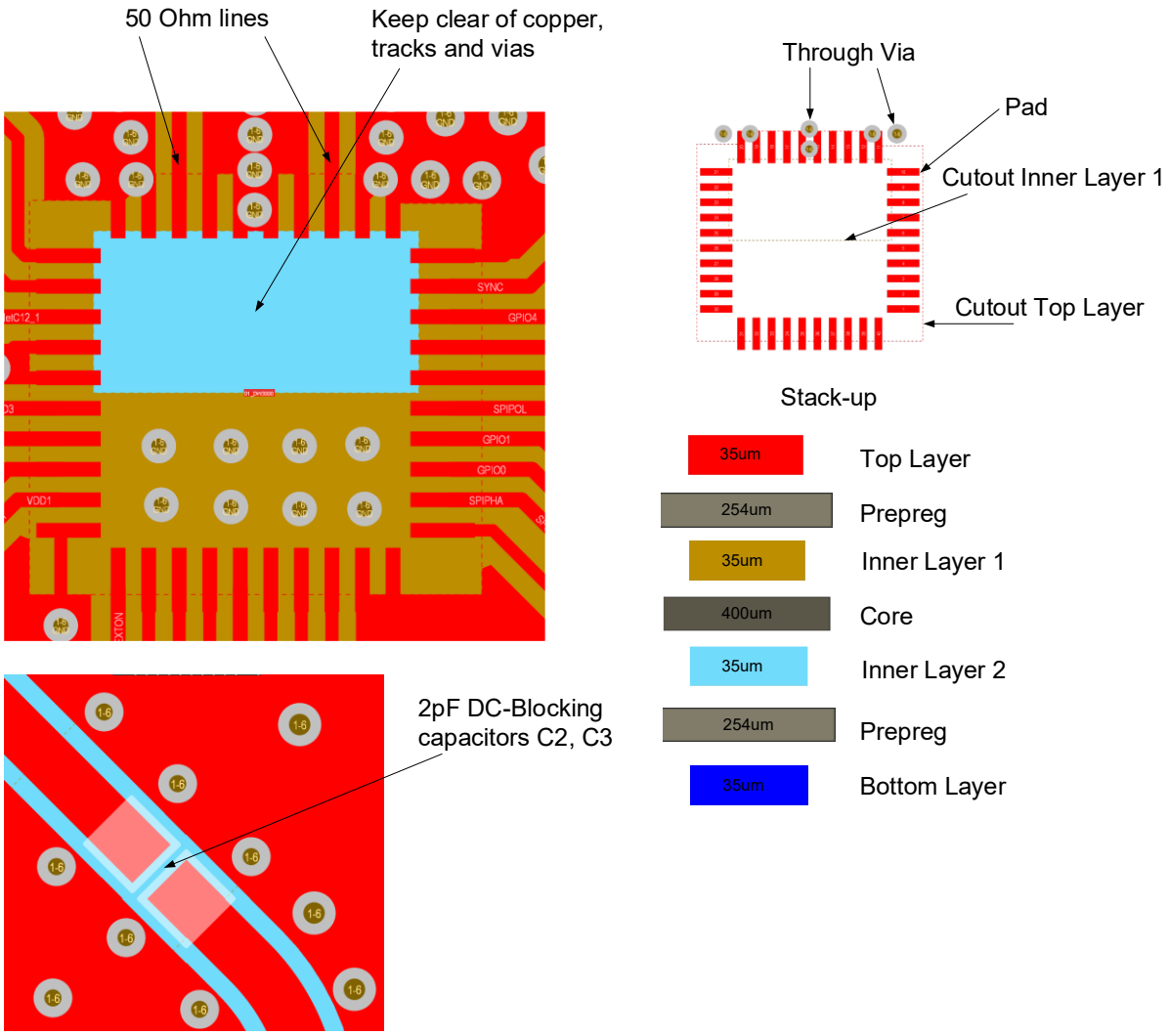


Figure 35 Recommended QFN Stack-up

7.4 Recommended Components

The list of components tested and approved by Decawave are shown in the table below. The use of DC-DC regulators and TCXO's is optional.

Table 22 Recommended Components

Function	Manufacturer	Part Number	Web Link
Antenna	Partron	ACS5200HFAUWB	www.partron.co.kr
	TDK	ANT167250ST-1210A1	www.tdk.com
	The Antenna Company	AC710xx (xx = 06, 16, 26, 46)	www.antennacompany.com
Crystal (38.4 MHz +/-10 ppm)	TXC	8Y38472012	www.txccorp.com
	Rakon	RSX-10	www.rakon.com
DC-DC 3V3	Torex	XC9258B33CER-G	www.torexsemi.com
DC-DC 2V5		XC9282B25D0R-G	
DC-DC 1V6		XC9282B16D0R-G	
DC-DC	TI	TPS62743	www.ti.com
TCXO	TXC	7Z38470005	www.txccorp.com
	Rakon	IT2200K	www.rakon.com

8 REFLOW PROFILES

8.1 Reflow profile of the WLCSP package

The DW31x0 should be soldered using the reflow profile specified below.

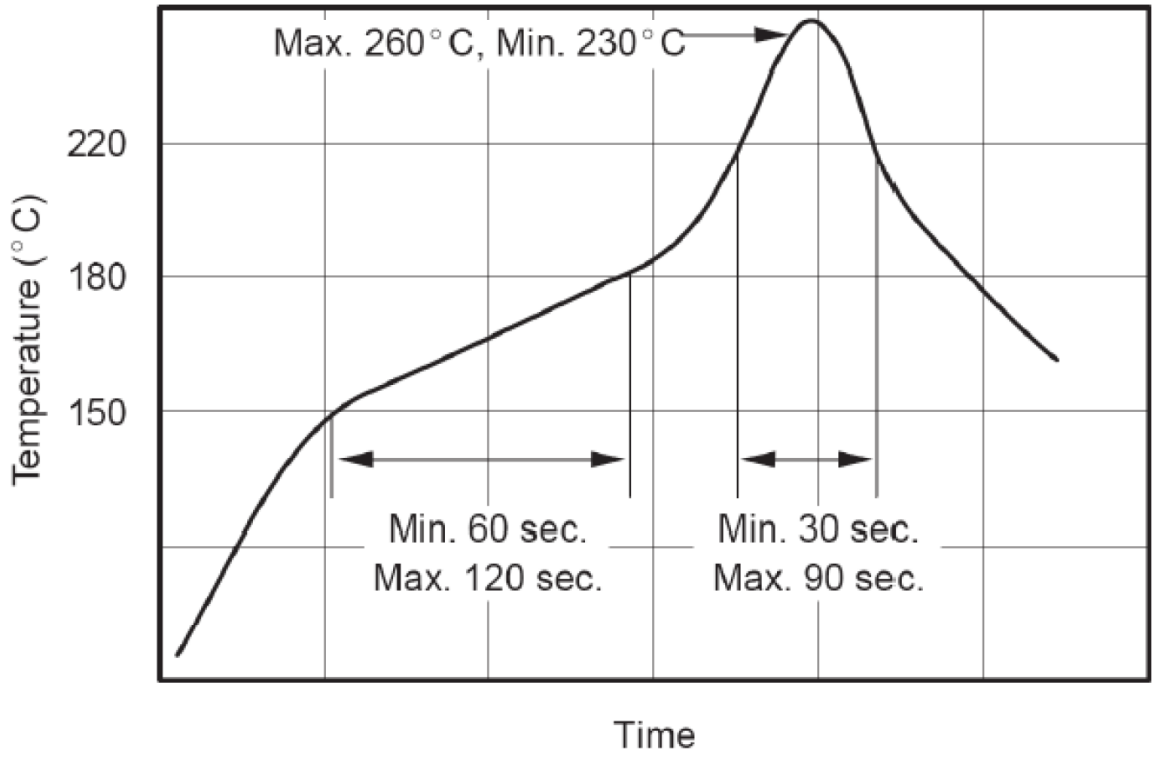


Figure 36 Reflow Profile of the WLCSP package

Table 23 Critical Parameters for Lead Free Solder of the WLSCP package

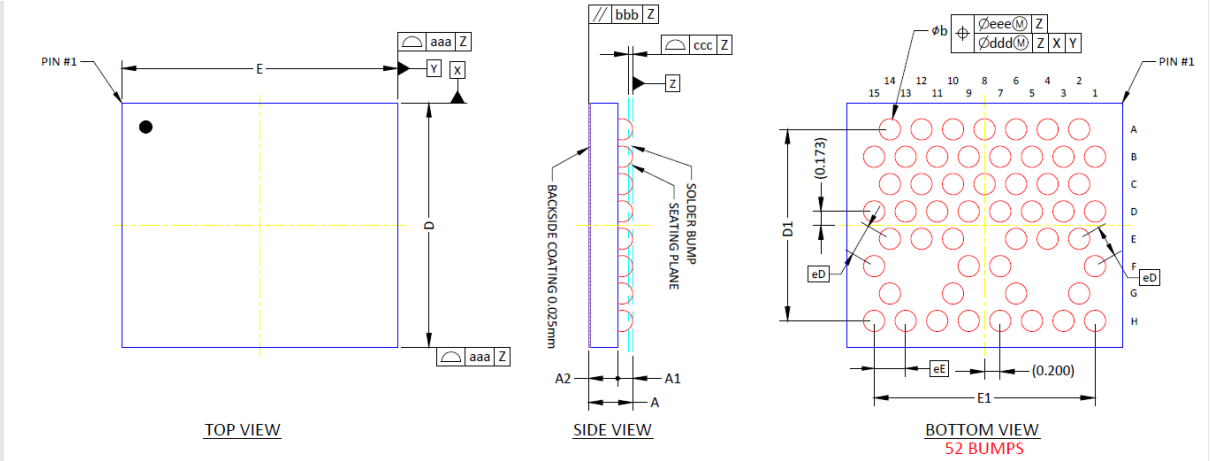
Process Step	Lead Free Solder
Ramp Rate	3˚C/sec
Pre-Heat	150˚C to 180˚C, 60 to 180 seconds
Time above Liquidius, 220˚C	30 to 90 seconds
Peak Temperature	255˚C +/- 5˚C
Time within 5˚C of Peak Temperature	10 to 20 seconds
Ramp Down Rate	6˚C/sec Max, 0.8˚C/sec to 0.4˚C recommended

8.2 Reflow profile of the QFN package

The DW32x0 should be soldered using the reflow profile specified in JEDEC J-STD-020 as adapted for the particular PCB onto which the IC is being soldered.

9 PACKAGING & ORDERING INFORMATION

9.1 Package Dimensions WLCSP



Control dimensions are in millimeter

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.560	0.600	0.020	0.022	0.024
A1	0.175	0.190	0.205	0.007	0.007	0.008
A2	0.345	0.370	0.395	0.014	0.015	0.016
D	3.0661	3.0961	3.1261	0.121	0.122	0.123
E	3.4688	3.4988	3.5288	0.137	0.138	0.139
D1	-	2.425	-	-	0.095	-
E1	-	2.800	-	-	0.110	-
eD	-	0.400	-	-	0.016	-
eE	-	0.400	-	-	0.016	-
b	0.245	0.270	0.295	0.010	0.011	0.012
aaa		0.050			0.002	
bbb		0.050			0.002	
ccc		0.030			0.001	
ddd		0.050			0.002	
eee		0.015			0.001	

Figure 37: Package Dimensions WLCSP

9.2 QFN chip variant

9.2.1 Package Dimensions QFN

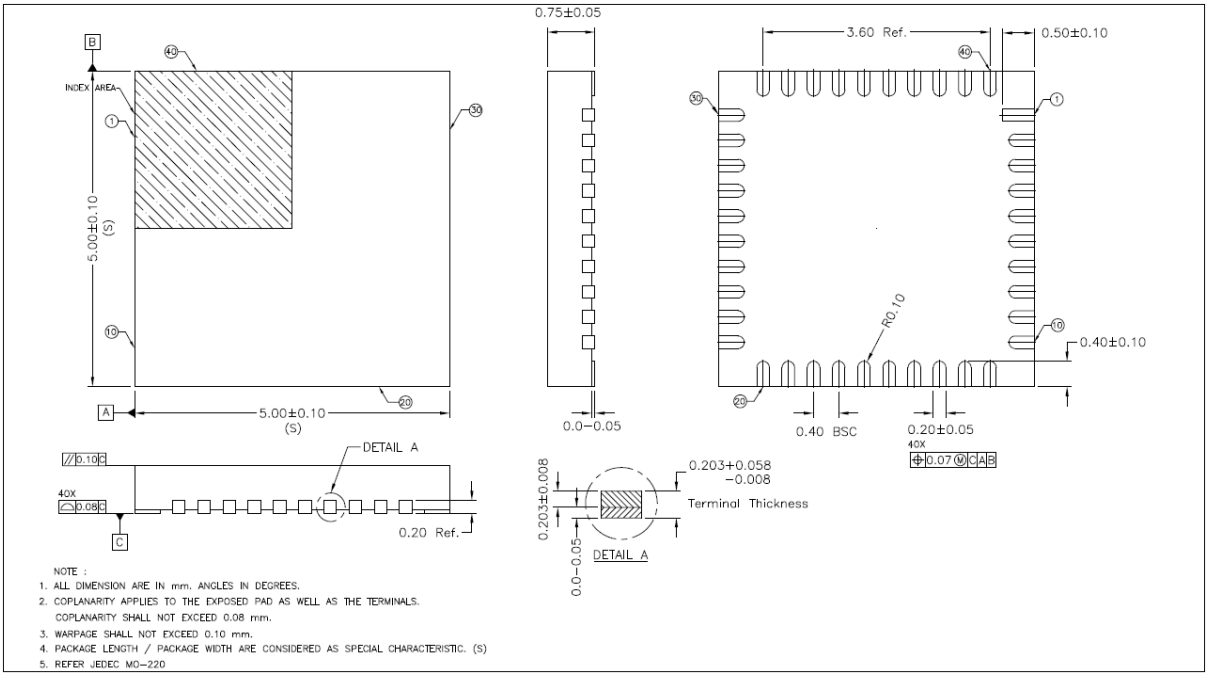
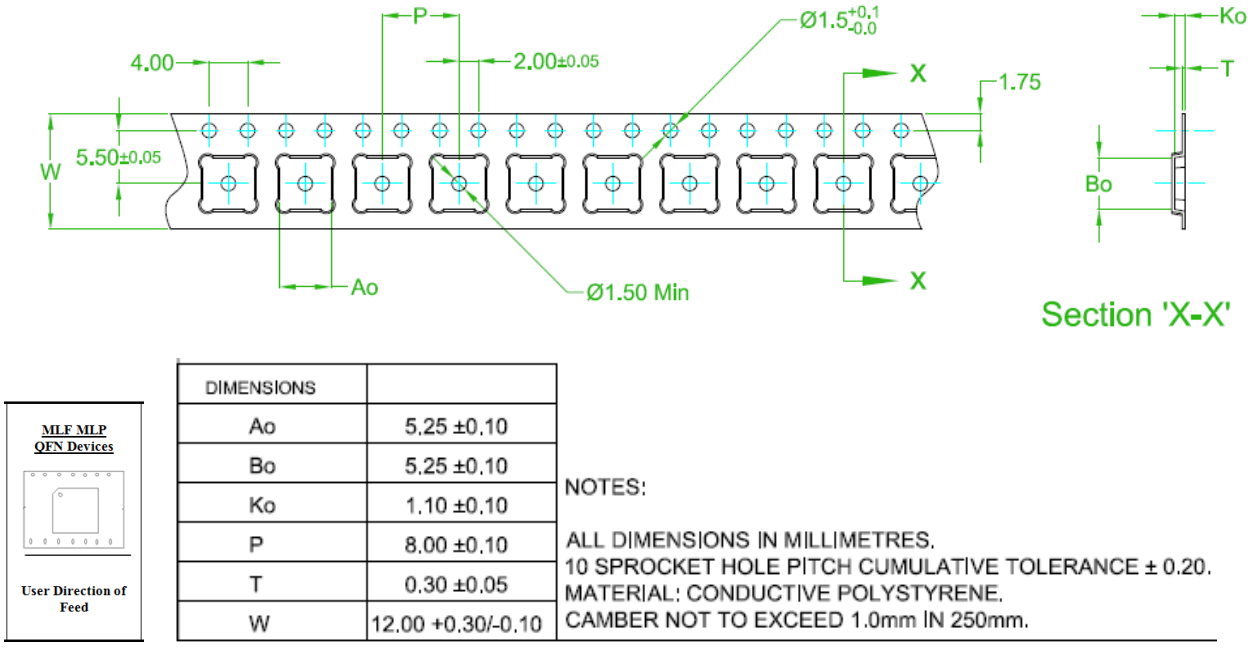


Figure 38: Package Dimensions QFN

9.2.2 Tape and Reel packaging information: QFN chip variant

Tape orientation and dimensions:



DIMENSIONS	
Ao	5.25 ±0.10
Bo	5.25 ±0.10
Ko	1.10 ±0.10
P	8.00 ±0.10
T	0.30 ±0.05
W	12.00 +0.30/-0.10

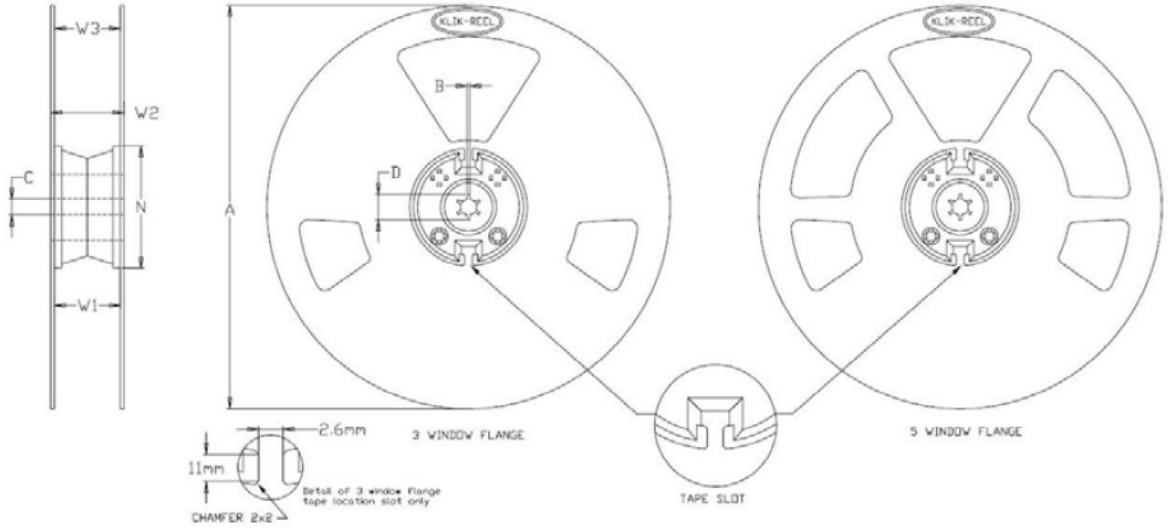
NOTES:

ALL DIMENSIONS IN MILLIMETRES.
10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.20.
MATERIAL: CONDUCTIVE POLYSTYRENE.
CAMBER NOT TO EXCEED 1.0mm IN 250mm.

Figure 39 QFN Tape Orientation and Dimensions

REEL INFORMATION : 330mm REEL (13")

Base material: High Impact Polystyrene with Integrated Antistatic Additive.
Surface resistivity: Antistatic with surface resistivity less than 1 x 10e12ohms per square.



Tape width	A Diameter	B (min)	C	D (min)	N Hub	W1 (max)	W2 (max)	W3 (min)	W3 (max)
12	330/380	1.5	13 +/-0.2	20.2	100 +/-1	12.4 +2/-0	18.4	11.9	15.4

Figure 40 QFN Reel Information

All dimensions and tolerances are fully compliant with EIA 481-C and are specified in millimeters (mm). Quantity per reel = 4000 units.

9.2.3 Tape and Reel packaging information: WLCSP chip variant

Tape orientation and dimensions:

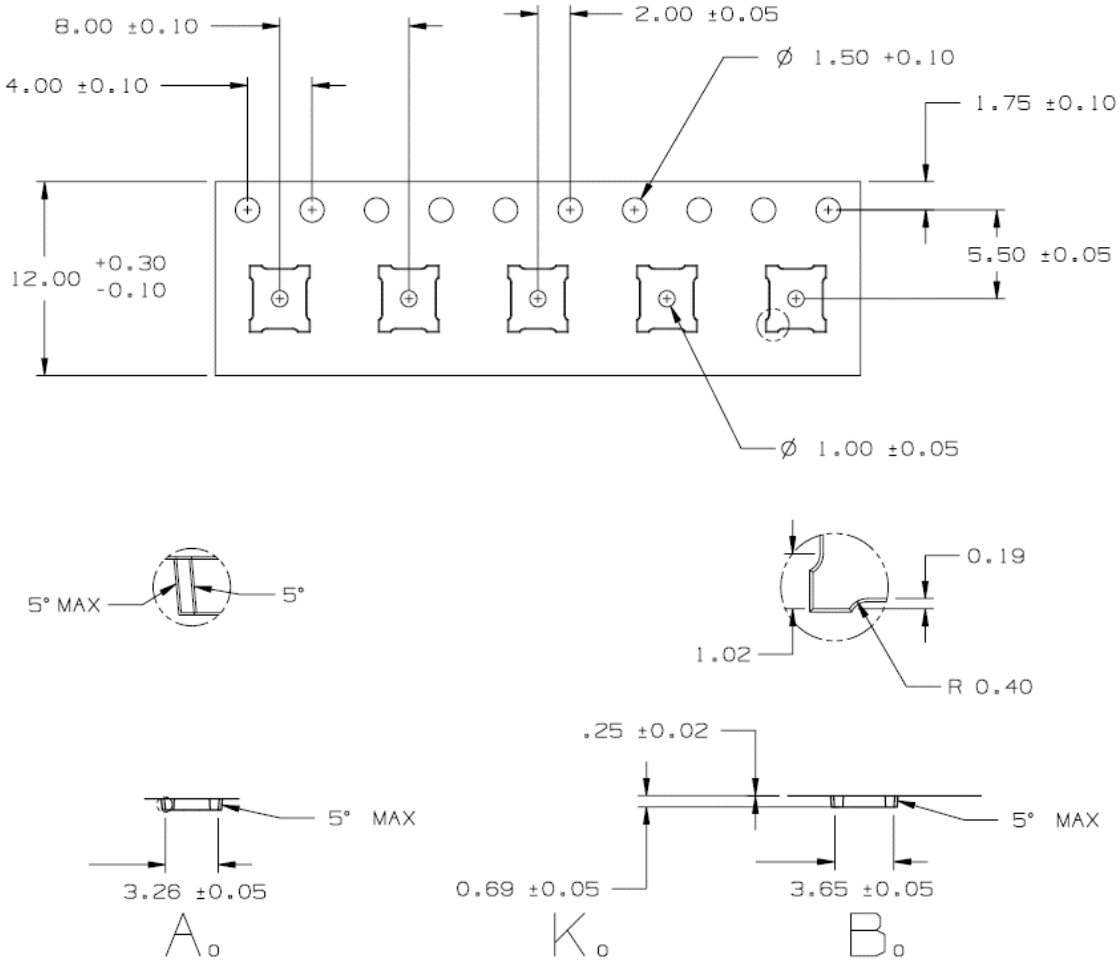
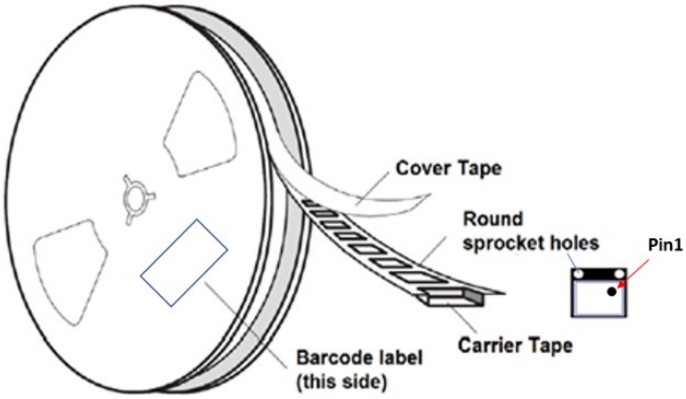
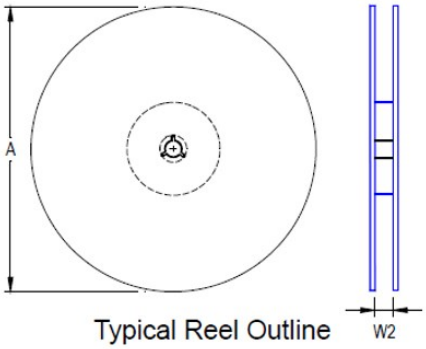


Figure 41 WLCSP Tape Orientation and Dimensions

REEL INFORMATION: 330mm REEL (13”)



Pin1 Orientation In Carrier Tape



Typical Reel Outline

Package size	Tape Size	Pocket Pitch	Reel size (A) min/max	Reel width (w2) min/max	Units per reel	Pre/Post empty pocket
3.1 x 3.5 mm	12 mm	8 mm	330 mm (13”)	12.4/13.4 mm	3000	200/200

Figure 42 WLCSP Reel Information

9.2.4 WLCSP, QFN Device Package Marking

The diagram below shows the package markings for DW3210, DW3220, DW3110 and DW3120.

Figure 43: Device Package Markings

Legend:

DW3xx0	Part number
XXXXXXXX	Lot number
ZZYYWW	Assembly site ID (ZZ), A2 for QFN B2 for WLCSP Year (YY) and Week (WW) number

10 GLOSSARY

Table 24: Glossary of Terms

Abbreviation	Full Title	Explanation
EIRP	Equivalent Isotropically Radiated Power	The amount of power that a theoretical isotropic antenna (which evenly distributes power in all directions) would emit to produce the peak power density observed in the direction of maximum gain of the antenna being used.
BPRF	Base PRF mode	64MHz PRF Mode
GPIO	General Purpose Input / Output	Pin of an IC that can be configured as an input or output under software control and has no specifically identified function.
IEEE	Institute of Electrical and Electronic Engineers	Is the world's largest technical professional society. It is designed to serve professionals involved in all aspects of the electrical, electronic and computing fields and related areas of science and technology.
LoS	Line of Sight	Physical radio channel configuration in which there is a direct line of sight between the transmitter and the receiver.
Open Drain	Open Drain	A technique allowing a signal to be driven by more than one device. Generally, each device is permitted to pull the signal to ground but when not doing so it must allow the signal to float. Devices should not drive the signal high so as to prevent contention with devices attempting to pull it low.
NLoS	Non Line of Sight	Physical radio channel configuration in which there is no direct line of sight between the transmitter and the receiver.
PLL	Phase Locked Loop	Circuit designed to generate a signal at a particular frequency whose phase is related to an incoming "reference" signal.
PPM	Parts Per Million	Used to quantify very small relative proportions. Just as 1% is one out of a hundred, 1 ppm is one part in a million.
RF	Radio Frequency	Generally used to refer to signals in the range of 3 kHz to 300 GHz. In the context of a radio receiver, the term is generally used to refer to circuits in a receiver before down-conversion takes place and in a transmitter after up-conversion takes place.
RTLS	Real Time Location System	System intended to provide information on the location of various items in real-time.
SFD	Start of Frame Delimiter	Defined in the context of the IEEE802.15.4-2011 standard.
SPI	Serial Peripheral Interface	An industry standard method for interfacing between IC's using a synchronous serial scheme first introduced by Motorola.
TWR	Two Way Ranging	Method of measuring the physical distance between two radio units by exchanging messages between the units and noting the times of transmission and reception. Refer to Decawave's website for further information.
TDoA	Time Difference of Arrival	Method of deriving information on the location of a transmitter. The time of arrival of a transmission at two physically different locations whose clocks are synchronized is noted and the difference in the arrival times provides information on the location of the transmitter. A number of such TDoA measurements at different locations can be used to uniquely determine the position of the transmitter. Refer to Decawave's website for further information.
PDoA	Phase Difference of Arrival	Method of determining the direction of propagation of a radio-frequency wave incident on an antenna array using the phase difference between the signal received on each antenna array element.

11 REFERENCES

[1] IEEE802.15.4-2011 or “IEEE Std 802.15.4™-2011” (Revision of IEEE Std 802.15.4-2006). IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[2] IEEE802.15.4-2015 or “IEEE Std 802.15.4™-2015” (Revision of IEEE Std 802.15.4-2011). IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

12 DOCUMENT HISTORY

Table 25: Document History

Revision	Date	Description
1.1	24 March 2021	Datasheet updated to reflect latest characterisation results and editorial changes. - Chip characterization results including chip start-up time - Current consumption profiles - Application and Boost Circuit Diagrams - Stack-up information - Reflow profiles - Packaging information - MSL Level. Note: QFN parts are qualified as MSL-1 but packaged/shipped as MSL-3.
1.0	21 August 2020	Initial release.