EB 2ED2410 Family

Evaluation mother/daughterboards user guide

About this document

Scope and purpose

This user guide is intended to enable users to easily “plug and play” evaluation board EB 2ED2410 3M “motherboard” with its daughterboards:

- EB 2ED2410 3D 1BCD
- EB 2ED2410 3D 1BCS
- EB 2ED2410 3D 1BCDP
- EB 2ED2410 3D 1BCSP

and assesses the features it offers.

This document describes functionalities, set-up protections, layout choices that have been implemented, and shows how to test them.

Intended audience

This document is intended for qualified electronic engineers who need a smart N-channel MOSFET gate driver with integrated bi-directional current sense, wire protection and strong gate drive capability for automotive or industrial fail safe and fail operational applications.

Table of contents

1 Overview

EB 2ED2410 board family is based on a “3M” mother-/ “3D” daughterboard concept with a semiconductor-based solution of a fail-safe/fail operational power switch for automotive or industrial applications including electronic fuse functionality plus an I-t wire protection.

Those boards are primarily intended to test the basic functionality of the 2ED2410-EM gate driver in different setups and not the switching or thermal performance in a real application.

1.1 Motherboard EB 2ED2410 3M

EB 2ED2410 3M features the 2ED2410-EM driver, control interface to microcontroller or waveform generators accessible via pin headers. 2ED2410-EM integrated protection logic, sensors inputs and diagnostics allows:

- Switch self- and wire protection (e.g. short-circuit or I-t wire protection),
- Fault identifications (via DGx pins),
- Switch operating conditions monitoring (PCB temperature and MOSFET gate source leakage)
- Failure mode analysis of connected MOSFET.

Note: Failure mode analysis of connected MOSFET needs a specific set-up: it is not treated in this document and will be described in a separate Infineon Application Note.

The gate driver is protected against overvoltage by a 100 nF (C_{VS}) plus optional 1 W zener (Z1) on pin VS.

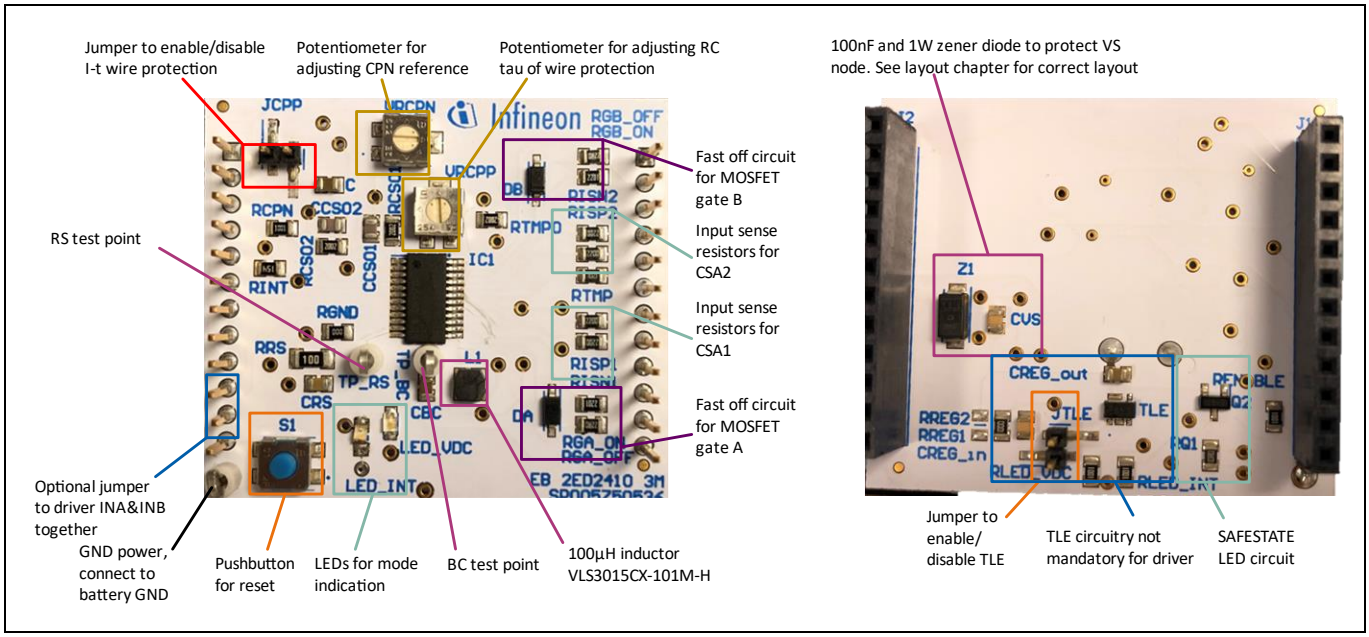

Figure 1 Top & back view EB 2ED2410 3M with features

Table 1 Infineon parts used in EB 2ED2410 3M

Type	Reference	PCS	Comment
Driver	2ED2410-EM (IC1)	**1**	Full analog driver
Power supply	TLE42962GV50 (TLE)	**1**	Can be replaced 1:1 with GV33 version
Signal PMOS	BSS83P (Q2)	**1**	For visualization of SAFESTATE mode.

See chapter 1.3 for high-level diagram of the motherboard.

1.2 Daughterboards EB 2ED2410 3D

EB 2ED2410 3D-1BCD, -1BCS, -1BCDP, -1BCSP feature N-channel MOSFET common drain, common sources structure with or without pre-charge circuit. It allows replacement of any mechanical relay by cutting the current flow in both directions. Additionally, the back-to-back structure blocks current in case of reverse battery situation.

The boards are designed for easy plug-and-play banana connectors.

Note: *2ED2410-EM driving capabilities are not limited to one MOSFET on each gate output: These daughterboards are primarily used to test basic functionality and not switching or thermal performance.*

Note: *Daughterboards EB 2ED2410 3D are intended to be used only with EB 2ED2410 3M. Gate-source resistors are not needed when operating with EB 2ED2410 3M, but can be added to check daughterboard stand-alone operation.*

Table 2 EB 2ED2410 3D daughterboards overview

Type	Topology	Comment
-1BCD	Common drain	Fully bi-directional
-1BCS	Common source	Recommended connection with shunt to the battery
-1BCDP	Common drain with pre-charge	Mandatory connection with pre-charge circuit to load side
-1BCSP	Common source with pre-charge	Mandatory connection with pre-charge circuit to load side

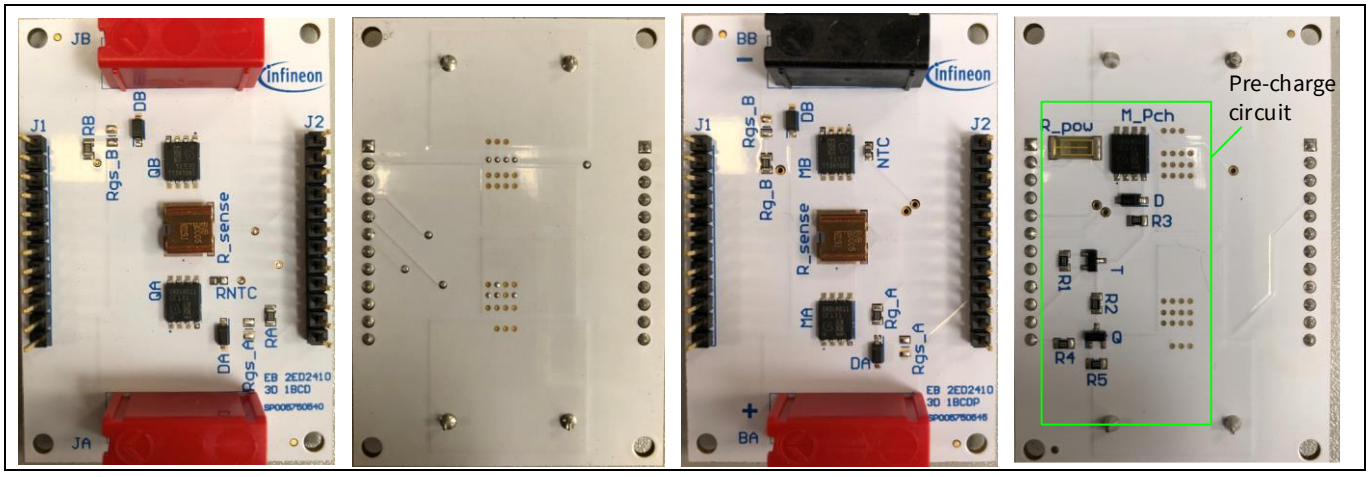

Figure 2 Top (main switch path) & back view of daughterboards EB 2ED2410 3D-1BCD and -1BCDP

Table 3 Infineon parts used in EB 2ED2410-EM 3D

Type	Reference	PCS	Comment
MOSFET	IAUC120N06S5N011	**(2)** **3**	(2: -1BCD, -1BCS) (3: -1BCDP, -1BCSP)
Signal NMOS	2N7002 (Q)	**1**	For pre-charge level shifter
Signal PMOS	BSS83P (T)	**1**	For pre-charge level shifter

See chapter 1.3 for high-level diagram of the different daughterboards' versions.

1.2.1 Daughterboards current rating

The daugherboards are designed for **continuous 20 A** operation, **30 A for 10 minutes** and **60 A for one minute** without the I-t wire protection. See chapter 4.2 for I-t wire protection adjustment.

Short-circuit limit is by default using 5 V Enable from TLE42926GV50 **@ 80 A**, see chapter 4.1 for details.

1.3 High level diagrams

The motherboard features a small low voltage generator to generate 5 V voltage, +VDC. It can be replaced 1:1 by the same TLE42962GV33 in 3.3 V version. +VDC supplies the references voltage for INT, CPN and EN pins. A pushbutton allows to pull-down this voltage, therefore, when the button is maintained pushed the driver is in SLEEP mode and a RESET is performed. See datasheet chapter 5 for details on driver operating modes.

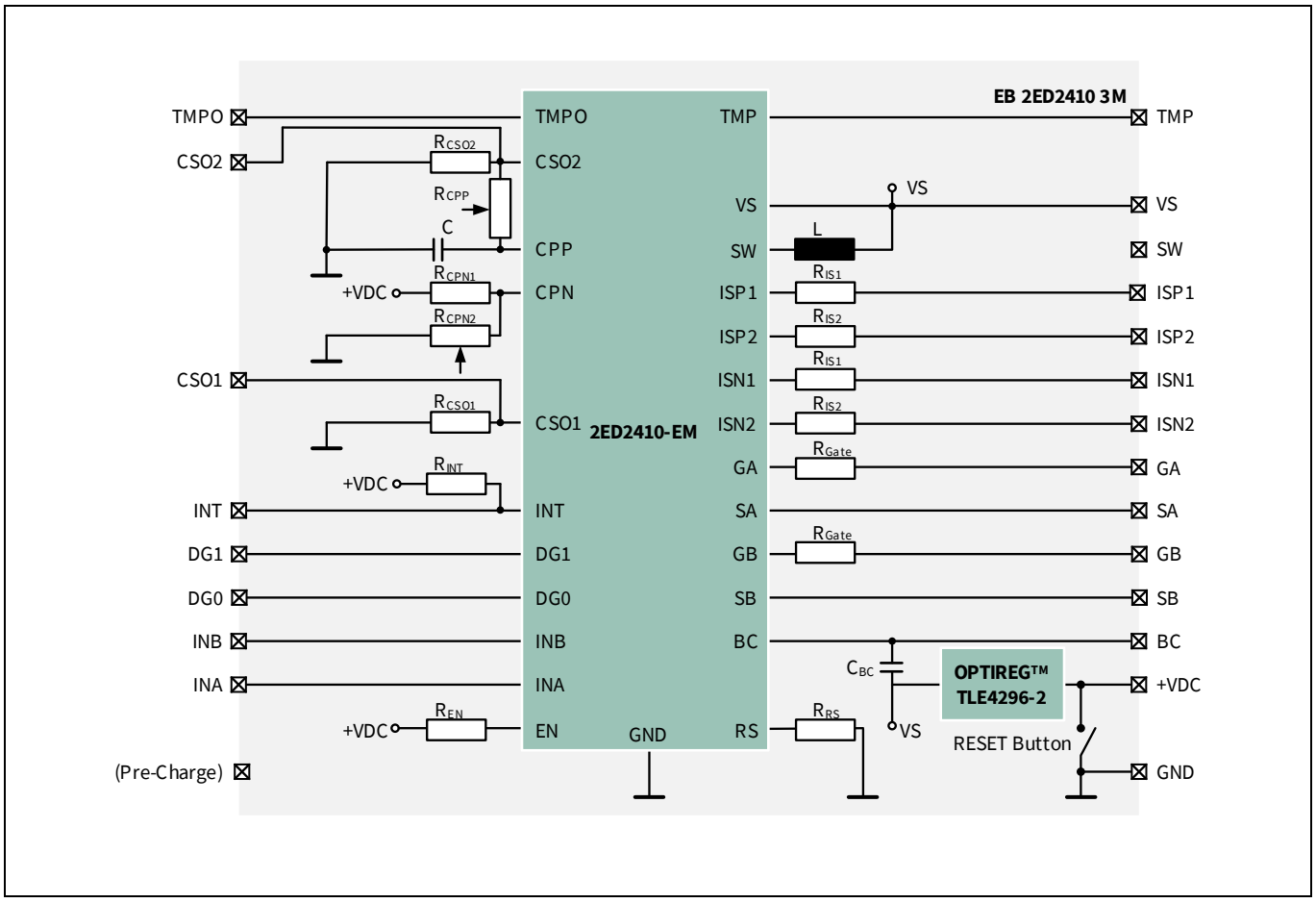

Figure 3 Overview of motherboard

The daughterboards' diagrams are shown below. It shows that pre-charge circuit can be implemented as an add-on with no interference on main current MOSFET switch.

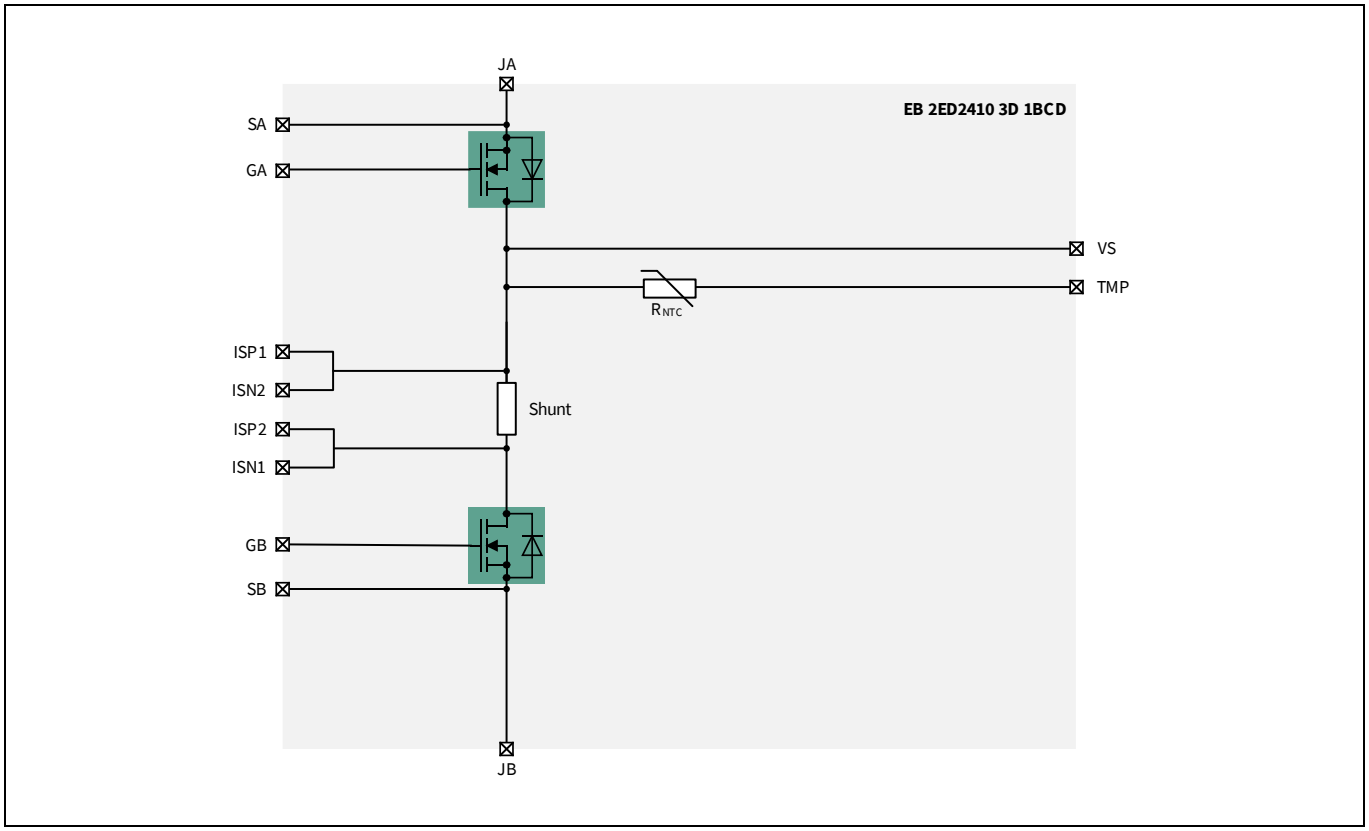

Figure 4 Overview of daughter board -1BCD

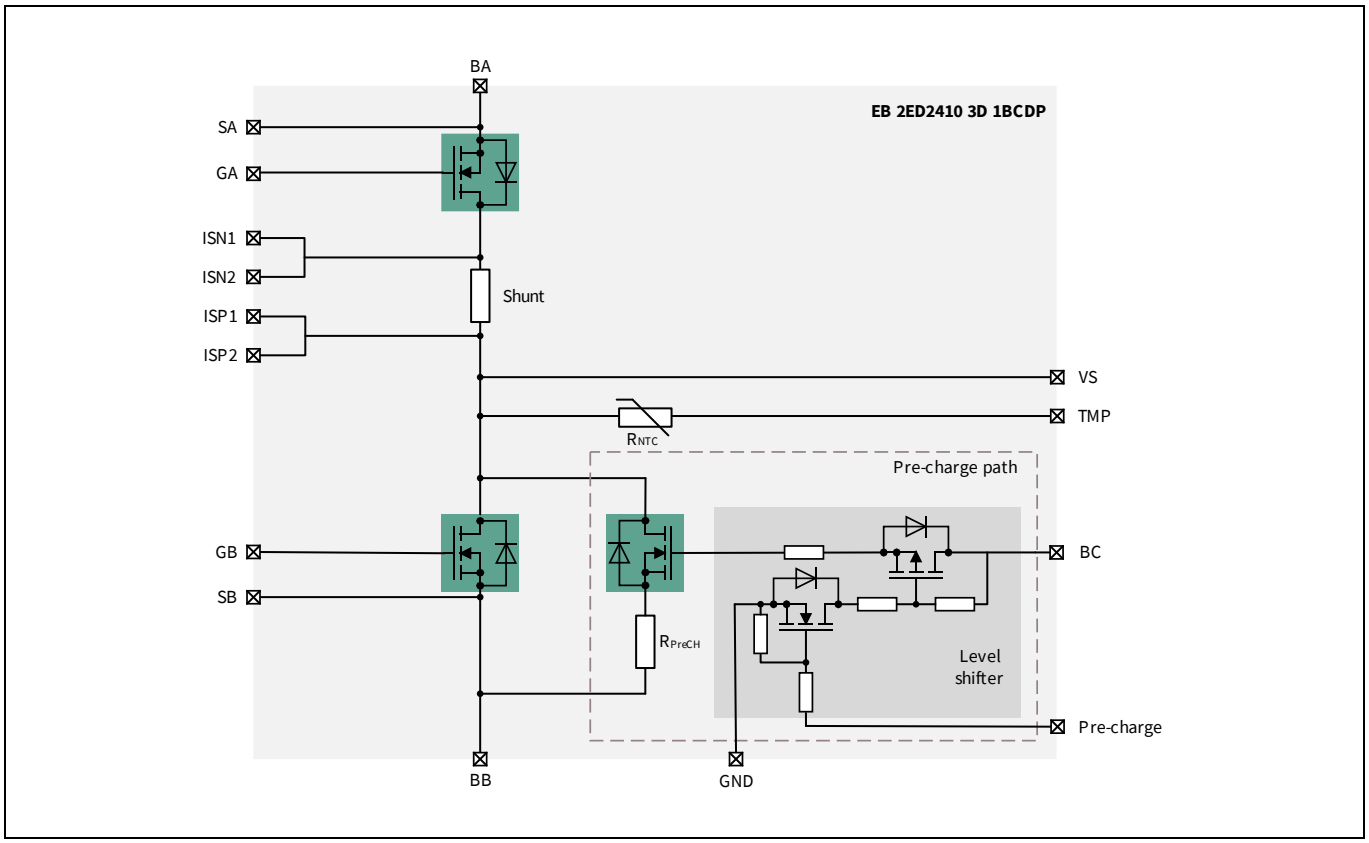

Figure 5 Overview of daughter board -1BCDP

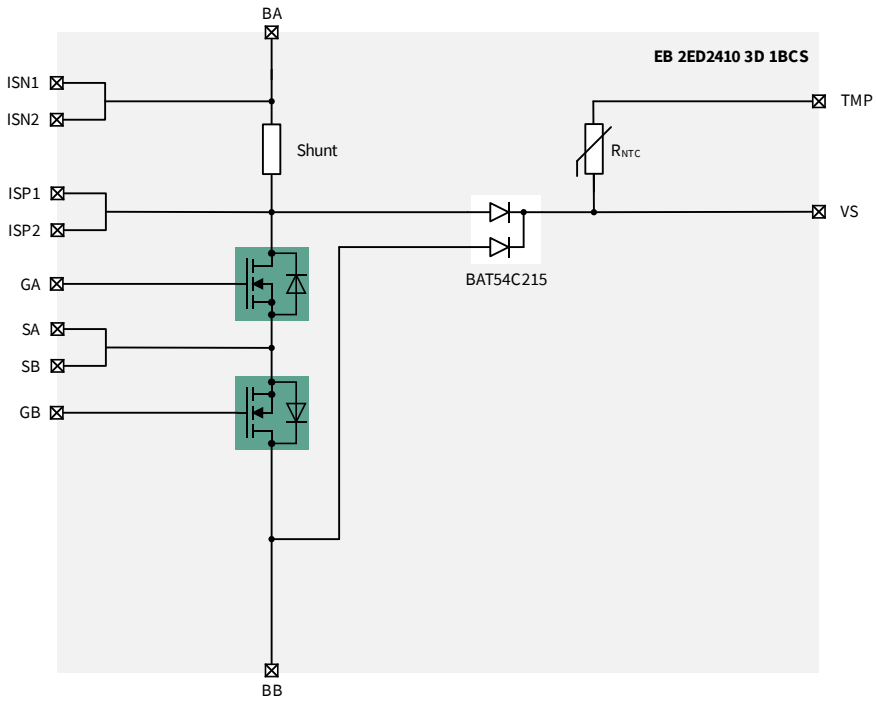

Figure 6 Overview of daughter board -1BCS

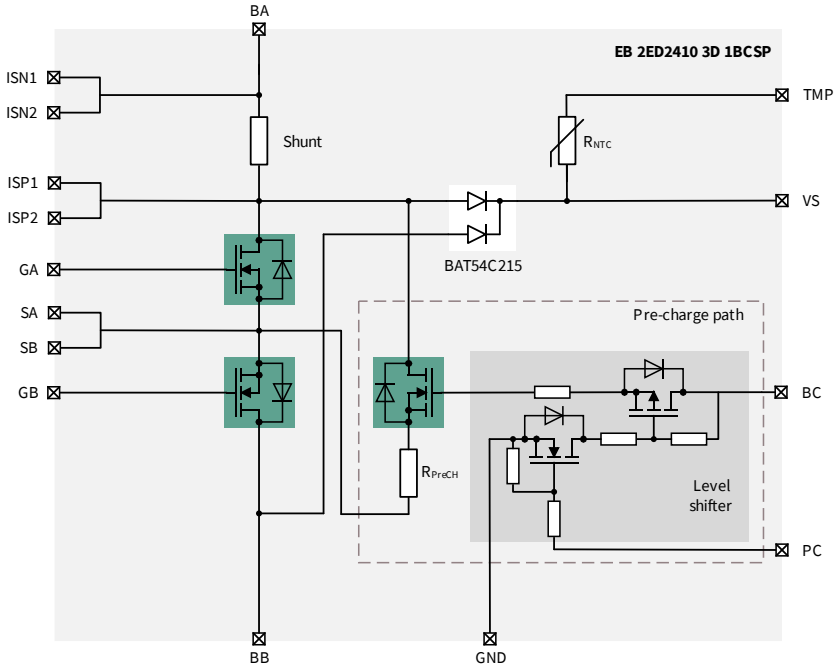

Figure 7 Overview of daughter board -1BCSP

Note: For boards -1BCS and -1BCSP, the OR-diode is put there for simplicity of use of the evaluation board and should not be re-used in a real design. VS pin connection to battery side is preferred.

2 Connecting and operating the board

This chapter describes how to connect the motherboard with the daughterboard and gives a non-exhaustive list of actions to avoid in order to keep 2ED2410-EM and the board operational.

2.1 Boards assembly

Step1: Bring the boards together, so top overlay (text) can be read on both boards.

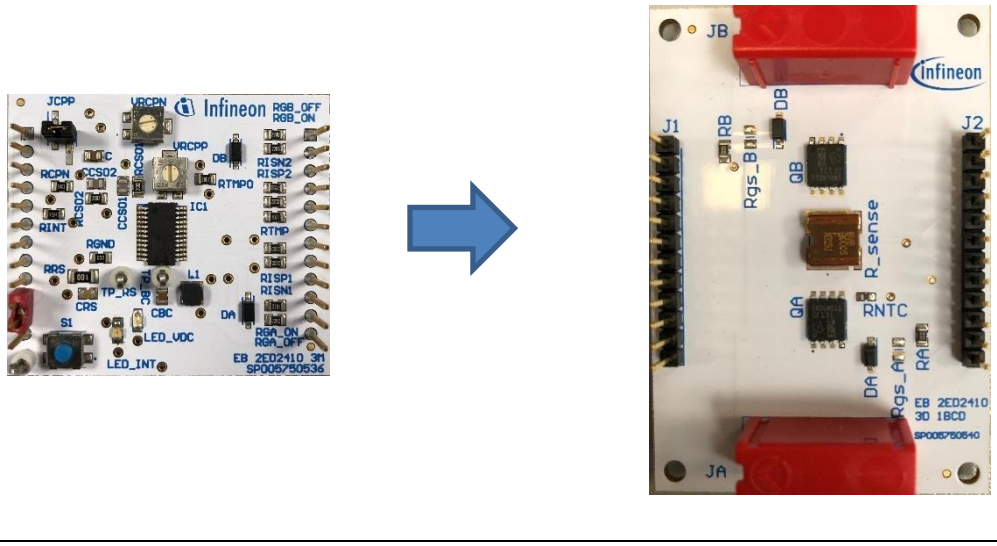

Figure 8 Board stack connection step 1

Step2: Pile up the boards gently, avoid bowing the headers

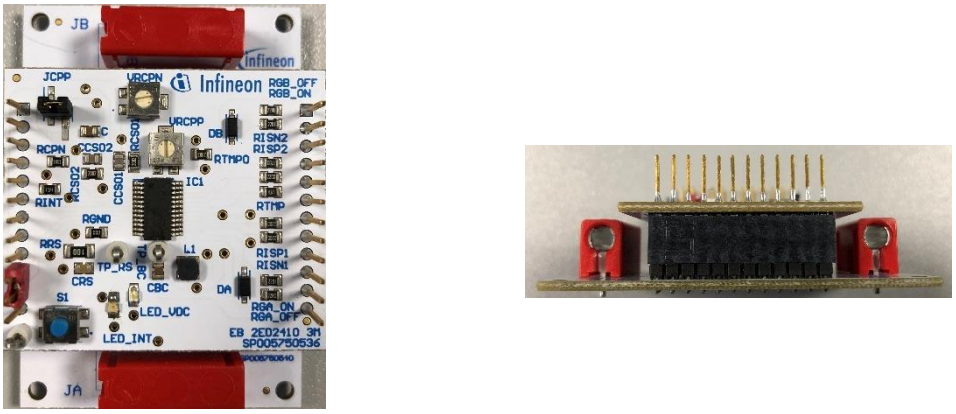

Figure 9 Board stack connection step 2

Boards are ready for use.

2.2 Power connection

Refer to table 2 for connection options for each daughterboard.

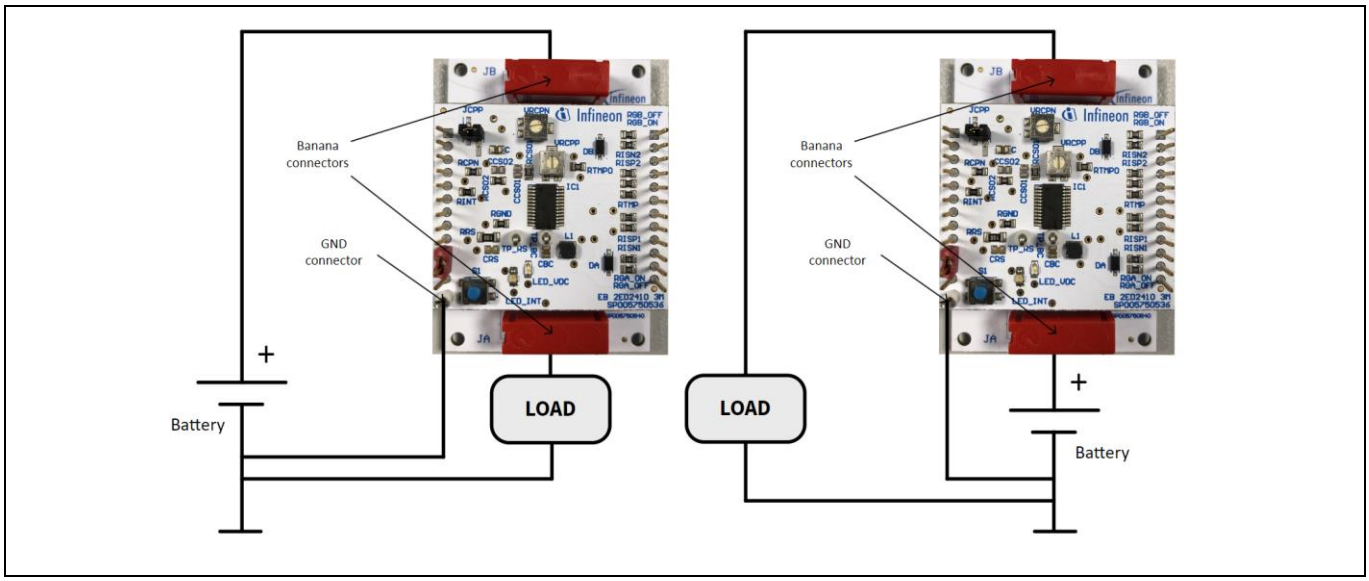

Figure 10 Power connection diagrams with 3D-1BCD

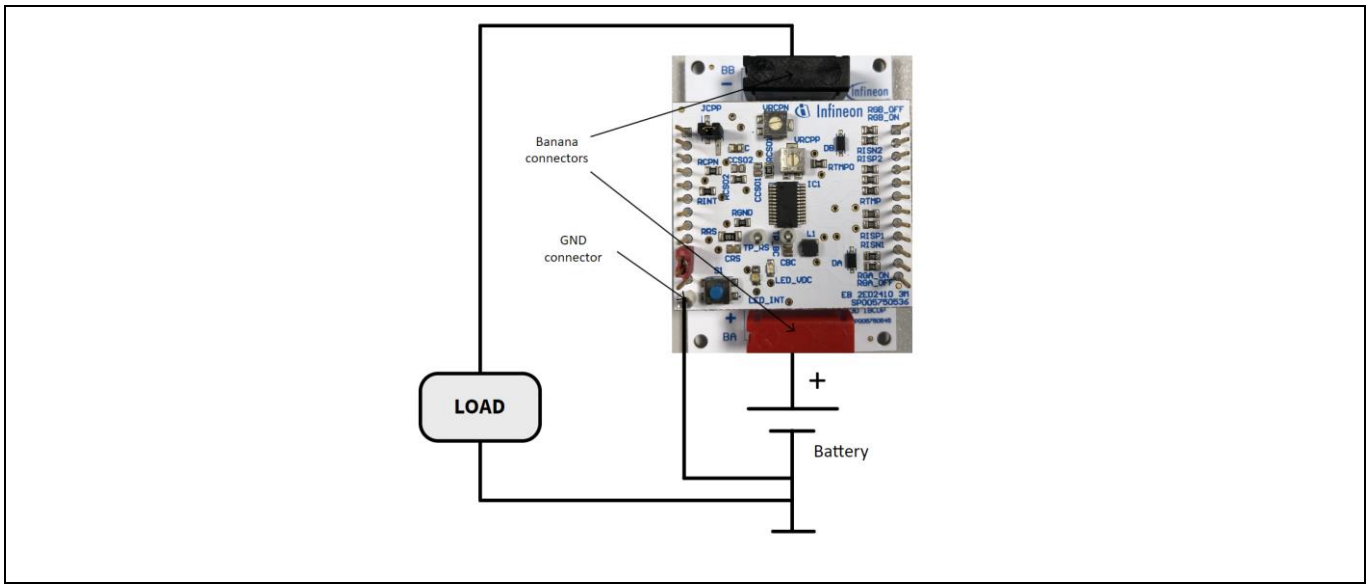

Figure 11 Power connection diagram with 3D-1BCDP, 3D-1BCS, 3D-1BCSP

LOAD: Electronic loads as well as classical passive elements are usable.

Battery: Lab bench power supplies and real batteries are usable.

2.3 Pins assignment and pins ratings

2ED2410-EM control, diagnostics and measurement pins are directly accessible through the left pin headers for direct use with waveform generators and oscilloscope. Can also be connected to a microcontroller control board/kit through small wires.

The right pin headers allow readings of all signals from and to the MOSFET and shunt for observation purposes, e.g. oscilloscope.

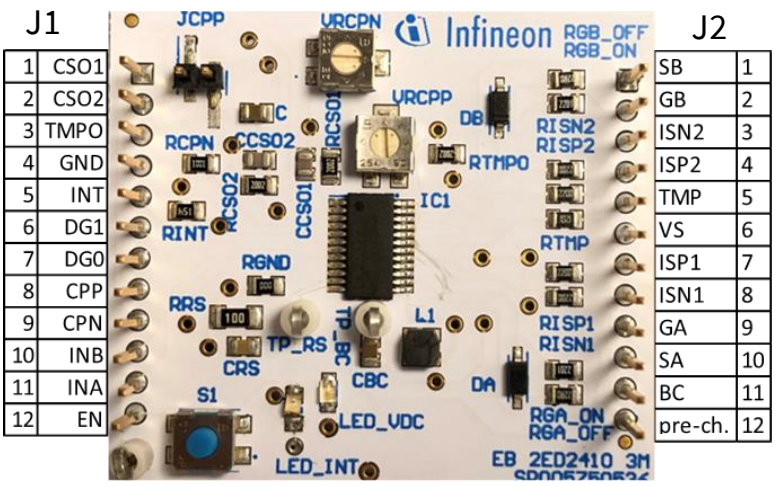

Figure 12 Pin header details with top view

Refer to 2ED2410-EM datasheet for details operating modes in chapter *5.1 Operating modes*.

Table 4 Pin ratings and visualization. Refer to component datasheet in case of doubt.

Pin	Min.	Max.	Unit	Visualization	Comment
CSO1, CSO2, TMPO	0	5.5	V	-	Analog outputs
ENABLE	0	5.5	V	LED_VDC	Turn-on ≥ 3V, turn-off ≤ 0.8V. Active by default if jumper JTLE is placed. JTLE can be removed and ENABLE supplied externally with pin header.
INA, INB	0	5.5	V	-	Turn-on ≥ 3V, turn-off ≤ 0.8V. Can be driven separately or together.
INT	0	V_{ENABLE}	V	LED_INT Red diode when SAFESTATE active	Low ≤ 0.5V indicates SAFESTATE.
CPP, CPN	0	5.5	V	-	Place JCPP to connect CPP to CSO2 through RC I-t wire. Adjust potentiometers to adjust wire protection.
DG0, DG1	0	V_{ENABLE}	V	-	Digital outputs
VS, SB, SA, ISxx, TMP	-42	45	V	-	Limited due to TLE42962 max. ratings. It is possible to remove and RREG1 and JTLE to enable board use up to VS=60V. adapt Z1 accordingly. Supply Enable pinexternally via pin header J1-12.
Pre-charge / 2N7002	0	10	V	-	To activate the level shifter which controls pre-charge MOSFET, only with 1BCDP and 1BCSP daughterboards.

2.4 Jumpers

Two 2mm jumpers are present on the board.

Table 5 Jumpers

Pin	Visualization	Comment
JCPP	On the top	Enables or disables the I-t wire protection. When taken off, RCPP and C are disconnected from CSO2. Connect the right side of JCPP pin header side to J1-4 (GND) to ground CPP pin if CP comparator is not used in your application.
JTLE	On the bottom	Enables or disables TLE42962GV50. When taken off, enable voltage can then be supplied externally from motherboard pin header J1-12.

2.5 Voltage ranges

Thanks to 2ED2410-EM wide operating and extended range, the next figure shows the voltage range that can be applied to 2ED2410-EM boards back-to-back compared to commonly accepted ranges based on ISO16750-2.

On the motherboard the TLE42862 is the limiting part regarding the maximum operating range.

Motherboard: - 45 V to + 45 V (or +58 V if TLE is disabled—JTLE open)

Daugherboards: - 60V to + 60 V (back to back 60 V MOSFET)

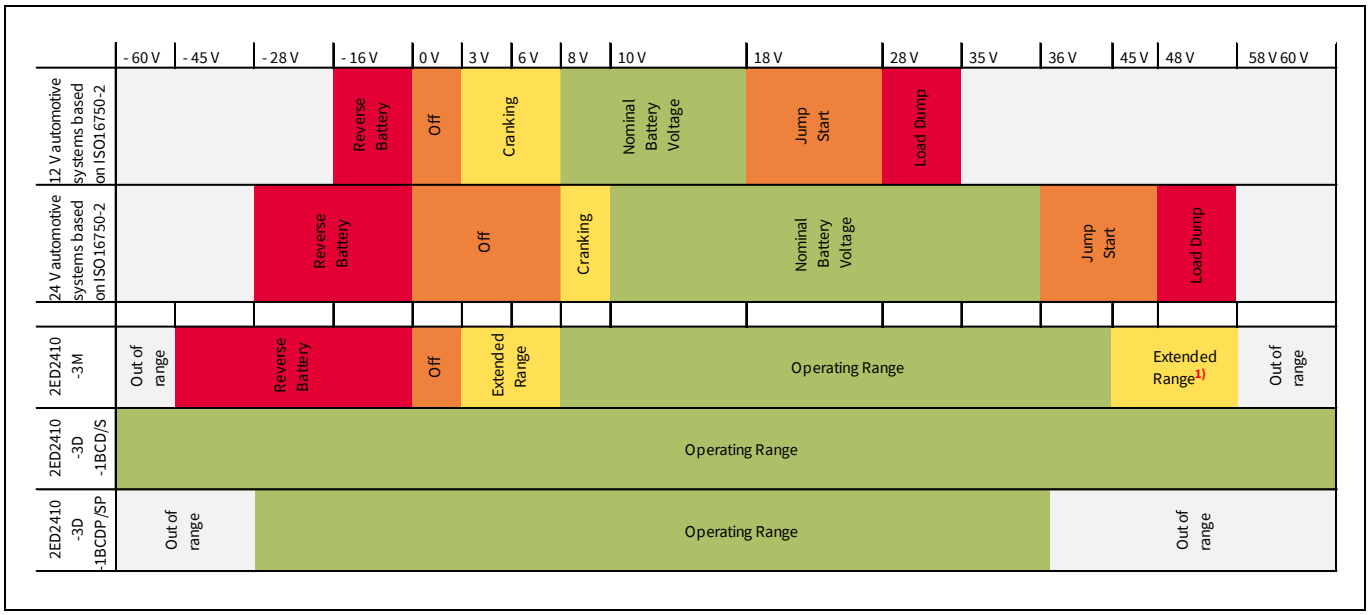

Figure 13 Voltage range for EB 2ED2410 3M/3D

2.6 Operation to avoid

Please never short the output BC of 2ED2410-EM to GND or to a potential lower than Vbat.

- ⇨ 2ED2410-EM will behave like a diode and will be destroyed (See diodes block diagram from 2ED2410-EM datasheet).
- ⇨ E.g. if you want to test UVLO protection feature (boost converter supply output) short BC to VS pin or battery-side connector.

2.7 Quiescent current

Quiescent current of 2ED2410-EM can be easily verified with back-to-back demoboard. The quiescent current is measured in SLEEP mode, the consumption is measured in IDLE mode and in ON mode in open load (to simulate no current drawn by load and consider only the consumption by the driver itself).

To assess quiescent current, ENABLE must be supplied externally and TLE42962GV50 must be disabled (take off jumper JTLE). Also, R_{LED_VDC} and V_{RCPN} must be removed (unsoldered) to save current consumption from LED_VDC and CPN voltage reference fixed by voltage divider (see schematic).

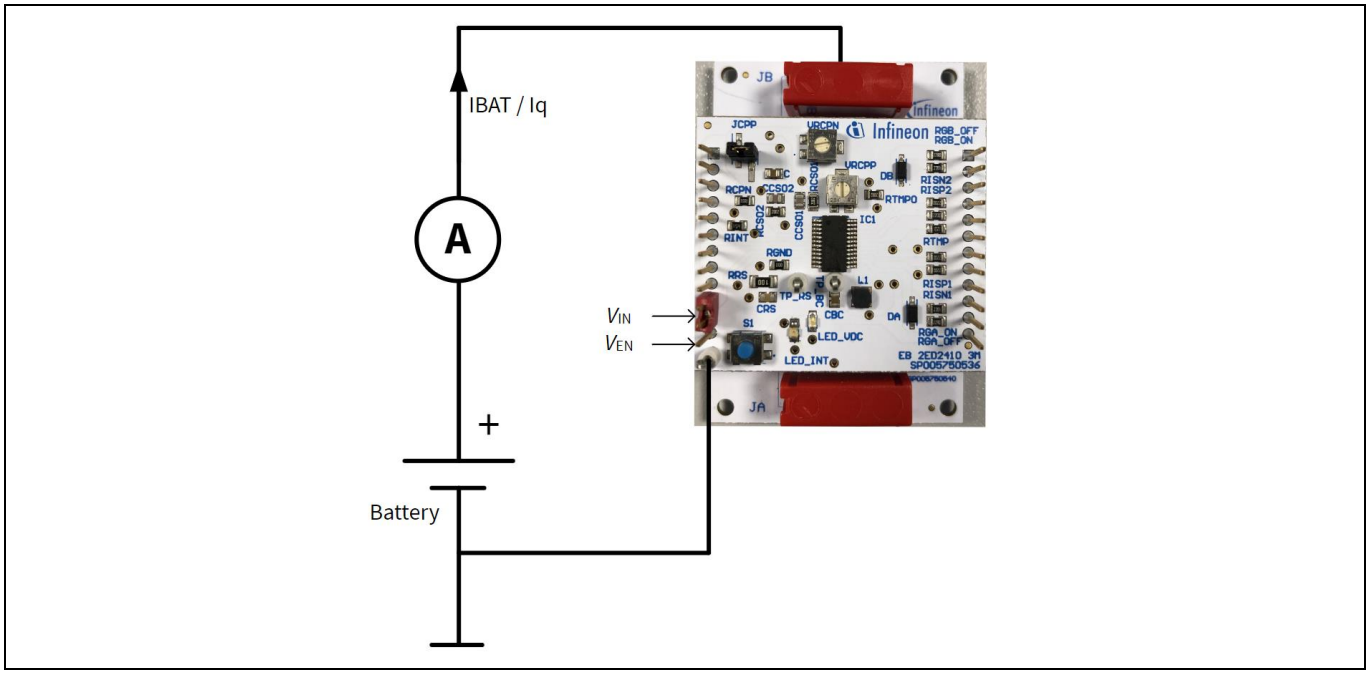

Figure 14 Test setup of quiescent current measurement

In some cases, CSA2 may not be needed in the application. Therefore, in the IBAT ON graph it is represented the consumption with the CSA2 disabled as per datasheet chapter 7.2. This allows a typical consumption <100 µA, at 12 V battery voltage, of the driver in ON mode when the load is not active or open.

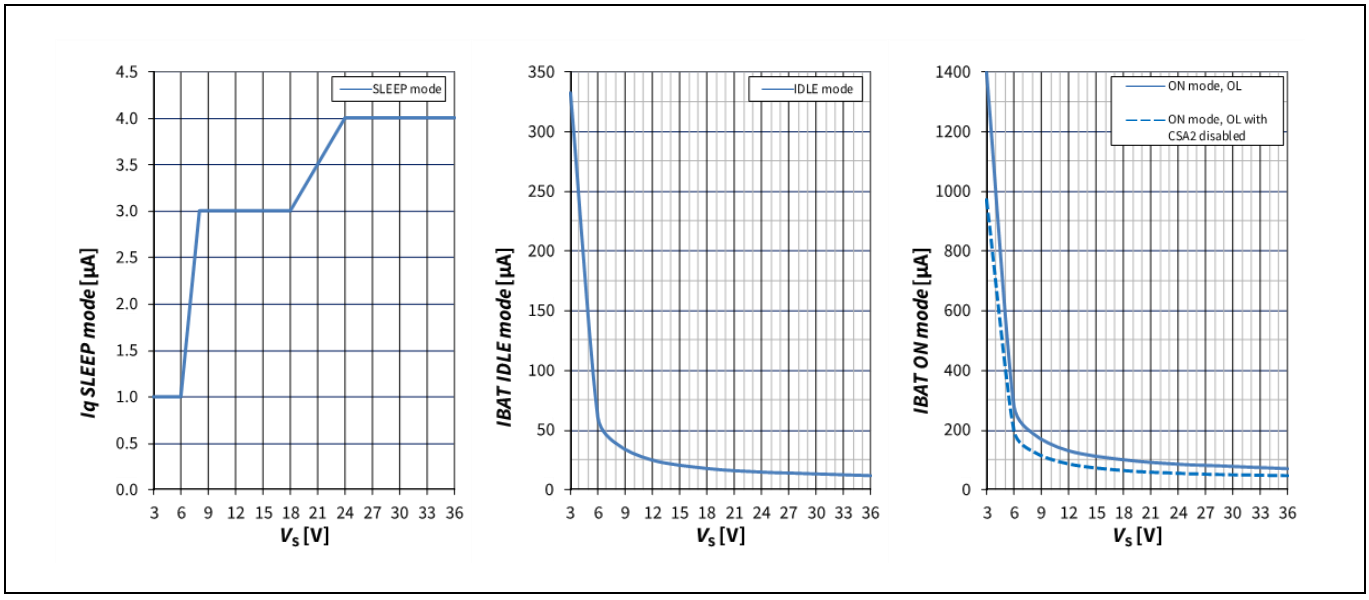

Figure 15 Quiescent current and consumption drawn from battery in SLEEP, IDLE and ON mode

3 Switching behavior

Note: Values shown in this chapter are measured under lab conditions and will vary for different cooling conditions and setups, and samples used.

3.1 Basic switching

Next figure shows switching behavior from SLEEP to IDLE mode. As soon as V_{EN} threshold is met, 2ED2410-EM powers up and the boost converter charges the driver supply C_{BC} (monitored by V_{BC}) in ~550 µs, given C_{BC}=1 µF, L1=100 µH, V_S=12 V. State machine is described in chap. 5 of 2ED2410-EM datasheet.

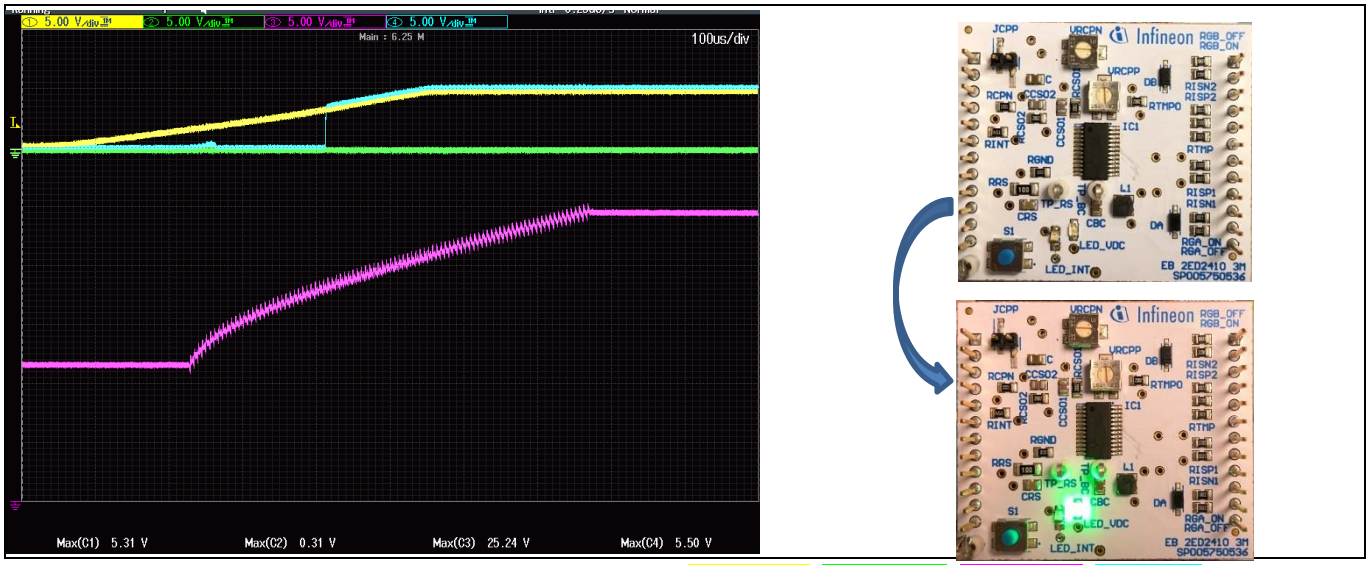

Figure 16 Waveforms from SLEEP to IDLE mode [Yellow V_{EN}; Green V_{DG0}; Purple V_{BC}; Blue V_{DG1}]

Next figure shows switching behavior from IDLE to ON mode. As current is pulled from C_{BC} to supply the gates, VBC-VS lowers and boost converter kicks in to regulate back the C_{BC} voltage. The pulses of the boost converter switch can be monitored on RS test point (TP_RS) or DG0 pin.

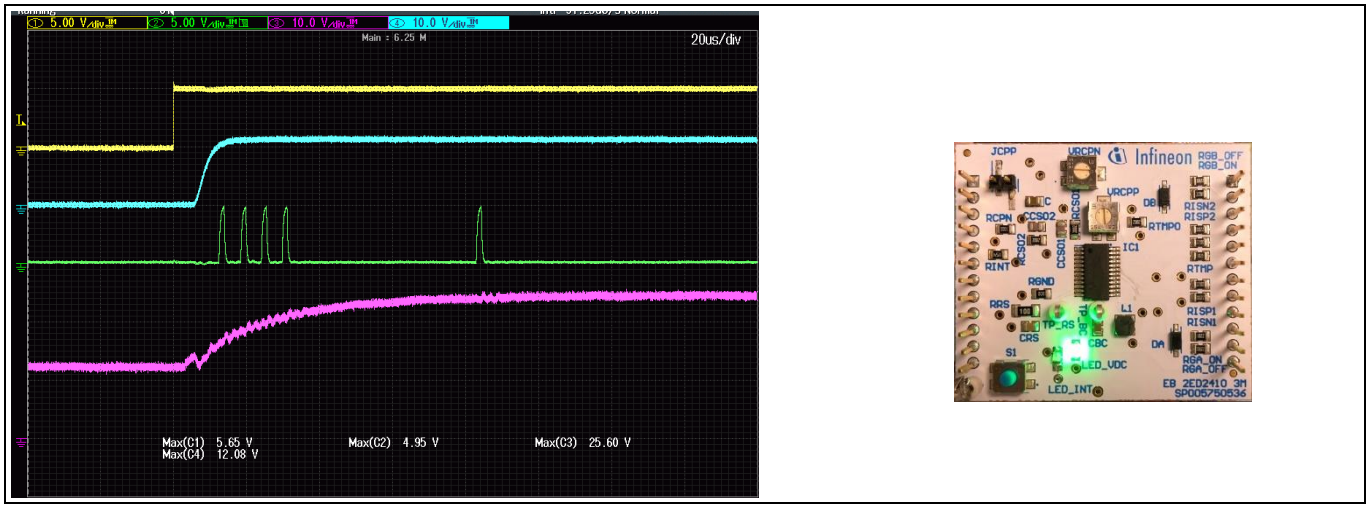

Figure 17 Waveforms from IDLE to ON [Yellow V_{IN}; Green V_{DG0}; Purple V_{GS}; Blue I_{LOAD}]

Next figure shows switching behavior from ON to IDLE mode, e.g. normal switch off of the switch.

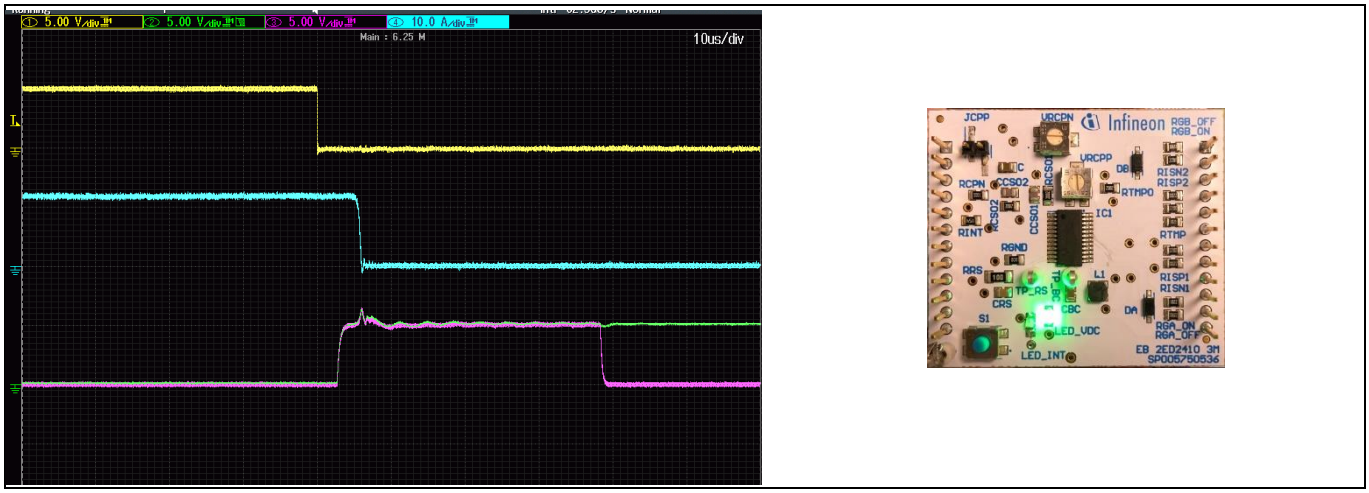

Figure 18 Waveforms from ON to IDLE [Yellow V_{IN}; Green V_{DG0}; Purple V_{DG1}; Blue I_{LOAD}]

3.2 Short-circuit event

Next figure shows switching behavior from ON to SAFESTATE mode. SAFESTATE mode is triggered here by a short circuit across the load resistor made by a loose wire, manually. The red LED_INT is lit.

In this example, Gain is set to 66.7 (R_{CSO1}=18 kΩ, R_{ISx1}=270 Ω), therefore the short-circuit limit is set to I_{SC} = 111 A.

Figure 19 Waveforms from ON to SAFESTATE [Yellow V_{INT}; Green V_{DG0}; Purple V_{DG1}; Blue V_{GS}]

To reset from SAFESTATE, press the push button S1 switch once. The driver will briefly go to SLEEP mode while the switch is pressed then will go back to IDLE mode if INA & INB are set to low. If INA or INB or both are set/remain high, the driver will go back to ON mode.

Note: INT signal in Figure 15 is slowed down by the Q2 PMOS (backside of the board) used to light the red LED_INT. Remove Q2 (unsolder) to check out INT pin falling edge signal. See 2ED2410-EM datasheet for INT pin details.

3.3 Pre-charge for capacitive loads (daughterboards -1BCSP / -1BCDP only)

Note: *This pre-charge circuit is only necessary if the embedded low by-pass current is not enough. See chapter 6 of 2ED2410-EM 's datasheet for a description of a low by-pass current feature.*

Pre-charge is controlled by pin J2-12 from mother board, provided that either board -1BCSP or -1BCDP is used. The goal of the pre-charge circuitry is to avoid or limit the inrush current due to the capacitive nature of the load, avoiding the unintended trigger of the short-circuit protection.

If no pre-charge is used, a capacitive load would trigger the short-circuit protection during turn-on of the switch, under normal operating conditions. In the example below, the inrush current reaches 79 A and the driver enters SAFESTATE (INT set to "low").

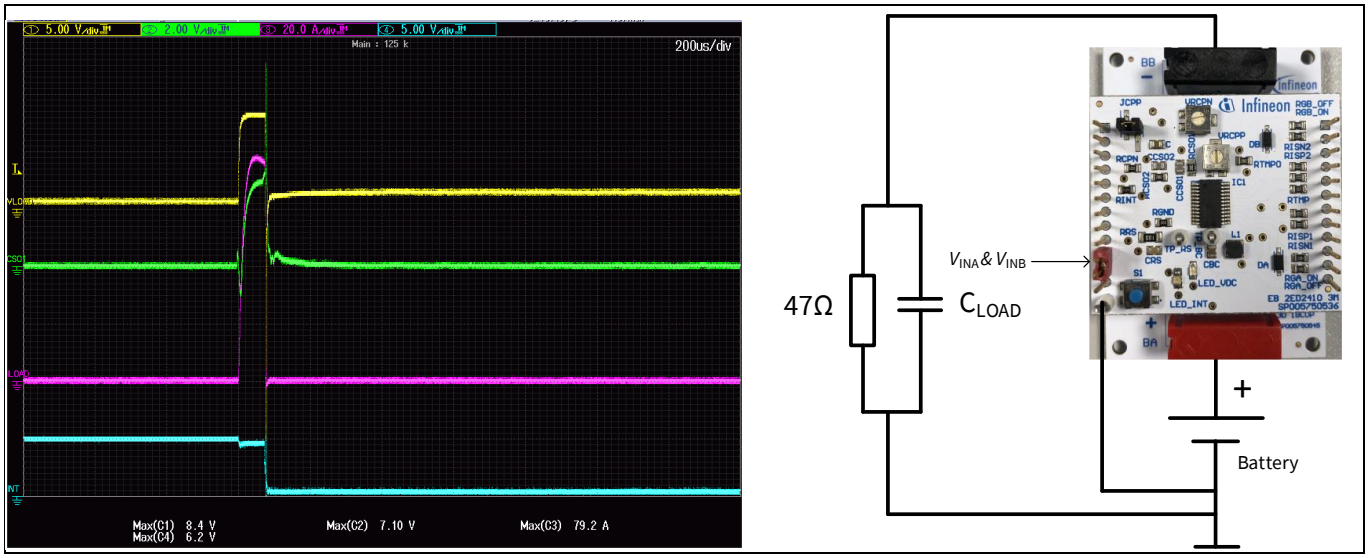

Figure 20 **Switching capacitive load with no pre-charge** [Yellow V_{LOAD}; Green V_{CS01}; Purple I_{LOAD}; Blue V_{INT}]

The pre-charged concept implemented on boards -1BCSP and -1BCDP, is a simple SMD resistor limiting the inrush current. The current is let throught the resistor with a MOSFET (M_pch), by-passing the main current path, and the MOSFET is driven by a push-pull providing the boosted BC voltage to the M_pch MOSFET gate. This circuit is an example of circuit re-using the 2ED2410-EM boost converter (BC) voltage and small signal Infineon MOSFET BSS83P and 2N7002.

Note: *There is no specific protection for the resistor R_pwr (6W resistor, see BOM). It is advised to limit the activation time of pre-charge pin to 150ms (either waveform generator or microcontroller). The circuit can be improved for more current/faster pre-charge time with two resistors in parallel.*

The following diagram shows the test set-up to for pre-charge control with a waveform generator. See table 4 for pre-charge pin rating J2-12.

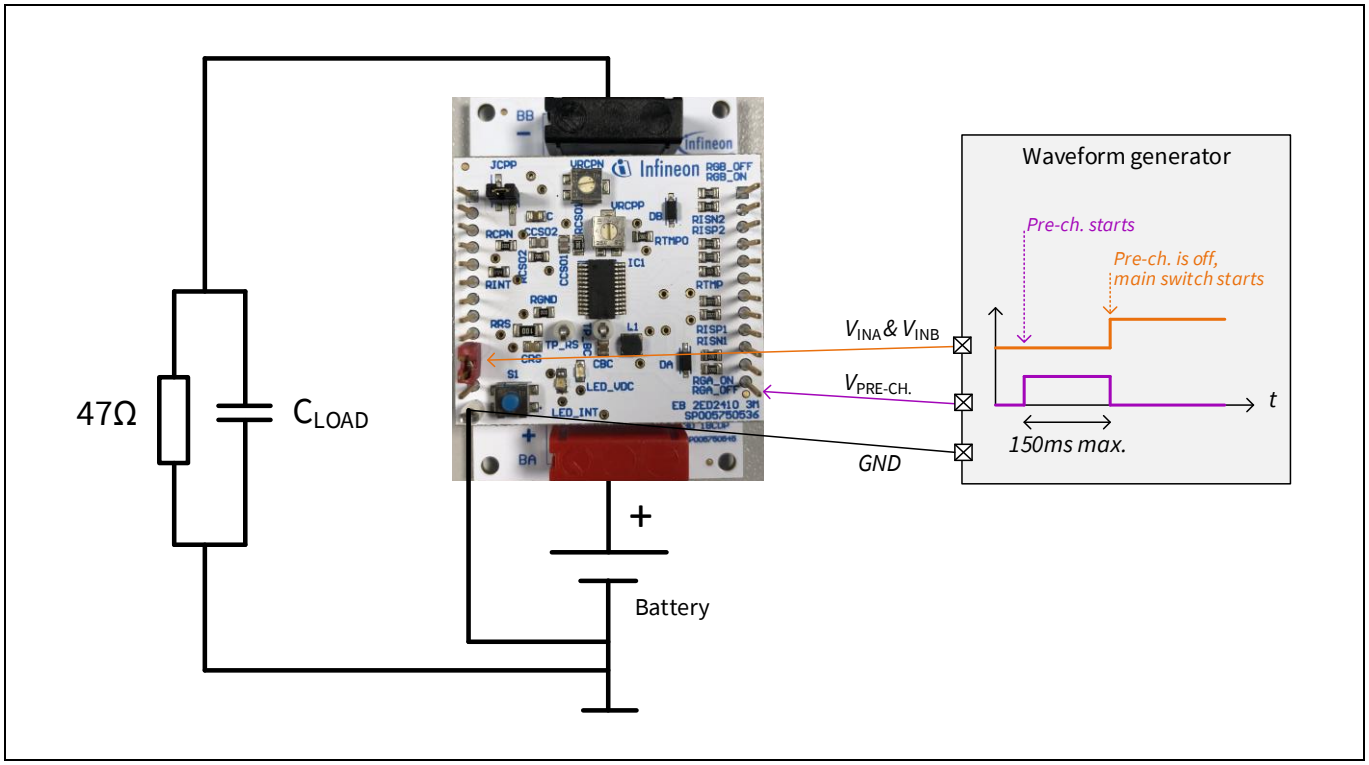

Figure 21 Test circuit of pre-charge control

The below picture shows a 150ms pre-charge of a capacitor C_{LOAD} = 6.8mF. The inrush is limited to 25 A and therefore short circuit protection/2ED2410-EM 's SAFESTATE is not triggered.

Figure 22 Switching capacitive load with pre-charge [Yellow V_{LOAD}; Green V_{CS01}; Purple I_{LOAD}; Blue V_{INT}]

4 Protections

4.1 2ED2410-EM short-circuit protection

Note: The EB 2ED2410-EM 3D boards are not designed for repetitive short-circuit operation. Short-circuit energy dissipation rely on MOSFET avalanche performance. Therfore the number of short-circuit cycles possible have to be calculated based on the customer's short-circuit test set-up.

2ED2410-EM has an internal short-circuit protection. By default, on the EB 2ED2410-EM 3M/3D this protection is set-up with:

- Shunt resistor value [on daughterboards 3D: $\boldsymbol{R_{SHUNT} = 500\ \mu\Omega}$].
- Gain used on amplifiers CSA1 [on motherboard 3M: $\boldsymbol{G = 91}$]. To adjust the gain on board, adapt R_{CSO1} or R_{CSO2} or R_{TMPO} within datasheet range and adapt R_{ISx} resistors based on datasheet gain range. Recommended to use 1 % error resistors or better.
- V_{ENABLE} [on motherboard 3M] is **5 V** from TLE42962GV50, but externally adjustable from **3 V to 5.5 V** if jumper JTLE is removed.

See 2ED2410-EM Getting started application note for details on calculation.

Table 6 Current short-circuit protection set on EB 2ED2410 3M depending on V_{ENABLE}

V_{ENABLE}	3	3.3	4	5	5.5	V	Given G = 91 and R_{SHUNT} = 500 µΩ as mounted on daughterboards.
Short-circuit current limit	49	54	65	80	90	A	

4.2 I-t wire protection with comparator CP

On the EB 2ED2410 3M board, jumper JCPP allow analog output CSO2 to be looped to comparator CP input CPP (positive input of comparator CP, see 2ED2410-EM datasheet).

I-t wire protection settings possibilities

- C value is fixed (10 µF)
- RCPP is adjustable between 0 and 250 kΩ with VRCPP potentiometer
- $V_{CP(REF)}$ on pin CPN is adjustable with potentiometer VRCPN, adapting voltage divider between VENABLE and CPN pin (see schematics for details). As a result, $V_{CP(REF)}$ can be set between 4.16 V and 1 V (see datasheet for $V_{CP(REF)}$ limitations).

Note: RCPN can be unsoldered and $V_{CP(REF)}$ fixed externally with pin header. C can be changed to desired value. VRCPP can also be changed for a fixed higher value resistor up to 470kΩ.

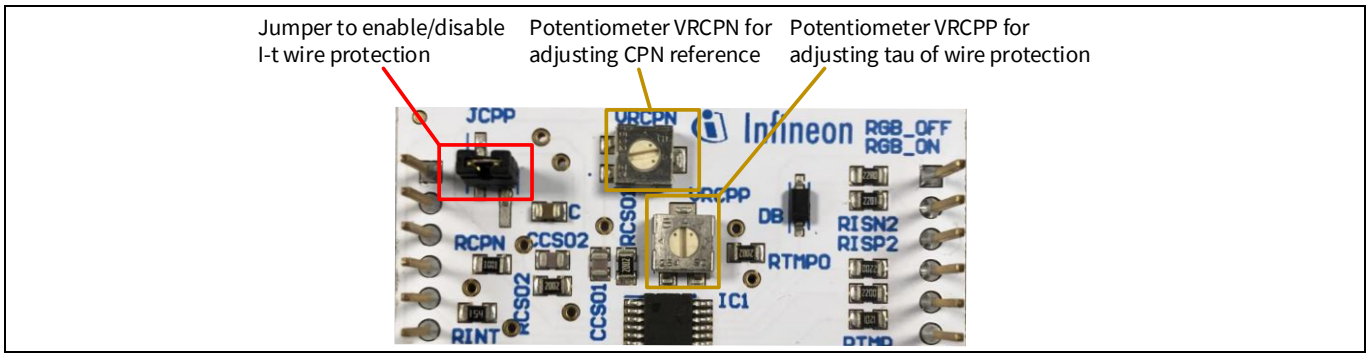

Figure 23 How to set I-t wire protection

The following graph shows the I-t wire protection curve adjustment area (in orange color) with VRCPN and VRCPP given the default short-circuit value and components on EB 2ED2410 3M/3D (EiceDRIVER™ 2ED2410 Tool, downloadable from the 2ED2410-EM website or Infineon Development Center in future).

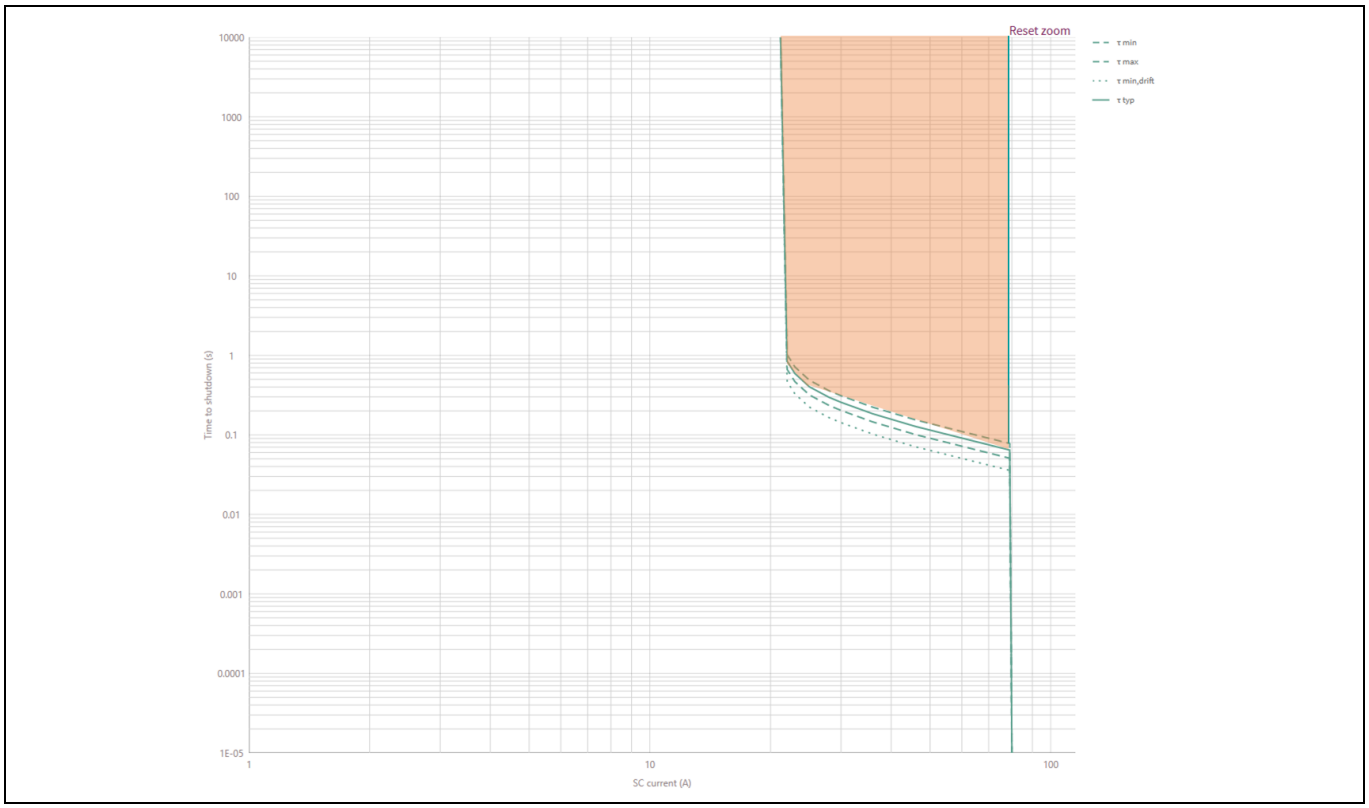

Figure 24 I-t wire setting range

4.3 Over temperature protection with comparator CP

To simply check **over temperature protection, disconnect JCPP and connect TMPO pin header to CPP** pin header with a jump wire.

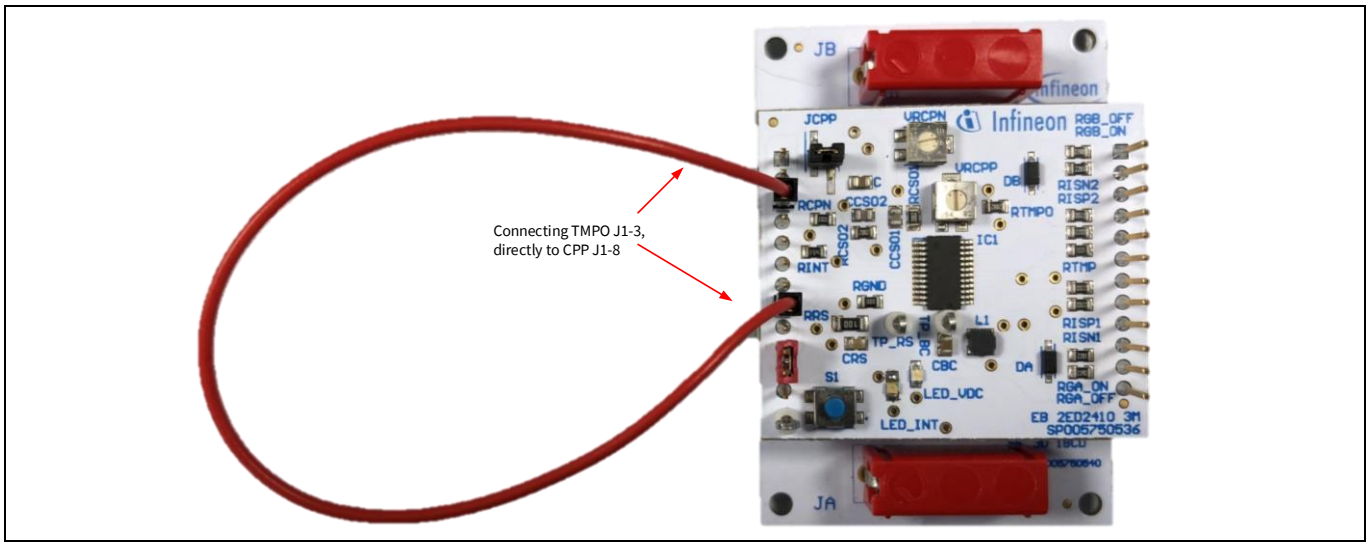

Figure 25 How to wire overtemperature protection

The threshold of overtemperature can be set with $V_{CP(REF)}$ on CPN pin, same operation as I-t wire threshold.

The below graph shows the implemented temperature curve in the EB 2ED2410 3M/3D boards, given V_{EN}= 5 V, RTMP, RNTC and RTMPO as described in the BOM chap. 5.1.
Depending on the target PCB temperature for shutdown, the threshold of the temperature has to be set accordingly. For example, for an overtemperature shutdown at a PCB temperature of 100°C, the threshold on CPN pin has to be set to $V_{CP(REF)}$ = 2.3 V.

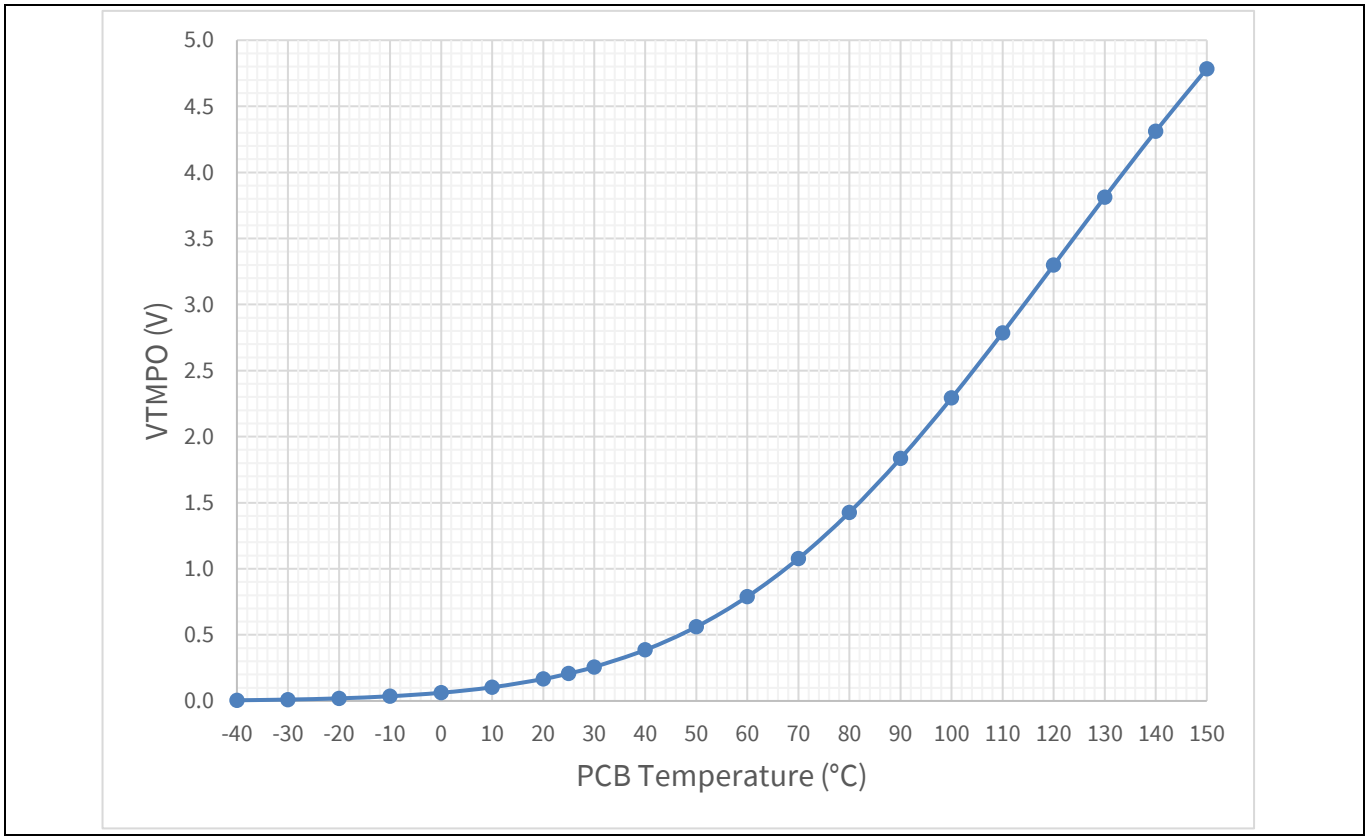

Figure 26 Temperature output curve vs. top PCB temperature

5 Electrical schematic

5.1 BOM

5.1.1 EB 2ED2410 3M

Reference	Description	Designator	Qty
10 µF / 10 V	Capacitor	C	1
1 µF / 25 V	Capacitor	CBC	1
100 pF/10 V	Capacitor	CCSO1, CCSO2	2
100 nF / 100 V	Capacitor	CREG_in, CVS	2
4.7 µF / 10 V	Capacitor	CREG_out	1
10 nF / 6.3 V	Capacitor	CRS	1
1N4148	Diode	DA, DB	2
2ED2410-EM	Integrated Circuit	IC1	1
SSQ-112-03-G-S	Connector	J1, J2	2
TMM-102-01-F-S-SM	Connector	JCPP, JTLE	2
VLS3015CX-101M-H	Inductor	L1, 100µH from TDK, AEC-Q200	1
597-3003-407F (RED)	LED	LED_INT	1
150080GS75000 (GREEN)	LED	LED_VDC	1
BSS83P	MOSFET (P-Channel)	Q2	1
1K (0805)	Resistor	RCPN, RENABLE, RLED_INT, RLED_VDC	4
20K (0805) 1%	Resistor	RCSO1, RCSO2, RTMPO	3
22R (0805) 1%	Resistor	RGA_OFF, RGB_OFF	2
2.2K (0805)	Resistor	RGA_ON, RGB_ON	2
0R (0805)	Resistor	RGND	1
150K (0805)	Resistor	RINT	1
220R (0805) 1%	Resistor	RISN1, RISN2, RISP1, RISP2	4
10R (0805)	Resistor	RQ1	1
100R (0805)	Resistor	RREG1	1
N.C. (0805)	Resistor	RREG2	1
10R (1206, 0.5 W min.)	Resistor	RRS	1
1.2K (0805)	Resistor	RTMP	1
7914G-1-000E	Switch	S1	1
TLE42962GV50	Integrated Circuit	TLE	1
20-313143	Test Point	TP_BC, TP_RS	2
3314G-1-502E	Variable Resistor	VRCPN	1
3314G-1-254E	Variable Resistor	VRCPP	1
SML4758AHE3_A_H	Zener Diode	Z1	1

5.1.2 EB 2ED2410 3D 1BCD or 1BCS

Reference	Description	Designator	Qty
973582101 - red	Connector	JA/BA, JB/BB	2
BAV23C-Q	Diode (1BCS only)	D	1
MMSZ5245BT1G	Zener Diode	DA, DB	2
TSW-112-07-G-S	Connector	J1, J2	2
973582101	Connector	JA, JB	2
IAUC120N06S5N011	MOSFET (N-Channel)	QA, QB	2
BVB-Z-R0005-1.0	Resistor	R_sense	1
100ohm, 0805	Resistor	RA, RB	2
100K / nc	Resistor	Rgs_A, Rgs_B	2
NCU18WB473F6SRB	Thermistor	RNTC	1

5.1.3 EB 2ED2410 3D 1BCDP or 1BCSP

Reference	Description	Designator	Qty
973582101 - red	Connector	BA	1
973582100 - black	Connector	BB	1
BAV23C-Q	Diode (1BCSP only)	D1	1
MMSZ5245BT1G	Zener Diode	D/D2	1
MMSZ5245BT1G	Zener Diode	DA, DB	2
TSW-112-07-G-S	Connector	J1, J2	2
IAUC120N06S5N011	MOSFET (N-Channel)	M_Pch, MA, MB	3
NCU18WB473F6SRB	Thermistor	NTC	1
2N7002	MOSFET (N-Channel)	Q	1
10K, 0805	Resistor	R1, R2, R3, R5	4
N.C. 0805	Resistor	Rgs_A, Rgs_B	2
100, 0805	Resistor	R4, Rg_A, Rg_B	3
10, 2512	PCNM2512E10R0BST5 Power Resistor	R_pow	1
BVB-Z-R0005-1.0	Resistor_shunt/ BVB-Z-R0005-1.0	R_sense	1
BSS83P	MOSFET (P-Channel)	T	1

5.2 Electrical diagrams

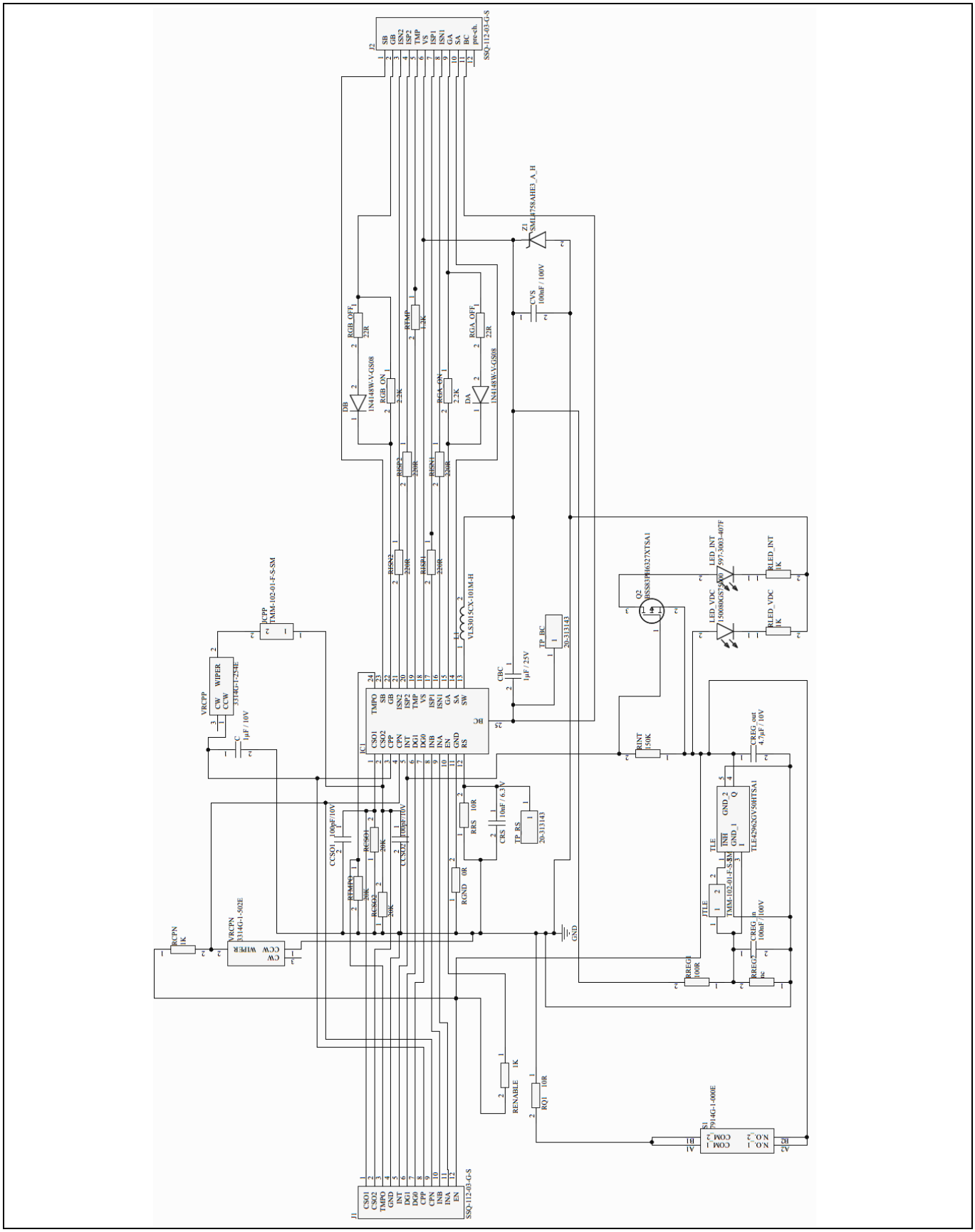

Figure 27 EB 2ED2410 3M

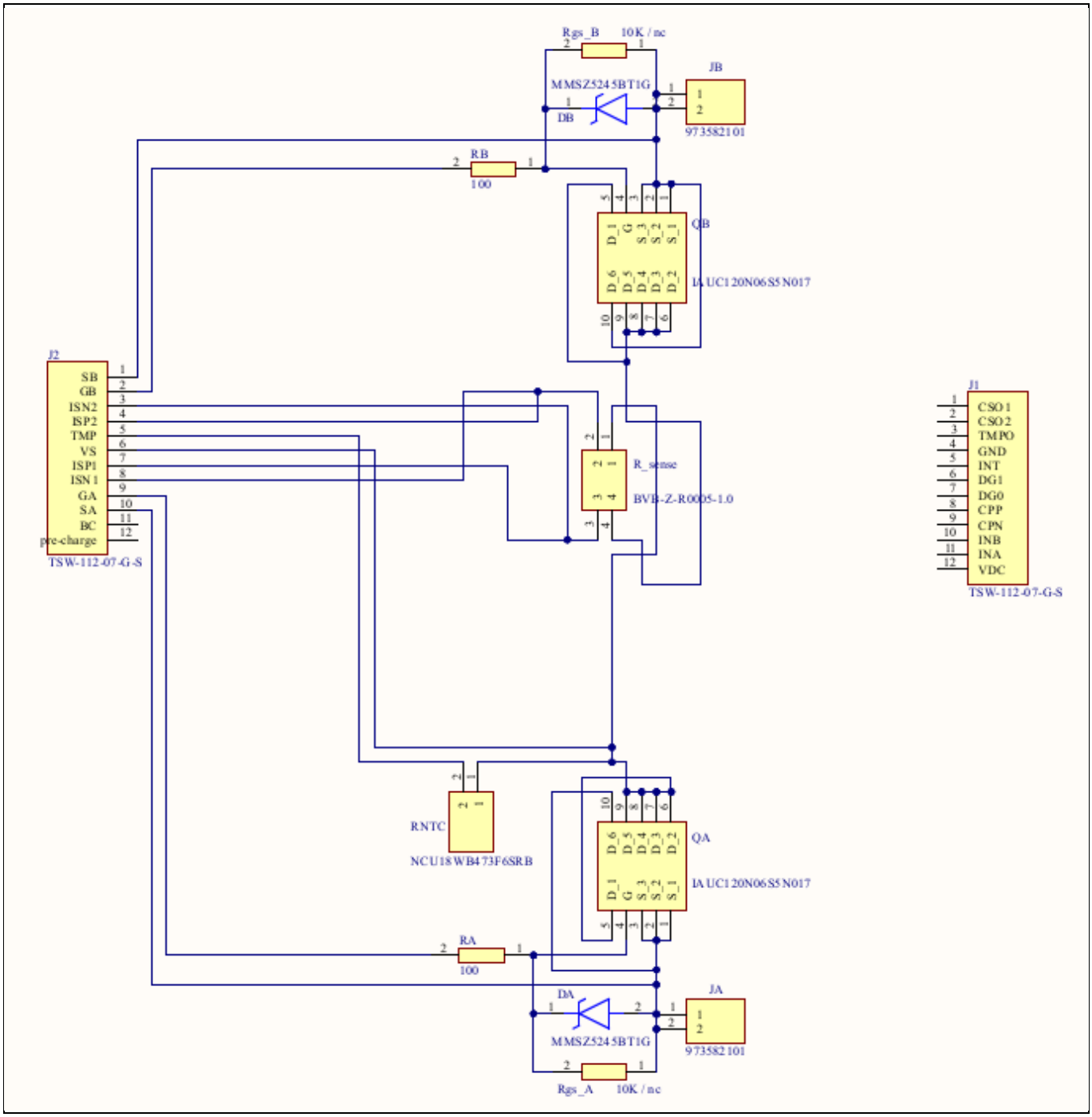

Figure 28 EB 2ED2410 3D 1BCD

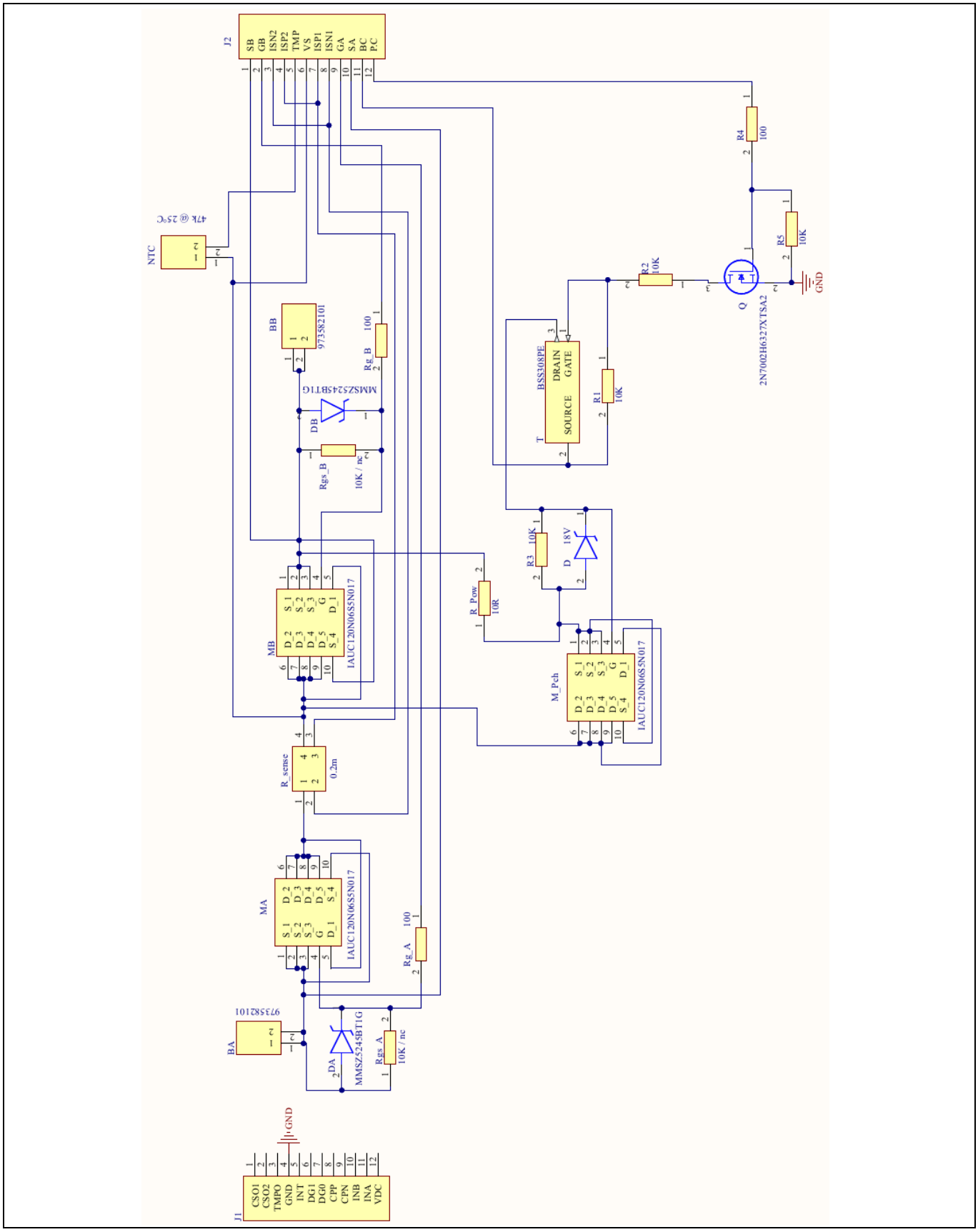

Figure 29 EB 2ED2410 3D 1BCDP

6 PCB details

EB 2ED2410 3M PCB is a 4-layers, HTG-150 material board.

EB 2ED2410 3M PCB is a 2-layers, HTG-150 material board.

Figure 30 EB 2ED2410 3M PCB layers 4 * 35µm

Figure 31 EB 2ED2410 3D PCB layers 2 * 70µm

6.1 Layers EB 2ED2410 3M

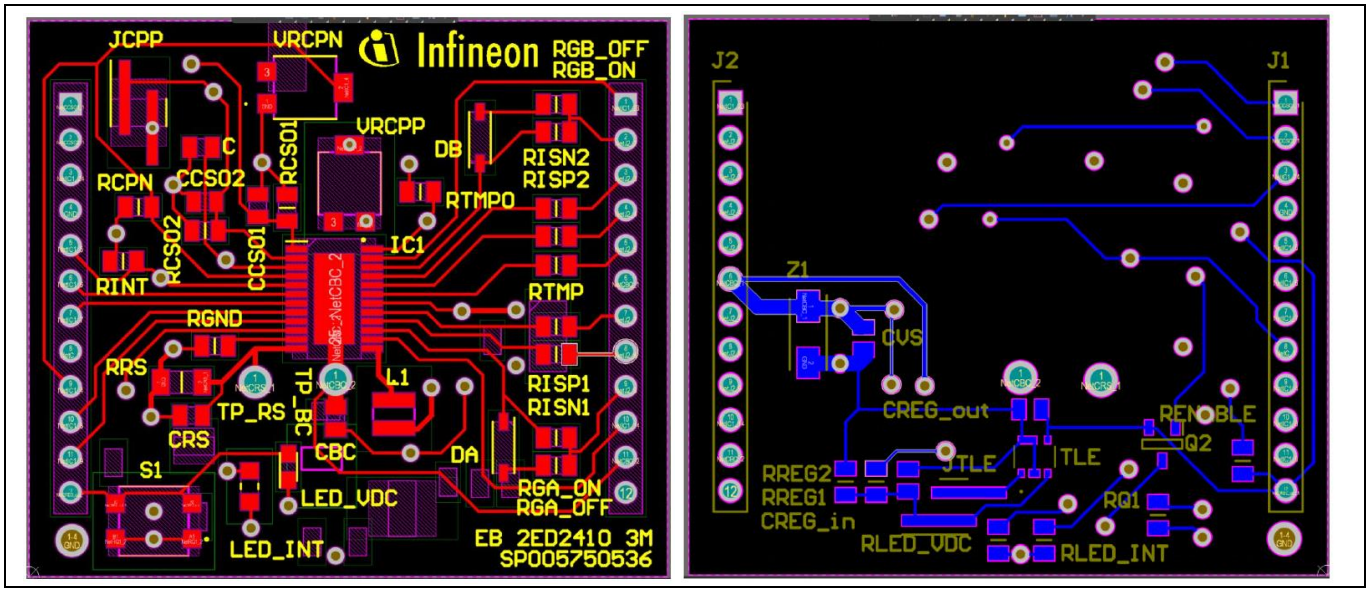

Figure 32 **Top layer signal** [35 µm] and **Bottom layer signal** [35 µm]

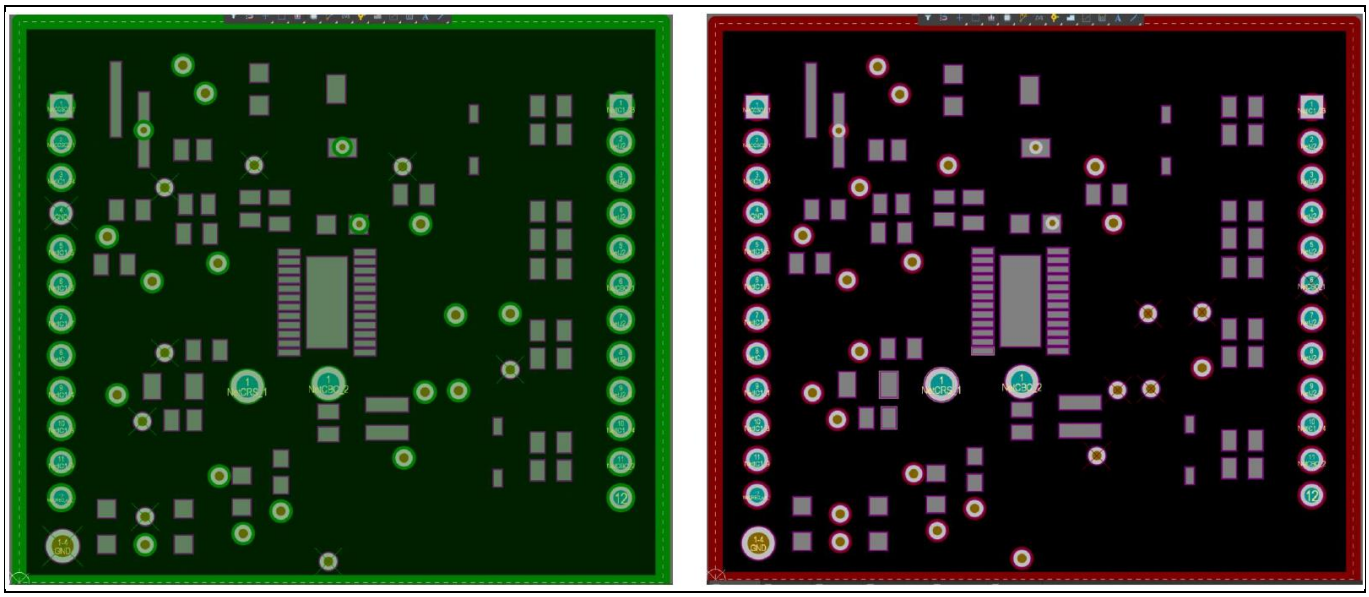

Figure 33 **Mid layers Vref** [35 µm] and **GND** [35 µm]

6.2 Layers EB 2ED2410 3D 1BCD

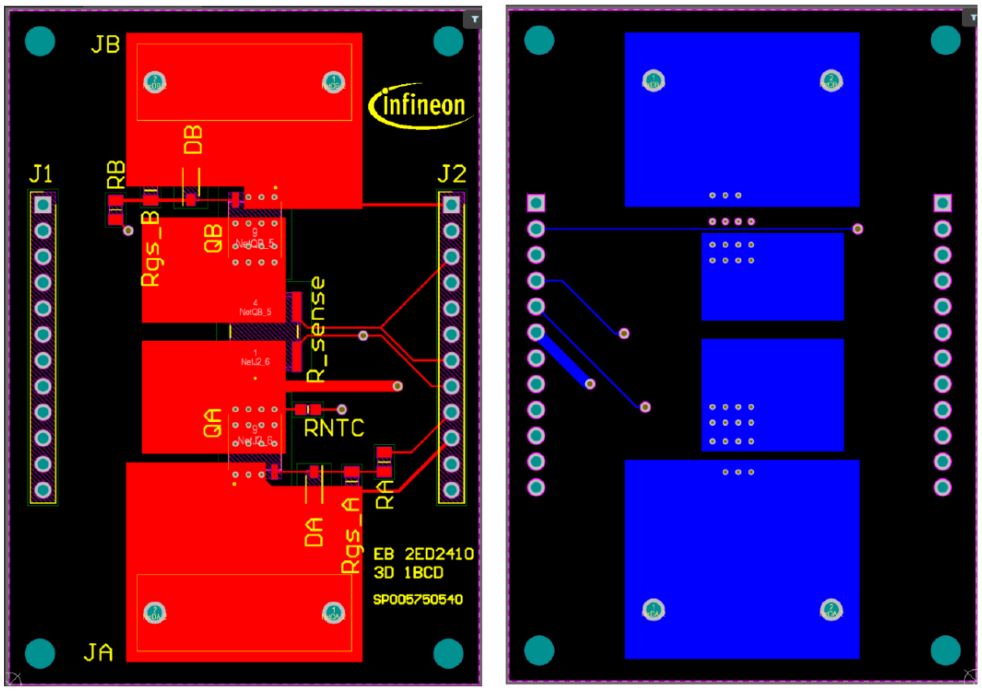

Figure 34 **Top Layer** [70µm] and **bottom layer** [70µm]

6.3 Layers EB 2ED2410 3D 1BCDP

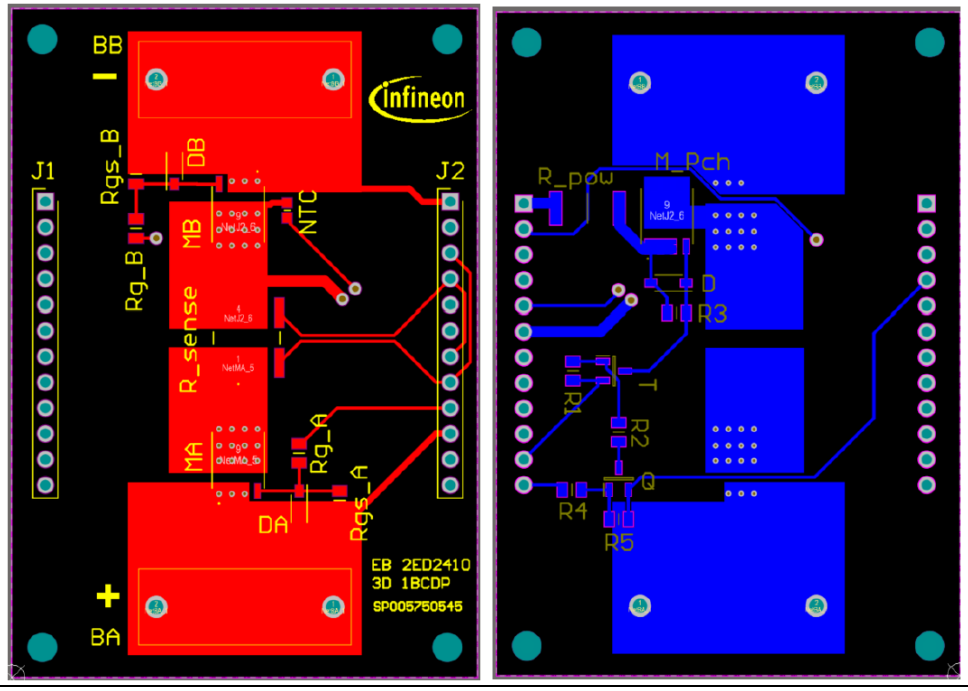

Figure 35 **Top Layer** [70µm] and **bottom layer** [70µm]

7 References

[1] Infineon Technologies AG, Datasheet: EiceDRIVER 2ED2410-EM V02_10

[2] Infineon Technologies AG, Application note , Getting started with 2ED2410-EM

[3] Infineon Technologies AG, Datasheet: OptiMOS™ -5 Power-Transistor 60 V – IAUC120N06S5N011

Revision history

Document version	Date of release	Description of changes
Rev.1.00	2022-07-27	First release
Rev.1.01	2023-03-15	Chapter 2.7 updated: for quiescent current measurement, remove V_{RCPN} and R_{LED_VDC}. Note added below figure 7.