

EFM32 Gecko Family

EFM32G Data Sheet



The EFM32 Gecko MCUs are the world's most energy-friendly microcontrollers.

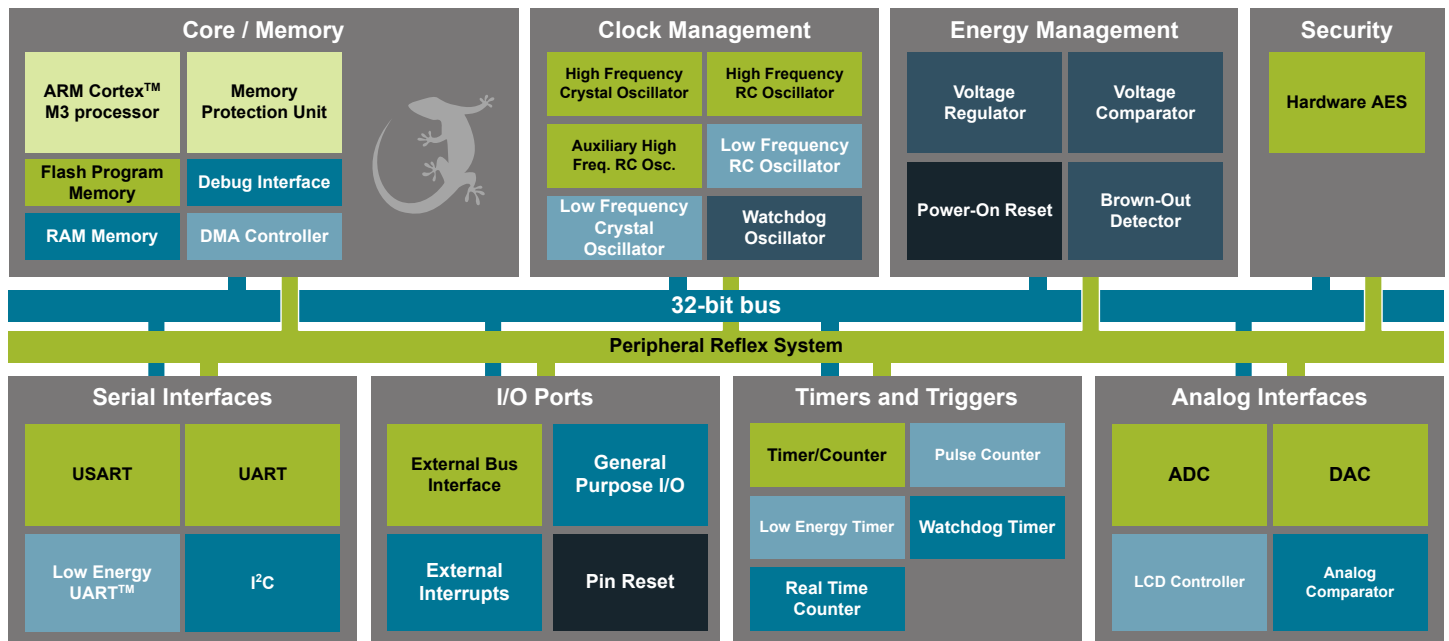
The EFM32G offers unmatched performance and ultra low power consumption in both active and sleep modes. EFM32G devices consume as little as 0.6 μA in Stop mode and 180 $\mu\text{A}/\text{MHz}$ in Run mode. It also features autonomous peripherals, high overall chip and analog integration, and the performance of the industry standard 32-bit ARM Cortex-M3 processor, making it perfect for battery-powered systems and systems with high-performance, low-energy requirements.

EFM32G applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation

KEY FEATURES

- ARM Cortex-M3 at 32 MHz
- Ultra low power operation
 - 0.6 μA current in Stop (EM3), with brown-out detection and RAM retention
 - 45 $\mu\text{A}/\text{MHz}$ in EM1
 - 180 $\mu\text{A}/\text{MHz}$ in Run mode (EM0)
- Fast wake-up time of 2 μs
- Hardware cryptography (AES)
- Up to 128 kB of Flash and 16 kB of RAM



Lowest power mode with peripheral operational:



1. Feature List

- ARM Cortex-M3 CPU platform
 - High Performance 32-bit processor @ up to 32 MHz
 - Memory Protection Unit
 - Wake-up Interrupt Controller
 - SysTick System Timer
- Flexible Energy Management System
 - 20 nA @ 3 V Shutoff Mode
 - 0.6 μ A @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 0.9 μ A @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 45 μ A/MHz @ 3 V Sleep Mode
 - 180 μ A/MHz @ 3 V Run Mode, with code executed from flash
- 128/64/32 KB Flash
- 16/8 KB RAM
- Up to 90 General Purpose I/O pins
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 16 asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- 8 Channel DMA Controller
- 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Hardware AES with 128/256-bit keys in 54/75 cycles
- Timers/Counters
 - 3 \times 16-bit Timer/Counter
 - 3 \times 3 Compare/Capture/PWM channels
 - Dead-Time Insertion on TIMER0
 - 16-bit Low Energy Timer
 - 1 \times 24-bit Real-Time Counter
 - 3 \times 8-bit Pulse Counter
 - Watchdog Timer with dedicated RC oscillator @ 50 nA
- Integrated LCD Controller for up to 4 \times 40 segments
 - Voltage boost, adjustable contrast and autonomous animation
- External Bus Interface for up to 4 \times 64 MB of external memory mapped space
- Communication interfaces
 - Up to 3 \times Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
 - Triple buffered full/half-duplex operation
 - 1 \times Universal Asynchronous Receiver/Transmitter
 - 2 \times Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - I²C Interface with SMBus support
 - Address recognition in Stop Mode
- Ultra low power precision analog peripherals
 - 12-bit 1 Msamples/s Analog to Digital Converter
 - 8 single-ended channels/4 differential channels
 - On-chip temperature sensor
 - 12-bit 500 ksamples/s Digital to Analog Converter
 - 2 single-ended channels/1 differential channel
 - 2 \times Analog Comparator
 - Capacitive sensing with up to 16 inputs
 - Supply Voltage Comparator

- Ultra efficient Power-on Reset and Brown-Out Detector
- 2-pin Serial Wire Debug Interface
 - 1-pin Serial Wire Viewer
- Pre-Programmed UART Bootloader
- Temperature range -40 to 85 °C
- Single power supply 1.98 to 3.8 V
- Packages
 - BGA112
 - LQFP100
 - TQFP64
 - TQFP48
 - QFN64
 - QFN32

2. Ordering Information

The following table shows the available EFM32G devices.

Table 2.1. Ordering Information

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (°C) | Package |
|-------------------------|------------|----------|-----------------|--------------------|------------------|---------|
| EFM32G200F16G-E-QFN32 | 16 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32G200F32G-E-QFN32 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32G200F64G-E-QFN32 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32G210F128G-E-QFN32 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32G222F32G-E-QFP48 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32G222F64G-E-QFP48 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32G222F128G-E-QFP48 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32G230F32G-E-QFN64 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32G230F64G-E-QFN64 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32G230F128G-E-QFN64 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32G232F32G-E-QFP64 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32G232F64G-E-QFP64 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32G232F128G-E-QFP64 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32G280F32G-E-QFP100 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32G280F64G-E-QFP100 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32G280F128G-E-QFP100 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32G290F32G-E-BGA112 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32G290F64G-E-BGA112 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32G290F128G-E-BGA112 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32G840F32G-E-QFN64 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32G840F64G-E-QFN64 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32G840F128G-E-QFN64 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32G842F32G-E-QFP64 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32G842F64G-E-QFP64 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32G842F128G-E-QFP64 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32G880F32G-E-QFP100 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32G880F64G-E-QFP100 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32G880F128G-E-QFP100 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32G890F32G-E-BGA112 | 32 | 8 | 32 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32G890F64G-E-BGA112 | 64 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | BGA112 |
| EFM32G890F128G-E-BGA112 | 128 | 16 | 32 | 1.98 - 3.8 | -40 - 85 | BGA112 |

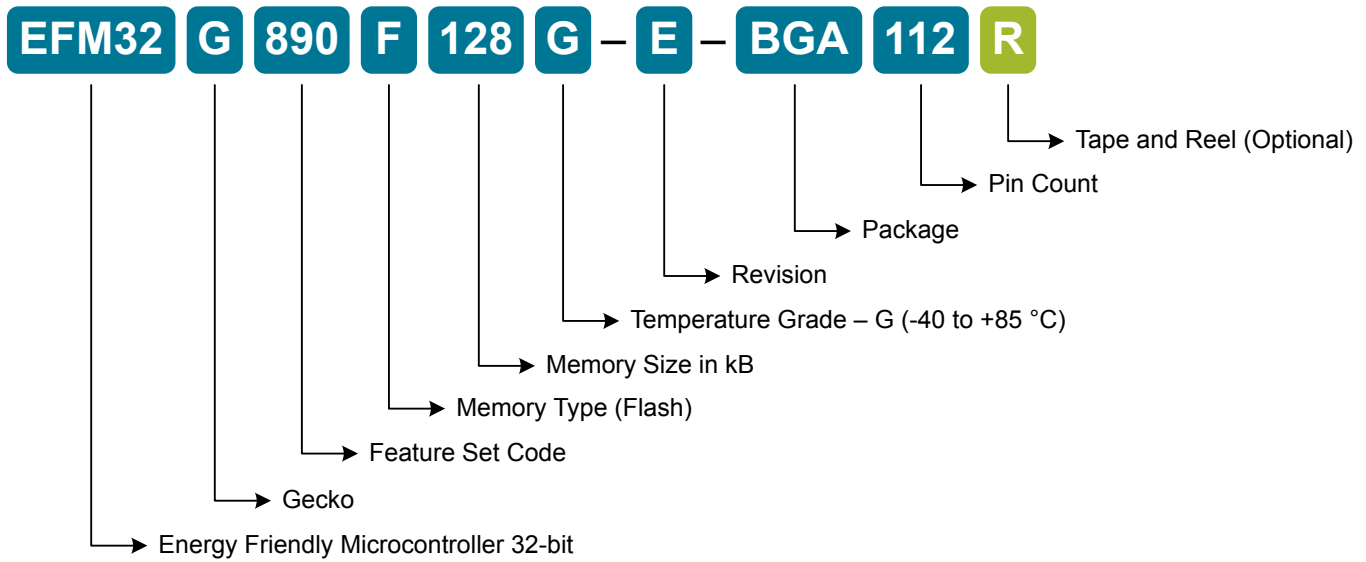


Figure 2.1. Ordering Code Decoder

Adding the suffix 'R' to the part number (e.g., EFM32G890F128G-E-BGA112R) denotes tape and reel.

Visit www.silabs.com for information on global distributors and representatives.

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3. System Overview

3.1 System Introduction

EFM32 MCUs are the world’s most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32G Reference Manual.

The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

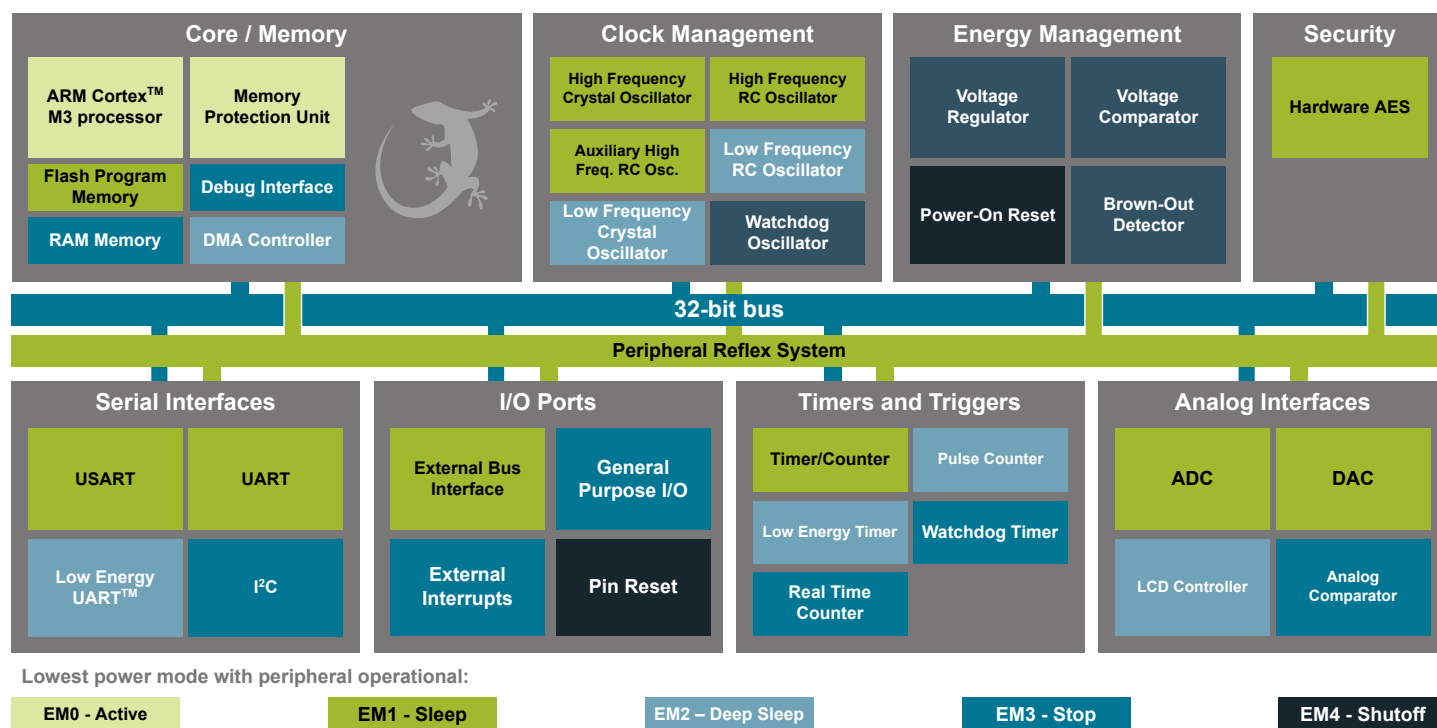


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32G Reference Manual.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32G.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manages all the low energy modes (EM) in EFM32G microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32G. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

3.1.11 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 Smart-Cards, and IrDA devices.

3.1.13 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0003.0 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

3.1.14 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

3.1.15 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/ s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.16 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

3.1.17 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.18 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

3.1.19 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.20 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.21 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.22 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

3.1.23 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single-ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

3.1.24 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

3.1.25 General Purpose Input/Output (GPIO)

General Purpose Input/Output (GPIO) pins are organized into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.1.26 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 4x40 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.2 Configuration Summary

3.2.1 EFM32G200

The features of the EFM32G200 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.1. EFM32G200 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:5], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[0] |
| GPIO | 24 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.2 EFM32G210

The features of the EFM32G210 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.2. EFM32G210 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:5], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[0] |
| AES | Full configuration | NA |
| GPIO | 24 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.3 EFM32G222

The features of the EFM32G222 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.3. EFM32G222 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[1] |
| AES | Full configuration | NA |
| GPIO | 37 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.4 EFM32G230

The features of the EFM32G230 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.4. EFM32G230 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 56 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.5 EFM32G232

The features of the EFM32G232 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.5. EFM32G232 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[15:8], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[0] |
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.6 EFM32G280

The features of the EFM32G280 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.6. EFM32G280 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0] |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 86 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.7 EFM32G290

The features of the EFM32G290 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.7. EFM32G290 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0] |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 90 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.8 EFM32G840

The features of the EFM32G840 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.8. EFM32G840 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:4], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 56 pins | Available pins are shown in Table 4.3 (p. 57) |
| LCD | Full configuration | LCD_SEG[23:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

3.2.9 EFM32G842

The features of the EFM32G842 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.9. EFM32G842 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[3:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:4], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[0] |
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in Table 4.3 (p. 57) |

3.2.10 EFM32G880

The features of the EFM32G880 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.10. EFM32G880 Configuration Summary

| Module | Module | Module |
|-----------|--|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0] |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 86 pins | Available pins are shown in Table 4.3 (p. 57) |

| Module | Module | Module |
|--------|--------------------|---|
| LCD | Full configuration | LCD_SEG[39:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

3.2.11 EFM32G890

The features of the EFM32G890 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.11. EFM32G890 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|--|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0] |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 90 pins | Available pins are shown in Table 4.3 (p. 57) |

| Module | Configuration | Pin Connections |
|--------|--------------------|---|
| LCD | Full configuration | LCD_SEG[39:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

3.3 Memory Map

The EFM32G memory map is shown in the figure below. RAM and Flash sizes are for the largest memory configuration.

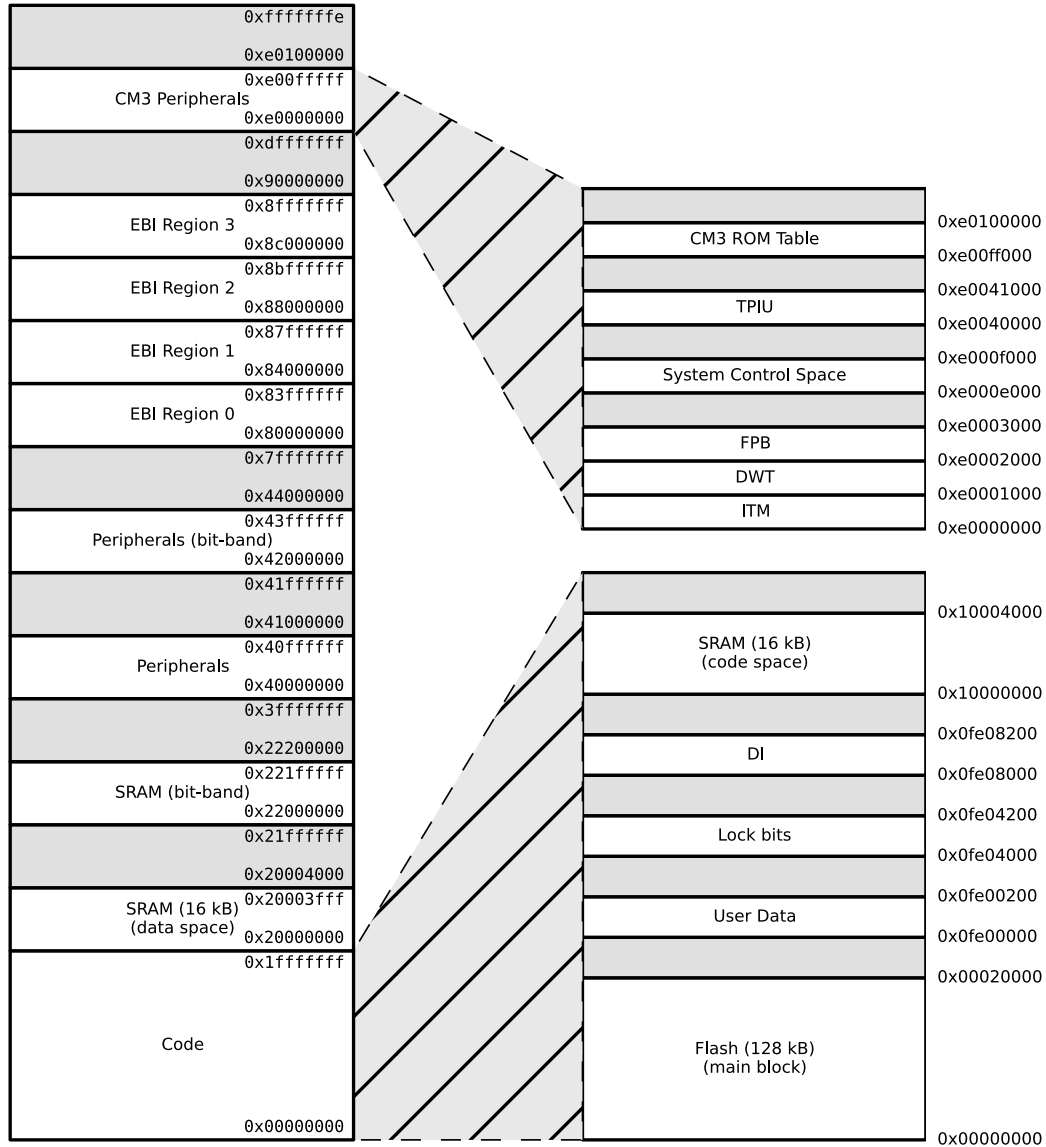


Figure 3.2. System Address Space with Core and Code Space Listing

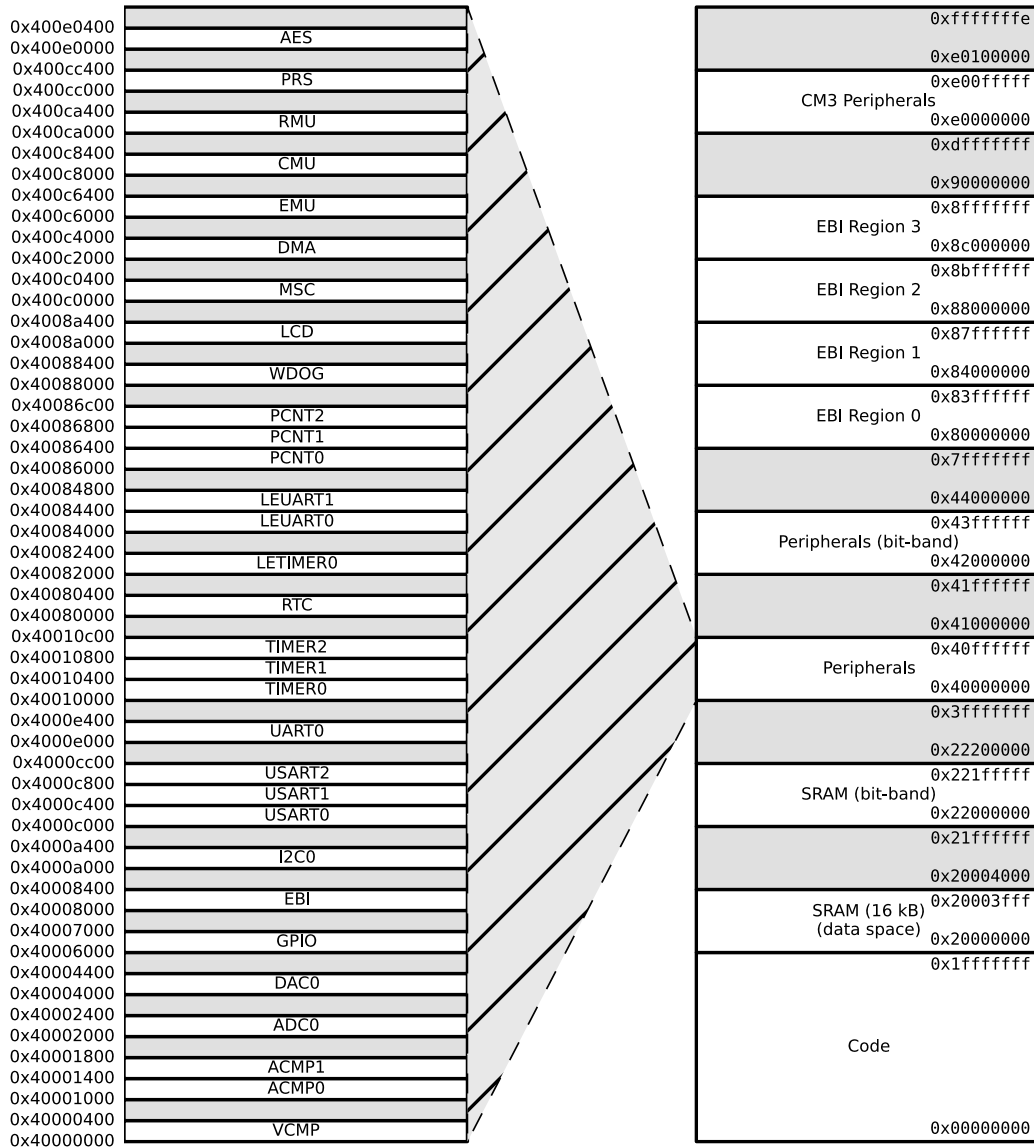


Figure 3.3. System Address Space with Peripheral Listing

4. Electrical Characteristics

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in [Table 4.2 General Operating Conditions on page 29](#), unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in [Table 4.2 General Operating Conditions on page 29](#), unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the following table may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in [Table 4.2 General Operating Conditions on page 29](#).

Table 4.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|---------------------|-------------------------------------|------|-----|--------------|--------------------|
| Storage temperature range | T_{STG} | | -40 | — | 150 | $^{\circ}\text{C}$ |
| Maximum soldering temperature | T_S | Latest IPC/JEDEC J-STD-020 Standard | — | — | 260 | $^{\circ}\text{C}$ |
| External main supply voltage | V_{DDMAX} | | 0 | — | 3.8 | V |
| Voltage on any I/O pin | V_{IOPIN} | | -0.3 | — | $V_{DD}+0.3$ | V |
| Current per I/O pin (sink) | I_{IOMAX_SINK} | | — | — | 100 | mA |
| Current per I/O pin (source) | I_{IOMAX_SOURCE} | | — | — | -100 | mA |

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------|------------|------|-----|-----|--------------------|
| Ambient temperature range | T_{AMB} | -40 | — | 85 | $^{\circ}\text{C}$ |
| Operating supply voltage | V_{DDOP} | 1.98 | — | 3.8 | V |
| Internal APB clock frequency | f_{APB} | — | — | 32 | MHz |
| Internal AHB clock frequency | f_{AHB} | — | — | 32 | MHz |

4.4 Current Consumption

Table 4.3. Current Consumption

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------|--|-----|------|-------|--------|
| EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz) | I _{EM0} | 32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 180 | — | μA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 181 | 206 | μA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 183 | 207 | μA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 185 | 211 | μA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 186 | 215 | μA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 191 | 218 | μA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 220 | — | μA/MHz |
| EM1 current (Production test condition = 14 MHz) | I _{EM1} | 32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 45 | — | μA/MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 47 | 62 | μA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 48 | 64 | μA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 50 | 69 | μA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 51 | 72 | μA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 56 | 83 | μA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 103 | — | μA/MHz |
| EM2 current | I _{EM2} | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25 °C | — | 0.9 | 1.5 | μA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =85 °C | — | 3.0 | 6.0 | μA |
| EM3 current | I _{EM3} | V _{DD} = 3.0 V, T _{AMB} =25 °C | — | 0.59 | 1.0 | μA |
| | | V _{DD} = 3.0 V, T _{AMB} =85 °C | — | 2.75 | 5.8 | μA |
| EM4 current | I _{EM4} | V _{DD} = 3.0 V, T _{AMB} =25 °C | — | 0.02 | 0.045 | μA |
| | | V _{DD} = 3.0 V, T _{AMB} =85 °C | — | 0.25 | 0.7 | μA |

4.4.1 EM0 Current Consumption

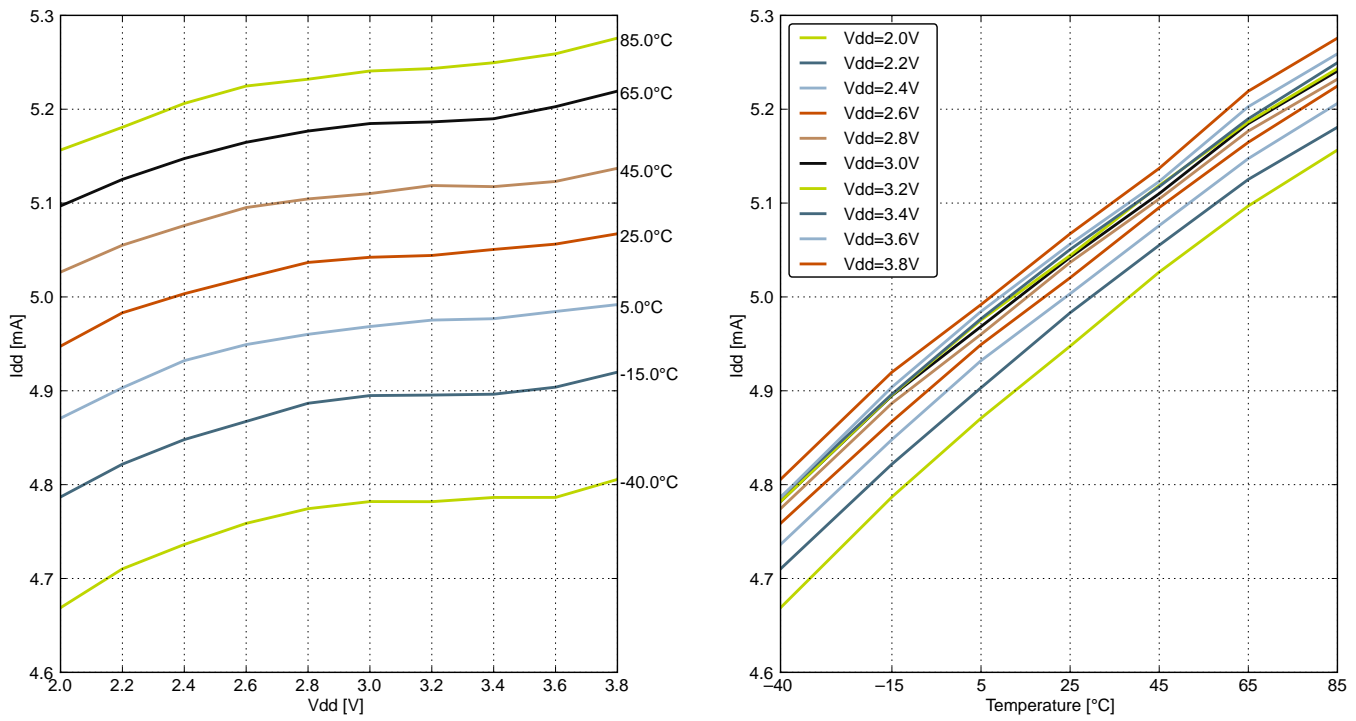


Figure 4.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28 MHz

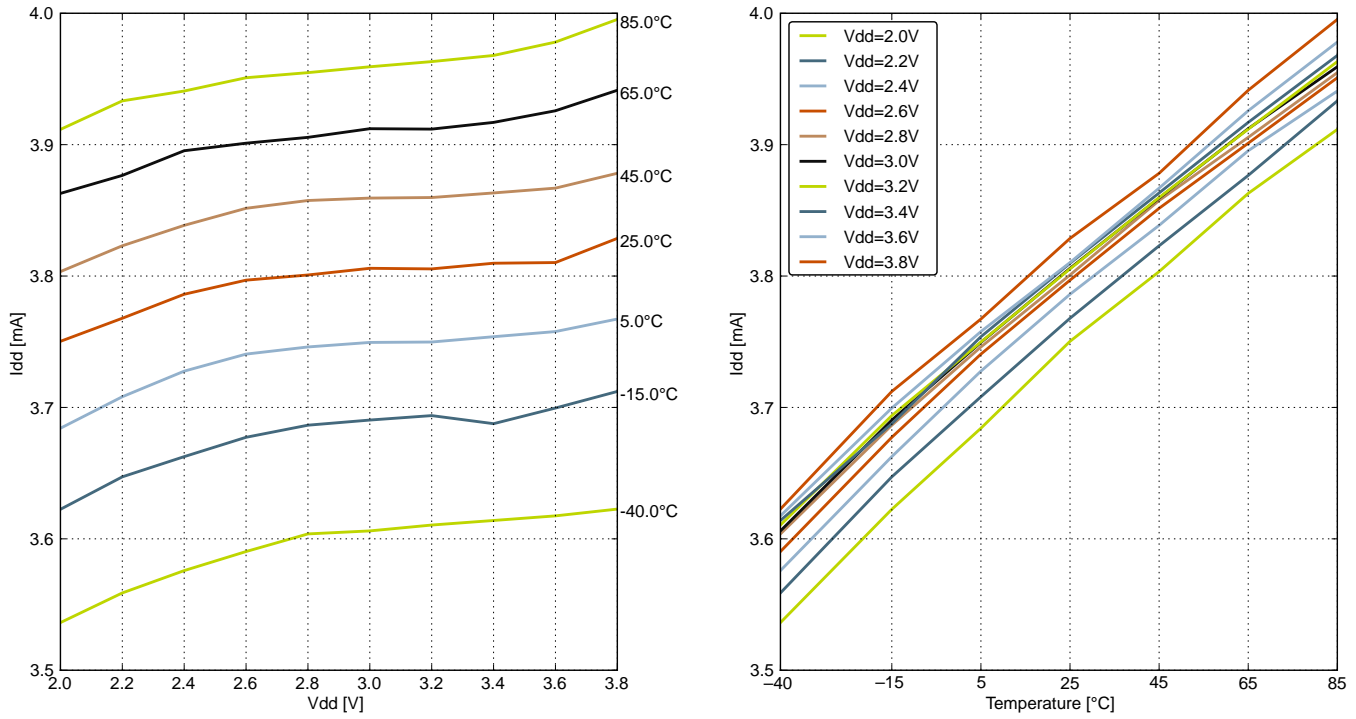


Figure 4.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz

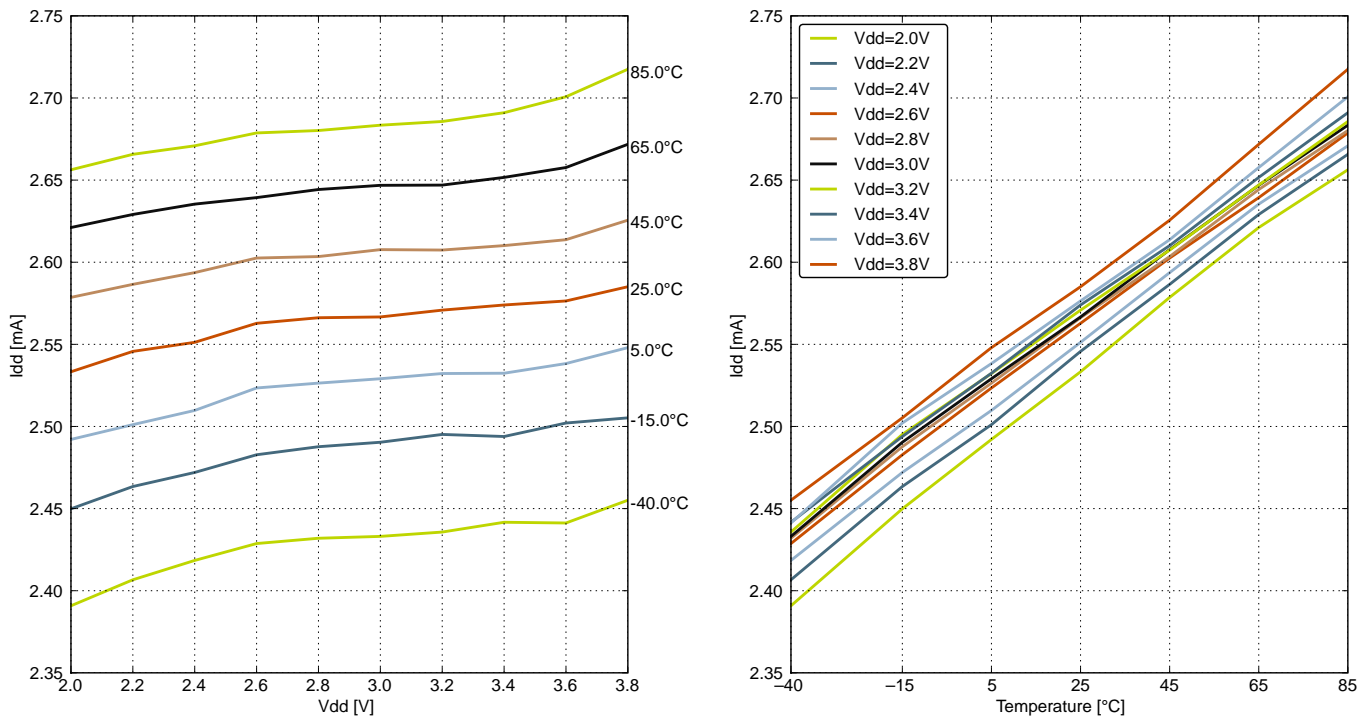


Figure 4.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

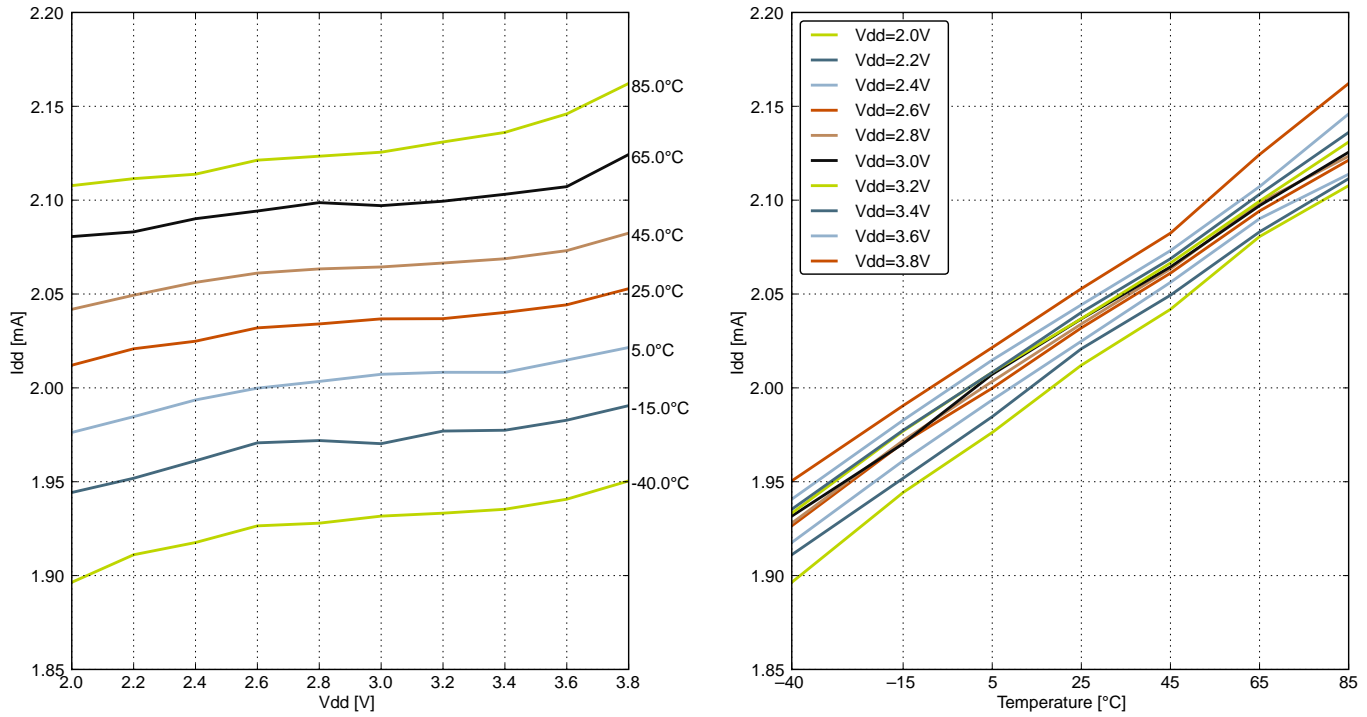


Figure 4.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz

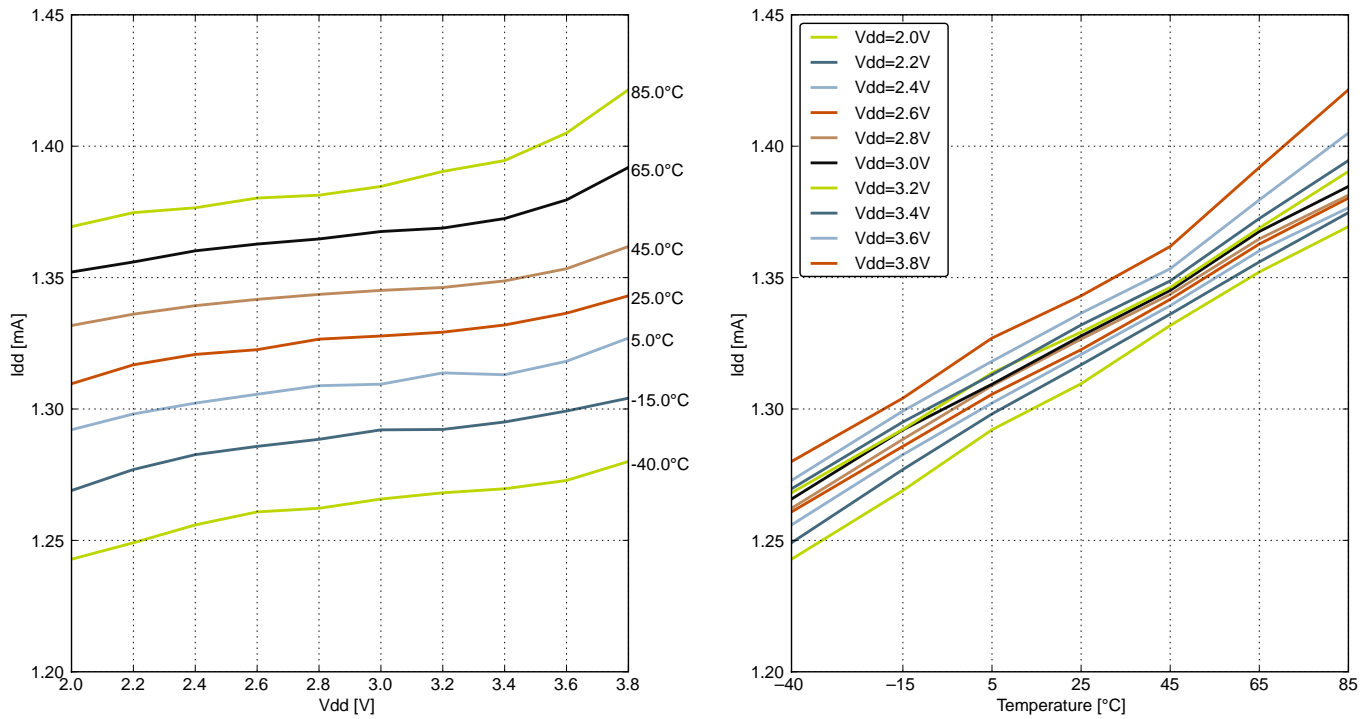


Figure 4.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 7 MHz

4.4.2 EM1 Current Consumption

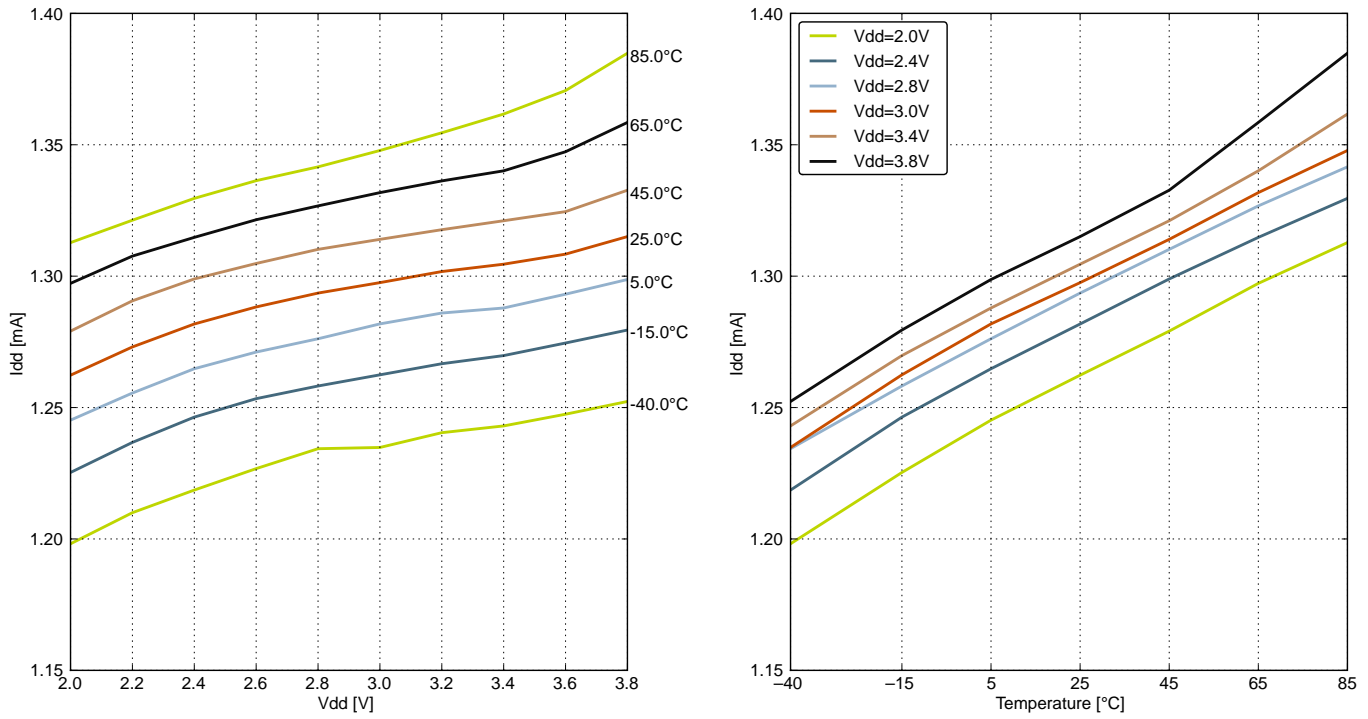


Figure 4.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28 MHz

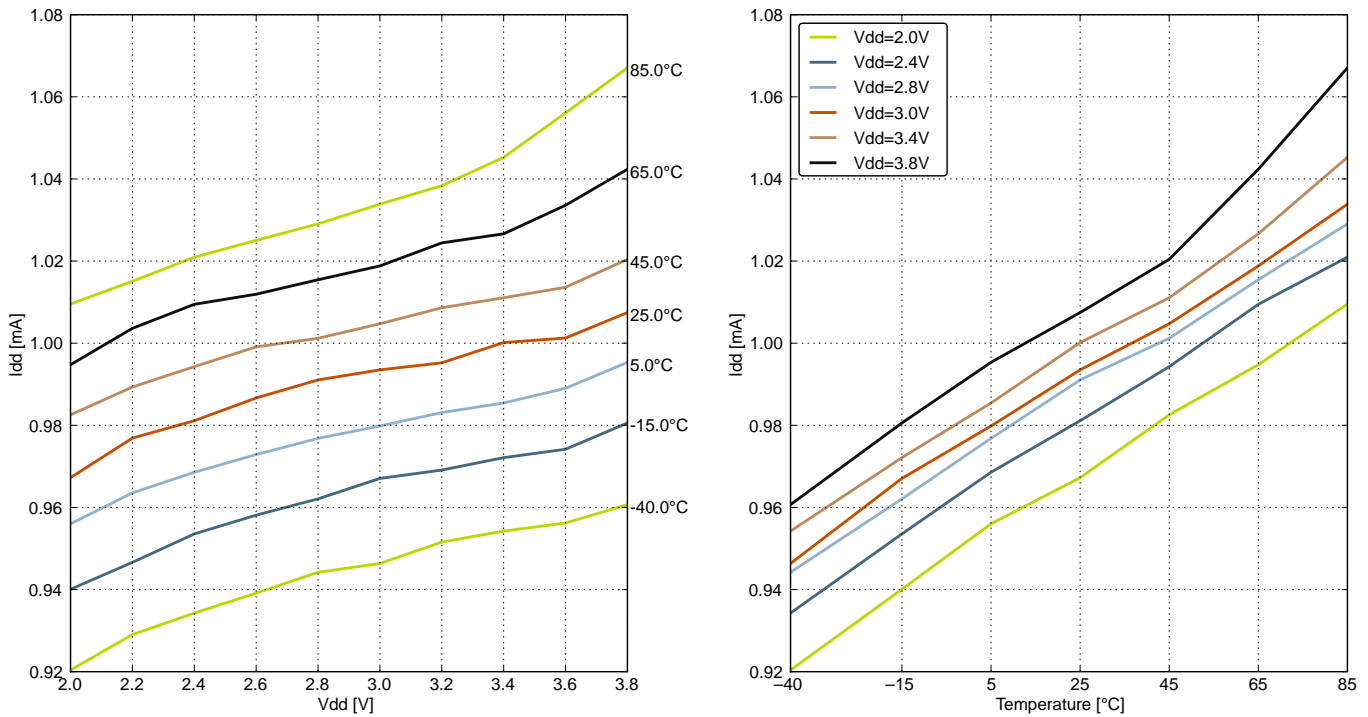


Figure 4.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz

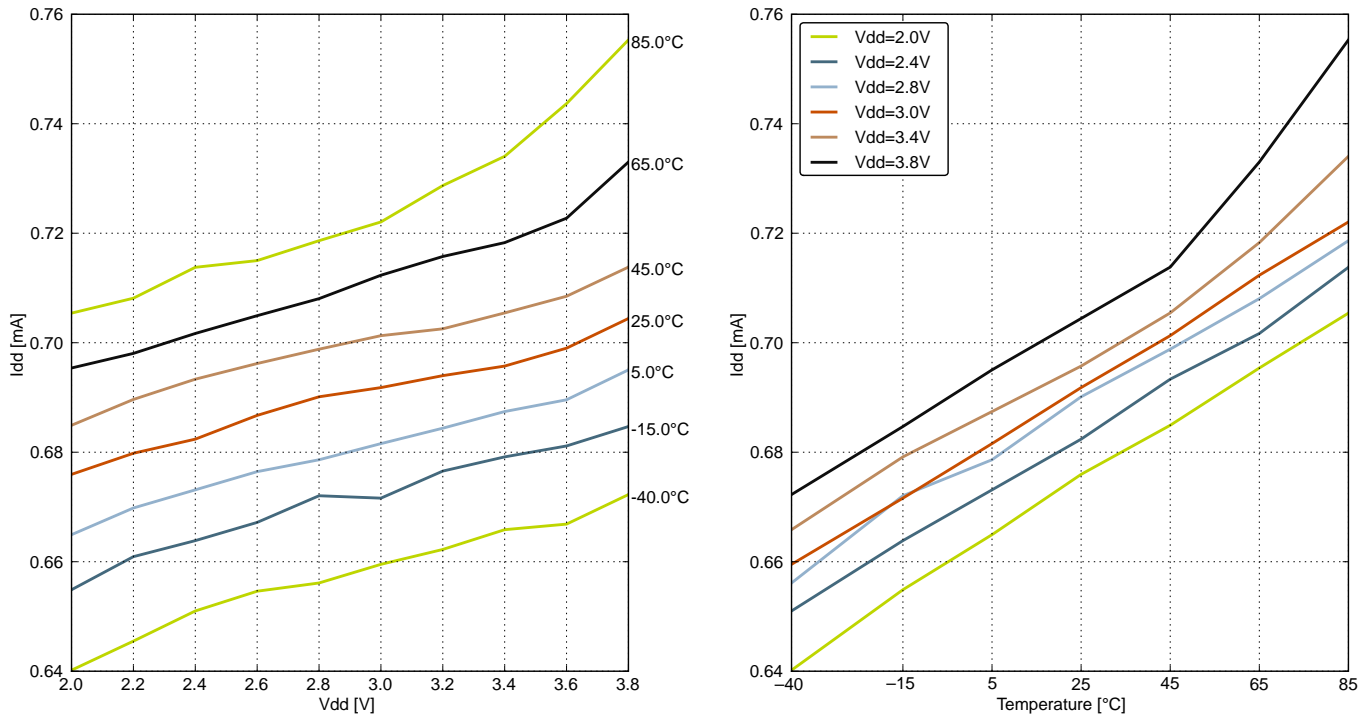


Figure 4.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz

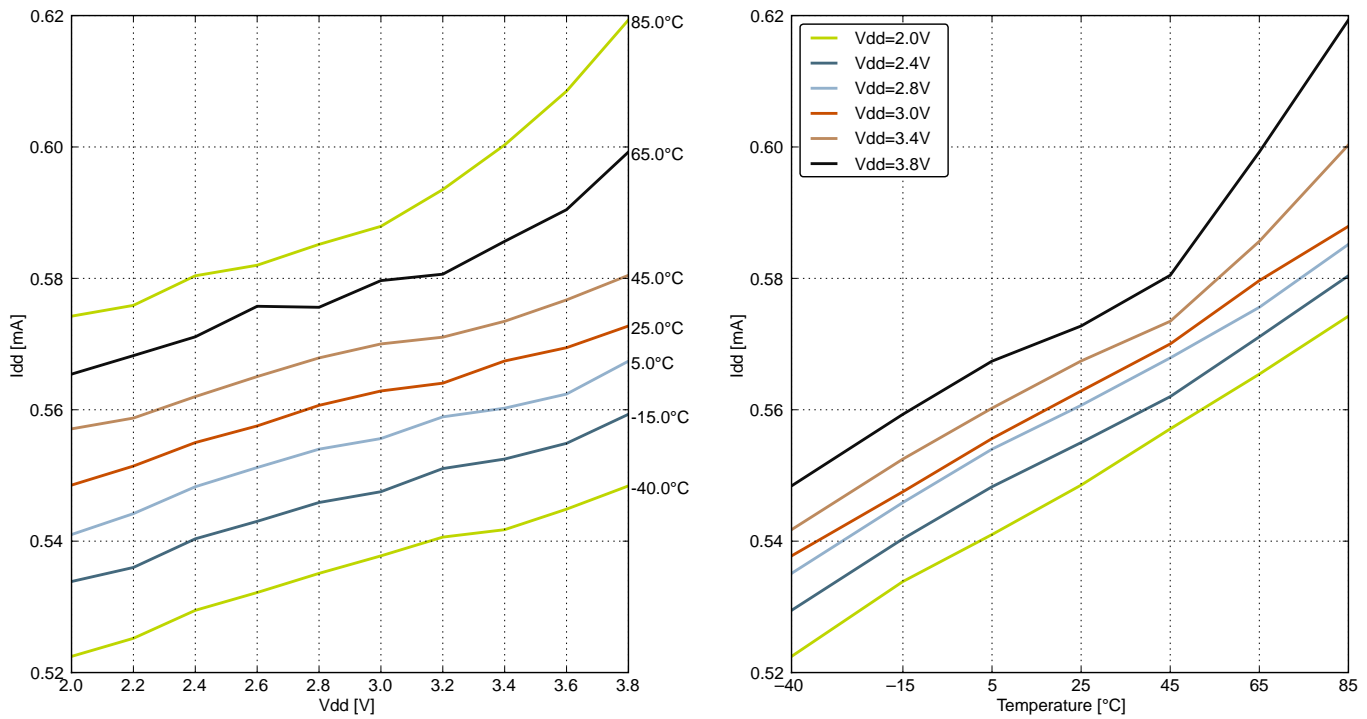


Figure 4.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

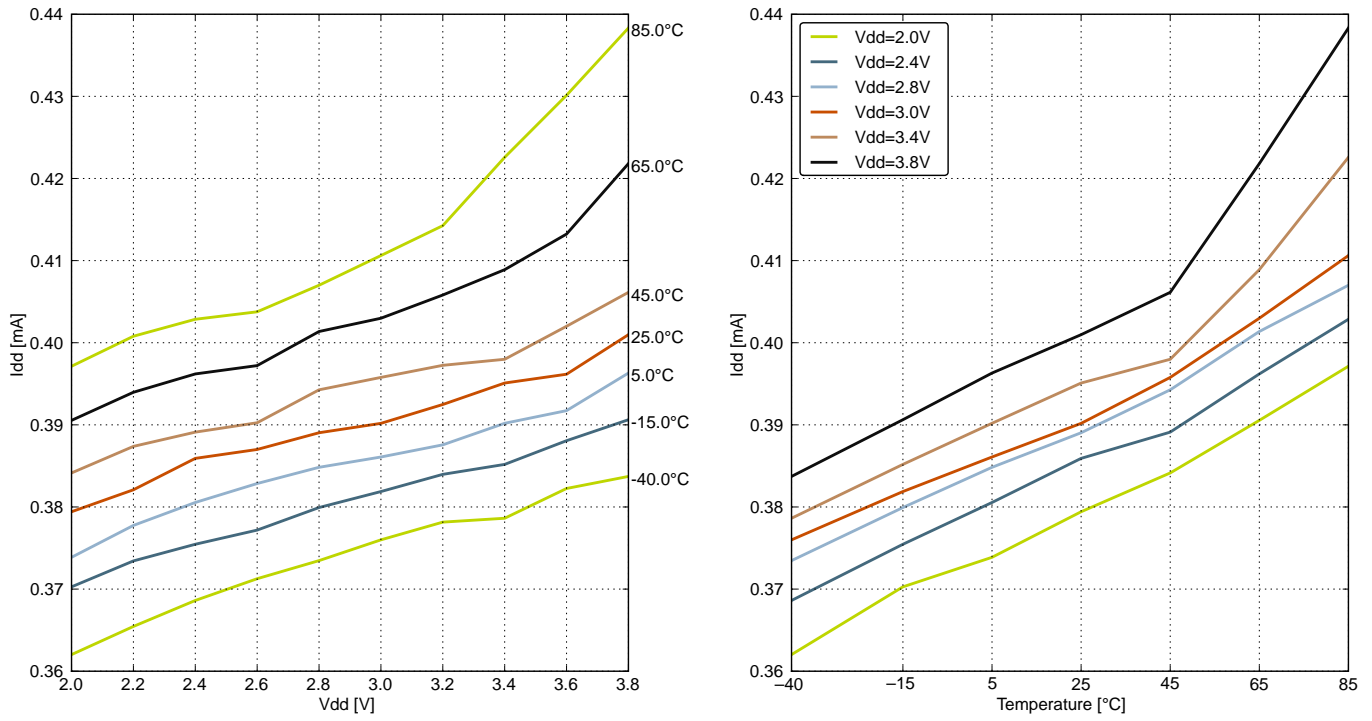


Figure 4.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 7 MHz

4.4.3 EM2 Current Consumption

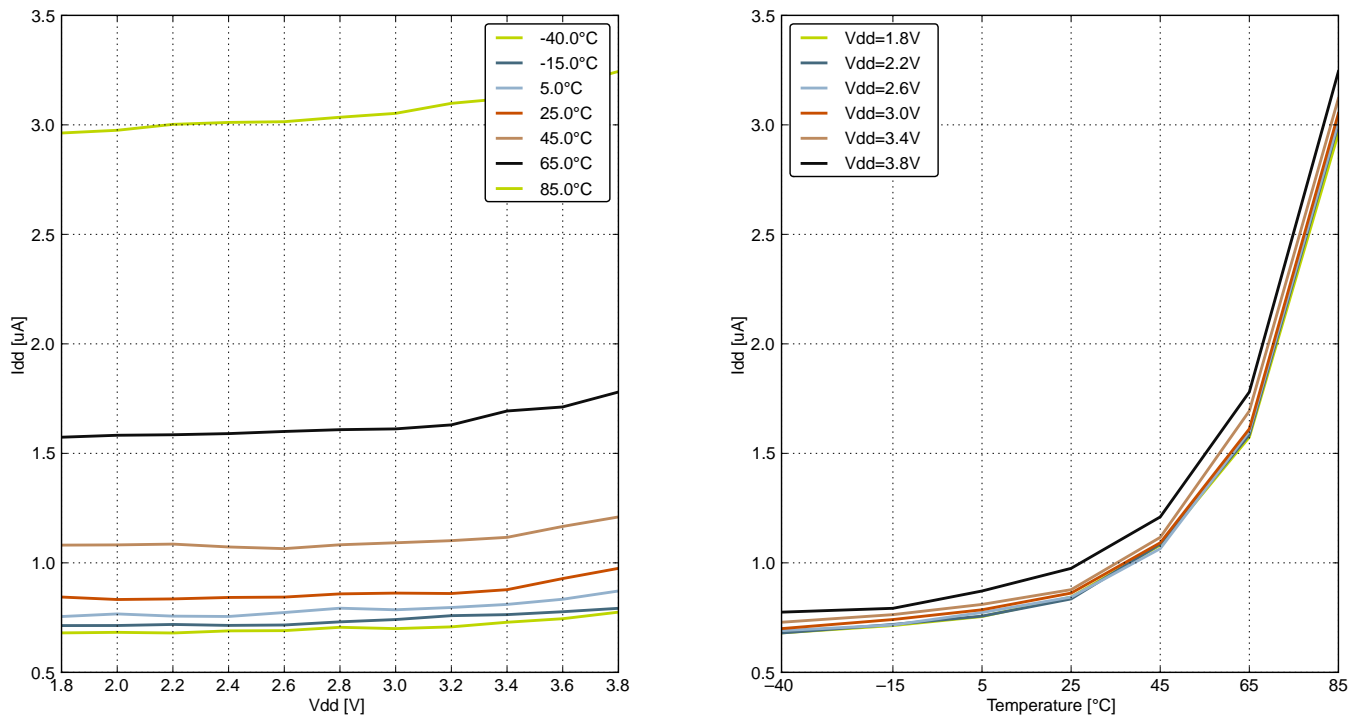


Figure 4.11. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO

4.4.4 EM3 Current Consumption

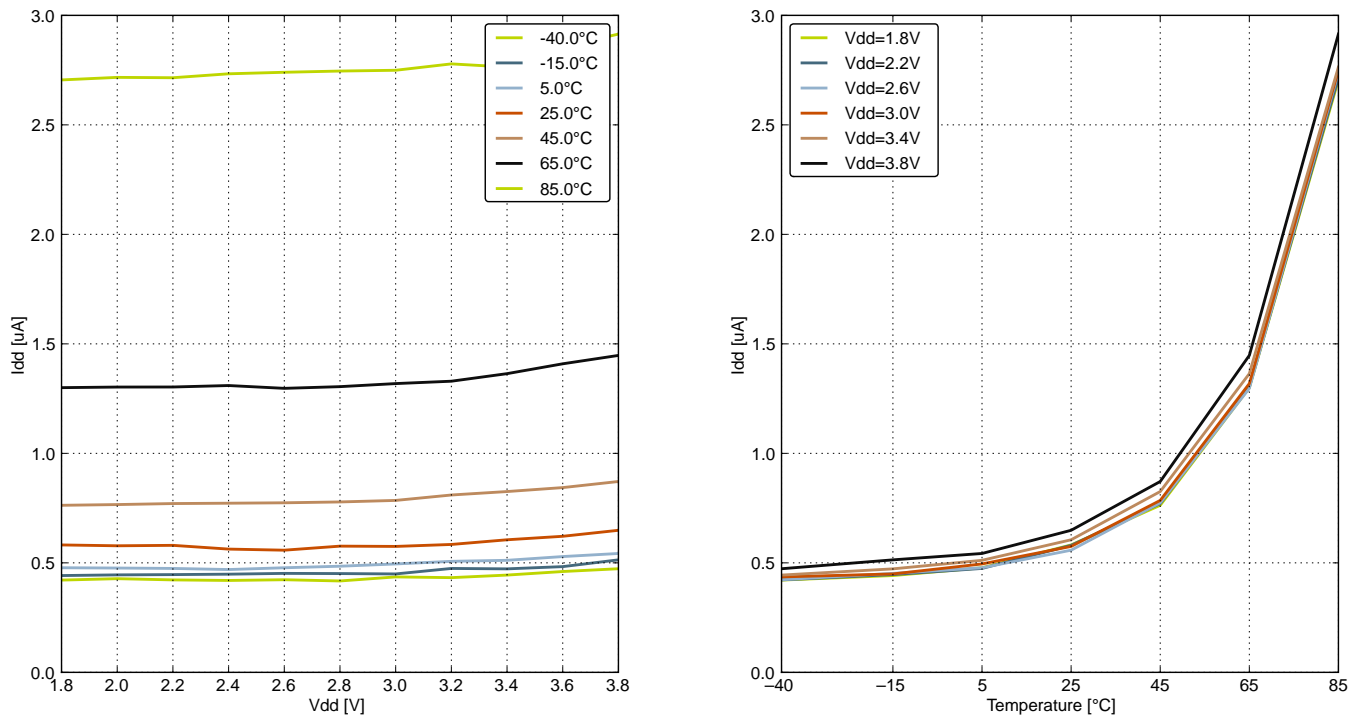


Figure 4.12. EM3 Current Consumption

4.4.5 EM4 Current Consumption

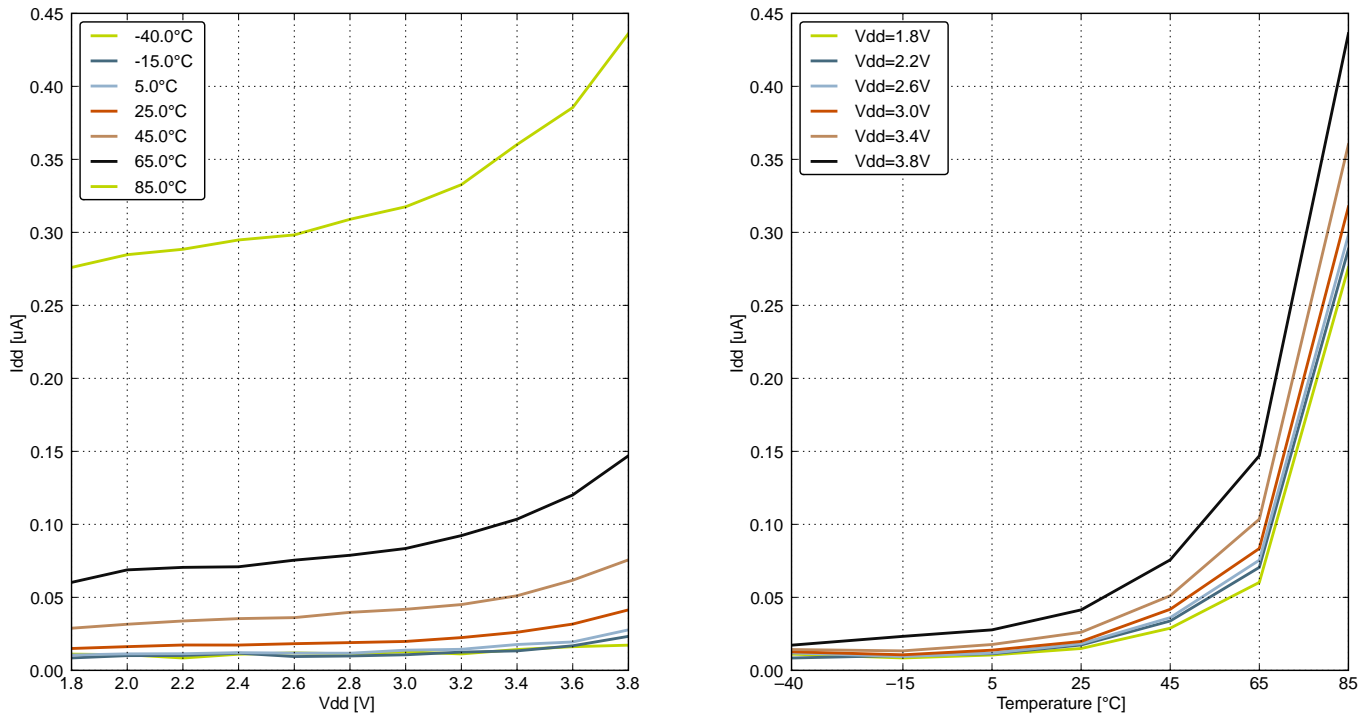


Figure 4.13. EM4 Current Consumption

4.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.4. Energy Modes Transitions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------|------------|-----|-----|-----|------------------|
| Transition time from EM1 to EM0 | t_{EM10} | — | 0 | — | HFCORECLK cycles |
| Transition time from EM2 to EM0 | t_{EM20} | — | 2 | — | μs |
| Transition time from EM3 to EM0 | t_{EM30} | — | 2 | — | μs |
| Transition time from EM4 to EM0 | t_{EM40} | — | 163 | — | μs |

4.6 Power Management

The EFM32G requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 4.5. Power Management

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------|--|------|------|------|---------|
| BOD threshold on falling external supply voltage | $V_{BODextthr-}$ | EM0 | 1.74 | — | 1.96 | V |
| | | EM1 | 1.74 | — | 1.96 | V |
| | | EM2 | 1.74 | — | 1.96 | V |
| BOD threshold on rising external supply voltage | $V_{BODextthr+}$ | EM0 | — | 1.85 | — | V |
| Power-on Reset (POR) threshold on rising external supply voltage | $V_{PORthr+}$ | | — | — | 1.98 | V |
| Delay from reset is released until program execution starts | $t_{RESETdy}$ | Applies to Power-on Reset, Brown-out Reset and pin reset. | — | 163 | — | μ s |
| negative pulse length to ensure complete reset of device | t_{RESET} | | 50 | — | — | ns |
| Voltage regulator decoupling capacitor. | $C_{DECOUPLE}$ | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | — | 1 | — | μ F |

4.7 Flash

Table 4.6. Flash

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|--------------------------|-------|------|----------------|--------|
| Flash erase cycles before failure | EC _{FLASH} | | 20000 | — | — | cycles |
| Flash word write cycles between erase | WWC _{FLASH} | | — | — | 2 ¹ | cycles |
| Flash data retention | RET _{FLASH} | T _{AMB} <150 °C | 10000 | — | — | h |
| | | T _{AMB} <85 °C | 10 | — | — | years |
| | | T _{AMB} <70 °C | 20 | — | — | years |
| Word (32-bit) programming time | t _{W_PROG} | | 20 | — | — | µs |
| Page erase time ² | t _{P_ERASE} | | 20.7 | 22.0 | 24.8 | ms |
| Device erase time ³ | t _{D_ERASE} | | 41.8 | 45.0 | 49.2 | ms |
| Erase current | I _{ERASE} | | — | — | 7 ⁴ | mA |
| Write current | I _{WRITE} | | — | — | 7 ⁴ | mA |
| Supply voltage during flash erase and write | V _{FLASH} | | 1.98 | — | 3.8 | V |

Note:

1. There is a maximum of two writes to the same word between each erase due to a physical limitation of the flash. No bit should be written to '0' more than once between erases. To write a word twice between erases, any bit written to '0' by the first write should be written to '1' by the second write. This preserves the specified flash write/erase endurance and does not change the '0' written by the first write.
2. From setting ERASEPAGE bit in MSC_WRITECMD to 1 to reading 1 in ERASE bit in MSC_IF. Internal setup and hold times for flash control signals are included.
3. From setting DEVICEERASE bit in AAP_CMD to 1 to reading 0 in ERASEBUSY bit in AAP_STATUS. Internal setup and hold times for flash control signals are included.
4. Measured at 25 °C.

4.8 General Purpose Input Output

Table 4.7. GPIO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|---|------------------------|----------------------|------------------------|------|
| Input low voltage | V_{IOIL} | | — | — | $0.30 \times V_{DD}^1$ | V |
| Input high voltage | V_{IOIH} | | $0.70 \times V_{DD}^1$ | — | — | V |
| Output high voltage (Production test condition = 3.0 V, DRIVE-MODE = STANDARD) | V_{IOOH} | Sourcing 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | $0.80 \times V_{DD}$ | — | V |
| | | Sourcing 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | $0.90 \times V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.85 \times V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.90 \times V_{DD}$ | — | V |
| | | Sourcing 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.75 \times V_{DD}$ | — | — | V |
| | | Sourcing 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.85 \times V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.60 \times V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.80 \times V_{DD}$ | — | — | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|--|---------------------|----------------------|----------------------|------------|
| Output low voltage (Production test condition = 3.0 V, DRIVE-MODE = STANDARD) | V_{IOOL} | Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | $0.20 \times V_{DD}$ | — | V |
| | | Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST | — | $0.10 \times V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.10 \times V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.05 \times V_{DD}$ | — | V |
| | | Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | $0.30 \times V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | $0.20 \times V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | $0.35 \times V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | $0.25 \times V_{DD}$ | V |
| Input leakage current | I_{IOLEAK} | High Impedance IO connected to GROUND or V_{DD} | — | ± 0.1 | ± 40 | nA |
| I/O pin pull-up resistor | R_{PU} | | — | 40 | — | k Ω |
| I/O pin pull-down resistor | R_{PD} | | — | 40 | — | k Ω |
| Internal ESD series resistor | R_{IOESD} | | — | 200 | — | Ω |
| Pulse width of pulses to be removed by the glitch suppression filter | $t_{IOGLITCH}$ | | 10 | — | 50 | ns |
| Output fall time | t_{IOOF} | GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5-25$ pF. | $20+0.1C_L$ | — | 250 | ns |
| | | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600$ pF | $20+0.1C_L$ | — | 250 | ns |
| I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-}) | V_{IOHYST} | $V_{DD} = 1.98 - 3.8$ V | $0.1 \times V_{DD}$ | — | — | V |
| Note: | | | | | | |
| 1. If the GPIO input voltage is between $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$, the current consumption will increase. | | | | | | |

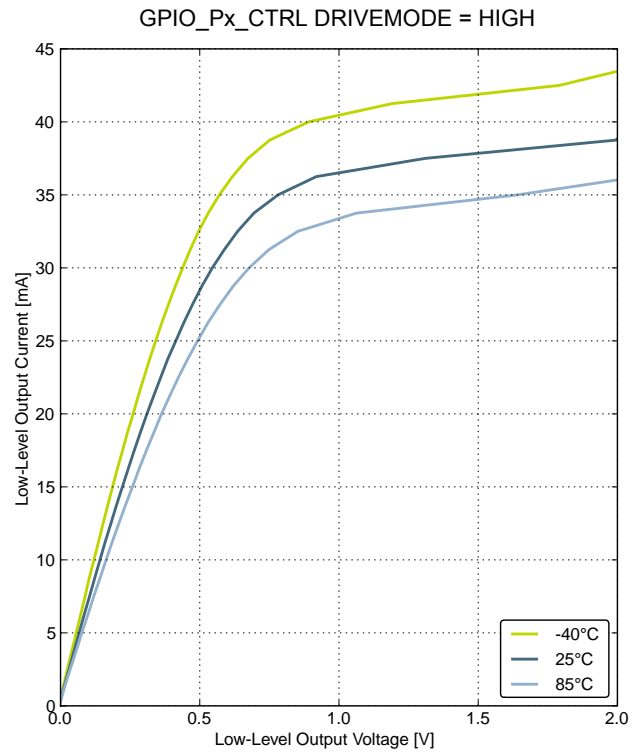
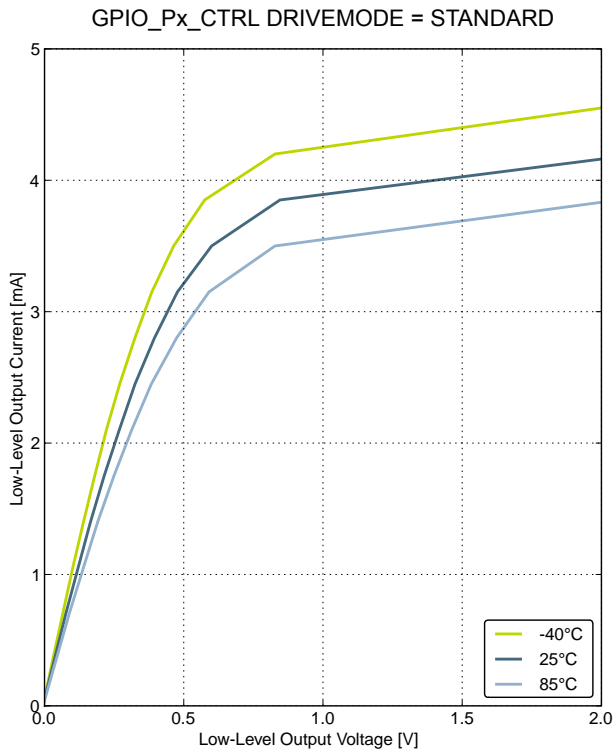
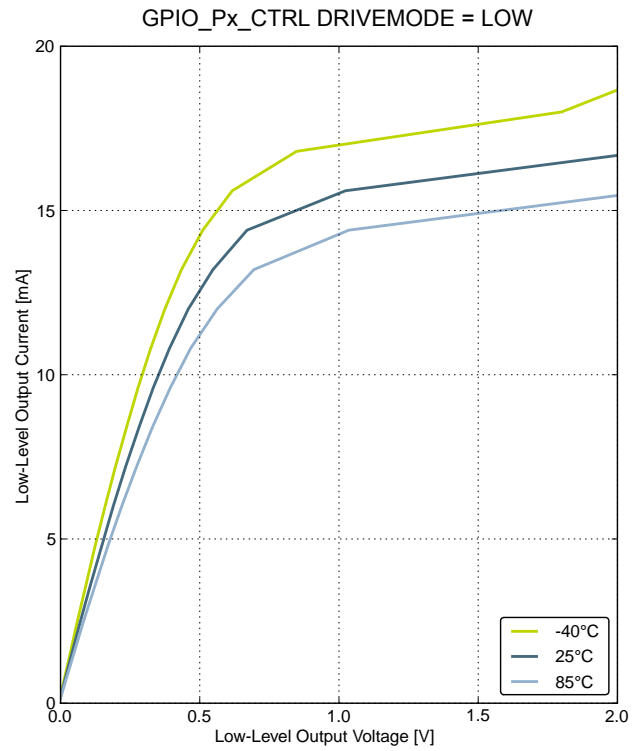
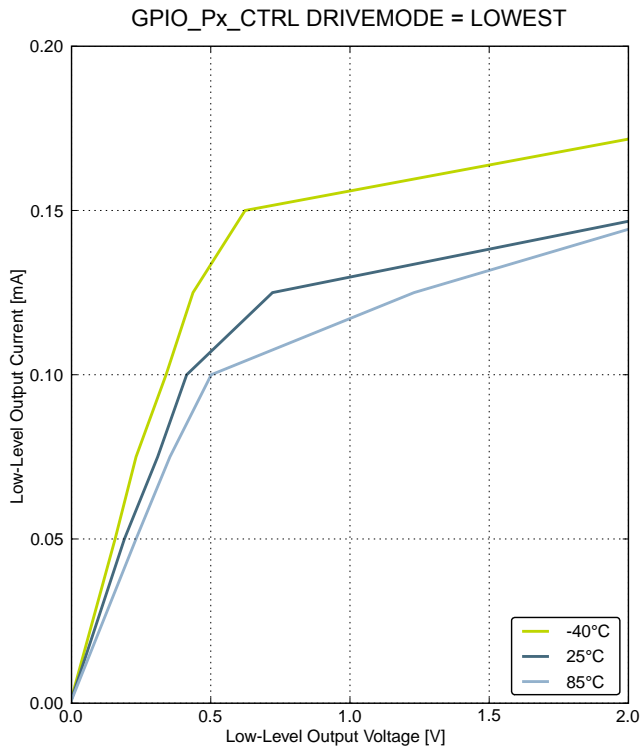


Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage

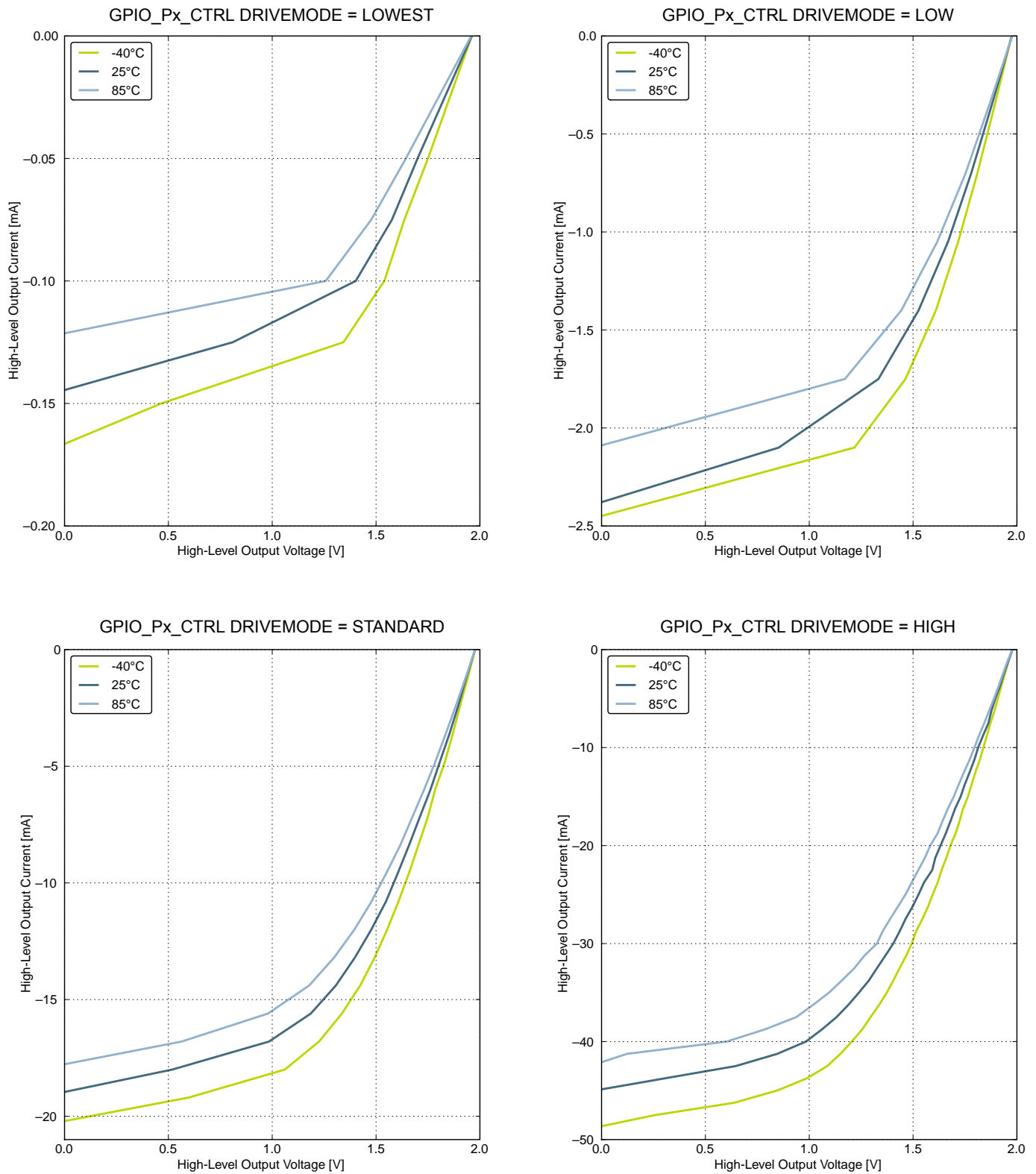


Figure 4.15. Typical High-Level Output Current, 2V Supply Voltage

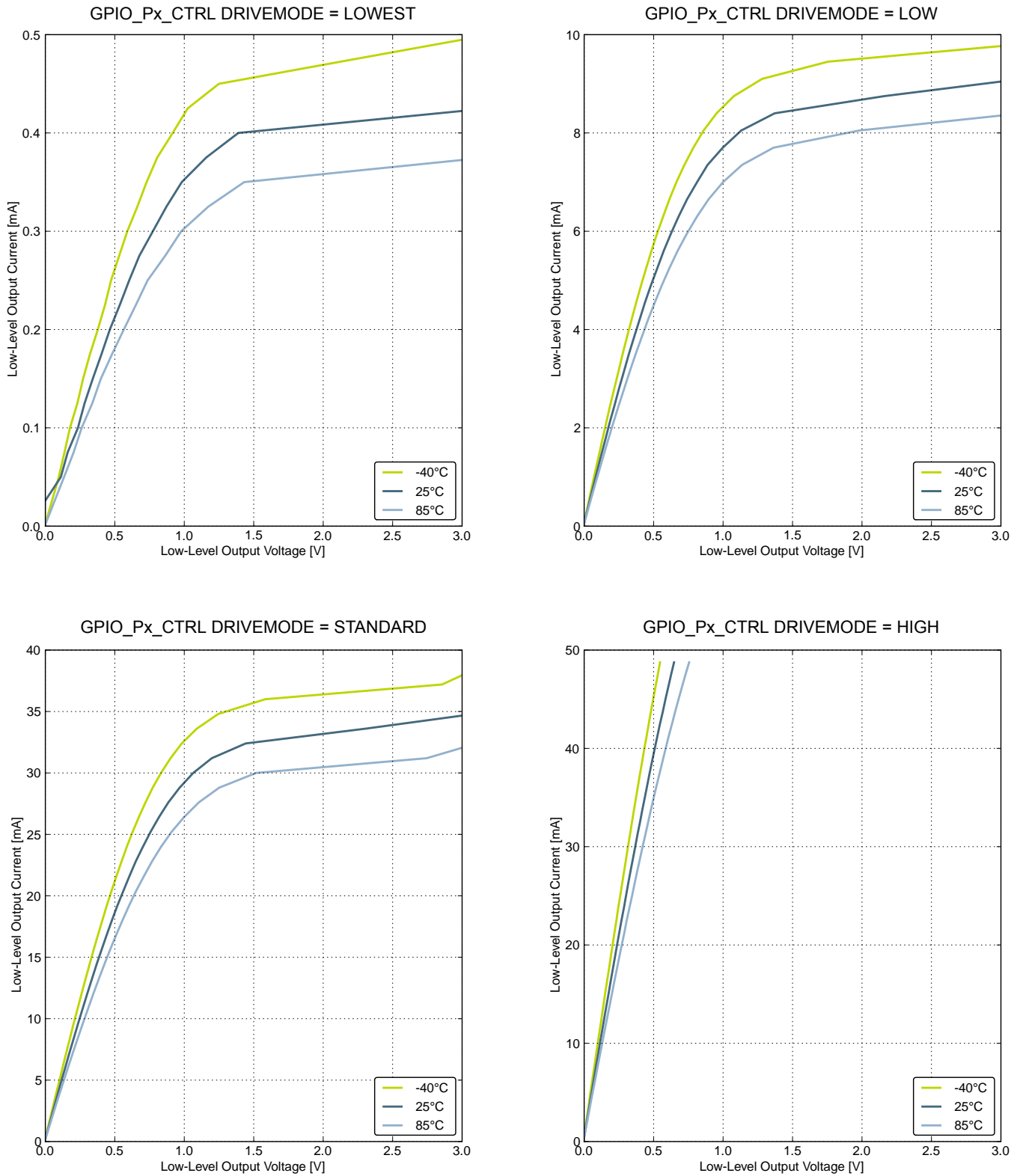


Figure 4.16. Typical Low-Level Output Current, 3V Supply Voltage

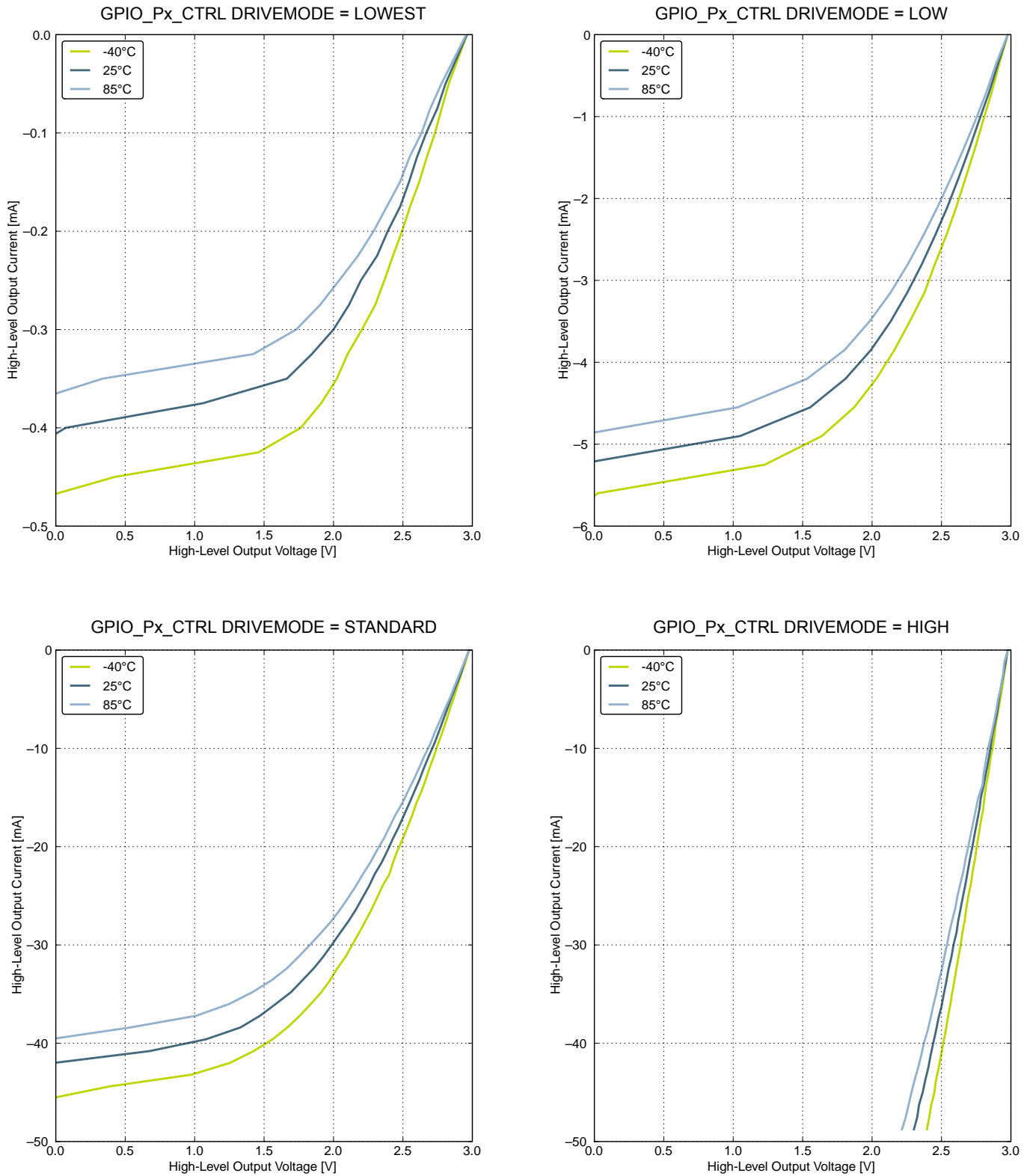


Figure 4.17. Typical High-Level Output Current, 3V Supply Voltage

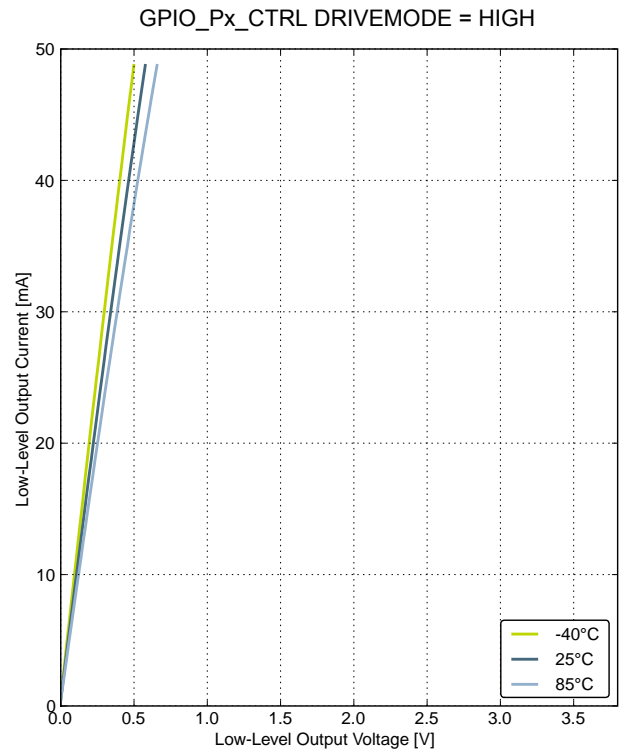
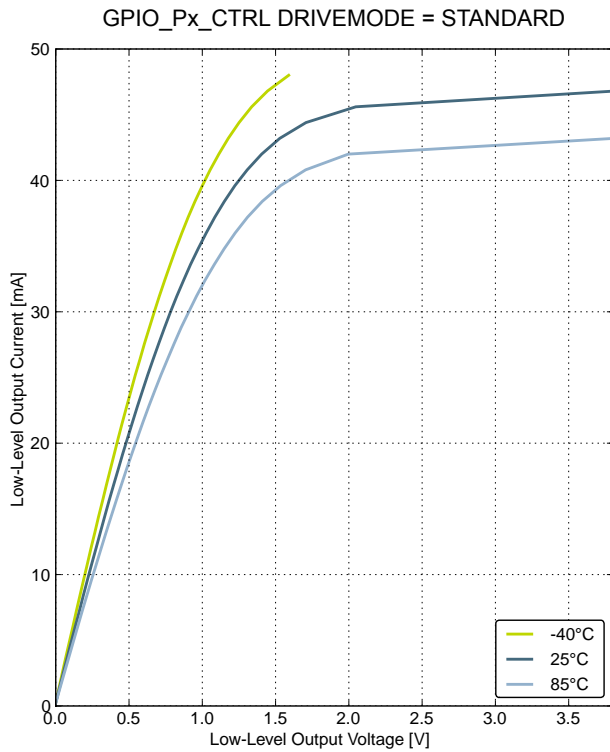
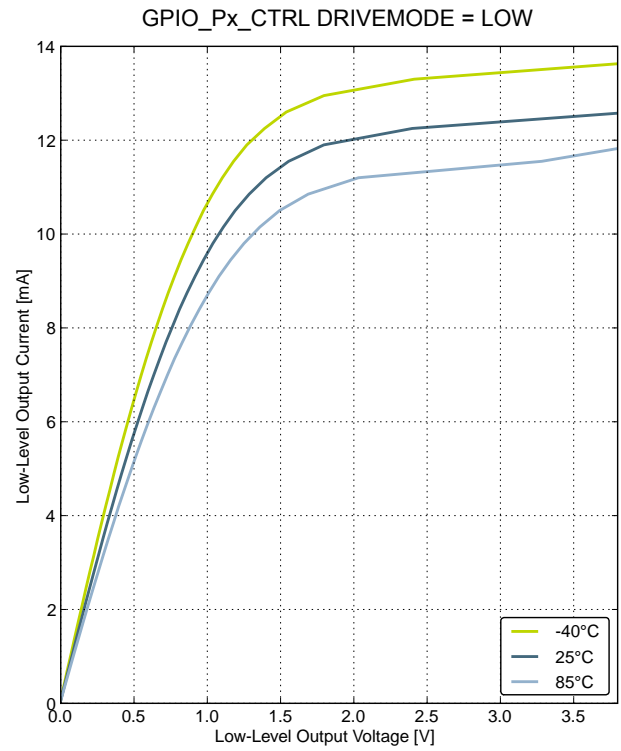
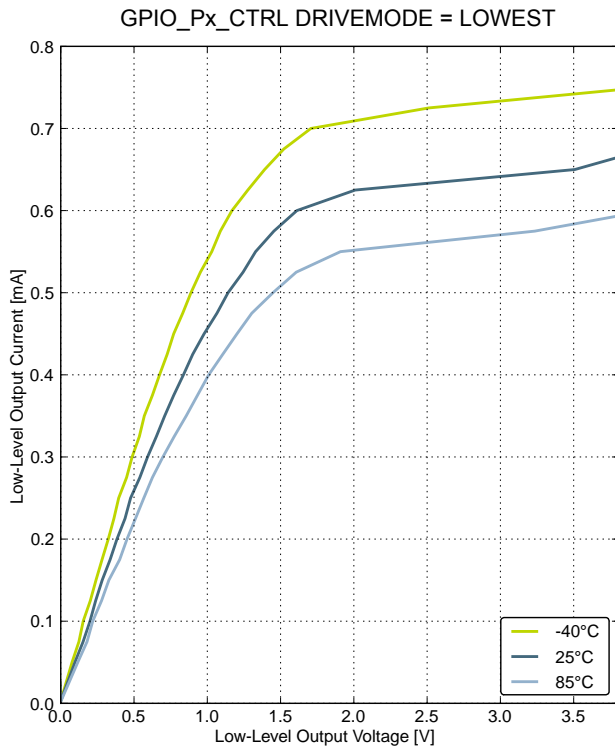


Figure 4.18. Typical Low-Level Output Current, 3.8V Supply Voltage

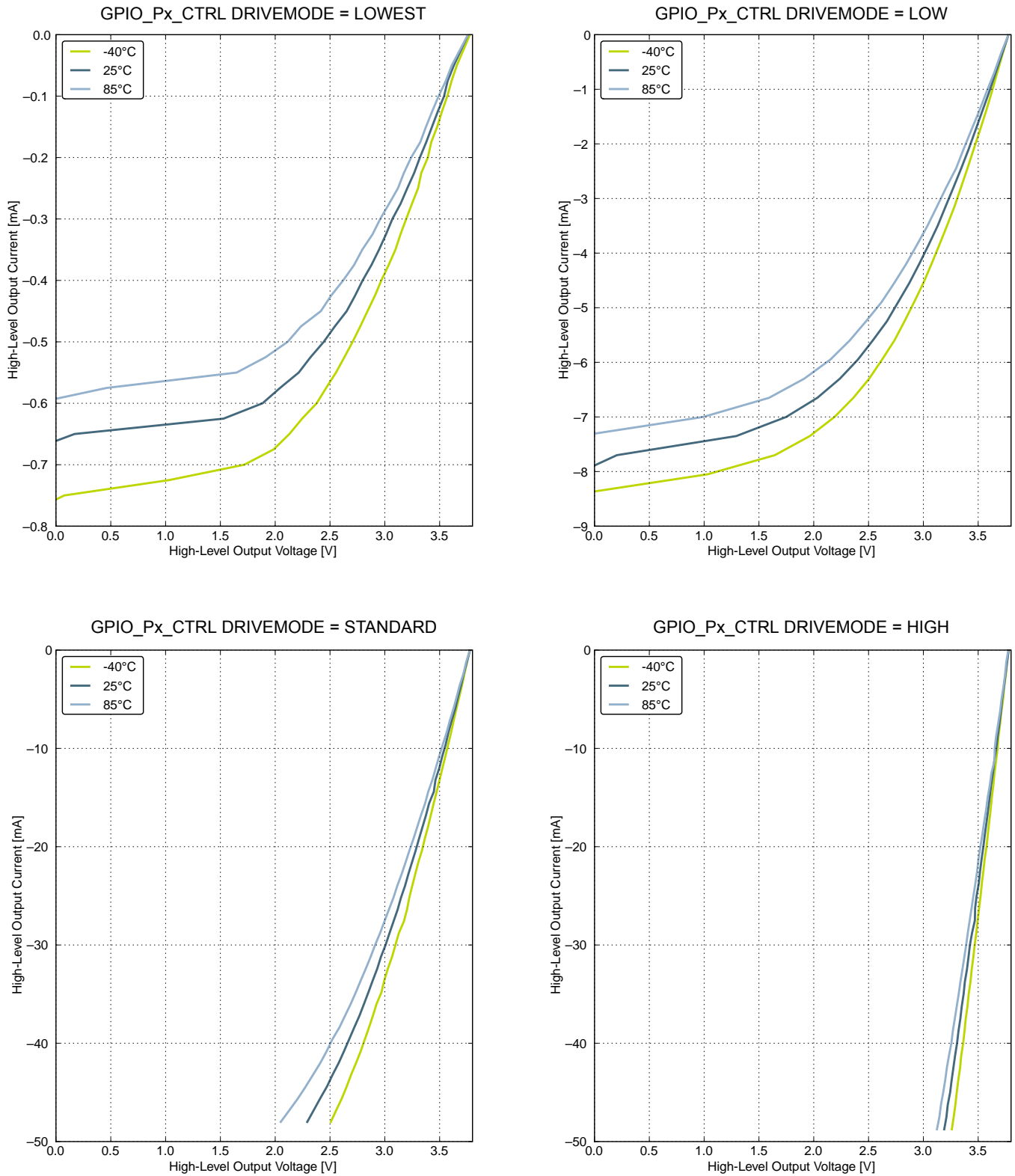


Figure 4.19. Typical High-Level Output Current, 3.8V Supply Voltage

4.9 Oscillators

4.9.1 LFXO

Table 4.8. LFXO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------|---|----------------|--------|-----|------|
| Supported nominal crystal frequency | f_{LFXO} | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{LFXO} | | — | 30 | 120 | kOhm |
| Supported crystal external load range | C_{LFXOL} | | X ¹ | — | 25 | pF |
| Current consumption for core and buffer after startup | I_{LFXO} | ESR=30 kΩ, C _L =10 pF, LFXO-BOOST in CMU_CTRL is 1 | — | 190 | — | nA |
| Start-up time | t_{LFXO} | ESR=30 kΩ, C _L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1 | — | 400 | — | ms |

Note:

1. See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in Configurator in Simplicity Studio.

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

4.9.2 HFXO

Table 4.9. HFXO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|-----|------|---------------|
| Supported nominal crystal Frequency | f_{HFXO} | | 4 | — | 32 | MHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{HFXO} | Crystal frequency 32 MHz | — | 30 | 60 | Ω |
| | | Crystal frequency 4 MHz | — | 400 | 1500 | Ω |
| The transconductance of the HFXO input transistor at crystal startup | g_{mHFXO} | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | — | — | mS |
| Supported crystal external load range | C_{HFXOL} | | 5 | — | 25 | pF |
| Current consumption for HFXO after startup | I_{HFXO} | 4 MHz: ESR=400 Ω , C_L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 85 | — | μA |
| | | 32 MHz: ESR=30 Ω , C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 165 | — | μA |
| Startup time | t_{HFXO} | 32 MHz: ESR=30 Ω , C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 400 | — | μs |
| Pulse width removed by glitch detector | | | 1 | — | 4 | ns |

4.9.3 LFRCO

Table 4.10. LFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|----------------|-------|------------|-------|-----------------------|
| Oscillation frequency, $V_{DD}=3.0$ V, $T_{AMB}=25^{\circ}\text{C}$ | f_{LFRCO} | | 31.29 | 32.768 | 34.24 | kHz |
| Startup time not including software calibration | t_{LFRCO} | | — | 150 | — | μs |
| Current consumption | I_{LFRCO} | | — | 190 | — | nA |
| Temperature coefficient | TC_{LFRCO} | | — | ± 0.02 | — | $\%/^{\circ}\text{C}$ |
| Supply voltage coefficient | VC_{LFRCO} | | — | ± 15 | — | $\%/V$ |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{LFRCO}$ | | — | 1.5 | — | % |

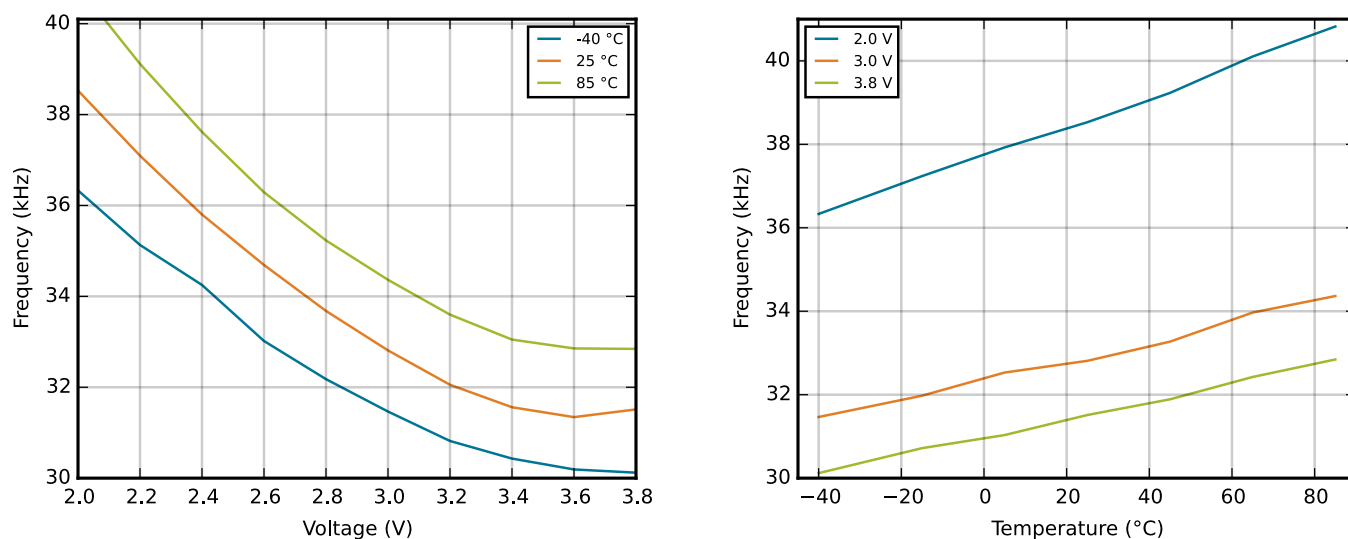


Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

4.9.4 HFRCO

Table 4.11. HFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------|--------------------------------------|-------|------------------|-------|--------|
| Oscillation frequency, $V_{DD}= 3.0$ V, $T_{AMB}=25$ °C | f_{HFRCO} | 28 MHz frequency band | 27.16 | 28 | 28.84 | MHz |
| | | 21 MHz frequency band | 20.37 | 21 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.402 | 6.6 ¹ | 6.798 | MHz |
| | | 1 MHz frequency band | 1.164 | 1.2 ² | 1.236 | MHz |
| Settling time | $t_{HFRCO_settling}$ | After start-up, $f_{HFRCO} = 14$ MHz | — | 0.6 | — | Cycles |
| | | After band switch | — | 25 | — | Cycles |
| Current consumption (Production test condition = 14 MHz) | I_{HFRCO} | $f_{HFRCO} = 28$ MHz | — | 158 | 190 | μA |
| | | $f_{HFRCO} = 21$ MHz | — | 125 | 155 | μA |
| | | $f_{HFRCO} = 14$ MHz | — | 99 | 120 | μA |
| | | $f_{HFRCO} = 11$ MHz | — | 88 | 110 | μA |
| | | $f_{HFRCO} = 6.6$ MHz | — | 72 | 90 | μA |
| | | $f_{HFRCO} = 1.2$ MHz | — | 24 | 32 | μA |
| Duty cycle | DC_{HFRCO} | $f_{HFRCO} = 14$ MHz | 48.5 | 50 | 51 | % |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{HFRCO}$ | | — | 0.3 ³ | — | % |

Note:

1. For devices with prod. rev. < 19, Typ = 7 MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1 MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

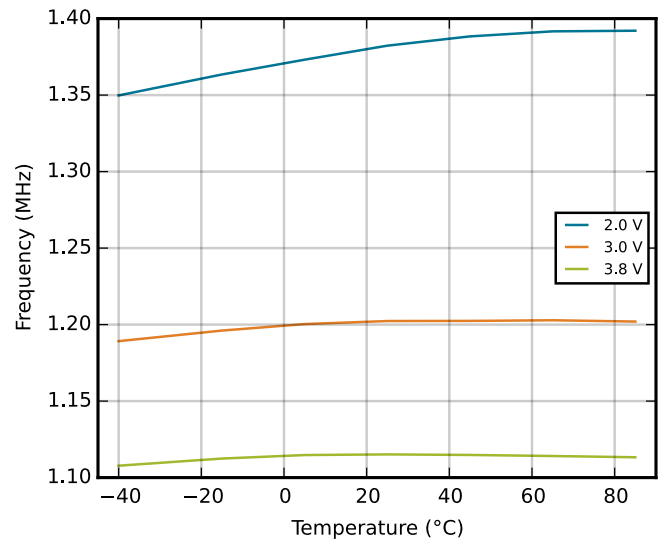
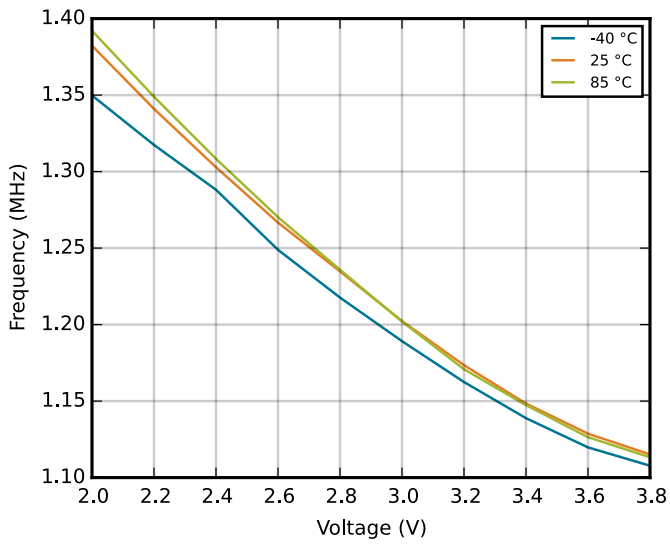


Figure 4.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

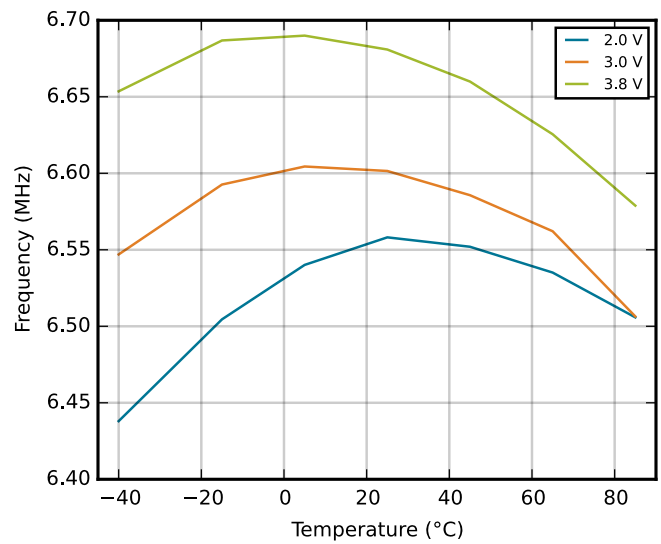
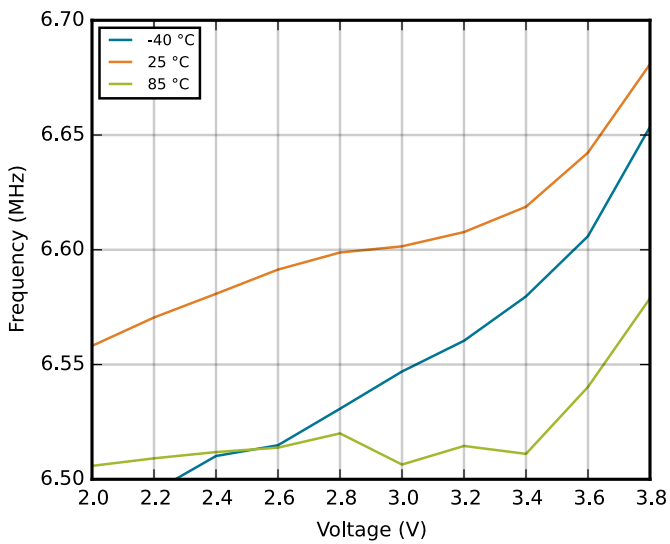


Figure 4.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

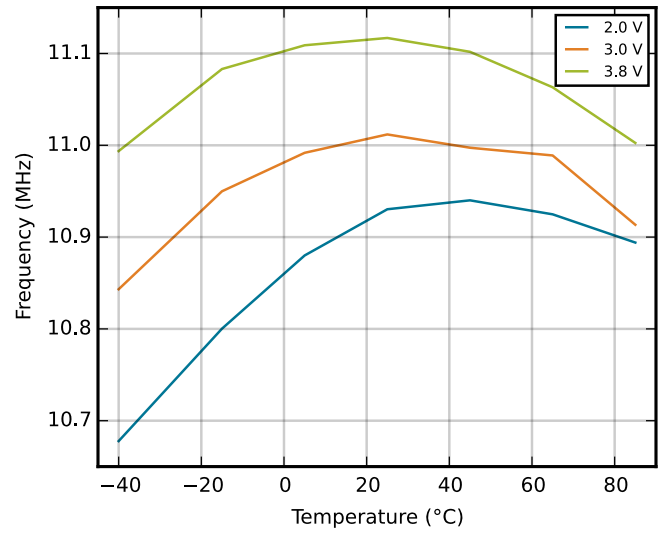
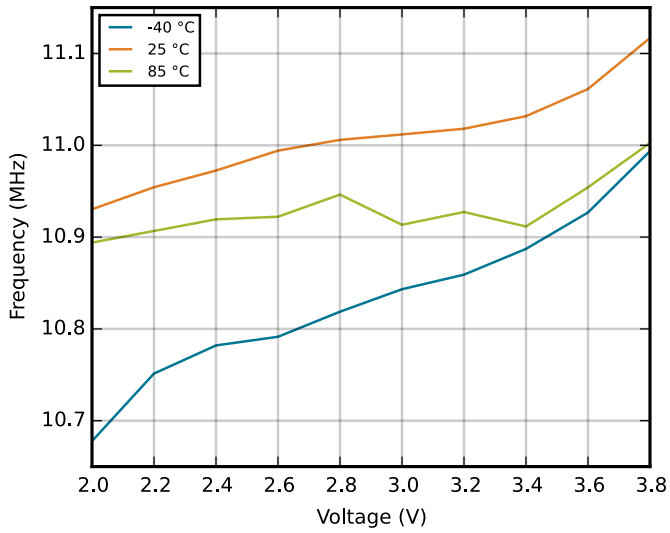


Figure 4.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

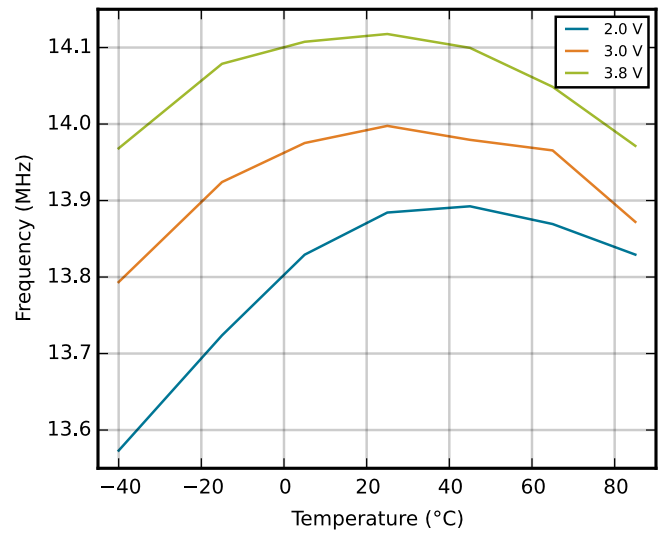
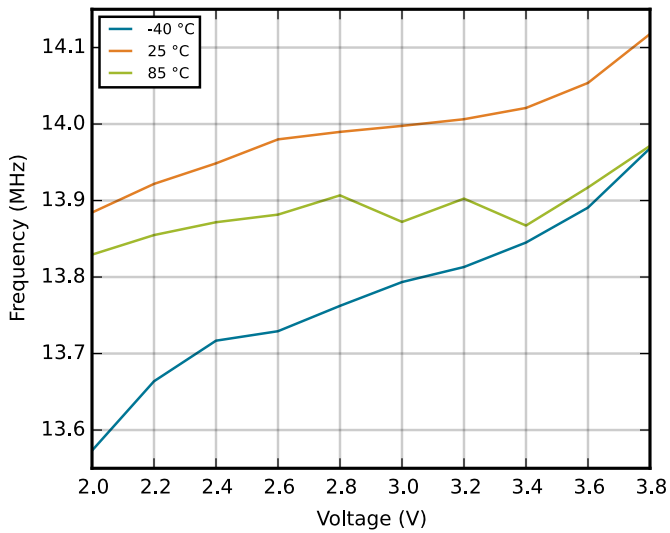


Figure 4.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

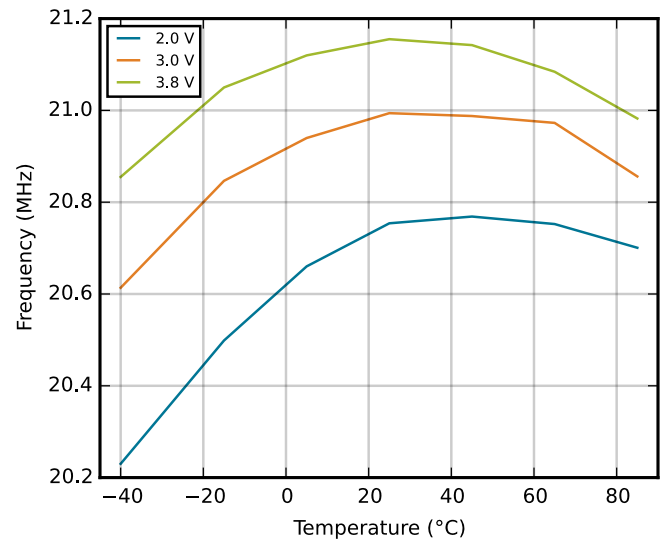
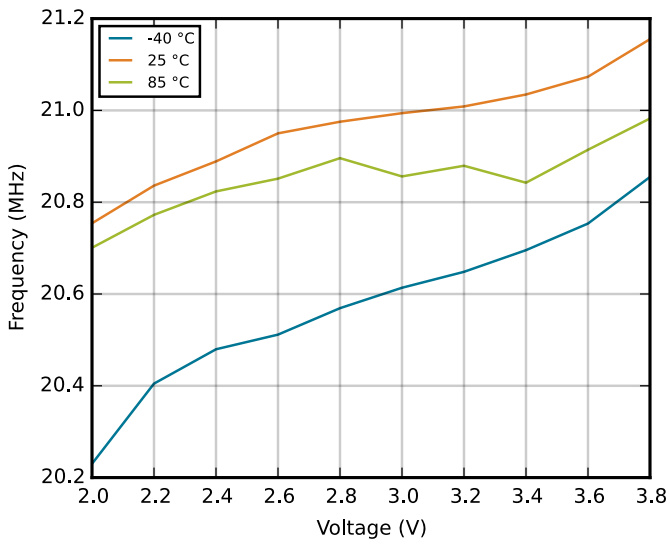


Figure 4.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

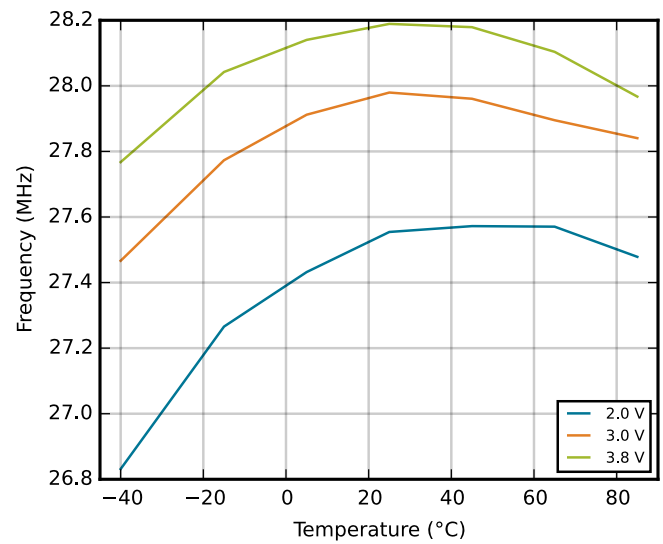
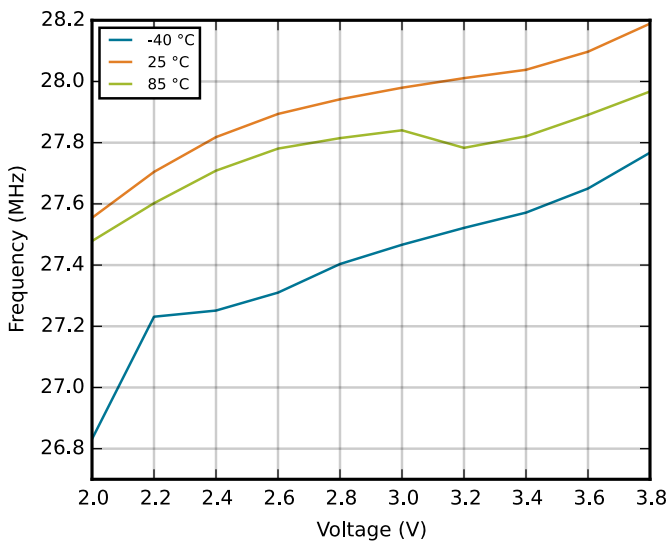


Figure 4.26. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature

4.9.5 AUXHFRCO

Table 4.12. AUXHFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------------|-------------------------|--------|------------------|--------|--------|
| Oscillation frequency, $V_{DD} = 3.0$ V, $T_{AMB} = 25$ °C | $f_{AUXHFRCO}$ | 14 MHz frequency band | 13.580 | 14.0 | 14.420 | MHz |
| Settling time after start-up | $t_{AUXHFRCO_settling}$ | $f_{AUXHFRCO} = 14$ MHz | — | 0.6 | — | Cycles |
| Duty cycle | $DC_{AUXHFRCO}$ | $f_{AUXHFRCO} = 14$ MHz | 48.5 | 50 | 51 | % |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{AUXHFRCO}$ | | — | 0.3 ¹ | — | % |

Note:

1. The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value in the 14 MHz range across operating conditions.

4.9.6 ULFRCO

Table 4.13. ULFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------|---------------|----------------|-----|-------|------|------|
| Oscillation frequency | f_{ULFRCO} | 25 °C, 3 V | 0.7 | — | 1.75 | kHz |
| Temperature coefficient | TC_{ULFRCO} | | — | 0.05 | — | %/°C |
| Supply voltage coefficient | VC_{ULFRCO} | | — | -18.2 | — | %/V |

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|---|--------------|------------------|----------------|------|
| Input voltage range | V_{ADCIN} | Single-ended | 0 | — | V_{REF} | V |
| | | Differential | $-V_{REF}/2$ | — | $V_{REF}/2$ | V |
| Input range of external reference voltage, single-ended and differential | $V_{ADCREFIN}$ | | 1.25 | — | V_{DD} | V |
| Input range of external negative reference voltage on channel 7 | $V_{ADCREFIN_CH7}$ | See $V_{ADCREFIN}$ | 0 | — | $V_{DD} - 1.1$ | V |
| Input range of external positive reference voltage on channel 6 | $V_{ADCREFIN_CH6}$ | See $V_{ADCREFIN}$ | 0.625 | — | V_{DD} | V |
| Common mode input range | $V_{ADCCMIN}$ | | 0 | — | V_{DD} | V |
| Input current | I_{ADCIN} | 2 pF sampling capacitors | — | <100 | — | nA |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | | — | 65 | — | dB |
| Average active current | I_{ADC} | 1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 735 ¹ | — | μA |
| | | 1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 760 ¹ | — | μA |
| | | 500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 346 ¹ | — | μA |
| | | 500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 354 ¹ | — | μA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 52 ¹ | — | μA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 50 ¹ | — | μA |
| | | 10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 54 ¹ | — | μA |
| Input capacitance | C_{ADCIN} | | — | 2 | — | pF |
| Input ON resistance | R_{ADCIN} | | 300 | — | 800 | Ω |
| Input RC filter resistance | $R_{ADCFILT}$ | | — | 10 | — | kΩ |
| Input RC filter/decoupling capacitance | $C_{ADCFILT}$ | | — | 250 | — | fF |
| Input bias current | $I_{ADCBIASIN}$ | $V_{SS} < V_{IN} < V_{DD}$ | -40 | — | 40 | nA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------|------------------|-----|-----|-----|---------------|
| Input offset current | $I_{ADCOFFSETIN}$ | VSS < VIN < VDD | -40 | — | 40 | nA |
| ADC Clock Frequency | f_{ADCCLK} | BIASPROG=0x747 | — | — | 7 | MHz |
| | | BIASPROG=0xF4B | — | — | 13 | MHz |
| Conversion time | $t_{ADCCONV}$ | 6 bit | 7 | — | — | ADCCLK Cycles |
| | | 8 bit | 11 | — | — | ADCCLK Cycles |
| | | 12 bit | 13 | — | — | ADCCLK Cycles |
| Acquisition time | t_{ADCACQ} | Programmable | 1 | — | 256 | ADCCLK Cycles |
| Required acquisition time for VDD/3 reference | $t_{ADCACQVDD3}$ | | 2 | — | — | μ s |
| Startup time of reference generator and ADC core | $t_{ADCSTART}$ | NORMAL mode | — | 5 | — | μ s |
| | | KEEPADCWARM mode | — | 1 | — | μ s |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------|--------------------|---|-----|-----|-----|------|
| Signal-to-Noise Ratio (SNR) | SNR _{ADC} | 1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 59 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 67 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | 63 | 69 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 70 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 62 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 67 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------|--------------------|--|-----|-----|-----|------|
| Signal-to-Noise Ratio (SNR) | SNR _{ADC} | 200 kSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | 63 | 69 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 70 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|---|-----|-----|-----|------|
| Signal-to-Noise And Distortion Ratio (SINAD) | SINAD _{ADC} | 1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 58 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 62 | — | dB |
| | | 1 MSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | 62 | 68 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 68 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 61 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 62 | — | dB |
| | | 200 kSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference, ADC_CLK= 7 MHz, BIASPROG = 0x747 | — | 66 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|--|-----|-----|-----|------|
| Signal-to-Noise And Distortion Ratio (SINAD) | SINAD _{ADC} | 200 kSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | 62 | 68 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 69 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------------------|---------------------|---|-----|-----|-----|------|
| Spurious-Free Dynamic Range (SFDR) | SFDR _{ADC} | 1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 75 | — | dBc |
| | | 1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 78 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 77 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | 68 | 79 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single-ended, V _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 76 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 78 | — | dBc |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|--|-------|-------------------|--------------------|--------------|
| Spurious-Free Dynamic Range (SFDR) | SFDR _{ADC} | 200 kSamples/s, 12 bit, differential, V _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | 68 | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2xV _{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | — | 79 | — | dBc |
| Offset voltage | V _{ADCOFFSET} | After calibration, single-ended | — | 0.3 | — | mV |
| | | After calibration, differential | -4 | 0.3 | 4 | mV |
| Thermometer output gradient | TGRAD _{ADCTH} | | — | -1.92 | — | mV/°C |
| | | | — | -6.3 | — | ADC Codes/°C |
| Differential non-linearity (DNL) | DNL _{ADC} | V _{DD} = 3.0 V, external 2.5 V reference | -1 | ±0.7 | 4 | LSB |
| Integral non-linearity (INL), End point method | INL _{ADC} | V _{DD} = 3.0 V, external 2.5 V reference | — | ±1.2 | ±3 | LSB |
| Missing codes | MC _{ADC} | V _{DD} = 3.0 V, external 2.5 V reference | — | — | 3 | LSB |
| Gain error drift | GAIN _{ED} | 1.25 V reference | — | 0.01 ² | 0.033 ³ | %/°C |
| | | 2.5 V reference | — | 0.01 ² | 0.03 ³ | %/°C |
| Offset error drift | OFFSET _{ED} | 1.25 V reference | — | 0.00 ² | 0.06 ³ | LSB/°C |
| | | 2.5 V reference | — | 0.00 ² | 0.04 ³ | LSB/°C |
| VREF voltage | V _{REF} | 1.25 V reference | 1.2 | 1.25 | 1.3 | V |
| | | 2.5 V reference | 2.4 | 2.5 | 2.6 | V |
| VREF voltage drift | V _{REF_VDRIFT} | 1.25 V reference | -12.4 | 2.9 | 18.2 | mV/V |
| | | 2.5 V reference, V _{DD} > 2.5 V | -24.6 | 5.7 | 35.2 | mV/V |
| VREF temperature drift | V _{REF_TDRIFT} | 1.25 V reference | -132 | 272 | 677 | µV/°C |
| | | 2.5 V reference | -231 | 545 | 1271 | µV/°C |
| VREF current consumption | I _{VREF} | 1.25 V reference | — | 67 | 114 | µA |
| | | 2.5 V reference | — | 55 | 82 | µA |
| ADC and DAC VREF matching | V _{REF_MATCH} | 1.25 V reference | — | 99.85 | — | % |
| | | 2.5 V reference | — | 100.01 | — | % |

Note:

1. Includes required contribution from the voltage reference.
2. Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.
3. Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following figures.

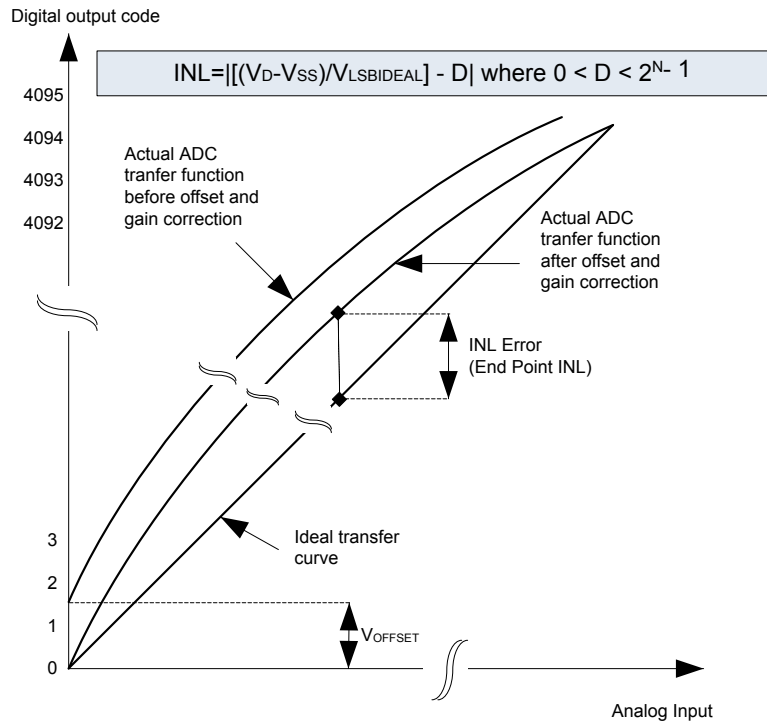


Figure 4.27. Integral Non-Linearity (INL)

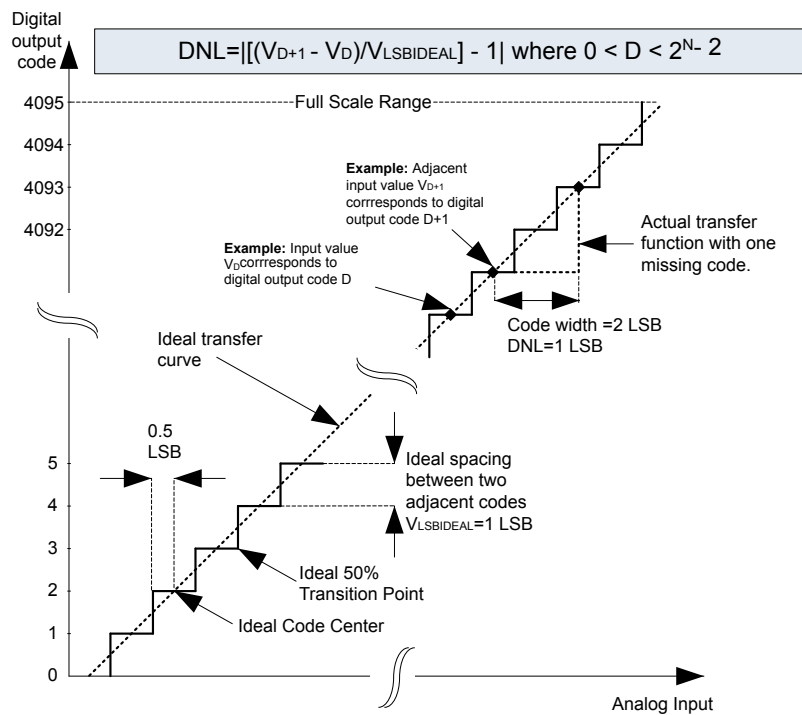


Figure 4.28. Differential Non-Linearity (DNL)

4.10.1 Typical Performance

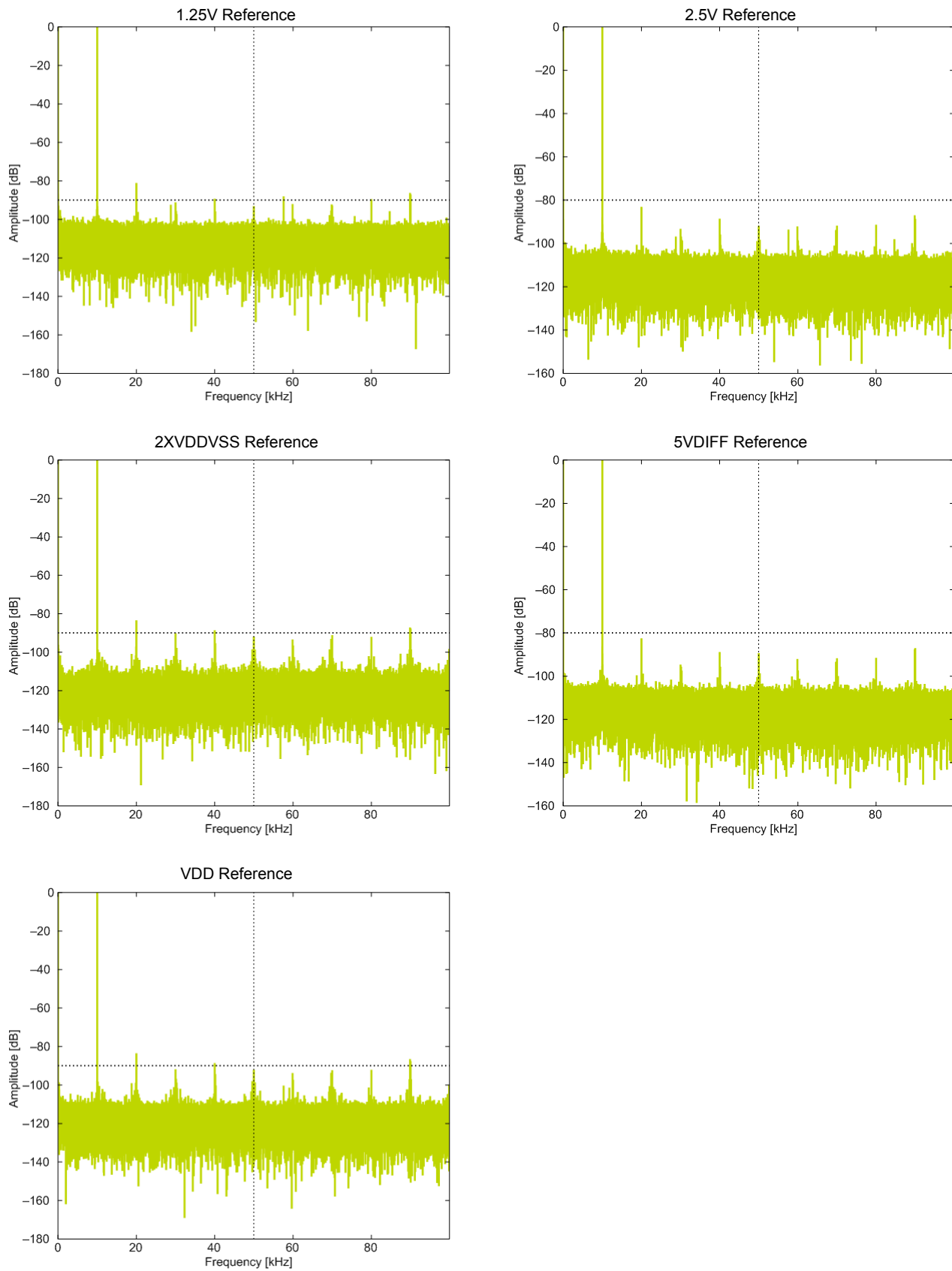


Figure 4.29. ADC Frequency Spectrum, VDD = 3V, Temp = 25°C



Figure 4.30. ADC Integral Linearity Error vs Code, VDD = 3V, Temp = 25°C



Figure 4.31. ADC Differential Linearity Error vs Code, VDD = 3V, Temp = 25°C

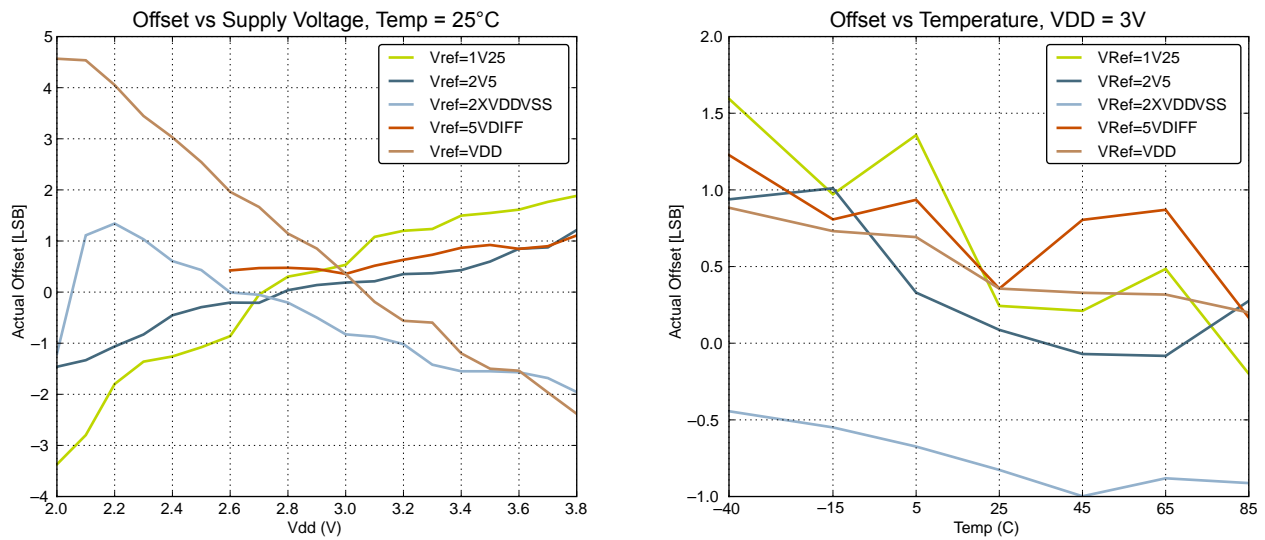


Figure 4.32. ADC Absolute Offset, Common Mode = VDD/2

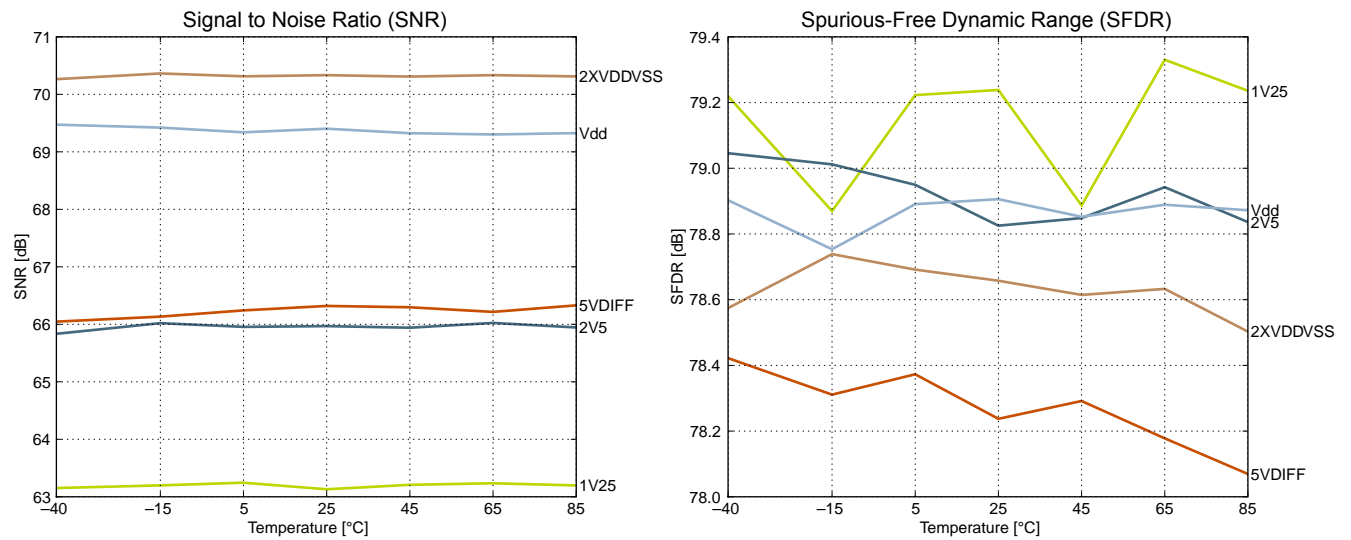


Figure 4.33. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3V

4.11 Digital Analog Converter (DAC)

Table 4.15. DAC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|-----------------|---|-----------|------------------|------------------|------------|
| Output voltage range | V_{DACOUT} | VDD voltage reference, single-ended | 0 | — | V_{DD} | V |
| | | VDD voltage reference, differential | $-V_{DD}$ | — | V_{DD} | V |
| Output common mode voltage range | V_{DACCM} | | 0 | — | V_{DD} | V |
| Average active current | I_{DAC} | 500 kSamples/s, 12 bit, internal 1.25 V reference, Continuous Mode | — | 400 ¹ | 650 ¹ | μ A |
| | | 100 kSamples/s, 12 bit, internal 1.25 V reference, Sample/Hold Mode | — | 200 ¹ | 250 ¹ | μ A |
| | | 1 kSamples/s 12 bit, internal 1.25 V reference, Sample/Off Mode | — | 17 ¹ | 25 ¹ | μ A |
| Sample rate | SR_{DAC} | | — | — | 500 | ksamples/s |
| DAC clock frequency | f_{DAC} | Continuous Mode | — | — | 1000 | kHz |
| | | Sample/Hold Mode | — | — | 250 | kHz |
| | | Sample/Off Mode | — | — | 250 | kHz |
| Clock cycles per conversion | $CYC_{DACCONV}$ | | — | 2 | — | cycles |
| Conversion time | $t_{DACCONV}$ | | 2 | — | — | μ s |
| Settling time | $t_{DACSETTLE}$ | | — | 5 | — | μ s |
| Signal-to-Noise Ratio (SNR) | SNR_{DAC} | 500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference | — | 59 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25 V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5 V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, V_{DD} reference | — | 59 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------------|---|-------|--------|------|-------|
| Signal-to-Noise plus Distortion Ratio (SNDR) | SNDR _{DAC} | 500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference | — | 57 | — | dB |
| | | 500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference | — | 54 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25 V reference | — | 56 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5 V reference | — | 53 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, V _{DD} reference | — | 55 | — | dB |
| Spurious-Free Dynamic Range (SFDR) | SFDR _{DAC} | 500 kSamples/s, 12 bit, single-ended, internal 1.25V reference | — | 62 | — | dBc |
| | | 500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference | — | 56 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25 V reference | — | 61 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5 V reference | — | 55 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, V _{DD} reference | — | 60 | — | dBc |
| Offset voltage | V _{DACOFFSET} | After calibration, single-ended | — | 2 | — | mV |
| | | After calibration, differential | — | 2 | — | mV |
| Sample-hold mode voltage drift | V _{DACSHMDRIFT} | | — | 540 | — | μV/ms |
| Differential non-linearity | DNL _{DAC} | | — | ±1 | — | LSB |
| Integral non-linearity | INL _{DAC} | | — | ±5 | — | LSB |
| No missing codes | MC _{DAC} | | — | 12 | — | bits |
| Load current | I _{LOAD_DC} | | — | — | 11 | mA |
| VREF voltage | V _{REF} | 1.25 V reference | 1.2 | 1.25 | 1.3 | V |
| | | 2.5 V reference | 2.4 | 2.5 | 2.6 | V |
| VREF voltage drift | V _{REF_VDRIFT} | 1.25 V reference | -12.4 | 2.9 | 18.2 | mV/V |
| | | 2.5 V reference, V _{DD} > 2.5 V | -24.6 | 5.7 | 35.2 | mV/V |
| VREF temperature drift | V _{REF_TDRIFT} | 1.25 V reference | -132 | 272 | 677 | μV/°C |
| | | 2.5 V reference | -231 | 545 | 1271 | μV/°C |
| VREF current consumption | I _{VREF} | 1.25 V reference | — | 67 | 114 | μA |
| | | 2.5 V reference | — | 55 | 82 | μA |
| ADC and DAC VREF matching | V _{REF_MATCH} | 1.25 V reference | — | 99.85 | — | % |
| | | 2.5 V reference | — | 100.01 | — | % |

Note:

1. Measured with a static input code and no loading on the output. Includes required contribution from the voltage reference.

4.12 Analog Comparator (ACMP)

Table 4.16. ACMP

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------|---|-----|-------|----------|------------|
| Input voltage range | V_{ACMPIN} | | 0 | — | V_{DD} | V |
| ACMP Common Mode voltage range | V_{ACMPCM} | | 0 | — | V_{DD} | V |
| Active current | I_{ACMP} | BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register | — | 55 | 600 | nA |
| | | BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | — | 2.82 | 12 | μ A |
| | | BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register | — | 250 | 520 | μ A |
| Current consumption of internal voltage reference | $I_{ACMPREF}$ | Internal voltage reference off. Using external voltage reference | — | 0 | 0.5 | μ A |
| | | Internal voltage reference, LPREF=1 | — | 0.050 | 3 | μ A |
| | | Internal voltage reference, LPREF=0 | — | 6 | — | μ A |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | -12 | 0 | 12 | mV |
| ACMP hysteresis | $V_{ACMPHYST}$ | Programmable | — | 17 | — | mV |
| Capacitive Sense Internal Resistance | R_{CSRES} | CSRESSEL=0b00 in ACMPn_INPUTSEL | — | 39 | — | k Ω |
| | | CSRESSEL=0b01 in ACMPn_INPUTSEL | — | 71 | — | k Ω |
| | | CSRESSEL=0b10 in ACMPn_INPUTSEL | — | 104 | — | k Ω |
| | | CSRESSEL=0b11 in ACMPn_INPUTSEL | — | 136 | — | k Ω |
| Startup time | $t_{ACMPSTART}$ | | — | — | 10 | μ s |

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in the following equation. $I_{ACMPREF}$ is zero if an external voltage reference is used.

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

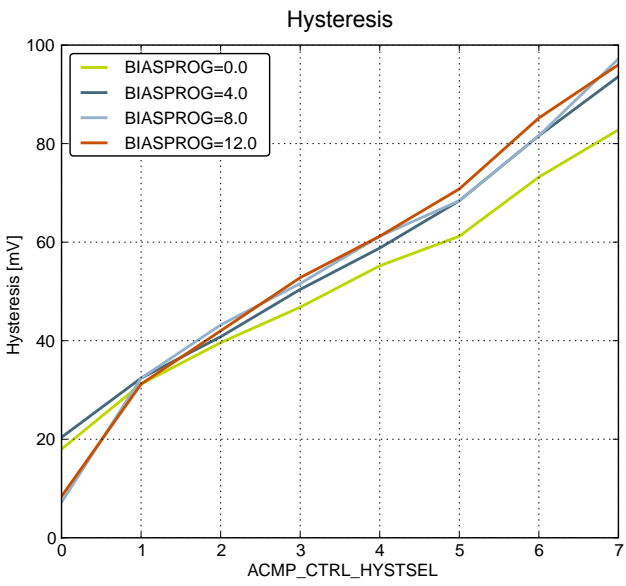
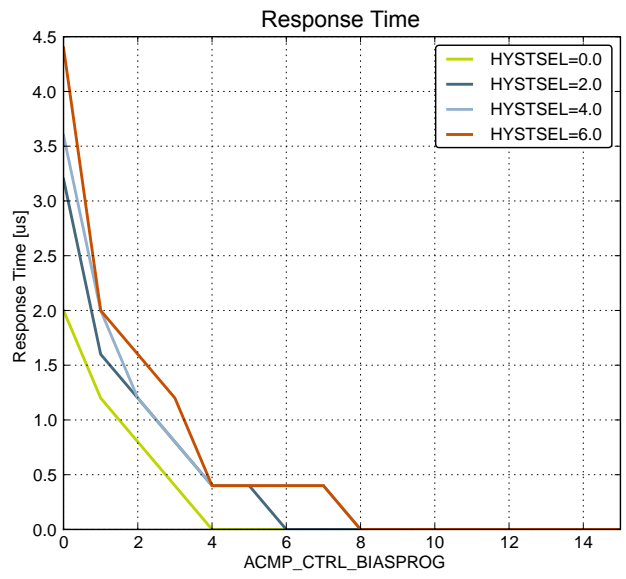
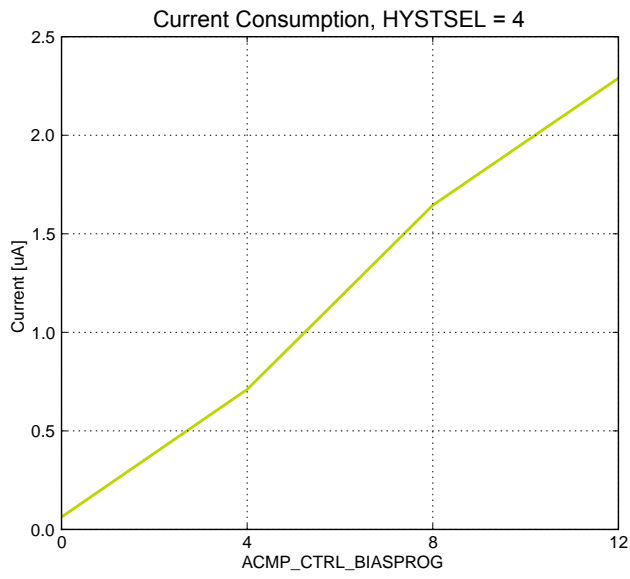


Figure 4.34. ACMP Characteristics, VDD = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1

4.13 Voltage Comparator (VCMP)

Table 4.17. VCMP

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|------------------------------------|--|-----|-----------------|-----|------|
| Input voltage range | V _{VCMPIN} | | — | V _{DD} | — | V |
| VCMP Common Mode voltage range | V _{VCMP_{CM}} | | — | V _{DD} | — | V |
| Active current | I _{VCMP} | BIASPROG=0b0000 and HALF-BIAS=1 in VCMPn_CTRL register | — | 0.3 | 1 | μA |
| | | BIASPROG=0b1111 and HALF-BIAS=0 in VCMPn_CTRL register. LPREF=0. | — | 22 | 30 | μA |
| Startup time reference generator | t _{VCMPREF} | NORMAL | — | 10 | — | μs |
| Offset voltage | V _{VCMP_{OFFSET}} | Single-ended | — | 10 | — | mV |
| | | Differential | — | 10 | — | mV |
| VCMP hysteresis | V _{VCMP_{HYST}} | | — | 40 | — | mV |
| Startup time | t _{VCMP_{START}} | | — | — | 10 | μs |

The V_{DD} Trigger Level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{DD \text{ Trigger Level}} = 1.667V + 0.034 \times \text{TRIGLEVEL}$$

4.14 LCD

Table 4.18. LCD

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|---|-----|------|-----|------|
| Frame rate | f_{LCDFR} | | 30 | — | 200 | Hz |
| Number of segments supported | NUM _{SEG} | | — | 4×40 | — | seg |
| LCD supply voltage range | V_{LCD} | Internal boost circuit enabled | 2.0 | — | 3.8 | V |
| Steady state current consumption. | I_{LCD} | Display disconnected, static mode, framerate 32 Hz, all segments on. | — | 250 | — | nA |
| | | Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONE-THIRD in LCD_DISPCTRL register. | — | 550 | — | nA |
| Steady state Current contribution of internal boost. | $I_{LCDBOOST}$ | Internal voltage boost off | — | 0 | — | μA |
| | | Internal voltage boost on, boosting from 2.2 V to 3.0 V. | — | 8.4 | — | μA |
| Boost Voltage | V_{BOOST} | VBLEV of LCD_DISPCTRL register to LEVEL0 | — | 3.0 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL1 | — | 3.08 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL2 | — | 3.17 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL3 | — | 3.26 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL4 | — | 3.34 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL5 | — | 3.43 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL6 | — | 3.52 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL7 | — | 3.6 | — | V |

The total LCD current is given by the following equation. $I_{LCDBOOST}$ is zero if internal boost is off.

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST}$$

4.15 I2C

Table 4.19. I2C Standard-mode (Sm)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|-----|-----|---------------------|---------|
| SCL clock frequency | f_{SCL} | 0 | — | 100 ¹ | kHz |
| SCL clock low time | t_{LOW} | 4.7 | — | — | μ s |
| SCL clock high time | t_{HIGH} | 4.0 | — | — | μ s |
| SDA set-up time | $t_{SU,DAT}$ | 250 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | 3450 ^{2,3} | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 4.7 | — | — | μ s |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 4.0 | — | — | μ s |
| STOP condition set-up time | $t_{SU,STO}$ | 4.0 | — | — | μ s |
| Bus free time between a STOP and a START condition | t_{BUF} | 4.7 | — | — | μ s |

Note:

1. For the minimum HPPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32G Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((3450 \cdot 10^{-9} [s] \cdot f_{HPPERCLK} [Hz]) - 4)$.

Table 4.20. I2C Fast-mode (Fm)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|-----|-----|--------------------|---------|
| SCL clock frequency | f_{SCL} | 0 | — | 400 ¹ | kHz |
| SCL clock low time | t_{LOW} | 1.3 | — | — | μ s |
| SCL clock high time | t_{HIGH} | 0.6 | — | — | μ s |
| SDA set-up time | $t_{SU,DAT}$ | 100 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | 900 ^{2,3} | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.6 | — | — | μ s |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.6 | — | — | μ s |
| STOP condition set-up time | $t_{SU,STO}$ | 0.6 | — | — | μ s |
| Bus free time between a STOP and a START condition | t_{BUF} | 1.3 | — | — | μ s |

Note:

1. For the minimum HPPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32G Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((900 \cdot 10^{-9} [s] \cdot f_{HPPERCLK} [Hz]) - 4)$.

Table 4.21. I2C Fast-mode Plus (Fm+)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|------|-----|-------------------|---------|
| SCL clock frequency | f_{SCL} | 0 | — | 1000 ¹ | kHz |
| SCL clock low time | t_{LOW} | 0.5 | — | — | μs |
| SCL clock high time | t_{HIGH} | 0.26 | — | — | μs |
| SDA set-up time | $t_{SU,DAT}$ | 50 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | — | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.26 | — | — | μs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.26 | — | — | μs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.26 | — | — | μs |
| Bus free time between a STOP and a START condition | t_{BUF} | 0.5 | — | — | μs |

Note:

1. For the minimum HPPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32G Reference Manual.

4.16 Digital Peripherals

Table 4.22. Digital Peripherals

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------|---------------|-------------------------------------|-----|------|-----|-------------|
| USART current | I_{USART} | USART idle current, clock enabled | — | 7.5 | — | $\mu A/MHz$ |
| UART current | I_{UART} | UART idle current, clock enabled | — | 5.63 | — | $\mu A/MHz$ |
| LEUART current | I_{LEUART} | LEUART idle current, clock enabled | — | 150 | — | nA |
| I2C current | I_{I2C} | I2C idle current, clock enabled | — | 6.25 | — | $\mu A/MHz$ |
| TIMER current | I_{TIMER} | TIMER_0 idle current, clock enabled | — | 8.75 | — | $\mu A/MHz$ |
| LETIMER current | $I_{LETIMER}$ | LETIMER idle current, clock enabled | — | 150 | — | nA |
| PCNT current | I_{PCNT} | PCNT idle current, clock enabled | — | 100 | — | nA |
| RTC current | I_{RTC} | RTC idle current, clock enabled | — | 100 | — | nA |
| LCD current | I_{LCD} | LCD idle current, clock enabled | — | 100 | — | nA |
| AES current | I_{AES} | AES idle current, clock enabled | — | 2.5 | — | $\mu A/MHz$ |
| GPIO current | I_{GPIO} | GPIO idle current, clock enabled | — | 5.31 | — | $\mu A/MHz$ |
| EBI current | I_{EBI} | EBI idle current, clock enabled | — | 1.56 | — | $\mu A/MHz$ |
| PRS current | I_{PRS} | PRS idle current | — | 2.81 | — | $\mu A/MHz$ |
| DMA current | I_{DMA} | Clock enable | — | 8.12 | — | $\mu A/MHz$ |

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32G.

5. Pin Definitions

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32G.

5.1 EFM32G200 & EFM32G210 (QFN32)

5.1.1 Pinout

The EFM32G200 and EFM32G210 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bit-field in the *_ROUTE register in the module in question.

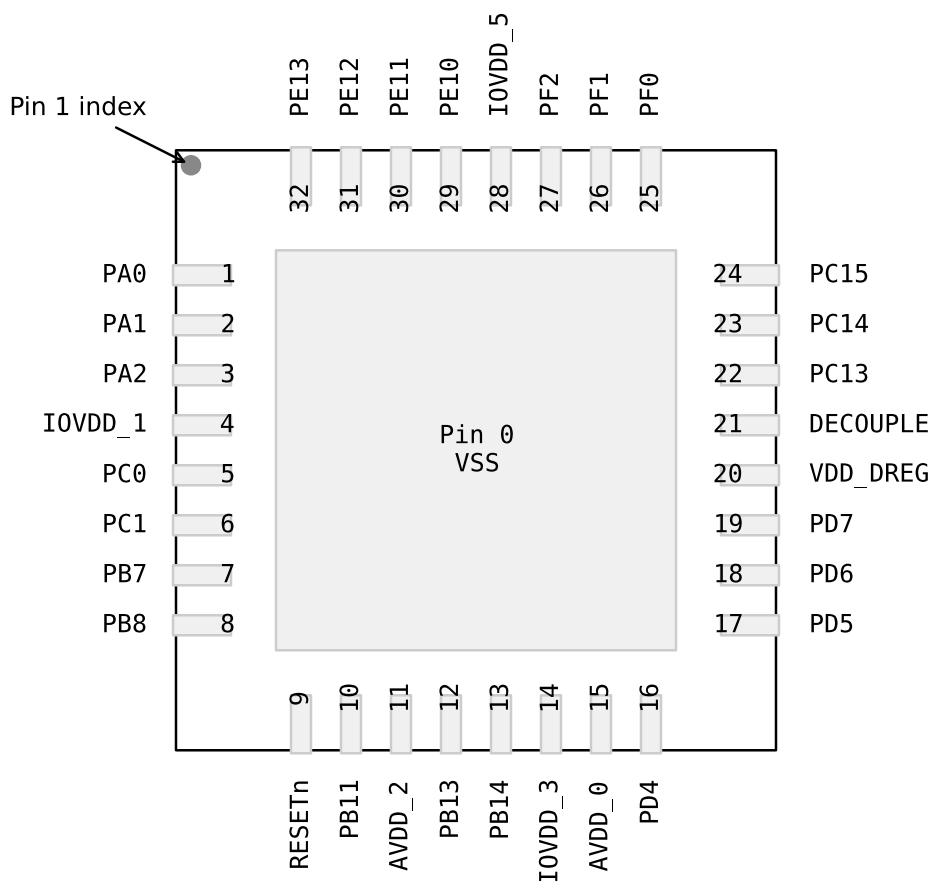


Figure 5.1. EFM32G200 & EFM32G210 Pinout (top view, not to scale)

Table 5.1. Device Pinout

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|---|---------------|-----------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_1 | Digital IO power supply 1. | | | |
| 5 | PC0 | ACMP0_CH0 | PCNT0_S0IN #2 | US1_TX #0 | |
| 6 | PC1 | ACMP0_CH1 | PCNT0_S1IN #2 | US1_RX #0 | |
| 7 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 8 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 9 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 10 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 11 | AVDD_2 | Analog power supply 2. | | | |
| 12 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 13 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 14 | IOVDD_3 | Digital IO power supply 3. | | | |
| 15 | AVDD_0 | Analog power supply 0. | | | |
| 16 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 17 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 18 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 19 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 20 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 21 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 22 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 23 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 24 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 25 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| 26 | PF1 | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 27 | PF2 | | | | ACMP1_O #0 DBG_SWO #0 |
| 28 | IOVDD_5 | Digital IO power supply 5. | | | |
| 29 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 30 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------|---------------|------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 31 | PE12 | | TIM1_CC2 #1 | US0_CLK #0 | |
| 32 | PE13 | | | US0_CS #0 | ACMP0_O #0 |

5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.2. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|-----|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | | | Clock Management Unit, clock output number 1. |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | | Low Energy Timer LETIM0, output channel 0. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|-----|------|---|
| | 0 | 1 | 2 | 3 | |
| LETIM0_OUT1 | PD7 | | PF1 | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | | Pulse Counter PCNT0 input number 1. |
| TIM0_CC0 | PA0 | PA0 | | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | | PC13 | | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | | PC14 | | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | | USART0 clock input / output. |
| US0_CS | PE13 | | | | USART0 chip select input / output. |
| US0_RX | PE11 | | | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | | | USART1 clock input / output. |
| US1_CS | PB8 | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G200 and EFM32G210 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.3. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | — | — | — | — | — | — | — | — | — | — | — | — | — | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | — | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | PC15 | PC14 | PC13 | — | — | — | — | — | — | — | — | — | — | — | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | — | PD7 | PD6 | PD5 | PD4 | — | — | — | — |
| Port E | — | — | PE13 | PE12 | PE11 | PE10 | — | — | — | — | — | — | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | — | — | — | PF2 | PF1 | PF0 |

5.2 EFM32G222 (TQFP48)

5.2.1 Pinout

The EFM32G222 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

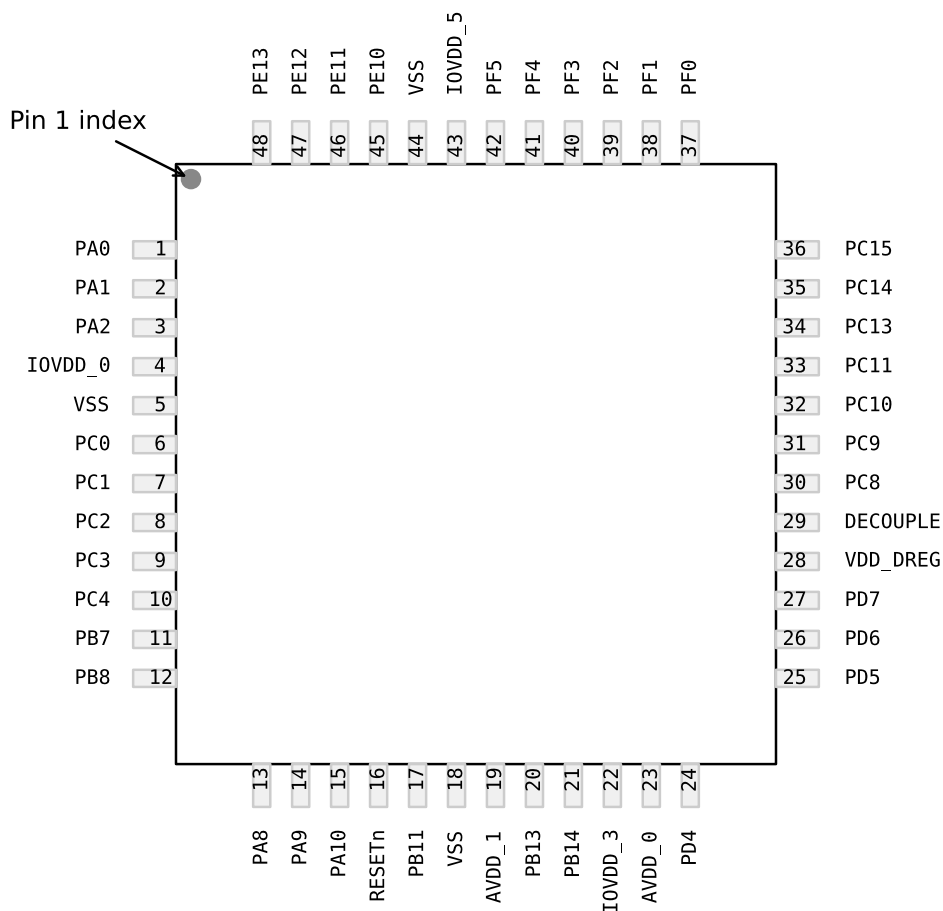


Figure 5.2. EFM32G222 Pinout (top view, not to scale)

Table 5.4. Device Pinout

| TQFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|---------------|---------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | VSS | Ground. | | | |

| TQFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|--|---------------|----------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 6 | PC0 | ACMP0_CH0 | PCNT0_S0IN #2 | US1_TX #0 | |
| 7 | PC1 | ACMP0_CH1 | PCNT0_S1IN #2 | US1_RX #0 | |
| 8 | PC2 | ACMP0_CH2 | | | |
| 9 | PC3 | ACMP0_CH3 | | | |
| 10 | PC4 | ACMP0_CH4 | LETIM0_OUT0 #3 PCNT1_S0IN #0 | | |
| 11 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 12 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 13 | PA8 | | TIM2_CC0 #0 | | |
| 14 | PA9 | | TIM2_CC1 #0 | | |
| 15 | PA10 | | TIM2_CC2 #0 | | |
| 16 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 17 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 18 | VSS | Ground. | | | |
| 19 | AVDD_1 | Analog power supply 1. | | | |
| 20 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 21 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 22 | IOVDD_3 | Digital IO power supply 3. | | | |
| 23 | AVDD_0 | Analog power supply 0. | | | |
| 24 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 25 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 26 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 27 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 28 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 30 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | |
| 31 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | |
| 32 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | |
| 33 | PC11 | ACMP1_CH3 | | US0_TX #2 | |
| 34 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 35 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 36 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 37 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |

| TQFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|----------------|---------------|-----------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 38 | PF1 | | LETIM0_OUT1 #2 | | DBG_SWDDIO #0/1 |
| 39 | PF2 | | | | ACMP1_O #0 DBG_SWO #0 |
| 40 | PF3 | | TIM0_CDTI0 #2 | | |
| 41 | PF4 | | TIM0_CDTI1 #2 | | |
| 42 | PF5 | | TIM0_CDTI2 #2 | | |
| 43 | IOVDD_5 | Digital IO power supply 5. | | | |
| 44 | VSS | Ground. | | | |
| 45 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 46 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 47 | PE12 | | TIM1_CC2 #1 | US0_CLK #0 | |
| 48 | PE13 | | | US0_CS #0 | ACMP0_O #0 |

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|-----|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | | | Clock Management Unit, clock output number 1. |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | | | | Pulse Counter PCNT1 input number 0. |
| TIM0_CC0 | PA0 | PA0 | | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | | PC13 | PF3 | PC13 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1 | | PC14 | PF4 | PC14 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | PF5 | PC15 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | Description |
|-----------|----------|---|------|---|---|
| | 0 | 1 | 2 | 3 | |
| US0_TX | PE10 | | PC11 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | | | USART1 clock input / output. |
| US1_CS | PB8 | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.2.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G222 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.6. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | — | — | — | — | — | PA10 | PA9 | PA8 | — | — | — | — | — | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | — | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | PC15 | PC14 | PC13 | — | PC11 | PC10 | PC9 | PC8 | — | — | — | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | — | PD7 | PD6 | PD5 | PD4 | — | — | — | — |
| Port E | — | — | PE13 | PE12 | PE11 | PE10 | — | — | — | — | — | — | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.3 EFM32G230 (QFN64)

5.3.1 Pinout

The EFM32G230 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

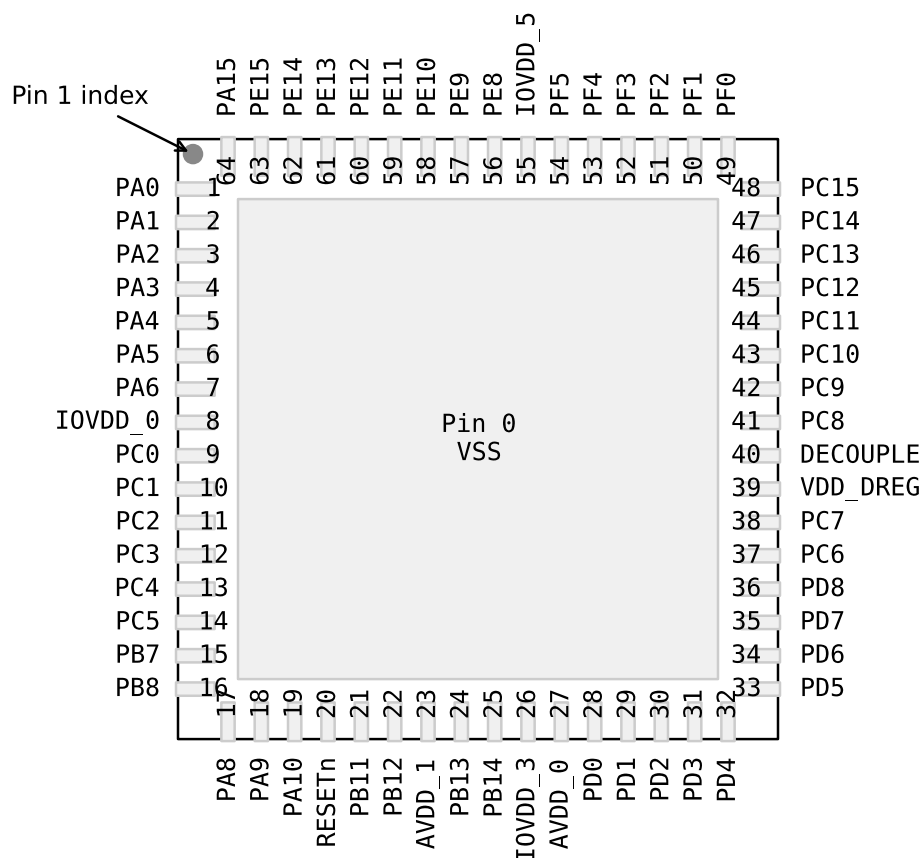


Figure 5.3. EFM32G230 Pinout (top view, not to scale)

Table 5.7. Device Pinout

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|---------------|---------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | | TIM0_CDTI0 #0 | | |
| 5 | PA4 | | TIM0_CDTI1 #0 | | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|---------------------------------|------------------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| 6 | PA6 | | | LEU1_RX #1 | |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PC0 | | PCNT0_S0IN #1 | US1_TX #0 | |
| 10 | PC1 | | PCNT0_S1IN #1 | US1_RX #0 | |
| 11 | PC2 | | | US2_TX #0 | |
| 12 | PC3 | | | US2_RX #0 | |
| 13 | PC4 | ACMP0_CH4 | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 14 | PC5 | ACMP0_CH5 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 15 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 22 | PB12 | DAC0_OUT1 | LETIM0_OUT1 #1 | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 35 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|---|---------------|-----------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | |
| 42 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | |
| 43 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | |
| 45 | PC12 | ACMP1_CH4 | | | CMU_CLK0 #1 |
| 46 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 47 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 48 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 49 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| 50 | PF1 | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 51 | PF2 | | | | ACMP1_O #0 DBG_SWO #0 |
| 52 | PF3 | | TIM0_CDTI0 #2 | | |
| 53 | PF4 | | TIM0_CDTI1 #2 | | |
| 54 | PF5 | | TIM0_CDTI2 #2 | | |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | | PCNT2_S0IN #1 | | |
| 57 | PE9 | | PCNT2_S1IN #1 | | |
| 58 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 60 | PE12 | | TIM1_CC2 #1 | US0_CLK #0 | |
| 61 | PE13 | | | US0_CS #0 | ACMP0_O #0 |
| 62 | PE14 | | | LEU0_TX #2 | |
| 63 | PE15 | | | LEU0_RX #2 | |
| 64 | PA15 | | | | |

5.3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.8. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP2, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP3, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP4, channel 3. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|------|------|---|---|
| | 0 | 1 | 2 | 3 | |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | | | | USART2 clock input / output. |
| US2_CS | PC5 | | | | USART2 chip select input / output. |
| US2_RX | PC3 | | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G230 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.9. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | — | — | — | — | PA10 | PA8 | PA8 — | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | — | — | — | — | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.4 EFM32G232 (TQFP64)

5.4.1 Pinout

The EFM32G232 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

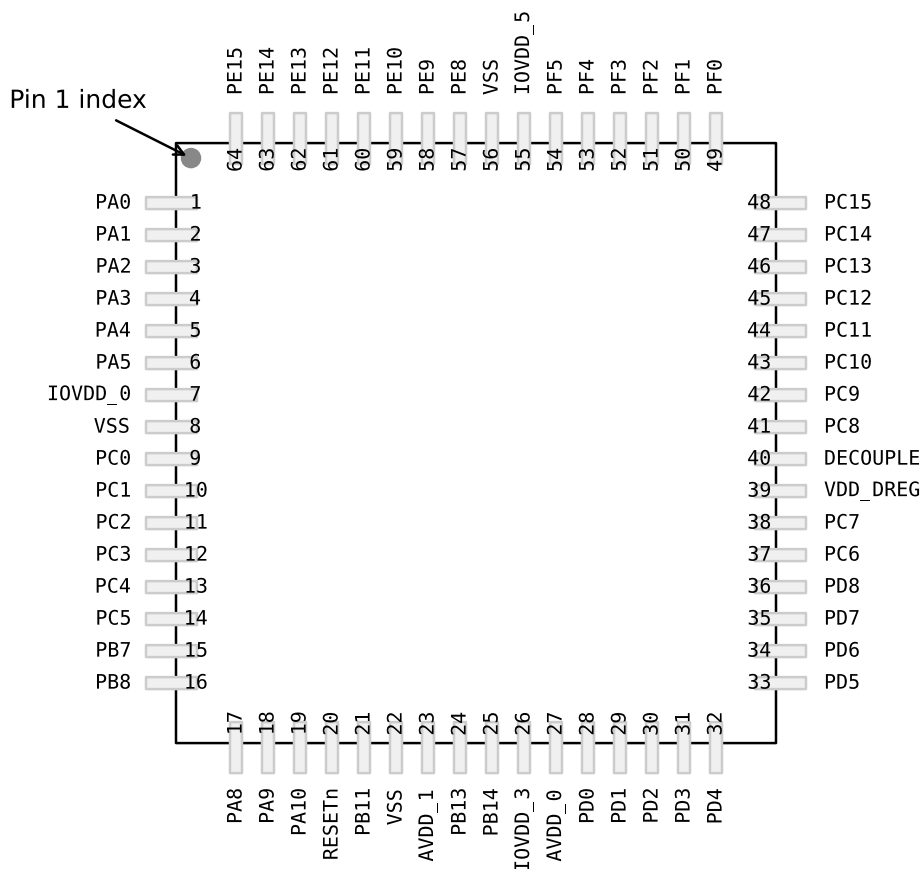


Figure 5.4. EFM32G232 Pinout (top view, not to scale)

Table 5.10. Device Pinout

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|---------------|---------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | | TIM0_CDTI0 #0 | | |
| 5 | PA4 | | TIM0_CDTI1 #0 | | |

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|---------------------------------|------------------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PC0 | ACMP0_CH0 | PCNT0_S0IN #1 | US1_TX #0 | |
| 10 | PC1 | ACMP0_CH1 | PCNT0_S1IN #1 | US1_RX #0 | |
| 11 | PC2 | ACMP0_CH2 | | US1_CLK #1 | |
| 12 | PC3 | ACMP0_CH3 | | US1_CS #1 | |
| 13 | PC4 | ACMP0_CH4 | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 14 | PC5 | ACMP0_CH5 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 15 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 35 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | |

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|---|---------------|-----------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | |
| 42 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | |
| 43 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | |
| 45 | PC12 | ACMP1_CH4 | | | CMU_CLK0 #1 |
| 46 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 47 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 48 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 49 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| 50 | PF1 | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 51 | PF2 | | | | ACMP1_O #0 DBG_SWO #0 |
| 52 | PF3 | | TIM0_CDTI0 #2 | | |
| 53 | PF4 | | TIM0_CDTI1 #2 | | |
| 54 | PF5 | | TIM0_CDTI2 #2 | | |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | | PCNT2_S0IN #1 | | |
| 58 | PE9 | | PCNT2_S1IN #1 | | |
| 59 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 61 | PE12 | | TIM1_CC2 #1 | US0_CLK #0 | |
| 62 | PE13 | | | US0_CS #0 | ACMP0_O #0 |
| 63 | PE14 | | | LEU0_TX #2 | |
| 64 | PE15 | | | LEU0_RX #2 | |

5.4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.11. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH4 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH5 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH6 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH7 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | | USART0 clock input / output. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|-----|------|---|---|
| | 0 | 1 | 2 | 3 | |
| US0_CS | PE13 | | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MI-SO). |
| US0_TX | PE10 | | PC11 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MI-SO). |
| US1_TX | PC0 | PD0 | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | | | | USART2 clock input / output. |
| US2_CS | PC5 | | | | USART2 chip select input / output. |
| US2_RX | PC3 | | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MI-SO). |
| US2_TX | PC2 | | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G2322 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.12. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | — | — | — | — | — | PA10 | PA9 | PA8 | — | — | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | — | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | — | — | — | — | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.5 EFM32G280 (LQFP100)

5.5.1 Pinout

The EFM32G280 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

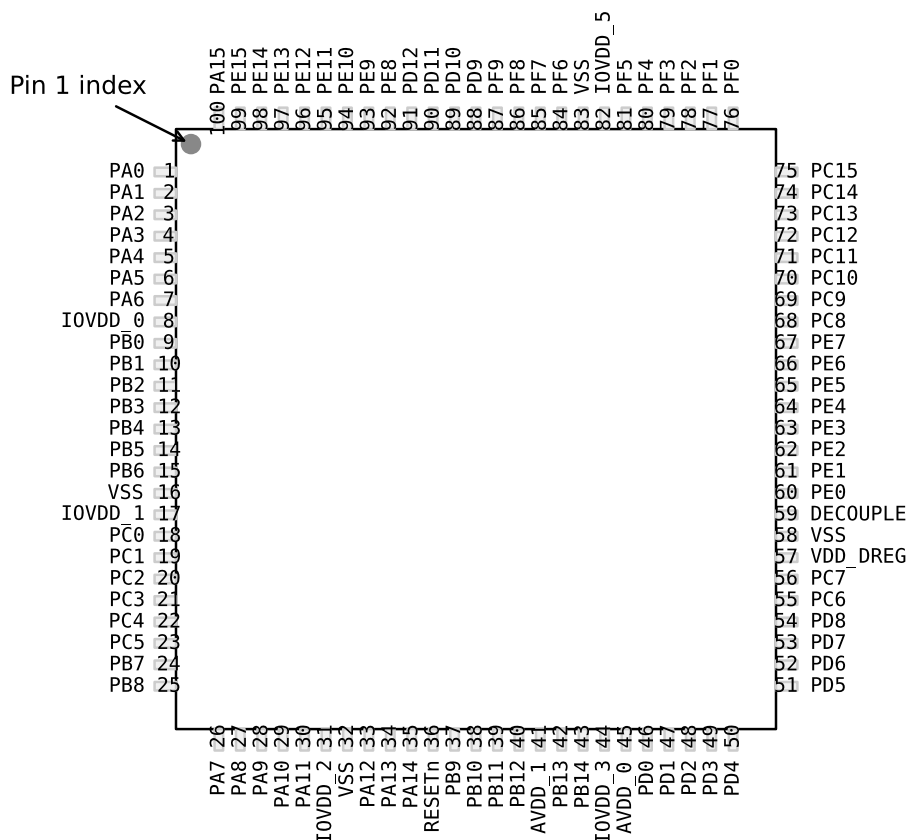


Figure 5.5. EFM32G280 Pinout (top view, not to scale)

Table 5.13. Device Pinout

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|---------------|---------------|-------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | | EBI_AD09 #0 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | EBI_AD10 #0 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | EBI_AD11 #0 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | | EBI_AD12 #0 | TIM0_CDT10 #0 | U0_TX #2 | |
| 5 | PA4 | | EBI_AD13 #0 | TIM0_CDT11 #0 | U0_RX #2 | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|---------------------------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 6 | PA5 | | EBI_AD14 #0 | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| 7 | PA6 | | EBI_AD15 #0 | | LEU1_RX #1 | |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | | | TIM1_CC0 #2 | | |
| 10 | PB1 | | | TIM1_CC1 #2 | | |
| 11 | PB2 | | | TIM1_CC2 #2 | | |
| 12 | PB3 | | | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | | | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | | | | US2_CLK #1 | |
| 15 | PB6 | | | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_C H0 | | PCNT0_S0IN #2 | US1_TX #0 | |
| 19 | PC1 | ACMP0_C H1 | | PCNT0_S1IN #2 | US1_RX #0 | |
| 20 | PC2 | ACMP0_C H2 | | | US2_TX #0 | |
| 21 | PC3 | ACMP0_C H3 | | | US2_RX #0 | |
| 22 | PC4 | ACMP0_C H4 | | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 23 | PC5 | ACMP0_C H5 | | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 24 | PB7 | LFXTAL_P | | | US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | | US1_CS #0 | |
| 26 | PA7 | | | | | |
| 27 | PA8 | | | TIM2_CC0 #0 | | |
| 28 | PA9 | | | TIM2_CC1 #0 | | |
| 29 | PA10 | | | TIM2_CC2 #0 | | |
| 30 | PA11 | | | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 32 | VSS | Ground. | | | | |
| 33 | PA12 | | | TIM2_CC0 #1 | | |
| 34 | PA13 | | | TIM2_CC1 #1 | | |
| 35 | PA14 | | | TIM2_CC2 #1 | | |
| 36 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|---------------|---|-----|------------------------------|---------------------------|-------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 37 | PB9 | | | | | |
| 38 | PB10 | | | | | |
| 39 | PB11 | DAC0_OU T0 | | LETIM0_OUT0 #1 | | |
| 40 | PB12 | DAC0_OU T1 | | LETIM0_OUT1 #1 | | |
| 41 | AVDD_1 | Analog power supply 1. | | | | |
| 42 | PB13 | HFXTAL_ P | | | LEU0_TX #1 | |
| 43 | PB14 | HFXTAL_ N | | | LEU0_RX #1 | |
| 44 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 45 | AVDD_0 | Analog power supply 0. | | | | |
| 46 | PD0 | ADC0_CH 0 | | PCNT2_S0IN #0 | US1_TX #1 | |
| 47 | PD1 | ADC0_CH 1 | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| 48 | PD2 | ADC0_CH 2 | | TIM0_CC1 #3 | US1_CLK #1 | |
| 49 | PD3 | ADC0_CH 3 | | TIM0_CC2 #3 | US1_CS #1 | |
| 50 | PD4 | ADC0_CH 4 | | | LEU0_TX #0 | |
| 51 | PD5 | ADC0_CH 5 | | | LEU0_RX #0 | |
| 52 | PD6 | ADC0_CH 6 | | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 53 | PD7 | ADC0_CH 7 | | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 54 | PD8 | | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_C H6 | | | LEU1_TX #0 I2C0_SDA #2 | |
| 56 | PC7 | ACMP0_C H7 | | | LEU1_RX #0 I2C0_SCL #2 | |
| 57 | VDD_DRE G | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOU- PLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | | |
| 60 | PE0 | | | PCNT0_S0IN #1 | U0_TX #1 | |
| 61 | PE1 | | | PCNT0_S1IN #1 | U0_RX #1 | |
| 62 | PE2 | | | | | ACMP0_O #1 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|---|---------------|--------------------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 63 | PE3 | | | | | ACMP1_O #1 |
| 64 | PE4 | | | | US0_CS #1 | |
| 65 | PE5 | | | | US0_CLK #1 | |
| 66 | PE6 | | | | US0_RX #1 | |
| 67 | PE7 | | | | US0_TX #1 | |
| 68 | PC8 | ACMP1_C H0 | | TIM2_CC0 #2 | US0_CS #2 | |
| 69 | PC9 | ACMP1_C H1 | | TIM2_CC1 #2 | US0_CLK #2 | |
| 70 | PC10 | ACMP1_C H2 | | TIM2_CC2 #2 | US0_RX #2 | |
| 71 | PC11 | ACMP1_C H3 | | | US0_TX #2 | |
| 72 | PC12 | ACMP1_C H4 | | | | CMU_CLK0 #1 |
| 73 | PC13 | ACMP1_C H5 | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 74 | PC14 | ACMP1_C H6 | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | U0_TX #3 | |
| 75 | PC15 | ACMP1_C H7 | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | U0_RX #3 | DBG_SWO #1 |
| 76 | PF0 | | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| 77 | PF1 | | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 78 | PF2 | | EBI_ARDY #0 | | | ACMP1_O #0 DBG_SWO #0 |
| 79 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2 | | |
| 80 | PF4 | | EBI_WEn #0 | TIM0_CDTI1 #2 | | |
| 81 | PF5 | | EBI_REn #0 | TIM0_CDTI2 #2 | | |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | | | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | | | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | | | TIM0_CC2 #2 | | |
| 87 | PF9 | | | | | |
| 88 | PD9 | | EBI_CS0 #0 | | | |
| 89 | PD10 | | EBI_CS1 #0 | | | |
| 90 | PD11 | | EBI_CS2 #0 | | | |
| 91 | PD12 | | EBI_CS3 #0 | | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|---------------|---------------|------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 92 | PE8 | | EBI_AD00 #0 | PCNT2_S0IN #1 | | |
| 93 | PE9 | | EBI_AD01 #0 | PCNT2_S1IN #1 | | |
| 94 | PE10 | | EBI_AD02 #0 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | | EBI_AD03 #0 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 96 | PE12 | | EBI_AD04 #0 | TIM1_CC2 #1 | US0_CLK #0 | |
| 97 | PE13 | | EBI_AD05 #0 | | US0_CS #0 | ACMP0_O #0 |
| 98 | PE14 | | EBI_AD06 #0 | | LEU0_TX #2 | |
| 99 | PE15 | | EBI_AD07 #0 | | LEU0_RX #2 | |
| 100 | PA15 | | EBI_AD08 #0 | | | |

5.5.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.14. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_AD00 | PE8 | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | | | | External Bus Interface (EBI) Address Latch Enable output. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| EBI_ARDY | PF2 | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_CS0 | PD9 | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_REn | PF5 | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_WEn | PF4 | | | | External Bus Interface (EBI) Write Enable output. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | | Timer 1 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| TIM2_CC0 | PA8 | PA12 | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | UART0 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G280 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.15. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.6 EFM32G290 (BGA112)

5.6.1 Pinout

The EFM32G290 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

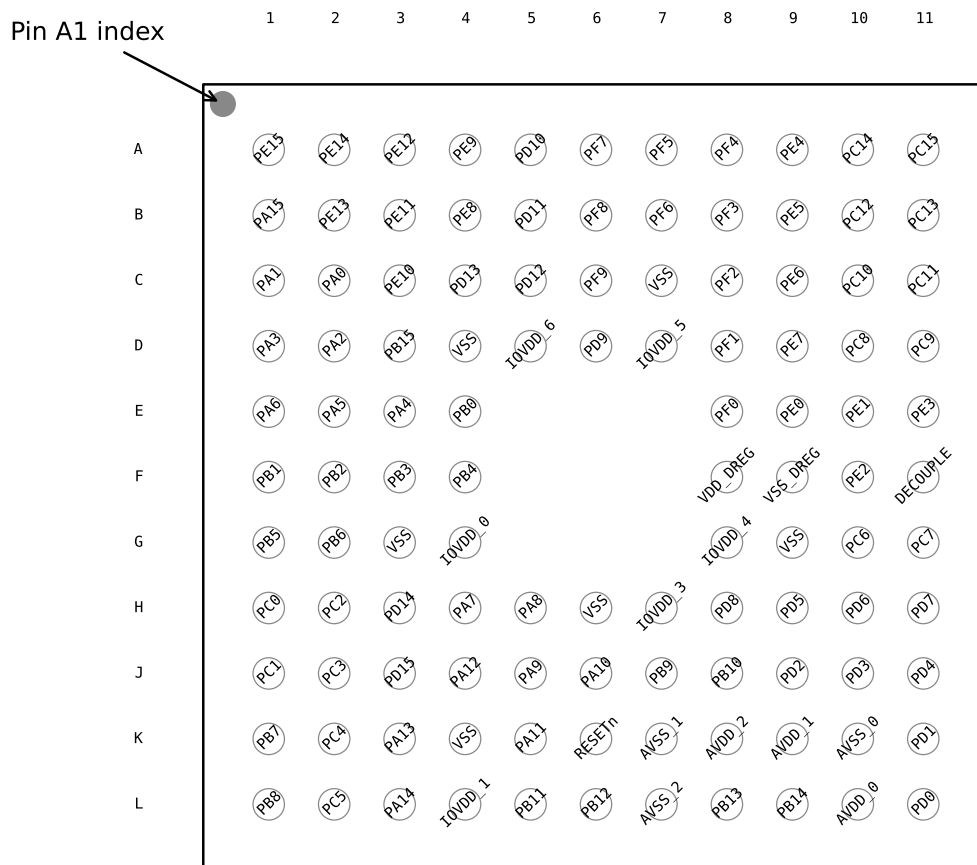


Figure 5.6. EFM32G280 Pinout (top view, not to scale)

Table 5.16. Device Pinout

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-------------|---------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | | EBI_AD07 #0 | | LEU0_RX #2 | |
| A2 | PE14 | | EBI_AD06 #0 | | LEU0_TX #2 | |
| A3 | PE12 | | EBI_AD04 #0 | TIM1_CC2 #1 | US0_CLK #0 | |
| A4 | PE9 | | EBI_AD01 #0 | PCNT2_S1IN #1 | | |
| A5 | PD10 | | EBI_CS1 #0 | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-------------|---|---------------|--------------------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A6 | PF7 | | | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | | EBI_REn #0 | TIM0_CDTI2 #2 | | |
| A8 | PF4 | | EBI_WEn #0 | TIM0_CDTI1 #2 | | |
| A9 | PE4 | | | | US0_CS #1 | |
| A10 | PC14 | ACMP1_C H6 | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | U0_TX #3 | |
| A11 | PC15 | ACMP1_C H7 | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | U0_RX #3 | DBG_SWO #1 |
| B1 | PA15 | | EBI_AD08 #0 | | | |
| B2 | PE13 | | EBI_AD05 #0 | | US0_CS #0 | ACMP0_O #0 |
| B3 | PE11 | | EBI_AD03 #0 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0 | PCNT2_S0IN #1 | | |
| B5 | PD11 | | EBI_CS2 #0 | | | |
| B6 | PF8 | | | TIM0_CC2 #2 | | |
| B7 | PF6 | | | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2 | | |
| B9 | PE5 | | | | US0_CLK #1 | |
| B10 | PC12 | ACMP1_C H4 | | | | CMU_CLK0 #1 |
| B11 | PC13 | ACMP1_C H5 | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| C1 | PA1 | | EBI_AD10 #0 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| C2 | PA0 | | EBI_AD09 #0 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| C3 | PE10 | | EBI_AD02 #0 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | |
| C5 | PD12 | | EBI_CS3 #0 | | | |
| C6 | PF9 | | | | | |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | | EBI_ARDY #0 | | | ACMP1_O #0 DBG_SWO #0 |
| C9 | PE6 | | | | US0_RX #1 | |
| C10 | PC10 | ACMP1_C H2 | | TIM2_CC2 #2 | US0_RX #2 | |
| C11 | PC11 | ACMP1_C H3 | | | US0_TX #2 | |
| D1 | PA3 | | EBI_AD12 #0 | TIM0_CDTI0 #0 | U0_TX #2 | |
| D2 | PA2 | | EBI_AD11 #0 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|---------------|---|-------------|----------------|---------------|----------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| D3 | PB15 | | | | | |
| D4 | VSS | Ground. | | | | |
| D5 | IOVDD_6 | Digital IO power supply 6. | | | | |
| D6 | PD9 | LCD_SEG 28 | EBI_CS0 #0 | | | |
| D7 | IOVDD_5 | Digital IO power supply 5. | | | | |
| D8 | PF1 | | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| D9 | PE7 | | | | US0_TX #1 | |
| D10 | PC8 | ACMP1_C H0 | | TIM2_CC0 #2 | US0_CS #2 | |
| D11 | PC9 | ACMP1_C H1 | | TIM2_CC1 #2 | US0_CLK #2 | |
| E1 | PA6 | | EBI_AD15 #0 | | LEU1_RX #1 | |
| E2 | PA5 | | EBI_AD14 #0 | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| E3 | PA4 | | EBI_AD13 #0 | TIM0_CDTI1 #0 | U0_RX #2 | |
| E4 | PB0 | | | TIM1_CC0 #2 | | |
| E8 | PF0 | | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| E9 | PE0 | | | PCNT0_S0IN #1 | U0_TX #1 | |
| E10 | PE1 | | | PCNT0_S1IN #1 | U0_RX #1 | |
| E11 | PE3 | | | | | ACMP1_O #1 |
| F1 | PB1 | | | TIM1_CC1 #2 | | |
| F2 | PB2 | | | TIM1_CC2 #2 | | |
| F3 | PB3 | | | PCNT1_S0IN #1 | US2_TX #1 | |
| F4 | PB4 | | | PCNT1_S1IN #1 | US2_RX #1 | |
| F8 | VDD_DRE G | Power supply for on-chip voltage regulator. | | | | |
| F9 | VSS_DRE G | Ground for on-chip voltage regulator. | | | | |
| F10 | PE2 | | | | | ACMP0_O #1 |
| F11 | DECOU- PLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | | |
| G1 | PB5 | | | | US2_CLK #1 | |
| G2 | PB6 | | | | US2_CS #1 | |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-----|---------------------------------|---------------------------|-------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| G10 | PC6 | ACMP0_C H6 | | | LEU1_TX #0 I2C0_SDA #2 | |
| G11 | PC7 | ACMP0_C H7 | | | LEU1_RX #0 I2C0_SCL #2 | |
| H1 | PC0 | ACMP0_C H0 | | PCNT0_S0IN #2 | US1_TX #0 | |
| H2 | PC2 | ACMP0_C H2 | | | US2_TX #0 | |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | | | | | |
| H5 | PA8 | | | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | | | | | CMU_CLK1 #1 |
| H9 | PD5 | ADC0_CH 5 | | | LEU0_RX #0 | |
| H10 | PD6 | ADC0_CH 6 | | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| H11 | PD7 | ADC0_CH 7 | | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| J1 | PC1 | ACMP0_C H1 | | PCNT0_S1IN #2 | US1_RX #0 | |
| J2 | PC3 | ACMP0_C H3 | | | US2_RX #0 | |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | | | TIM2_CC0 #1 | | |
| J5 | PA9 | | | TIM2_CC1 #0 | | |
| J6 | PA10 | | | TIM2_CC2 #0 | | |
| J7 | PB9 | | | | | |
| J8 | PB10 | | | | | |
| J9 | PD2 | ADC0_CH 2 | | TIM0_CC1 #3 | US1_CLK #1 | |
| J10 | PD3 | ADC0_CH 3 | | TIM0_CC2 #3 | US1_CS #1 | |
| J11 | PD4 | ADC0_CH 4 | | | LEU0_TX #0 | |
| K1 | PB7 | LFXTAL_P | | | US1_CLK #0 | |
| K2 | PC4 | ACMP0_C H4 | | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| K3 | PA13 | | | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-----|---------------------------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| K5 | PA11 | | | | | |
| K6 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH 1 | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| L1 | PB8 | LFXTAL_N | | | US1_CS #0 | |
| L2 | PC5 | ACMP0_C H5 | | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| L3 | PA14 | | | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OU T0 | | LETIM0_OUT0 #1 | | |
| L6 | PB12 | DAC0_OU T1 | | LETIM0_OUT1 #1 | | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_ P | | | LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_ N | | | LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH 0 | | PCNT2_S0IN #0 | US1_TX #1 | |

5.6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.17. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_AD00 | PE8 | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | | | | External Bus Interface (EBI) Address Latch Enable output. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| EBI_ARDY | PF2 | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_CS0 | PD9 | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_REn | PF5 | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_WEn | PF4 | | | | External Bus Interface (EBI) Write Enable output. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | | Timer 1 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| TIM2_CC0 | PA8 | PA12 | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | UART0 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.6.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G290 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.18. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.7 EFM32G840 (QFN64)

5.7.1 Pinout

The EFM32G840 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

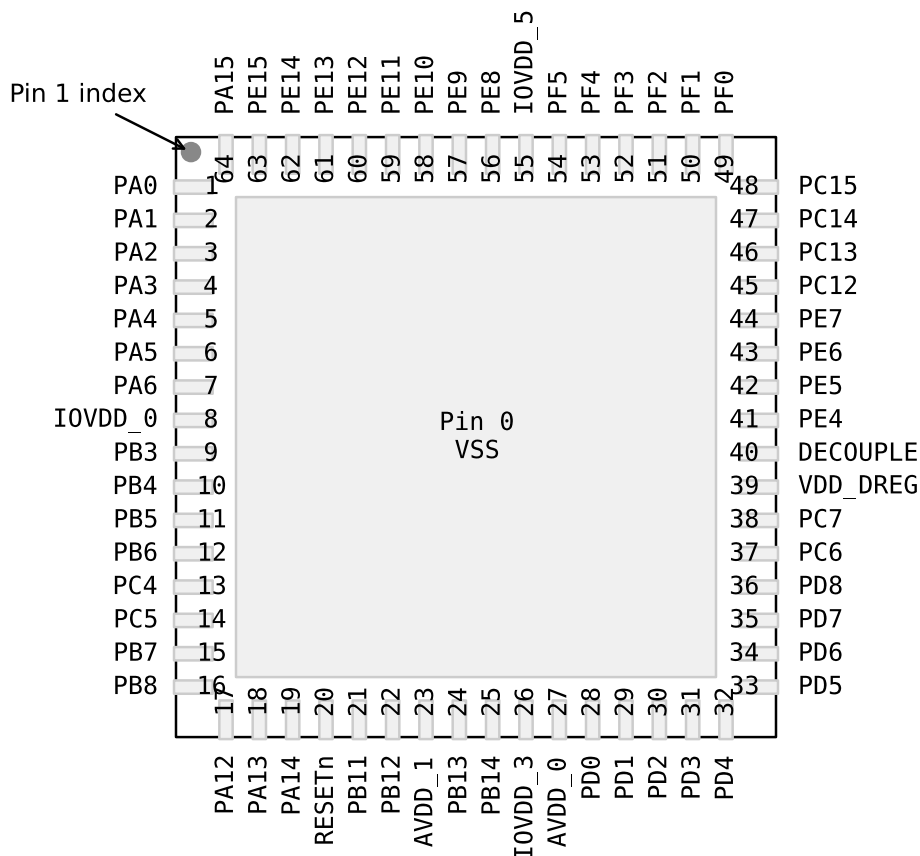


Figure 5.7. EFM32G840 Pinout (top view, not to scale)

Table 5.19. Device Pinout

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|---------------|---------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | LCD_SEG16 | TIM0_CDTI0 #0 | | |
| 5 | PA4 | LCD_SEG17 | TIM0_CDTI1 #0 | | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|---------------------------------|------------------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 6 | PA5 | LCD_SEG18 | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| 6 | PA6 | LCD_SEG19 | | LEU1_RX #1 | |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PB3 | LCD_SEG20 | PCNT1_S0IN #1 | US2_TX #1 | |
| 10 | PB4 | LCD_SEG21 | PCNT1_S1IN #1 | US2_RX #1 | |
| 11 | PB5 | LCD_SEG22 | | US2_CLK #1 | |
| 12 | PB6 | LCD_SEG23 | | US2_CS #1 | |
| 13 | PC4 | ACMP0_CH4 | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 14 | PC5 | ACMP0_CH5 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 15 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | TIM2_CC0 #1 | | |
| 18 | PA13 | LCD_BCAP_N | TIM2_CC1 #1 | | |
| 19 | PA14 | LCD_BEXT | TIM2_CC2 #1 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 22 | PB12 | DAC0_OUT1 | LETIM0_OUT1 #1 | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 35 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|---|------------------------|-----------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | PC12 | ACMP1_CH4 | | | CMU_CLK0 #1 |
| 46 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 47 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 48 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 49 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| 50 | PF1 | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 51 | PF2 | LCD_SEG0 | | | ACMP1_O #0 DBG_SWO #0 |
| 52 | PF3 | LCD_SEG1 | TIM0_CDTI0 #2 | | |
| 53 | PF4 | LCD_SEG2 | TIM0_CDTI1 #2 | | |
| 54 | PF5 | LCD_SEG3 | TIM0_CDTI2 #2 | | |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | LCD_SEG4 | PCNT2_S0IN #1 | | |
| 57 | PE9 | LCD_SEG5 | PCNT2_S1IN #1 | | |
| 58 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 60 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_CLK #0 | |
| 61 | PE13 | LCD_SEG9 | | US0_CS #0 | ACMP0_O #0 |
| 62 | PE14 | LCD_SEG10 | | LEU0_TX #2 | |
| 63 | PE15 | LCD_SEG11 | | LEU0_RX #2 | |
| 64 | PA15 | LCD_SEG12 | | | |

5.7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.20. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |

| Alternate | LOCATION | | | | |
|---------------|----------|------|-----|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFX TAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|-----|---|
| | 0 | 1 | 2 | 3 | |
| LCD_SEG9 | PE13 | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20 | PB3 | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG21 | PB4 | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG22 | PB5 | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG23 | PB6 | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | | | Pulse Counter PCNT0 input number 1. |

| Alternate | LOCATION | | | | Description |
|------------|----------|------|-----|------|--|
| | 0 | 1 | 2 | 3 | |
| PCNT1_S0IN | PC4 | PB3 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | PA12 | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | PA13 | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | PA14 | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | USART2 chip select input / output. |
| US2_RX | | PB4 | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | |
|---------------|----------|-----|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| US2_TX | | PB3 | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.7.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G840 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.21. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | PA14 | PA13 | PA12 | — | — | — | — | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | — | — | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | — | — | — | — | PC7 | PC6 | PC5 | PC4 | — | — | — | — |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.8 EFM32G842 (TQFP64)

5.8.1 Pinout

The EFM32G842 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

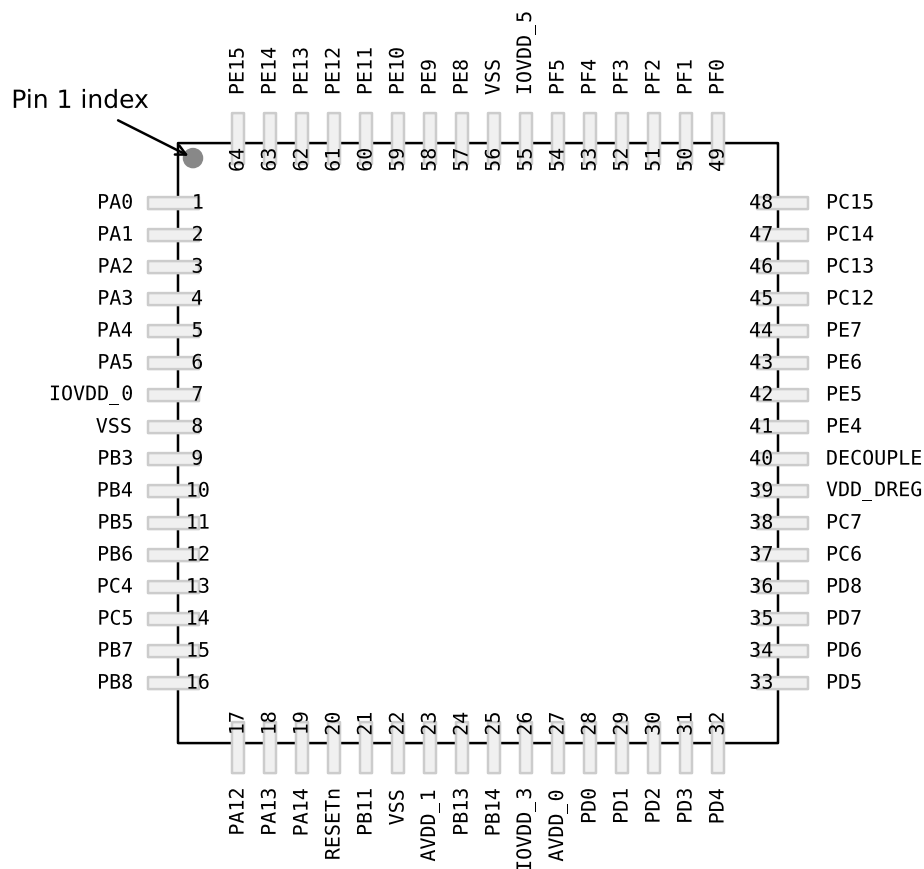


Figure 5.8. EFM32G842 Pinout (top view, not to scale)

Table 5.22. Device Pinout

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|---------------|---------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | LCD_SEG16 | TIM0_CDTI0 #0 | | |
| 5 | PA4 | LCD_SEG17 | TIM0_CDTI1 #0 | | |

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|---------------------------------|------------------------|-------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 6 | PA5 | LCD_SEG18 | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PB3 | LCD_SEG20 | PCNT1_S0IN #1 | US2_TX #1 | |
| 10 | PB4 | LCD_SEG21 | PCNT1_S1IN #1 | US2_RX #1 | |
| 11 | PB5 | LCD_SEG22 | | US2_CLK #1 | |
| 12 | PB6 | LCD_SEG23 | | US2_CS #1 | |
| 13 | PC4 | ACMP0_CH4 | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 14 | PC5 | ACMP0_CH5 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 15 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | TIM2_CC0 #1 | | |
| 18 | PA13 | LCD_BCAP_N | TIM2_CC1 #1 | | |
| 19 | PA14 | LCD_BEXT | TIM2_CC2 #1 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 35 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0 I2C0_SDA #2 | |

| TQFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|----------------------|----------|---|---|------------------------|-----------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0 I2C0_SCL #2 | |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | PC12 | ACMP1_CH4 | | | CMU_CLK0 #1 |
| 46 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 47 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 48 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 49 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |
| 50 | PF1 | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 51 | PF2 | LCD_SEG0 | | | ACMP1_O #0 DBG_SWO #0 |
| 52 | PF3 | LCD_SEG1 | TIM0_CDTI0 #2 | | |
| 53 | PF4 | LCD_SEG2 | TIM0_CDTI1 #2 | | |
| 54 | PF5 | LCD_SEG3 | TIM0_CDTI2 #2 | | |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | LCD_SEG4 | PCNT2_S0IN #1 | | |
| 58 | PE9 | LCD_SEG5 | PCNT2_S1IN #1 | | |
| 59 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 61 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_CLK #0 | |
| 62 | PE13 | LCD_SEG9 | | US0_CS #0 | ACMP0_O #0 |
| 63 | PE14 | LCD_SEG10 | | LEU0_TX #2 | |
| 64 | PE15 | LCD_SEG11 | | LEU0_RX #2 | |

5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.23. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |

| Alternate | LOCATION | | | | Description |
|------------|----------|------|-----|---|---|
| | 0 | 1 | 2 | 3 | |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFX TAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|-----|---|
| | 0 | 1 | 2 | 3 | |
| LCD_SEG9 | PE13 | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG13 | PA0 | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20 | PB3 | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG21 | PB4 | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG22 | PB5 | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG23 | PB6 | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |

| Alternate | LOCATION | | | | Description |
|------------|----------|------|-----|------|--|
| | 0 | 1 | 2 | 3 | |
| TIM0_CC0 | PA0 | PA0 | | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDT10 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDT11 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDT12 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | PA12 | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | PA13 | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | PA14 | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | USART2 chip select input / output. |
| US2_RX | | PB4 | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | | PB3 | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.8.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G842 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.24. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | — | PA14 | PA13 | PA12 | — | — | — | — | — | — | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | — | PB11 | — | — | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | — | — | — | — | PC7 | PC6 | PC5 | PC4 | — | — | — | — |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.9 EFM32G880 (LQFP100)

5.9.1 Pinout

The EFM32G880 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

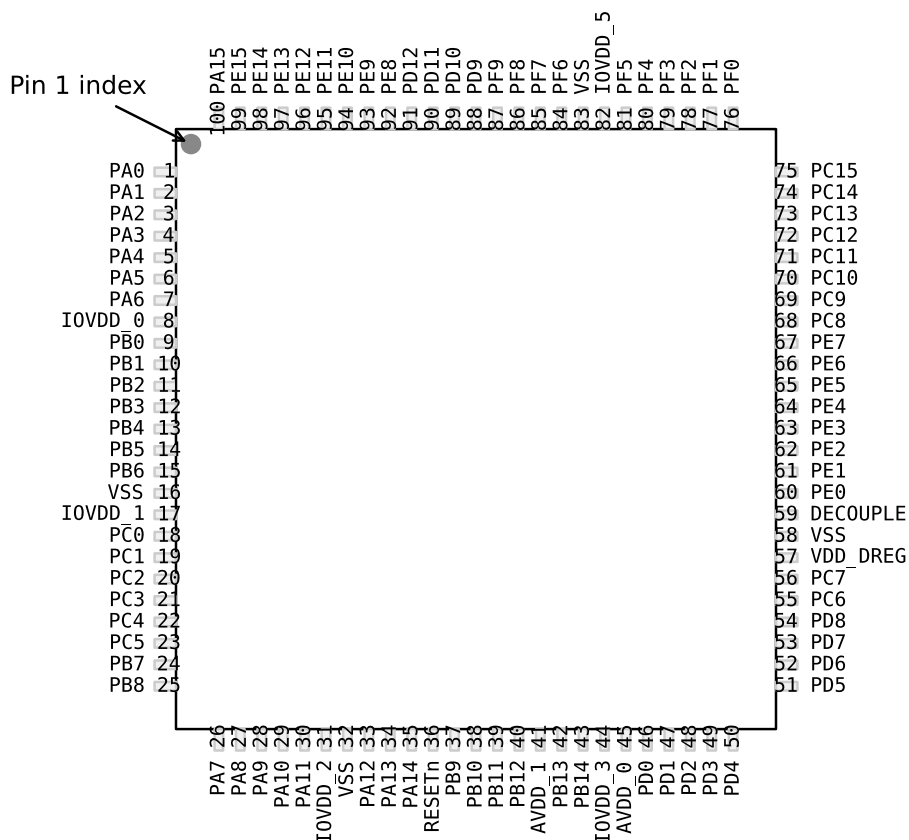


Figure 5.9. EFM32G880 Pinout (top view, not to scale)

Table 5.25. Device Pinout

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|---------------|---------------|-------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG 13 | EBI_AD09 #0 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | LCD_SEG 14 | EBI_AD10 #0 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | LCD_SEG 15 | EBI_AD11 #0 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|---------------------------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 4 | PA3 | LCD_SEG 16 | EBI_AD12 #0 | TIM0_CDT10 #0 | U0_TX #2 | |
| 5 | PA4 | LCD_SEG 17 | EBI_AD13 #0 | TIM0_CDT11 #0 | U0_RX #2 | |
| 6 | PA5 | LCD_SEG 18 | EBI_AD14 #0 | TIM0_CDT12 #0 | LEU1_TX #1 | |
| 7 | PA6 | LCD_SEG 19 | EBI_AD15 #0 | | LEU1_RX #1 | |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | LCD_SEG 32 | | TIM1_CC0 #2 | | |
| 10 | PB1 | LCD_SEG 33 | | TIM1_CC1 #2 | | |
| 11 | PB2 | LCD_SEG 34 | | TIM1_CC2 #2 | | |
| 12 | PB3 | LCD_SEG 20 | | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | LCD_SEG 21 | | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | LCD_SEG 22 | | | US2_CLK #1 | |
| 15 | PB6 | LCD_SEG 23 | | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_C H0 | | PCNT0_S0IN #2 | US1_TX #0 | |
| 19 | PC1 | ACMP0_C H1 | | PCNT0_S1IN #2 | US1_RX #0 | |
| 20 | PC2 | ACMP0_C H2 | | | US2_TX #0 | |
| 21 | PC3 | ACMP0_C H3 | | | US2_RX #0 | |
| 22 | PC4 | ACMP0_C H4 | | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 23 | PC5 | ACMP0_C H5 | | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 24 | PB7 | LFXTAL_P | | | US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | | US1_CS #0 | |
| 26 | PA7 | LCD_SEG 35 | | | | |
| 27 | PA8 | LCD_SEG 36 | | TIM2_CC0 #0 | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-----|------------------------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 28 | PA9 | LCD_SEG 37 | | TIM2_CC1 #0 | | |
| 29 | PA10 | LCD_SEG 38 | | TIM2_CC2 #0 | | |
| 30 | PA11 | LCD_SEG 39 | | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 32 | VSS | Ground. | | | | |
| 33 | PA12 | LCD_BCA P_P | | TIM2_CC0 #1 | | |
| 34 | PA13 | LCD_BCA P_N | | TIM2_CC1 #1 | | |
| 35 | PA14 | LCD_BEX T | | TIM2_CC2 #1 | | |
| 36 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| 37 | PB9 | | | | | |
| 38 | PB10 | | | | | |
| 39 | PB11 | DAC0_OU T0 | | LETIM0_OUT0 #1 | | |
| 40 | PB12 | DAC0_OU T1 | | LETIM0_OUT1 #1 | | |
| 41 | AVDD_1 | Analog power supply 1. | | | | |
| 42 | PB13 | HFXTAL_ P | | | LEU0_TX #1 | |
| 43 | PB14 | HFXTAL_ N | | | LEU0_RX #1 | |
| 44 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 45 | AVDD_0 | Analog power supply 0. | | | | |
| 46 | PD0 | ADC0_CH 0 | | PCNT2_S0IN #0 | US1_TX #1 | |
| 47 | PD1 | ADC0_CH 1 | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| 48 | PD2 | ADC0_CH 2 | | TIM0_CC1 #3 | US1_CLK #1 | |
| 49 | PD3 | ADC0_CH 3 | | TIM0_CC2 #3 | US1_CS #1 | |
| 50 | PD4 | ADC0_CH 4 | | | LEU0_TX #0 | |
| 51 | PD5 | ADC0_CH 5 | | | LEU0_RX #0 | |
| 52 | PD6 | ADC0_CH 6 | | LETIM0_OUT0 #0 | I2C0_SDA #1 | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|---------------|---|-----|---|---------------------------|----------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 53 | PD7 | ADC0_CH7 | | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 54 | PD8 | | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_C H6 | | | LEU1_TX #0 I2C0_SDA #2 | |
| 56 | PC7 | ACMP0_C H7 | | | LEU1_RX #0 I2C0_SCL #2 | |
| 57 | VDD_DRE G | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOU- PLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | | |
| 60 | PE0 | | | PCNT0_S0IN #1 | U0_TX #1 | |
| 61 | PE1 | | | PCNT0_S1IN #1 | U0_RX #1 | |
| 62 | PE2 | | | | | ACMP0_O #1 |
| 63 | PE3 | | | | | ACMP1_O #1 |
| 64 | PE4 | LCD_COM0 | | | US0_CS #1 | |
| 65 | PE5 | LCD_COM1 | | | US0_CLK #1 | |
| 66 | PE6 | LCD_COM2 | | | US0_RX #1 | |
| 67 | PE7 | LCD_COM3 | | | US0_TX #1 | |
| 68 | PC8 | ACMP1_C H0 | | TIM2_CC0 #2 | US0_CS #2 | |
| 69 | PC9 | ACMP1_C H1 | | TIM2_CC1 #2 | US0_CLK #2 | |
| 70 | PC10 | ACMP1_C H2 | | TIM2_CC2 #2 | US0_RX #2 | |
| 71 | PC11 | ACMP1_C H3 | | | US0_TX #2 | |
| 72 | PC12 | ACMP1_C H4 | | | | CMU_CLK0 #1 |
| 73 | PC13 | ACMP1_C H5 | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 74 | PC14 | ACMP1_C H6 | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | U0_TX #3 | |
| 75 | PC15 | ACMP1_C H7 | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | U0_RX #3 | DBG_SWO #1 |
| 76 | PF0 | | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|----------------|---------------|--------------------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 77 | PF1 | | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 78 | PF2 | LCD_SEG_0 | EBI_ARDY #0 | | | ACMP1_O #0 DBG_SWO #0 |
| 79 | PF3 | LCD_SEG_1 | EBI_ALE #0 | TIM0_CDT10 #2 | | |
| 80 | PF4 | LCD_SEG_2 | EBI_WEn #0 | TIM0_CDT11 #2 | | |
| 81 | PF5 | LCD_SEG_3 | EBI_REn #0 | TIM0_CDT12 #2 | | |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | LCD_SEG_24 | | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | LCD_SEG_25 | | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | LCD_SEG_26 | | TIM0_CC2 #2 | | |
| 87 | PF9 | LCD_SEG_27 | | | | |
| 88 | PD9 | LCD_SEG_28 | EBI_CS0 #0 | | | |
| 89 | PD10 | LCD_SEG_29 | EBI_CS1 #0 | | | |
| 90 | PD11 | LCD_SEG_30 | EBI_CS2 #0 | | | |
| 91 | PD12 | LCD_SEG_31 | EBI_CS3 #0 | | | |
| 92 | PE8 | LCD_SEG_4 | EBI_AD00 #0 | PCNT2_S0IN #1 | | |
| 93 | PE9 | LCD_SEG_5 | EBI_AD01 #0 | PCNT2_S1IN #1 | | |
| 94 | PE10 | LCD_SEG_6 | EBI_AD02 #0 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | LCD_SEG_7 | EBI_AD03 #0 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 96 | PE12 | LCD_SEG_8 | EBI_AD04 #0 | TIM1_CC2 #1 | US0_CLK #0 | |
| 97 | PE13 | LCD_SEG_9 | EBI_AD05 #0 | | US0_CS #0 | ACMP0_O #0 |
| 98 | PE14 | LCD_SEG_10 | EBI_AD06 #0 | | LEU0_TX #2 | |
| 99 | PE15 | LCD_SEG_11 | EBI_AD07 #0 | | LEU0_RX #2 | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|-----------------------|----------|---|-------------|--------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 100 | PA15 | LCD_SEG 12 | EBI_AD08 #0 | | | |

5.9.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.26. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_AD00 | PE8 | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | | | | External Bus Interface (EBI) Address Latch Enable output. |

| Alternate | LOCATION | | | | Description |
|------------|----------|-----|-----|---|---|
| | 0 | 1 | 2 | 3 | |
| EBI_ARDY | PF2 | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_CS0 | PD9 | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_REn | PF5 | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_WEn | PF4 | | | | External Bus Interface (EBI) Write Enable output. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|---|---|---|---|
| | 0 | 1 | 2 | 3 | |
| LCD_SEG7 | PE11 | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20 | PB3 | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG21 | PB4 | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG22 | PB5 | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG23 | PB6 | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG24 | PF6 | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| LCD_SEG30 | PD11 | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |

| Alternate | LOCATION | | | | Description |
|------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | UART0 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.9.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G880 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.27. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.10 EFM32G890 (BGA112)

5.10.1 Pinout

The EFM32G890 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

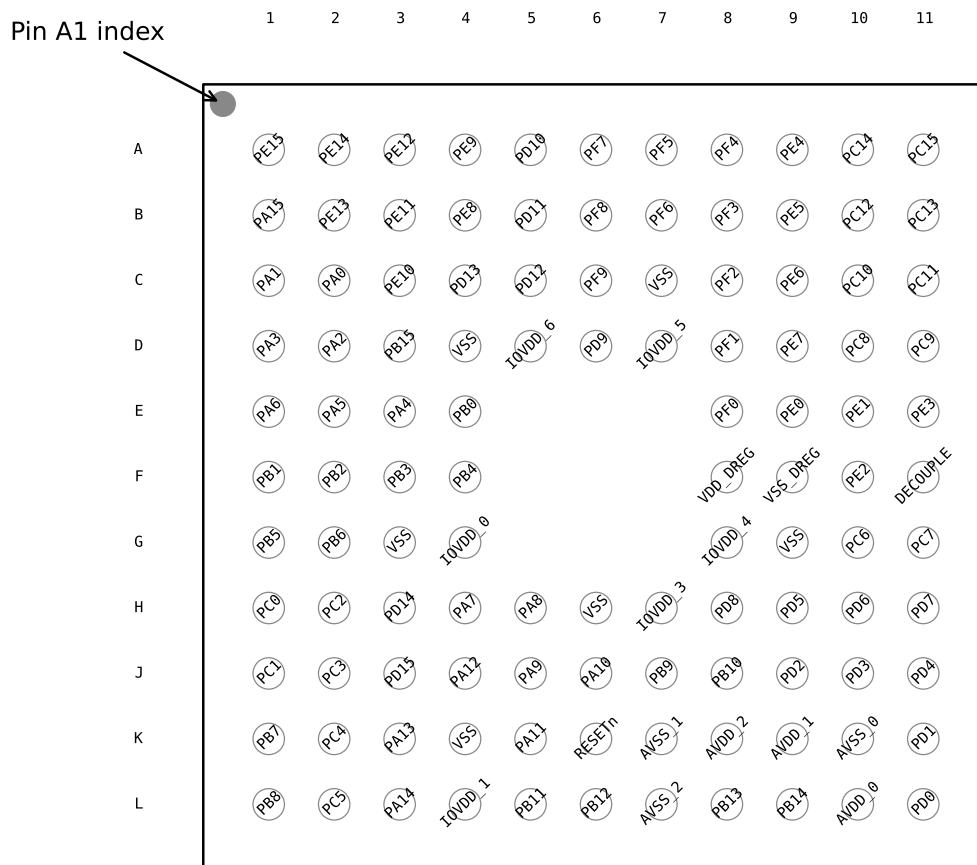


Figure 5.10. EFM32G890 Pinout (top view, not to scale)

Table 5.28. Device Pinout

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-------------|-------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | LCD_SEG_11 | EBI_AD07 #0 | | LEU0_RX #2 | |
| A2 | PE14 | LCD_SEG_10 | EBI_AD06 #0 | | LEU0_TX #2 | |
| A3 | PE12 | LCD_SEG_8 | EBI_AD04 #0 | TIM1_CC2 #1 | US0_CLK #0 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-------------|---|---------------|-------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A4 | PE9 | LCD_SEG 5 | EBI_AD01 #0 | PCNT2_S1IN #1 | | |
| A5 | PD10 | LCD_SEG 29 | EBI_CS1 #0 | | | |
| A6 | PF7 | LCD_SEG 25 | | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | LCD_SEG 3 | EBI_REn #0 | TIM0_CDTI2 #2 | | |
| A8 | PF4 | LCD_SEG 2 | EBI_WEn #0 | TIM0_CDTI1 #2 | | |
| A9 | PE4 | LCD_COM 0 | | | US0_CS #1 | |
| A10 | PC14 | ACMP1_C H6 | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | U0_TX #3 | |
| A11 | PC15 | ACMP1_C H7 | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | U0_RX #3 | DBG_SWO #1 |
| B1 | PA15 | LCD_SEG 12 | EBI_AD08 #0 | | | |
| B2 | PE13 | LCD_SEG 9 | EBI_AD05 #0 | | US0_CS #0 | ACMP0_O #0 |
| B3 | PE11 | LCD_SEG 7 | EBI_AD03 #0 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| B4 | PE8 | LCD_SEG 4 | EBI_AD00 #0 | PCNT2_S0IN #1 | | |
| B5 | PD11 | LCD_SEG 30 | EBI_CS2 #0 | | | |
| B6 | PF8 | LCD_SEG 26 | | TIM0_CC2 #2 | | |
| B7 | PF6 | LCD_SEG 24 | | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | PF3 | LCD_SEG 1 | EBI_ALE #0 | TIM0_CDTI0 #2 | | |
| B9 | PE5 | LCD_COM 1 | | | US0_CLK #1 | |
| B10 | PC12 | ACMP1_C H4 | | | | CMU_CLK0 #1 |
| B11 | PC13 | ACMP1_C H5 | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| C1 | PA1 | LCD_SEG 14 | EBI_AD10 #0 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| C2 | PA0 | LCD_SEG 13 | EBI_AD09 #0 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-------------|----------------|---------------|--------------------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C3 | PE10 | LCD_SEG 6 | EBI_AD02 #0 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | |
| C5 | PD12 | LCD_SEG 31 | EBI_CS3 #0 | | | |
| C6 | PF9 | LCD_SEG 27 | | | | |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | LCD_SEG 0 | EBI_ARDY #0 | | | ACMP1_O #0 DBG_SWO #0 |
| C9 | PE6 | LCD_COM 2 | | | US0_RX #1 | |
| C10 | PC10 | ACMP1_C H2 | | TIM2_CC2 #2 | US0_RX #2 | |
| C11 | PC11 | ACMP1_C H3 | | | US0_TX #2 | |
| D1 | PA3 | LCD_SEG 16 | EBI_AD12 #0 | TIM0_CDT10 #0 | U0_TX #2 | |
| D2 | PA2 | LCD_SEG 15 | EBI_AD11 #0 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| D3 | PB15 | | | | | |
| D4 | VSS | Ground. | | | | |
| D5 | IOVDD_6 | Digital IO power supply 6. | | | | |
| D6 | PD9 | LCD_SEG 28 | EBI_CS0 #0 | | | |
| D7 | IOVDD_5 | Digital IO power supply 5. | | | | |
| D8 | PF1 | | | LETIM0_OUT1 #2 | | DBG_SWPIO #0/1 |
| D9 | PE7 | LCD_COM 3 | | | US0_TX #1 | |
| D10 | PC8 | ACMP1_C H0 | | TIM2_CC0 #2 | US0_CS #2 | |
| D11 | PC9 | ACMP1_C H1 | | TIM2_CC1 #2 | US0_CLK #2 | |
| E1 | PA6 | LCD_SEG 19 | EBI_AD15 #0 | | LEU1_RX #1 | |
| E2 | PA5 | LCD_SEG 18 | EBI_AD14 #0 | TIM0_CDT12 #0 | LEU1_TX #1 | |
| E3 | PA4 | LCD_SEG 17 | EBI_AD13 #0 | TIM0_CDT11 #0 | U0_RX #2 | |
| E4 | PB0 | LCD_SEG 32 | | TIM1_CC0 #2 | | |
| E8 | PF0 | | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|---------------|---|-----|---------------|---------------------------|-------------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| E9 | PE0 | | | PCNT0_S0IN #1 | U0_TX #1 | |
| E10 | PE1 | | | PCNT0_S1IN #1 | U0_RX #1 | |
| E11 | PE3 | | | | | ACMP1_O #1 |
| F1 | PB1 | LCD_SEG 33 | | TIM1_CC1 #2 | | |
| F2 | PB2 | LCD_SEG 34 | | TIM1_CC2 #2 | | |
| F3 | PB3 | LCD_SEG 20 | | PCNT1_S0IN #1 | US2_TX #1 | |
| F4 | PB4 | LCD_SEG 21 | | PCNT1_S1IN #1 | US2_RX #1 | |
| F8 | VDD_DRE G | Power supply for on-chip voltage regulator. | | | | |
| F9 | VSS_DRE G | Ground for on-chip voltage regulator. | | | | |
| F10 | PE2 | | | | | ACMP0_O #1 |
| F11 | DECOU- PLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | | |
| G1 | PB5 | LCD_SEG 22 | | | US2_CLK #1 | |
| G2 | PB6 | LCD_SEG 23 | | | US2_CS #1 | |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |
| G10 | PC6 | ACMP0_C H6 | | | LEU1_TX #0 I2C0_SDA #2 | |
| G11 | PC7 | ACMP0_C H7 | | | LEU1_RX #0 I2C0_SCL #2 | |
| H1 | PC0 | ACMP0_C H0 | | PCNT0_S0IN #2 | US1_TX #0 | |
| H2 | PC2 | ACMP0_C H2 | | | US2_TX #0 | |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | LCD_SEG 35 | | | | |
| H5 | PA8 | LCD_SEG 36 | | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | | | | | CMU_CLK1 #1 |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-----|---------------------------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| H9 | PD5 | ADC0_CH 5 | | | LEU0_RX #0 | |
| H10 | PD6 | ADC0_CH 6 | | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| H11 | PD7 | ADC0_CH 7 | | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| J1 | PC1 | ACMP0_C H1 | | PCNT0_S1IN #2 | US1_RX #0 | |
| J2 | PC3 | ACMP0_C H3 | | | US2_RX #0 | |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | LCD_BCA P_P | | TIM2_CC0 #1 | | |
| J5 | PA9 | LCD_SEG 37 | | TIM2_CC1 #0 | | |
| J6 | PA10 | LCD_SEG 38 | | TIM2_CC2 #0 | | |
| J7 | PB9 | | | | | |
| J8 | PB10 | | | | | |
| J9 | PD2 | ADC0_CH 2 | | TIM0_CC1 #3 | US1_CLK #1 | |
| J10 | PD3 | ADC0_CH 3 | | TIM0_CC2 #3 | US1_CS #1 | |
| J11 | PD4 | ADC0_CH 4 | | | LEU0_TX #0 | |
| K1 | PB7 | LFXTAL_P | | | US1_CLK #0 | |
| K2 | PC4 | ACMP0_C H4 | | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| K3 | PA13 | LCD_BCA P_N | | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |
| K5 | PA11 | LCD_SEG 39 | | | | |
| K6 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH 1 | | TIM0_CC0 #3 PCNT2_S1IN #0 | US1_RX #1 | |
| L1 | PB8 | LFXTAL_N | | | US1_CS #0 | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|----------------------|----------|---|-----|---------------------------------|---------------|-------|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| L2 | PC5 | ACMP0_C H5 | | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| L3 | PA14 | LCD_BEX T | | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OU T0 | | LETIM0_OUT0 #1 | | |
| L6 | PB12 | DAC0_OU T1 | | LETIM0_OUT1 #1 | | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_ P | | | LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_ N | | | LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH 0 | | PCNT2_S0IN #0 | US1_TX #1 | |

5.10.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.29. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | Description |
|----------------------------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| ACMP0_CH0 | PC0 | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | | | Clock Management Unit, clock output number 1. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|------|---|---|---|
| | 0 | 1 | 2 | 3 | |
| DAC0_OUT0 | PB11 | | | | Digital to Analog Converter DAC0 output channel number 0. |
| DAC0_OUT1 | PB12 | | | | Digital to Analog Converter DAC0 output channel number 1. |
| DBG_SWCLK | PF0 | PF0 | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_AD00 | PE8 | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | | | | External Bus Interface (EBI) Address Latch Enable output. |

| Alternate | LOCATION | | | | Description |
|------------|----------|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | |
| EBI_ARDY | PF2 | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_CS0 | PD9 | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_REn | PF5 | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_WEn | PF4 | | | | External Bus Interface (EBI) Write Enable output. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |

| Alternate | LOCATION | | | | Description |
|-----------|----------|---|---|---|---|
| | 0 | 1 | 2 | 3 | |
| LCD_SEG7 | PE11 | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20 | PB3 | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG21 | PB4 | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG22 | PB5 | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG23 | PB6 | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. |
| LCD_SEG24 | PF6 | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |

| Alternate | LOCATION | | | | Description |
|-------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| LCD_SEG30 | PD11 | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | Pulse Counter PCNT2 input number 1. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | Timer 0 Complimentary Deat Time Insertion channel 0. |

| Alternate | LOCATION | | | | Description |
|------------|----------|------|------|------|---|
| | 0 | 1 | 2 | 3 | |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | UART0 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |

5.10.3 GPIO Pinout Overview

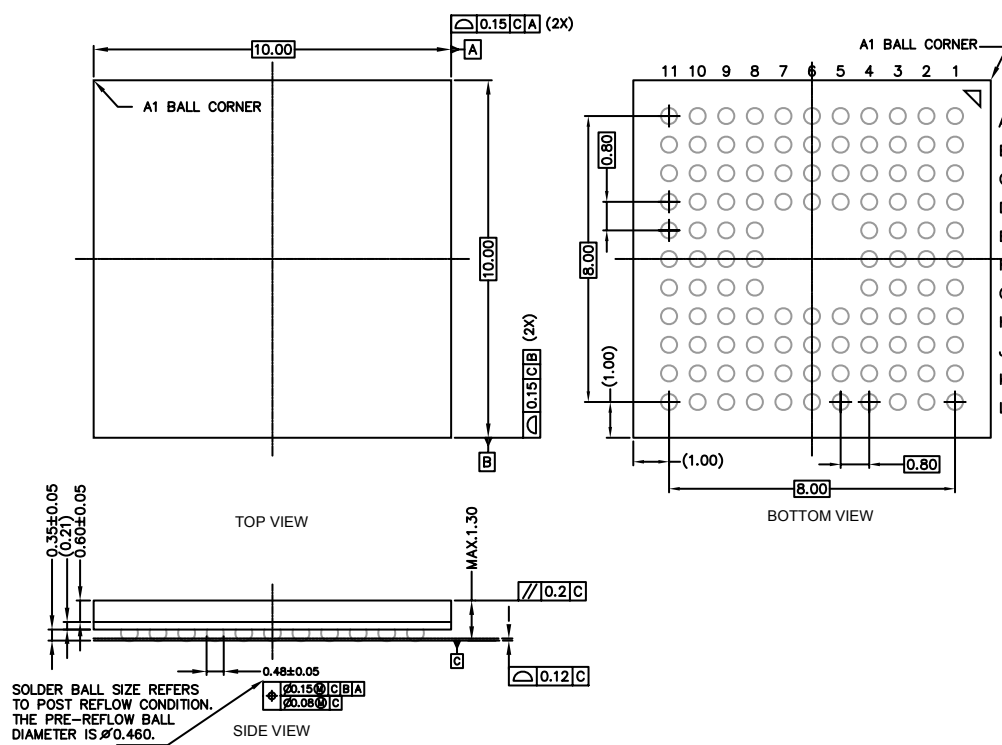
The specific GPIO pins available in EFM32G890 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.30. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

6. BGA112 Package Specifications

6.1 BGA112 Package Dimensions



Rev: 97SP01315A_X03_06.lum11

Figure 6.1. BGA112

Note:

1. The dimensions in parenthesis are reference.
2. Datum 'C' and seating plane are defined by the crown of the solder balls.
3. All dimensions are in millimeters.

6.2 BGA112 PCB Layout

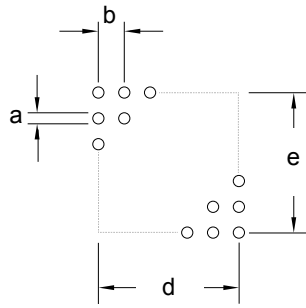


Figure 6.2. BGA112 PCB Land Pattern

Table 6.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.35 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

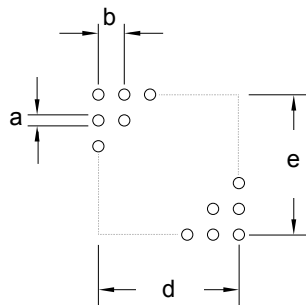


Figure 6.3. BGA112 PCB Solder Mask

Table 6.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.48 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

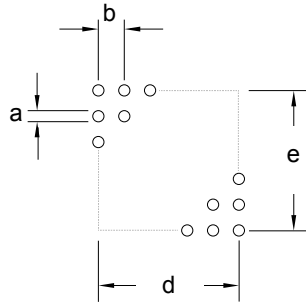


Figure 6.4. BGA112 PCB Stencil Design

Table 6.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.33 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

6.3 BGA112 Package Marking

In the illustration below package fields and position are shown.

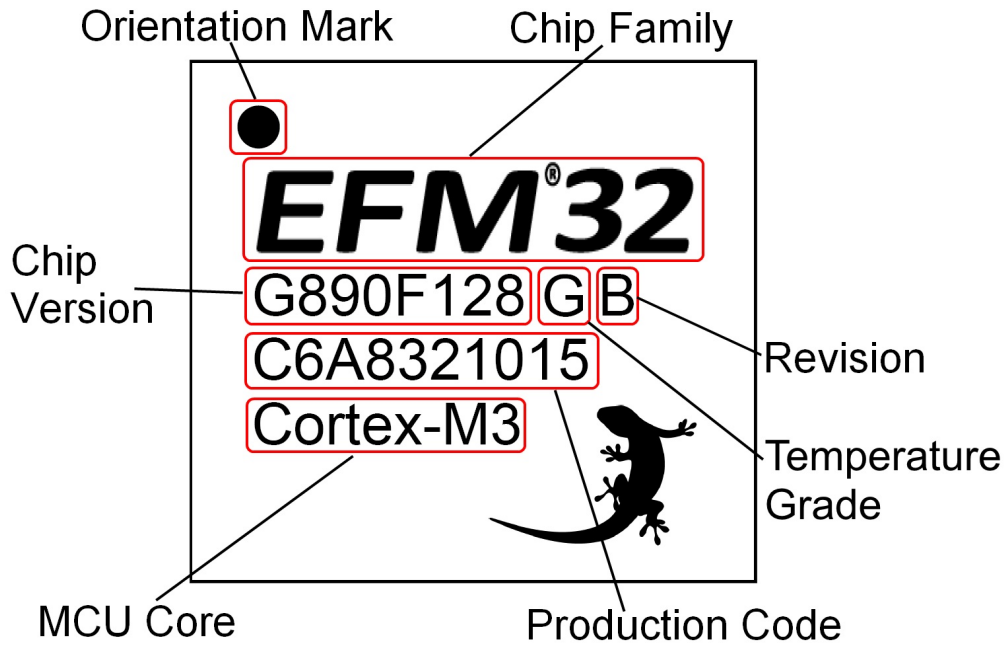


Figure 6.5. Example Chip Marking (Top View)

7. LQFP100 Package Specifications

7.1 LQFP100 Package Dimensions

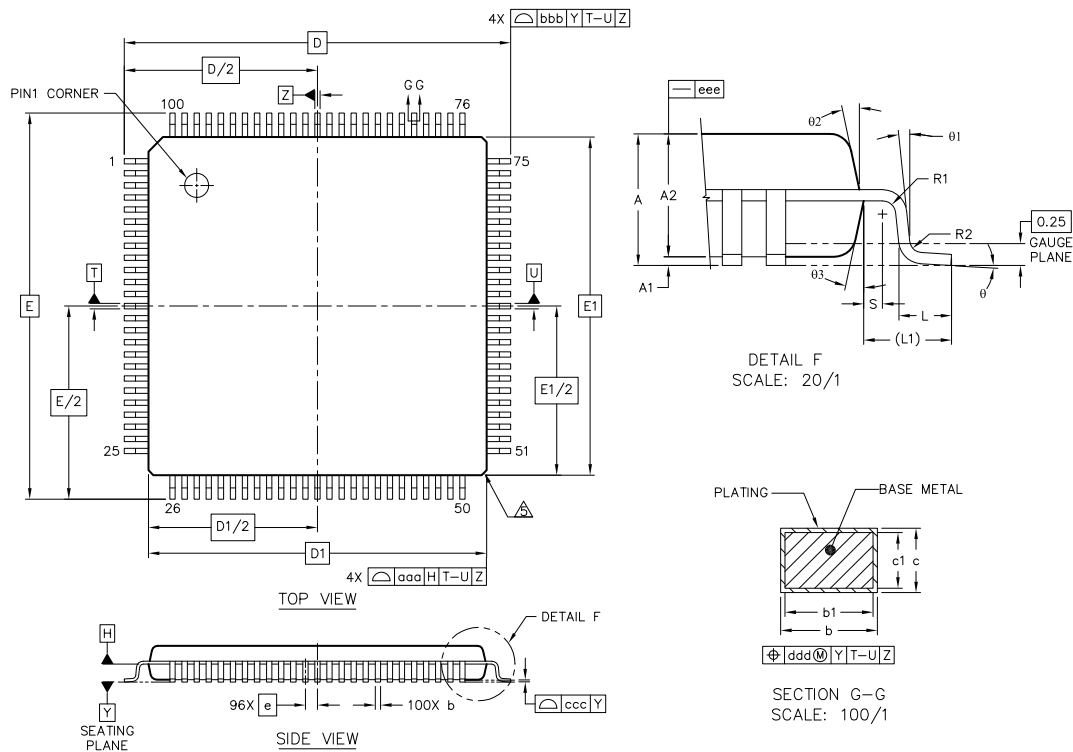


Figure 7.1. LQFP100

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

Table 7.1. LQFP100 (Dimensions in mm)

| | | SYMBOL | MIN | NOM | MAX |
|-------------------------|---|------------|---------|------|------|
| total thickness | | A | — | — | 1.6 |
| stand off | | A1 | 0.05 | — | 0.15 |
| mold thickness | | A2 | 1.35 | 1.4 | 1.45 |
| lead width (plating) | | b | 0.17 | 0.2 | 0.27 |
| lead width | | b1 | 0.17 | — | 0.23 |
| L/F thickness (plating) | | c | 0.09 | — | 0.2 |
| lead thickness | | c1 | 0.09 | — | 0.16 |
| | x | D | 16 BSC | | |
| | y | E | 16 BSC | | |
| body size | x | D1 | 14 BSC | | |
| | y | E1 | 14 BSC | | |
| lead pitch | | e | 0.5 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| footprint | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | $\theta 1$ | 0° | — | — |
| | | $\theta 2$ | 11° | 12° | 13° |
| | | $\theta 3$ | 11° | 12° | 13° |
| | | R1 | 0.08 | — | — |
| | | R1 | 0.08 | — | 0.2 |
| | | S | 0.2 | — | — |
| package edge tolerance | | aaa | 0.2 | | |
| lead edge tolerance | | bbb | 0.2 | | |
| coplanarity | | ccc | 0.08 | | |
| lead offset | | ddd | 0.08 | | |
| mold flatness | | eee | 0.05 | | |

7.2 LQFP100 PCB Layout

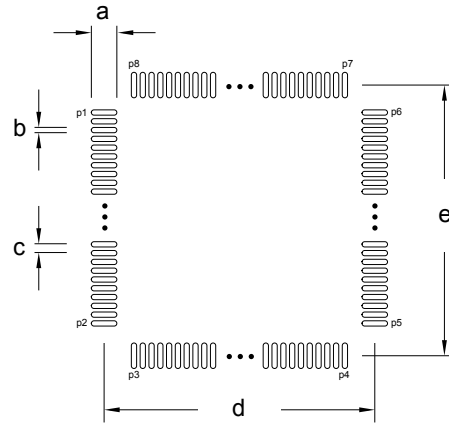


Figure 7.2. LQFP100 PCB Land Pattern

Table 7.2. LQFP100 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 1.45 | P1 | 1 | P6 | 75 |
| b | 0.30 | P2 | 25 | P7 | 76 |
| c | 0.50 | P3 | 26 | P8 | 100 |
| d | 15.40 | P4 | 50 | | |
| e | 15.40 | P5 | 51 | | |

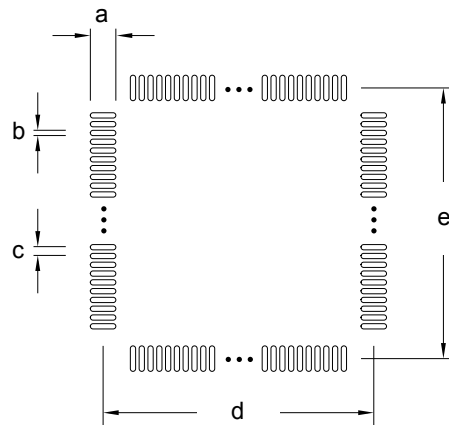


Figure 7.3. LQFP100 PCB Solder Mask

Table 7.3. LQFP100 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.57 |
| b | 0.42 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

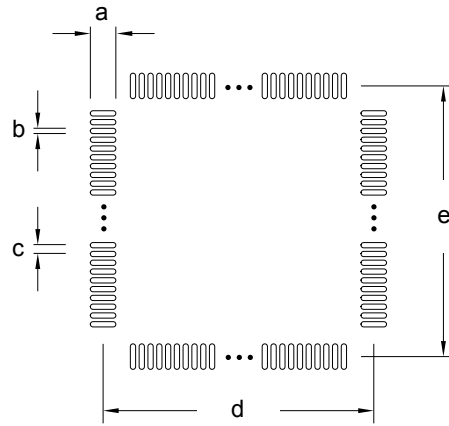


Figure 7.4. LQFP100 PCB Stencil Design

Table 7.4. LQFP100 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.35 |
| b | 0.20 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

7.3 LQFP100 Package Marking

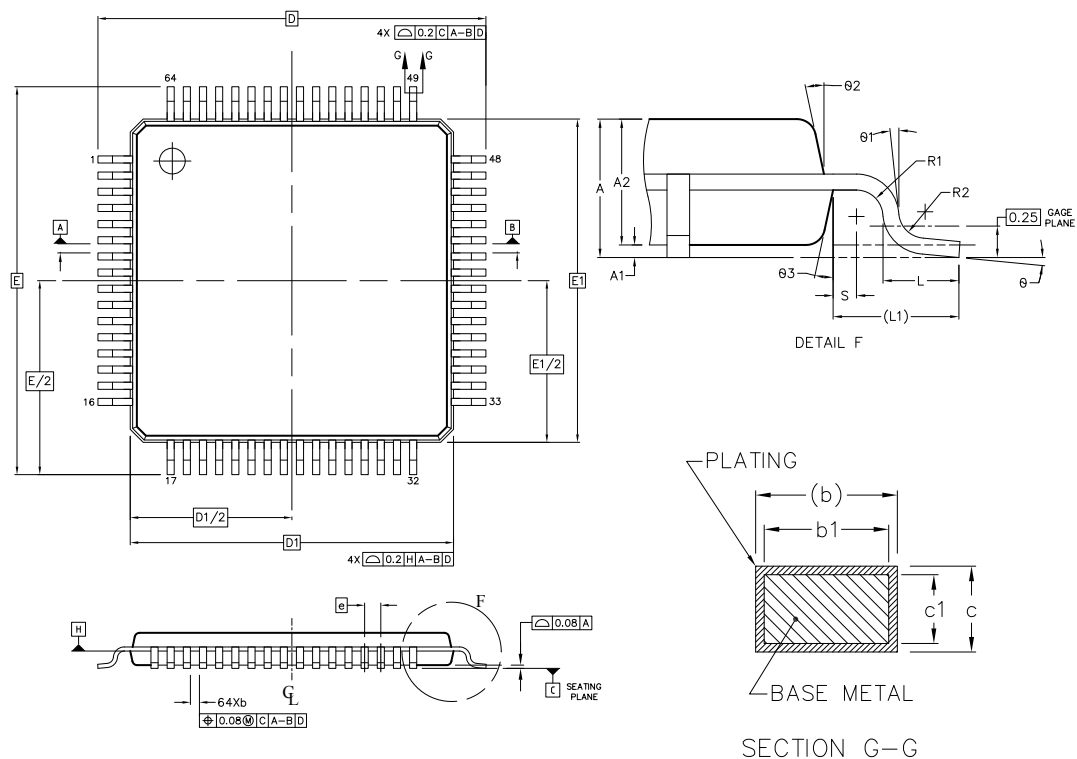
In the illustration below package fields and position are shown.



Figure 7.5. Example Chip Marking (Top View)

8. TQFP64 Package Specifications

8.1 TQFP64 Package Dimensions



Rev: 98SP64023A_X01_17MAR2011

Figure 8.1. TQFP64

Note:

- All dimensions & tolerancing confirm to ASME Y14.5M-1994.
- The top package body size may be smaller than the bottom package body size.
- Datum 'A,B', and 'B' to be determined at datum plane 'H'.
- To be determined at seating place 'C'.
- Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
- Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
- Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
- Exact shape of each corner is optional.
- These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
- All dimensions are in millimeters.

Table 8.1. QFP64 (Dimensions in mm)

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|-----|----------|------|------|-----|------|------|------|
| A | — | 1.10 | 1.20 | L1 | — | | |
| A1 | 0.05 | — | 0.15 | R1 | 0.08 | — | — |
| A2 | 0.95 | 1.00 | 1.05 | R2 | 0.08 | — | 0.20 |
| b | 0.17 | 0.22 | 0.27 | S | 0.20 | — | — |
| b1 | 0.17 | 0.20 | 0.23 | θ | 0° | 3.5° | 7° |
| c | 0.09 | — | 0.20 | θ1 | 0° | — | — |
| C1 | 0.09 | — | 0.16 | θ2 | 11° | 12° | 13° |
| D | 12.0 BSC | | | θ3 | 11° | 12° | 13° |
| D1 | 10.0 BSC | | | | | | |
| e | 0.50 BSC | | | | | | |
| E | 12.0 BSC | | | | | | |
| E1 | 10.0 BSC | | | | | | |
| L | 0.45 | 0.60 | 0.75 | | | | |

8.2 TQFP64 PCB Layout

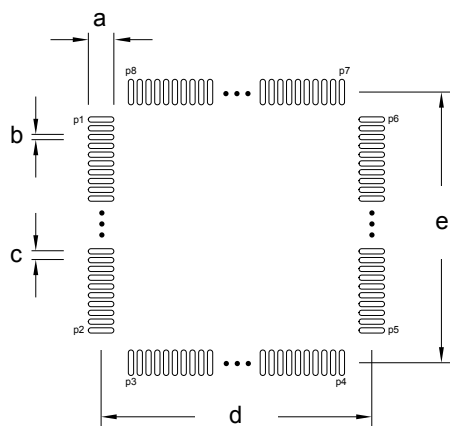


Figure 8.2. TQFP64 PCB Land Pattern

Table 8.2. TQFP64 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 1.60 | P1 | 1 | P6 | 48 |
| b | 0.30 | P2 | 16 | P7 | 49 |
| c | 0.50 | P3 | 17 | P8 | 64 |
| d | 11.50 | P4 | 32 | | |
| e | 11.50 | P5 | 33 | | |

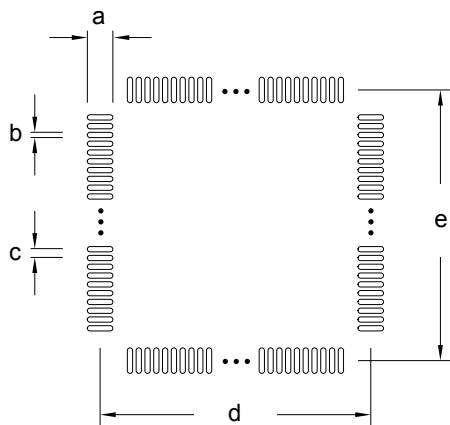


Figure 8.3. TQFP64 PCB Solder Mask

Table 8.3. TQFP64 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

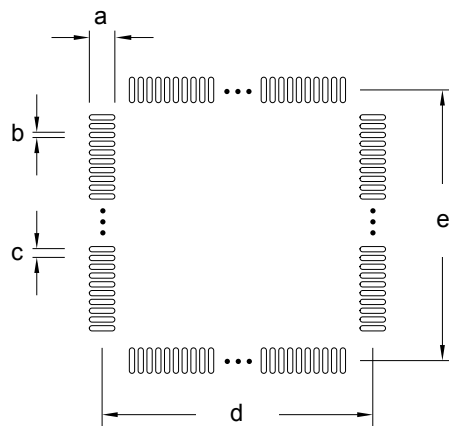


Figure 8.4. TQFP64 PCB Stencil Design

Table 8.4. TQFP64 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.50 |
| b | 0.20 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

8.3 TQFP64 Package Marking

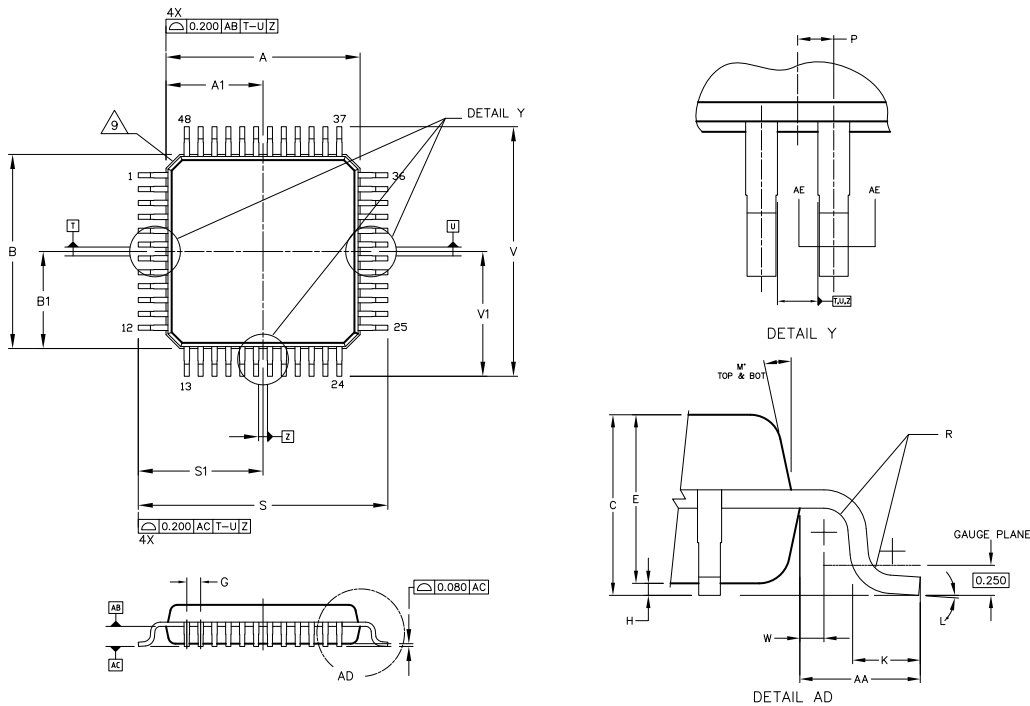
In the illustration below package fields and position are shown.



Figure 8.5. Example Chip Marking (Top View)

9. TQFP48 Package Specifications

9.1 TQFP48 Package Dimensions



Rev: 98SP48097A_XO_30Mar11

Figure 9.1. TQFP48

Note:

1. Dimensions and tolerance per ASME Y14.5M-1994
2. Control dimension: Millimeter
3. Datum plane AB is located at bottom of lead and is coincident with the lead where the lead exists from the plastic body at the bottom of the parting line.
4. Datums T, U and Z to be determined at datum plane AB.
5. Dimensions S and V to be determined at seating plane AC.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 per side. Dimensions A and B do include mold mismatch and are determined at datum AB.
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.350.
8. Minimum solder plate thickness shall be 0.0076.
9. Exact shape of each corner is optional.

Table 9.1. QFP48 (Dimensions in mm)

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|-----|-------|-----------|-------|-----|-------|-----------|-------|
| A | — | 7.000 BSC | — | M | — | 12DEG REF | |
| A1 | — | 3.500 BSC | — | N | 0.090 | — | 0.160 |
| B | — | 7.000 BSC | — | P | — | 0.250 BSC | — |
| B1 | — | 3.500 BSC | — | R | 0.150 | — | 0.250 |
| C | 1.000 | — | 1.200 | S | — | 9.000 BSC | — |
| D | 0.170 | — | 0.270 | S1 | — | 4.500 BSC | — |
| E | 0.950 | — | 1.050 | V | — | 9.000 BSC | — |
| F | 0.170 | — | 0.230 | V1 | — | 4.500 BSC | — |
| G | — | 0.500 BSC | — | W | — | 0.200 BSC | — |
| H | 0.050 | — | 0.150 | AA | — | 1.000 BSC | — |
| J | 0.090 | — | 0.200 | | | | |
| K | 0.500 | — | 0.700 | | | | |
| L | 0DEG | — | 7DEG | | | | |

The TQFP48 package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

9.2 TQFP48 PCB Layout

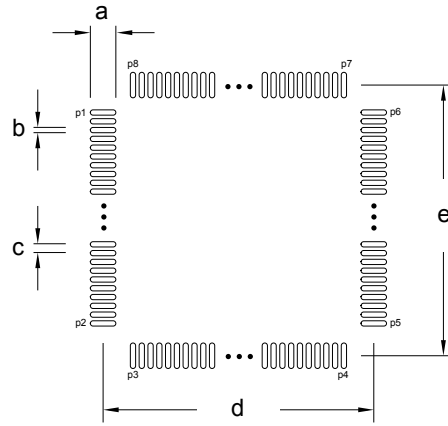


Figure 9.2. TQFP48 PCB Land Pattern

Table 9.2. TQFP48 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 1.60 | P1 | 1 | P6 | 36 |
| b | 0.30 | P2 | 12 | P7 | 37 |
| c | 0.50 | P3 | 13 | P8 | 48 |
| d | 8.50 | P4 | 24 | | |
| e | 8.50 | P5 | 25 | | |

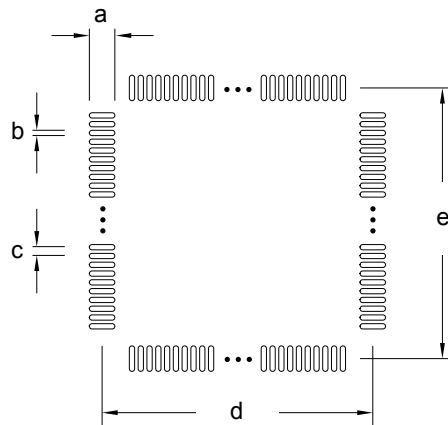


Figure 9.3. TQFP48 PCB Solder Mask

Table 9.3. TQFP48 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 8.50 |
| e | 8.50 |

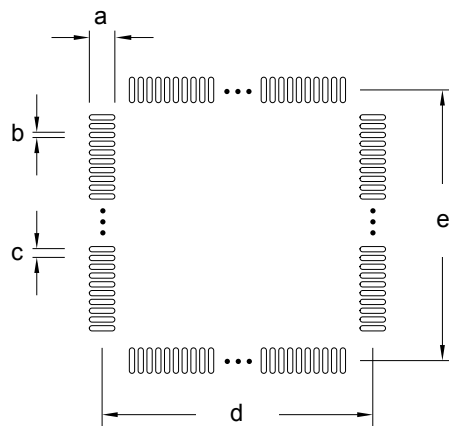


Figure 9.4. TQFP48 PCB Stencil Design

Table 9.4. TQFP48 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.50 |
| b | 0.20 |
| c | 0.50 |
| d | 8.50 |
| e | 8.50 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

9.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

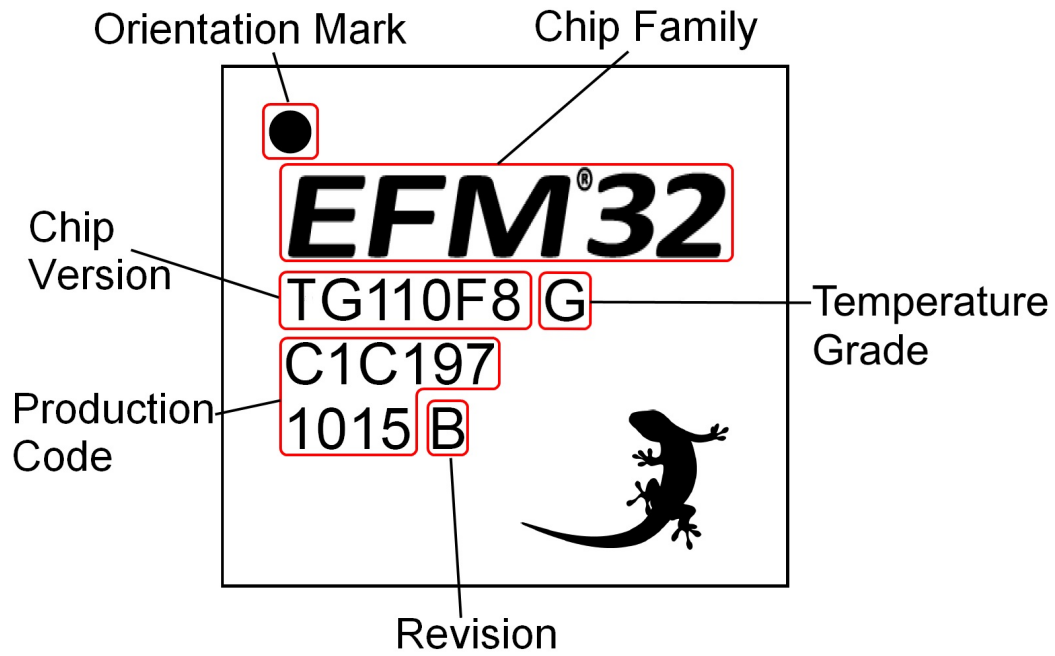
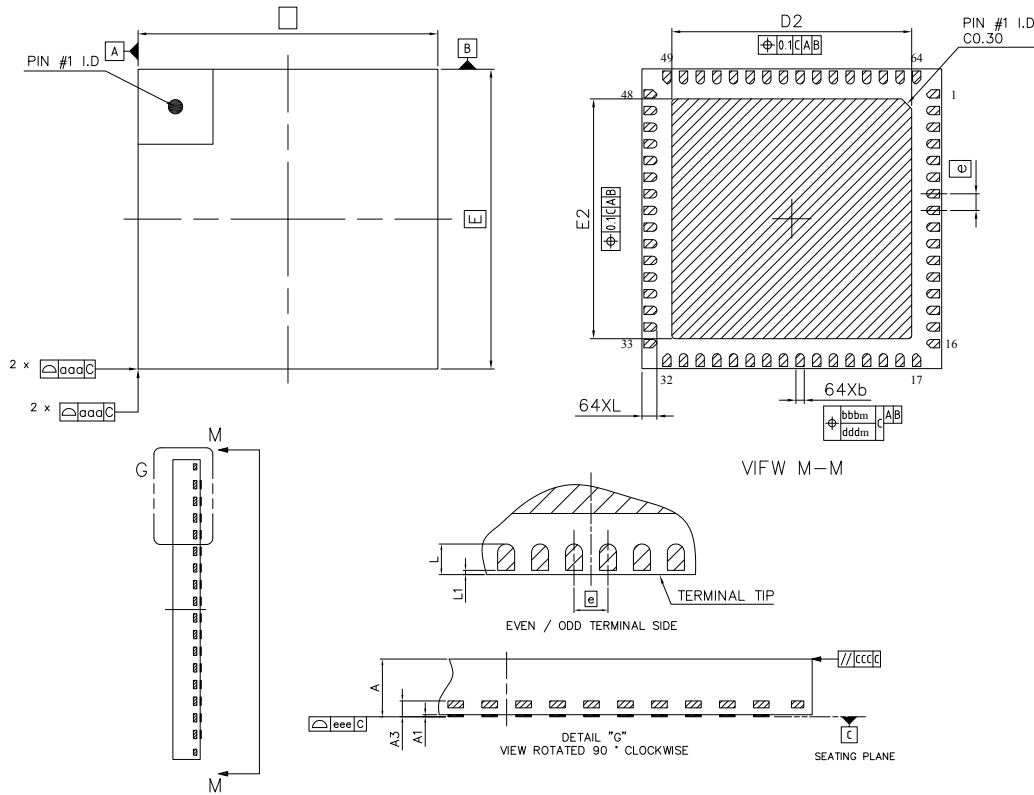


Figure 9.5. Example Chip Marking (Top View)

10. QFN64 Package Specifications

10.1 QFN64 Package Dimensions



Rev: 98SPR64048A_X01_08MAR2011

Figure 10.1. QFN64

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 10.1. QFN64 (Dimensions in mm)

| Symbol | Min | Nom | Max |
|--------|-----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | — | 0.05 |
| A3 | 0.203 REF | | |
| b | 0.25 | 0.30 | 0.35 |
| D | 9.00 BSC | | |
| E | 9.00 BSC | | |
| D2 | 7.10 | 7.20 | 7.30 |
| E2 | 7.10 | 7.20 | 7.30 |

| Symbol | Min | Nom | Max |
|--------|----------|------|------|
| e | 0.50 BSC | | |
| L | 0.40 | 0.45 | 0.50 |
| L1 | 0.00 | — | 0.10 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

10.2 QFN64 PCB Layout

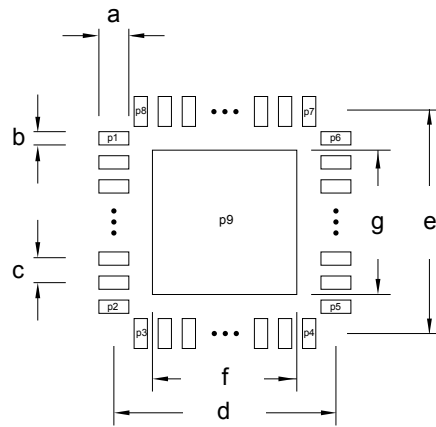


Figure 10.2. QFN64 PCB Land Pattern

Table 10.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 0.85 | P1 | 1 | P8 | 64 |
| b | 0.30 | P2 | 16 | P9 | 0 |
| c | 0.50 | P3 | 17 | | |
| d | 8.90 | P4 | 32 | | |
| e | 8.90 | P5 | 33 | | |
| f | 7.20 | P6 | 48 | | |
| g | 7.20 | P7 | 49 | | |

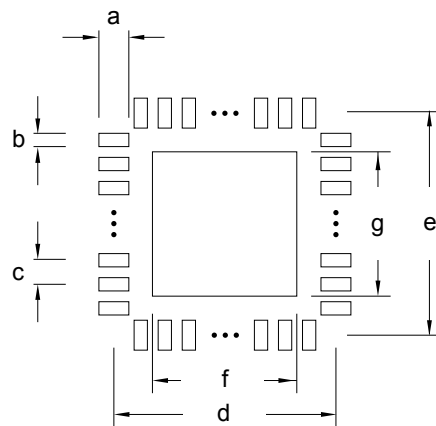


Figure 10.3. QFN64 PCB Solder Mask

Table 10.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|--------|-----------|--------|-----------|
| a | 0.97 | e | 8.90 |
| b | 0.42 | f | 7.32 |
| c | 0.50 | g | 7.32 |

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|--------|-----------|--------|-----------|
| d | 8.90 | - | - |



Figure 10.4. QFN64 PCB Stencil Design

Table 10.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|--------|-----------|--------|-----------|
| a | 0.75 | e | 8.90 |
| b | 0.22 | x | 2.70 |
| c | 0.50 | y | 2.70 |
| d | 8.90 | z | 0.80 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

10.3 QFN64 Package Marking

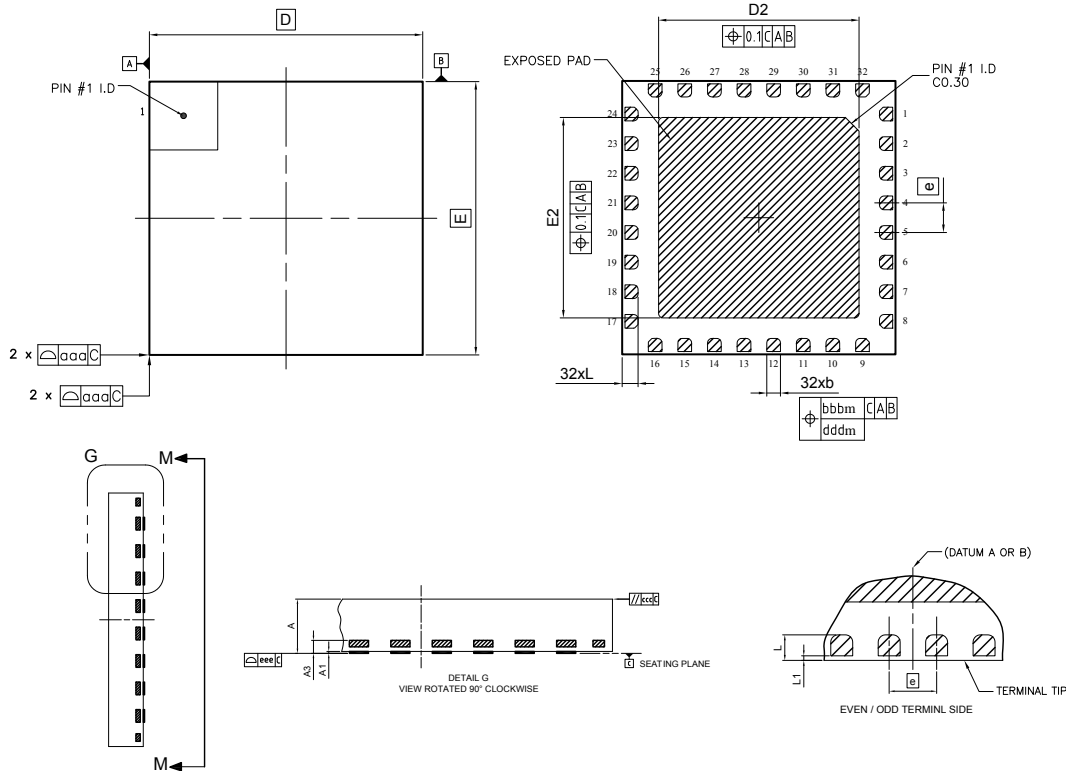
In the illustration below package fields and position are shown.



Figure 10.5. Example Chip Marking (Top View)

11. QFN32 Package Specifications

11.1 QFN32 Package Dimensions



Rev: 98SP2088A_X01_10MAR2011

Figure 11.1. QFN32

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 11.1. QFN32 (Dimensions in mm)

| Symbol | A | A1 | A3 | b | D | E | D2 | E2 | e | L | L1 | aaa | bbb | ccc | ddd | eee |
|--------|------|------|--------------|------|-------------|-------------|------|------|-------------|------|------|------|------|------|------|------|
| Min | 0.80 | 0.00 | 0.203 REF | 0.25 | 6.00 BSC | 6.00 BSC | 4.30 | 4.30 | 0.65 BSC | 0.30 | 0.00 | 0.10 | 0.10 | 0.10 | 0.05 | 0.08 |
| Nom | 0.85 | — | | 0.30 | | | 4.40 | 4.40 | | 0.35 | | | | | | |
| Max | 0.90 | 0.05 | | 0.35 | | | 4.50 | 4.50 | | 0.40 | 0.10 | | | | | |

The QFN32 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

11.2 QFN32 PCB Layout

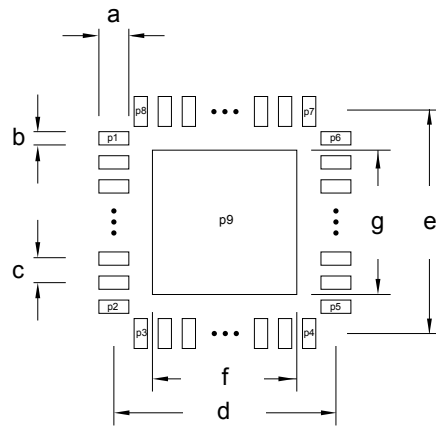


Figure 11.2. QFN32 PCB Land Pattern

Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 0.80 | P1 | 1 | P6 | 24 |
| b | 0.35 | P2 | 8 | P7 | 25 |
| c | 0.65 | P3 | 9 | P8 | 32 |
| d | 6.00 | P4 | 16 | P9 | 0 |
| e | 6.00 | P5 | 17 | | |
| f | 4.40 | | | | |
| g | 4.40 | | | | |

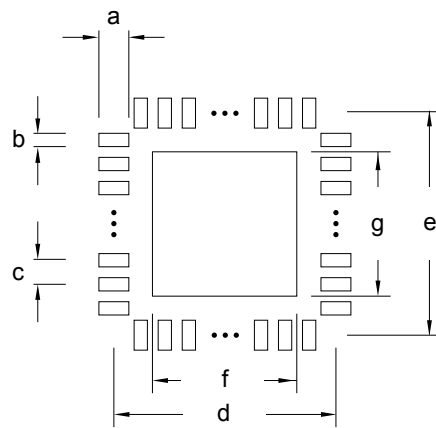


Figure 11.3. QFN32 PCB Solder Mask

Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.92 |
| b | 0.47 |
| c | 0.65 |

| Symbol | Dim. (mm) |
|--------|-----------|
| d | 6.00 |
| e | 6.00 |
| f | 4.52 |
| g | 4.52 |

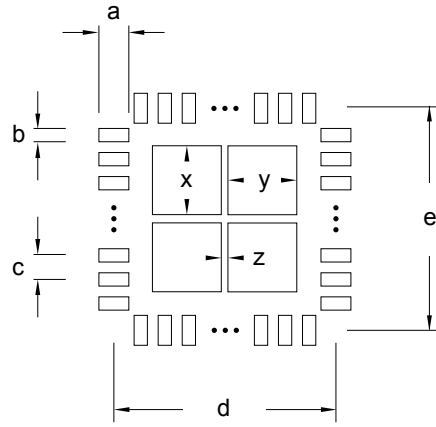


Figure 11.4. QFN32 PCB Stencil Design

Table 11.4. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.70 |
| b | 0.25 |
| c | 0.65 |
| d | 6.00 |
| e | 6.00 |
| x | 1.30 |
| y | 1.30 |
| z | 0.50 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

11.3 QFN32 Package Marking

In the illustration below package fields and position are shown.



Figure 11.5. Example Chip Marking (Top View)

12. Chip Revision, Solder Information, Errata

12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

12.3 Errata

See the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: <http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

13. Revision History

13.1 Revision 2.20

April, 2020

In [4.12 Analog Comparator \(ACMP\)](#):

- Corrected units for I_{ACMP} (BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register) from μA to nA.

In [4.10 Analog Digital Converter \(ADC\)](#):

- Input ON resistance (R_{ADCIN}) changed from 1 M Ω minimum to 300 Ω minimum and 800 Ω maximum.
- Added test conditions for missing codes specification (MC_{ADC}).

In [4.7 Flash](#):

- Added word write cycles between erase (WWC_{FLASH}) specification.

In [Table 5.7 Device Pinout on page 91](#) under [5.3 EFM32G230 \(QFN64\)](#):

- Communication functions on pins [12:11] (PC[3:2]) changed from US2_CS #0 and US2_CLK #0 to US2_RX #0 and US2_TX #0, respectively.

In [Table 5.10 Device Pinout on page 98](#) under [5.4 EFM32G232 \(TQFP64\)](#):

- Communication functions on pins [10:9] (PC[1:0]) changed from US1_RX #1 and US1_TX #1 to US1_RX #0 and US1_TX #0, respectively.
- Communication functions on pins [12:11] (PC[3:2]) changed from US1_CS #1 and US1_CLK #1 to US2_RX #0 and US2_TX #0, respectively.

In [6.1 BGA112 Package Dimensions](#):

- Removed statements regarding materials used.

In [10.2 QFN64 PCB Layout](#):

- Corrected pin number for symbol P9.

In [11.2 QFN32 PCB Layout](#):

- Corrected pin number for symbol P9.

13.2 Revision 2.10

July 19, 2017

In [4.8 General Purpose Input Output](#):

- Added missing multiply symbols.

In [4.10 Analog Digital Converter \(ADC\)](#):

- Updated average active current.
- Updated SNR.
- Updated SINAD.
- Updated SFDR.
- Renamed VREF Output Voltage to VREF Voltage.

In [4.11 Digital Analog Converter \(DAC\)](#):

- Renamed VREF Output Voltage to VREF Voltage.

13.3 Revision 2.00

May 10th, 2017

Consolidated all EFM32G data sheets:

- EFM32G200
- EFM32G210
- EFM32G222
- EFM32G230
- EFM32G232
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G842
- EFM32G880
- EFM32G890

New formatting throughout.

Added [1. Feature List](#).

Updated ordering codes in [2. Ordering Information](#) for Revision E and tape and reel.

Added [Figure 2.1 Ordering Code Decoder](#) on page 5.

Separated Memory Map figure into [Figure 3.2 System Address Space with Core and Code Space Listing](#) on page 27 and [Figure 3.3 System Address Space with Peripheral Listing](#) on page 28 for readability.

Removed footnote for storage temperature range in [4.2 Absolute Maximum Ratings](#).

In [4.6 Power Management](#):

- Updated EM0 condition for $V_{BODextthr-}$ specification.
- Added $V_{BODextthr-}$ in EM1 and EM2 specifications.
- Updated EM0 condition for $V_{BODextthr+}$ specification.

Updated Flash page erase time and device erase time in [4.7 Flash](#) and added footnotes.

Updated figures in [4.9.3 LFRCO](#).

Updated figures and HFRCO current consumption typical values in [4.9.4 HFRCO](#).

In [4.10 Analog Digital Converter \(ADC\)](#):

- Updated test conditions, updated specifications, and added footnote for average active current.
- Added input bias current.
- Added input offset current.
- Updated ADC clock frequency.
- Updated SNR, SINAD and SFDR.
- Updated offset voltage.
- Updated missing codes.
- Added gain error drift and offset error drift.
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

In [4.11 Digital Analog Converter \(DAC\)](#):

- Updated I_{DAC} parameter, test conditions, and footnote.
- Added DAC load current specification to [4.11 Digital Analog Converter \(DAC\)](#).
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

Updated ACMP active current (BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register) typical value in [4.12 Analog Comparator \(ACMP\)](#).

Updated VCMP hysteresis typical value in [4.13 Voltage Comparator \(VCMP\)](#).

Corrected pin number for symbol P3 in [Table 11.2 QFN32 PCB Land Pattern Dimensions \(Dimensions in mm\)](#) on page 191.

Updated package marking figures to include temperature grade.

13.4 Revision 1.90

May 22nd, 2015

For devices with an ADC, Added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated HFRCO table in the Electrical Characteristics section.

Updated EM0, EM2, EM3, and EM4 maximum current specifications in the Electrical Characteristics section.

Updated the Output Low Voltage maximum for sinking 20 mA with $VDD = 3.0$ V in the Electrical Characteristics section.

Updated the Input Leakage Current maximum in the Electrical Characteristics section.

Updated the minimum and maximum frequency specifications for the LFRCO, HFRCO, and AUXHFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Added some minimum ADC SNR, SNDR, and SFDR specifications in the Electrical Characteristics section.

Added some minimum and maximum ADC offset voltage, DNL, and INL specifications in the Electrical Characteristics section.

Added maximum DAC current specifications in the Electrical Characteristics section.

Added maximum ACMP current and maximum and minimum offset voltage specifications in the Electrical Characteristics section.

Added maximum VCMP current and updated typical VCMP current specifications in the Electrical Characteristics section.

Updated references to energyAware Designer to Configurator.

13.5 Revision 1.80

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

For devices with an ACMP, updated ACMP data.

13.6 Revision 1.71

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

For devices with a DAC, re-added missing DAC-data.

13.7 Revision 1.70

September 30th, 2013

For devices with an I2C, added I2C characterization data.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

For devices with an ADC, corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

For QFN64 devices, updated the Max V_{ESDCDM} value to 750 V.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

13.8 Revision 1.60

June 28th, 2013

For BGA devices, updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

13.9 Revision 1.50

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

For BGA devices, corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

Other minor corrections.

13.10 Revision 1.40

February 27th, 2012

Updated Power Management section.

Corrected operating voltage from 1.8 V to 1.85 V.

Corrected TGRAD_{ADCTH} parameter.

Corrected package drawing.

Updated PCB land pattern, solder mask and stencil design.

For LQFP48 devices, corrected available Pulse Counters from 3 to 2.

For LQFP48 devices, corrected available LEUARTs from 2 to 1.

For LQFP64 devices, corrected ordering codes in the ordering information table.

13.11 Revision 1.30

May 20th, 2011

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated LFXO load capacitance section.

13.12 Revision 1.20

December 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current.

For LQFP100 devices, updated ESD CDM value.

Added Flash current consumption.

Updated HFRCO data.

Updated LFRCO data.

Added graph for ADC Absolute Offset over temperature.

Added graph for ADC Temperature sensor readout.

13.13 Revision 1.11

November 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Corrected maximum DAC clock speed for continuous mode.

Added DAC sample-hold mode voltage drift rate.

Added pulse widths detected by the HFXO glitch detector.

Added power sequencing information to Power Management section.

13.14 Revision 1.10

September 13th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For LQFP100 devices, corrected number of GPIO pins.

Added typical values for R_{ADCFILT} and C_{ADCFILT} .

Added two conditions for DAC clock frequency; one for sample/hold and one for sample/off.

Added RoHS information and specified leadframe/solderballs material.

Added Serial Bootloader to feature list and system summary.

Updated ADC characterization data.

Updated DAC characterization data.

Updated RCO characterization data.

Updated ACMP characterization data.

Updated VCMP characterization data.

13.15 Revision 1.00

April 23rd, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

ADC_VCM line removed.

Added pinout illustration and additional pinout table.

Changed "Errata" chapter. Errata description moved to separate document.

Document changed status from "Preliminary".

Updated "Electrical Characteristics" chapter.

For EFM32G222

May 20th, 2011

Updated LFXO load capacitance section.

13.16 Revision 0.90

This revision applies the following devices:

- EFM32G222

Initial preliminary revision, April 14th, 2011

This revision applies the following devices:

- EFM32G232
- EFM32G842

Initial preliminary revision, June 30th, 2011

13.17 Revision 0.85

February 19th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Renamed DBG_SWV pin to DBG_SWO.

13.18 Revision 0.84

February 11th, 2010

This revision applies the following devices:

- EFM32G230
- EFM32G840

Corrected pinout tables.

13.19 Revision 0.83

January 25th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated errata section.

Specified flash word width in Flash Electrical Characteristics.

Added Capacitive Sense Internal Resistor values in ACMP Electrical Characteristics.

13.20 Revision 0.82

December 9th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For LQFP100 devices, incorrect pin 0 removed from pinout table.

Updated contact information.

ADC current consumption numbers updated in ADC Electrical Characteristics.

For devices with LCD, updated LCD supply voltage range in LCD Electrical Characteristics.

13.21 Revision 0.81

November 20th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For devices without a differential DAC, System Summary updated.

Electrical Characteristics updated.

Storage temperature in Electrical Characteristics updated.

Temperature coefficient of band-gap reference in Electrical Characteristics added.

Erase times in Flash Electrical Characteristics updated.

Definitions of DNL and INL added in ADC section.

For devices with and LCD, LCD Electrical Characteristics added.

Current consumption of digital peripherals added in Electrical Characteristics.

For LQFP100 devices, package information in Pinout and Package corrected.

For BGA112 devices, pinout information in Pinout table corrected.

Updated errata section.

13.22 Revision 0.80

October 19th, 2009

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Initial preliminary revision