

EFM32 Giant Gecko Series 1 Family

EFM32GG12 Family Data Sheet



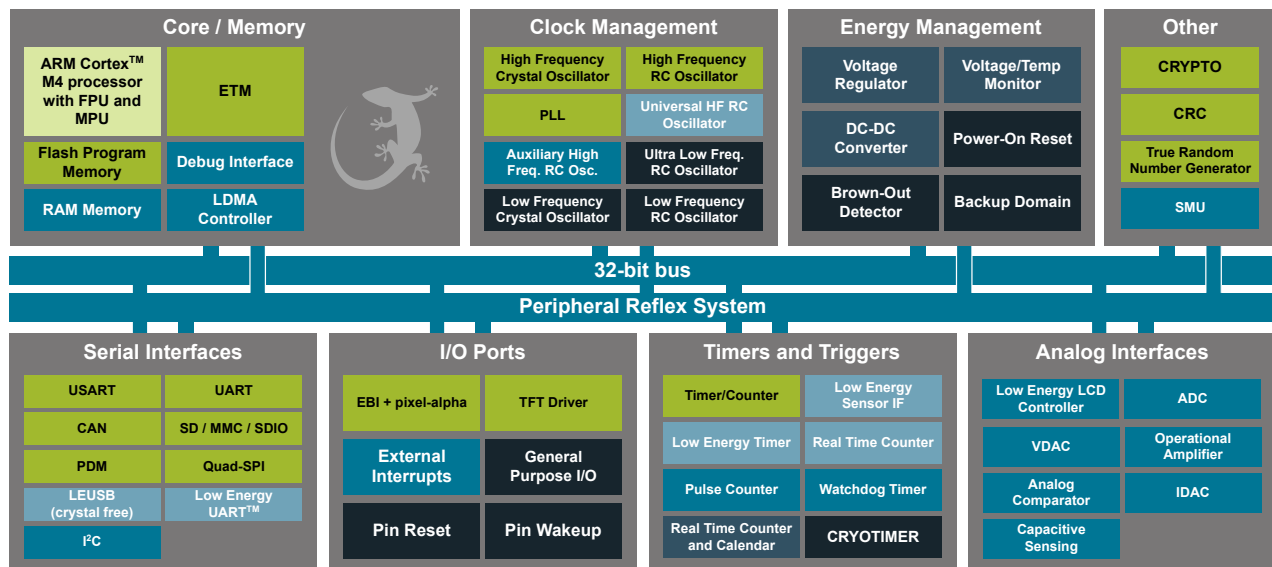
The EFM32 Giant Gecko Series 1 MCUs are the world's most energy-friendly microcontrollers, featuring new connectivity interfaces and user interface features.

EFM32GG12 includes a powerful 32-bit ARM® Cortex®-M4 and provides robust security via a unique cryptographic hardware engine supporting AES, ECC, SHA, and True Random Number Generator (TRNG). New features include an SD/MMC/SDIO controller, Octal/Quad-SPI memory controller, CAN bus controller, PDM interface, highly robust capacitive sensing, enhanced alpha blending graphics engine, and LESENSE/PCNT enhancements for smart energy meters. These features, combined with ultra-low current active mode and short wake-up time from energy-saving modes, make EFM32GG12 microcontrollers well suited for any battery-powered application, as well as other systems requiring high performance and low-energy consumption.

Example applications:

- Smart energy meters
- Industrial and factory automation
- Home automation and security
- Mid- and high-tier wearables
- IoT devices

- ARM Cortex-M4 at 72 MHz
- Ultra low energy operation
 - 76 μ A/MHz in Energy Mode 0 (EM0)
 - 1.8 μ A EM2 Deep Sleep current (RTCC running with state and RAM retention)
- Octal/Quad-SPI memory interface w/ XIP
- SD/MMC/SDIO Host Controller
- PDM Microphone/Sensor Interface
- Dual CAN 2.0 Bus Controller
- Crystal-free low-energy USB
- Hardware cryptographic engine supports AES, ECC, SHA, and TRNG
- Robust capacitive touch sense
- Footprint compatible with select EFM32 packages
- 5 V tolerant I/O



Lowest power mode with peripheral operational:

- EM0 - Active
- EM1 - Sleep
- EM2 - Deep Sleep
- EM3 - Stop
- EM4H - Hibernate
- EM4S - Shutoff

1. Feature List

The EFM32GG12 highlighted features are listed below.

- **ARM Cortex-M4 CPU Platform**
 - High performance 32-bit processor @ up to 72 MHz
 - DSP instruction support and Floating Point Unit
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 76 μ A/MHz in Active Mode (EM0)
 - 1.8 μ A EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC Buck Converter**
- **Up to 1024 kB Flash Program Memory**
 - Dual-bank with read-while-write support
- **192 kB RAM Data Memory**
 - Includes ECC (SEC-DED)
- **Octal/Quad-SPI Flash Memory Interface**
 - Supports 3 V and 1.8 V memories
 - 1/2/4/8-bit data bus
 - Quad-SPI Execute In Place (XIP)
- **Communication Interfaces**
 - Low-energy Universal Serial Bus (USB) with Device and Host support
 - Fully USB 2.0 compliant
 - On-chip PHY and embedded 5 V to 3.3 V regulator
 - Crystal-free Device mode operation
 - Patent-pending Low-Energy Mode (LEM)
 - SD/MMC/SDIO Host Controller
 - SD v3.01, SDIO v3.0 and MMC v4.51
 - 1/4/8-bit bus width
 - Up to 2 \times CAN Bus Controller
 - Version 2.0A and 2.0B up to 1 Mbps
 - 5 \times Universal Synchronous/Asynchronous Receiver/Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Ultra high speed (36 MHz) operation on one instance
 - 2 \times Universal Asynchronous Receiver/Transmitter
 - 2 \times Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - 2 \times I²C Interface with SMBus support
 - Address recognition in EM3 Stop Mode
- **Up to 95 General Purpose I/O Pins**
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 5 V tolerance on select pins
 - Asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- **Up to 12 Channel DMA Controller**
- **Up to 16 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 4x256 MB of external memory mapped space**
 - TFT Controller with Direct Drive
 - Per-pixel alpha-blending engine
- **Hardware Cryptography**
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True Random Number Generator (TRNG)
- **Hardware CRC Engine**
 - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
 - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 \times 36 segments**
 - Voltage boost, contrast and autonomous animation
 - Patented low-energy LCD driver
- **Backup Power Domain**
 - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
 - Operation from backup battery when main power absent/insufficient
- **Ultra Low-Power Precision Analog Peripherals**
 - 2 \times 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
 - On-chip temperature sensor
 - 2 \times 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
 - Digital to Analog Current Converter (IDAC)
 - Up to 3 \times Analog Comparator (ACMP)
 - Up to 4 \times Operational Amplifier (OPAMP)
 - Robust current-based capacitive sensing with wake-on-touch (CSEN)
 - Up to 83 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
 - Supply Voltage Monitor

- **Timers/Counters**
 - 4× 16-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
 - Dead-Time Insertion on two timer instances
 - 2× 32-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
 - Dead-Time Insertion on one timer instance
 - 32-bit Real Time Counter and Calendar (RTCC)
 - 24-bit Real Time Counter (RTC)
 - 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
 - 2× 16-bit Low Energy Timer for waveform generation
 - 3× 16-bit Pulse Counter with asynchronous operation
 - 2× Watchdog Timer with dedicated RC oscillator
- **Low Energy Sensor Interface (LESENSE)**
 - Autonomous sensor monitoring in Deep Sleep Mode
 - Wide range of sensors supported, including LC sensors and capacitive buttons
 - Up to 16 inputs
- **Ultra Efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
 - 2-pin Serial Wire Debug interface
 - 1-pin Serial Wire Viewer
 - 4-pin JTAG interface
 - Embedded Trace Macrocell (ETM)
- **Pre-Programmed Bootloader**
- **Wide Operating Range**
 - 1.8 V to 3.8 V single power supply
 - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
 - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
 - QFN64 (9x9 mm)
 - TQFP64 (10x10 mm)
 - TQFP100 (14x14 mm)
 - BGA112 (10x10 mm)
 - BGA120 (7x7 mm)

2. Ordering Information

Table 2.1. Ordering Information

| Ordering Code | Flash (kB) | RAM (kB) | DC-DC Converter | USB | QSPI | SDIO | LCD | GPIO | Package | Temp Range |
|---------------------------|------------|----------|-----------------|-----|------|------|-----|------|---------|---------------|
| EFM32GG12B810F1024GL120-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 95 | BGA120 | -40 to +85°C |
| EFM32GG12B810F1024IL120-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 95 | BGA120 | -40 to +125°C |
| EFM32GG12B830F512GL120-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 95 | BGA120 | -40 to +85°C |
| EFM32GG12B830F512IL120-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 95 | BGA120 | -40 to +125°C |
| EFM32GG12B810F1024GL112-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 89 | BGA112 | -40 to +85°C |
| EFM32GG12B810F1024IL112-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 89 | BGA112 | -40 to +125°C |
| EFM32GG12B830F512GL112-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 89 | BGA112 | -40 to +85°C |
| EFM32GG12B830F512IL112-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 89 | BGA112 | -40 to +125°C |
| EFM32GG12B810F1024GQ100-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 81 | QFP100 | -40 to +85°C |
| EFM32GG12B810F1024IQ100-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 81 | QFP100 | -40 to +125°C |
| EFM32GG12B830F512GQ100-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 81 | QFP100 | -40 to +85°C |
| EFM32GG12B830F512IQ100-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 81 | QFP100 | -40 to +125°C |
| EFM32GG12B810F1024GM64-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 51 | QFN64 | -40 to +85°C |
| EFM32GG12B810F1024GQ64-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 48 | QFP64 | -40 to +85°C |
| EFM32GG12B810F1024IM64-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 51 | QFN64 | -40 to +125°C |
| EFM32GG12B810F1024IQ64-A | 1024 | 192 | Yes | Yes | Yes | Yes | Yes | 48 | QFP64 | -40 to +125°C |
| EFM32GG12B830F512GM64-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 51 | QFN64 | -40 to +85°C |
| EFM32GG12B830F512GQ64-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 48 | QFP64 | -40 to +85°C |
| EFM32GG12B830F512IM64-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 51 | QFN64 | -40 to +125°C |
| EFM32GG12B830F512IQ64-A | 512 | 192 | Yes | Yes | Yes | Yes | Yes | 48 | QFP64 | -40 to +125°C |
| EFM32GG12B510F1024GL120-A | 1024 | 192 | Yes | No | No | No | Yes | 95 | BGA120 | -40 to +85°C |
| EFM32GG12B510F1024IL120-A | 1024 | 192 | Yes | No | No | No | Yes | 95 | BGA120 | -40 to +125°C |
| EFM32GG12B530F512GL120-A | 512 | 192 | Yes | No | No | No | Yes | 95 | BGA120 | -40 to +85°C |
| EFM32GG12B530F512IL120-A | 512 | 192 | Yes | No | No | No | Yes | 95 | BGA120 | -40 to +125°C |
| EFM32GG12B510F1024GL112-A | 1024 | 192 | Yes | No | No | No | Yes | 92 | BGA112 | -40 to +85°C |
| EFM32GG12B510F1024IL112-A | 1024 | 192 | Yes | No | No | No | Yes | 92 | BGA112 | -40 to +125°C |
| EFM32GG12B530F512GL112-A | 512 | 192 | Yes | No | No | No | Yes | 92 | BGA112 | -40 to +85°C |
| EFM32GG12B530F512IL112-A | 512 | 192 | Yes | No | No | No | Yes | 92 | BGA112 | -40 to +125°C |
| EFM32GG12B510F1024GQ100-A | 1024 | 192 | Yes | No | No | No | Yes | 81 | QFP100 | -40 to +85°C |
| EFM32GG12B510F1024IQ100-A | 1024 | 192 | Yes | No | No | No | Yes | 81 | QFP100 | -40 to +125°C |

| Ordering Code | Flash (kB) | RAM (kB) | DC-DC Converter | USB | QSPI | SDIO | LCD | GPIO | Package | Temp Range |
|---------------------------|------------|----------|-----------------|-----|------|------|-----|------|---------|---------------|
| EFM32GG12B530F512GQ100-A | 512 | 192 | Yes | No | No | No | Yes | 81 | QFP100 | -40 to +85°C |
| EFM32GG12B530F512IQ100-A | 512 | 192 | Yes | No | No | No | Yes | 81 | QFP100 | -40 to +125°C |
| EFM32GG12B510F1024GM64-A | 1024 | 192 | Yes | No | No | No | Yes | 54 | QFN64 | -40 to +85°C |
| EFM32GG12B510F1024GQ64-A | 1024 | 192 | Yes | No | No | No | Yes | 51 | QFP64 | -40 to +85°C |
| EFM32GG12B510F1024IM64-A | 1024 | 192 | Yes | No | No | No | Yes | 54 | QFN64 | -40 to +125°C |
| EFM32GG12B510F1024IQ64-A | 1024 | 192 | Yes | No | No | No | Yes | 51 | QFP64 | -40 to +125°C |
| EFM32GG12B530F512GM64-A | 512 | 192 | Yes | No | No | No | Yes | 54 | QFN64 | -40 to +85°C |
| EFM32GG12B530F512GQ64-A | 512 | 192 | Yes | No | No | No | Yes | 51 | QFP64 | -40 to +85°C |
| EFM32GG12B530F512IM64-A | 512 | 192 | Yes | No | No | No | Yes | 54 | QFN64 | -40 to +125°C |
| EFM32GG12B530F512IQ64-A | 512 | 192 | Yes | No | No | No | Yes | 51 | QFP64 | -40 to +125°C |
| EFM32GG12B410F1024GL120-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 93 | BGA120 | -40 to +85°C |
| EFM32GG12B410F1024IL120-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 93 | BGA120 | -40 to +125°C |
| EFM32GG12B430F512GL120-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 93 | BGA120 | -40 to +85°C |
| EFM32GG12B430F512IL120-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 93 | BGA120 | -40 to +125°C |
| EFM32GG12B410F1024GL112-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 87 | BGA112 | -40 to +85°C |
| EFM32GG12B410F1024IL112-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 87 | BGA112 | -40 to +125°C |
| EFM32GG12B430F512GL112-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 87 | BGA112 | -40 to +85°C |
| EFM32GG12B430F512IL112-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 87 | BGA112 | -40 to +125°C |
| EFM32GG12B410F1024GQ100-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 83 | QFP100 | -40 to +85°C |
| EFM32GG12B410F1024IQ100-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 83 | QFP100 | -40 to +125°C |
| EFM32GG12B430F512GQ100-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 83 | QFP100 | -40 to +85°C |
| EFM32GG12B430F512IQ100-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 83 | QFP100 | -40 to +125°C |
| EFM32GG12B410F1024GM64-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 53 | QFN64 | -40 to +85°C |
| EFM32GG12B410F1024GQ64-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 50 | QFP64 | -40 to +85°C |
| EFM32GG12B410F1024IM64-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 53 | QFN64 | -40 to +125°C |
| EFM32GG12B410F1024IQ64-A | 1024 | 192 | No | Yes | Yes | Yes | Yes | 50 | QFP64 | -40 to +125°C |
| EFM32GG12B430F512GM64-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 53 | QFN64 | -40 to +85°C |
| EFM32GG12B430F512GQ64-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 50 | QFP64 | -40 to +85°C |
| EFM32GG12B430F512IM64-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 53 | QFN64 | -40 to +125°C |
| EFM32GG12B430F512IQ64-A | 512 | 192 | No | Yes | Yes | Yes | Yes | 50 | QFP64 | -40 to +125°C |
| EFM32GG12B310F1024GL112-A | 1024 | 192 | No | No | No | No | Yes | 90 | BGA112 | -40 to +85°C |
| EFM32GG12B330F512GL112-A | 512 | 192 | No | No | No | No | Yes | 90 | BGA112 | -40 to +85°C |
| EFM32GG12B310F1024GQ100-A | 1024 | 192 | No | No | No | No | Yes | 86 | QFP100 | -40 to +85°C |
| EFM32GG12B330F512GQ100-A | 512 | 192 | No | No | No | No | Yes | 86 | QFP100 | -40 to +85°C |

| Ordering Code | Flash (kB) | RAM (kB) | DC-DC Converter | USB | QSPI | SDIO | LCD | GPIO | Package | Temp Range |
|--------------------------|------------|----------|-----------------|-----|------|------|-----|------|---------|---------------|
| EFM32GG12B110F1024GM64-A | 1024 | 192 | No | No | No | No | No | 56 | QFN64 | -40 to +85°C |
| EFM32GG12B110F1024GQ64-A | 1024 | 192 | No | No | No | No | No | 53 | QFP64 | -40 to +85°C |
| EFM32GG12B110F1024IM64-A | 1024 | 192 | No | No | No | No | No | 56 | QFN64 | -40 to +125°C |
| EFM32GG12B110F1024IQ64-A | 1024 | 192 | No | No | No | No | No | 53 | QFP64 | -40 to +125°C |
| EFM32GG12B130F512GM64-A | 512 | 192 | No | No | No | No | No | 56 | QFN64 | -40 to +85°C |
| EFM32GG12B130F512GQ64-A | 512 | 192 | No | No | No | No | No | 53 | QFP64 | -40 to +85°C |
| EFM32GG12B130F512IM64-A | 512 | 192 | No | No | No | No | No | 56 | QFN64 | -40 to +125°C |
| EFM32GG12B130F512IQ64-A | 512 | 192 | No | No | No | No | No | 53 | QFP64 | -40 to +125°C |



Figure 2.1. Ordering Code Key

Table of Contents

| | |
|---|-----------|
| 1. Feature List | 2 |
| 2. Ordering Information | 4 |
| 3. System Overview | 11 |
| 3.1 Introduction | 11 |
| 3.2 Power | 12 |
| 3.2.1 Energy Management Unit (EMU) | 12 |
| 3.2.2 DC-DC Converter | 12 |
| 3.2.3 5 V Regulator | 12 |
| 3.2.4 EM2 and EM3 Power Domains | 13 |
| 3.3 General Purpose Input/Output (GPIO) | 13 |
| 3.4 Clocking | 13 |
| 3.4.1 Clock Management Unit (CMU) | 13 |
| 3.4.2 Internal and External Oscillators | 14 |
| 3.5 Counters/Timers and PWM | 14 |
| 3.5.1 Timer/Counter (TIMER) | 14 |
| 3.5.2 Wide Timer/Counter (WTIMER) | 14 |
| 3.5.3 Real Time Counter and Calendar (RTCC) | 14 |
| 3.5.4 Low Energy Timer (LETIMER) | 14 |
| 3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER) | 14 |
| 3.5.6 Pulse Counter (PCNT) | 15 |
| 3.5.7 Watchdog Timer (WDOG) | 15 |
| 3.6 Communications and Other Digital Peripherals | 15 |
| 3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) | 15 |
| 3.6.2 Universal Asynchronous Receiver/Transmitter (UART) | 15 |
| 3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART) | 15 |
| 3.6.4 Inter-Integrated Circuit Interface (I ² C) | 15 |
| 3.6.5 External Bus Interface (EBI) | 15 |
| 3.6.6 Quad-SPI Flash Controller (QSPI) | 16 |
| 3.6.7 SDIO Host Controller (SDIO) | 16 |
| 3.6.8 Universal Serial Bus (USB) | 16 |
| 3.6.9 Controller Area Network (CAN) | 16 |
| 3.6.10 Peripheral Reflex System (PRS) | 16 |
| 3.6.11 Low Energy Sensor Interface (LESENSE) | 16 |
| 3.6.12 Pulse Density Modulation (PDM) Interface | 16 |
| 3.7 Security Features | 17 |
| 3.7.1 General Purpose Cyclic Redundancy Check (GPCRC) | 17 |
| 3.7.2 Crypto Accelerator (CRYPTO) | 17 |
| 3.7.3 True Random Number Generator (TRNG) | 17 |
| 3.7.4 Security Management Unit (SMU) | 17 |
| 3.8 Analog | 17 |
| 3.8.1 Analog Port (APORT) | 17 |
| 3.8.2 Analog Comparator (ACMP) | 17 |
| 3.8.3 Analog to Digital Converter (ADC) | 17 |

| | | |
|-----------|---|------------|
| 3.8.4 | Capacitive Sense (CSEN) | .18 |
| 3.8.5 | Digital to Analog Current Converter (IDAC) | .18 |
| 3.8.6 | Digital to Analog Converter (VDAC) | .18 |
| 3.8.7 | Operational Amplifiers | .18 |
| 3.8.8 | Liquid Crystal Display Driver (LCD) | .18 |
| 3.9 | Reset Management Unit (RMU) | .18 |
| 3.10 | Core and Memory | .18 |
| 3.10.1 | Processor Core | .18 |
| 3.10.2 | Memory System Controller (MSC) | .19 |
| 3.10.3 | Linked Direct Memory Access Controller (LDMA) | .19 |
| 3.10.4 | Bootloader | .19 |
| 3.11 | Memory Map | .20 |
| 3.12 | Configuration Summary | .22 |
| 4. | Electrical Specifications | .23 |
| 4.1 | Electrical Characteristics | .23 |
| 4.1.1 | Absolute Maximum Ratings | .24 |
| 4.1.2 | Operating Conditions | .25 |
| 4.1.3 | Thermal Characteristics | .27 |
| 4.1.4 | DC-DC Converter | .28 |
| 4.1.5 | 5V Regulator | .30 |
| 4.1.6 | Backup Supply Domain | .31 |
| 4.1.7 | Current Consumption | .32 |
| 4.1.8 | Wake Up Times | .39 |
| 4.1.9 | Brown Out Detector (BOD) | .40 |
| 4.1.10 | Oscillators | .41 |
| 4.1.11 | Flash Memory Characteristics | .48 |
| 4.1.12 | General-Purpose I/O (GPIO) | .49 |
| 4.1.13 | Voltage Monitor (VMON) | .51 |
| 4.1.14 | Analog to Digital Converter (ADC) | .52 |
| 4.1.15 | Analog Comparator (ACMP) | .54 |
| 4.1.16 | Digital to Analog Converter (VDAC) | .57 |
| 4.1.17 | Current Digital to Analog Converter (IDAC) | .60 |
| 4.1.18 | Capacitive Sense (CSEN) | .62 |
| 4.1.19 | Operational Amplifier (OPAMP) | .64 |
| 4.1.20 | LCD Driver | .67 |
| 4.1.21 | Pulse Counter (PCNT) | .68 |
| 4.1.22 | Analog Port (APORT) | .68 |
| 4.1.23 | I2C | .69 |
| 4.1.24 | USART SPI | .72 |
| 4.1.25 | External Bus Interface (EBI) | .75 |
| 4.1.26 | Serial Data I/O Host Controller (SDIO) | .84 |
| 4.1.27 | Quad SPI (QSPI) | .103 |
| 4.1.28 | PDM | .108 |
| 4.2 | Typical Performance Curves | .108 |
| 4.2.1 | Supply Current | .109 |
| 4.2.2 | DC-DC Converter | .115 |

| | |
|--|------------|
| 5. Pin Definitions | 117 |
| 5.1 EFM32GG12B8xx in BGA120 Device Pinout | 117 |
| 5.2 EFM32GG12B5xx in BGA120 Device Pinout | 120 |
| 5.3 EFM32GG12B4xx in BGA120 Device Pinout | 123 |
| 5.4 EFM32GG12B8xx in BGA112 Device Pinout | 126 |
| 5.5 EFM32GG12B5xx in BGA112 Device Pinout | 129 |
| 5.6 EFM32GG12B4xx in BGA112 Device Pinout | 132 |
| 5.7 EFM32GG12B3xx in BGA112 Device Pinout | 135 |
| 5.8 EFM32GG12B8xx in QFP100 Device Pinout | 138 |
| 5.9 EFM32GG12B5xx in QFP100 Device Pinout | 141 |
| 5.10 EFM32GG12B4xx in QFP100 Device Pinout | 144 |
| 5.11 EFM32GG12B3xx in QFP100 Device Pinout | 147 |
| 5.12 EFM32GG12B8xx in QFP64 Device Pinout | 150 |
| 5.13 EFM32GG12B5xx in QFP64 Device Pinout | 152 |
| 5.14 EFM32GG12B4xx in QFP64 Device Pinout | 154 |
| 5.15 EFM32GG12B1xx in QFP64 Device Pinout | 156 |
| 5.16 EFM32GG12B8xx in QFN64 Device Pinout | 158 |
| 5.17 EFM32GG12B5xx in QFN64 Device Pinout | 160 |
| 5.18 EFM32GG12B4xx in QFN64 Device Pinout | 162 |
| 5.19 EFM32GG12B1xx in QFN64 Device Pinout | 164 |
| 5.20 GPIO Functionality Table | 166 |
| 5.21 Alternate Functionality Overview | 178 |
| 5.22 Analog Port (APORT) Client Maps | 204 |
| 6. BGA120 Package Specifications | 216 |
| 6.1 BGA120 Package Dimensions | 216 |
| 6.2 BGA120 PCB Land Pattern | 218 |
| 6.3 BGA120 Package Marking | 220 |
| 7. BGA112 Package Specifications | 221 |
| 7.1 BGA112 Package Dimensions | 221 |
| 7.2 BGA112 PCB Land Pattern | 223 |
| 7.3 BGA112 Package Marking | 225 |
| 8. TQFP100 Package Specifications | 226 |
| 8.1 TQFP100 Package Dimensions | 226 |
| 8.2 TQFP100 PCB Land Pattern | 228 |
| 8.3 TQFP100 Package Marking | 229 |
| 9. TQFP64 Package Specifications | 230 |
| 9.1 TQFP64 Package Dimensions | 230 |

| | |
|---|------------|
| 9.2 TQFP64 PCB Land Pattern | 232 |
| 9.3 TQFP64 Package Marking | 233 |
| 10. QFN64 Package Specifications | 234 |
| 10.1 QFN64 Package Dimensions. | 234 |
| 10.2 QFN64 PCB Land Pattern. | 236 |
| 10.3 QFN64 Package Marking | 238 |
| 11. Revision History. | 239 |

3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in [Figure 3.1 Detailed EFM32GG12 Block Diagram on page 11](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

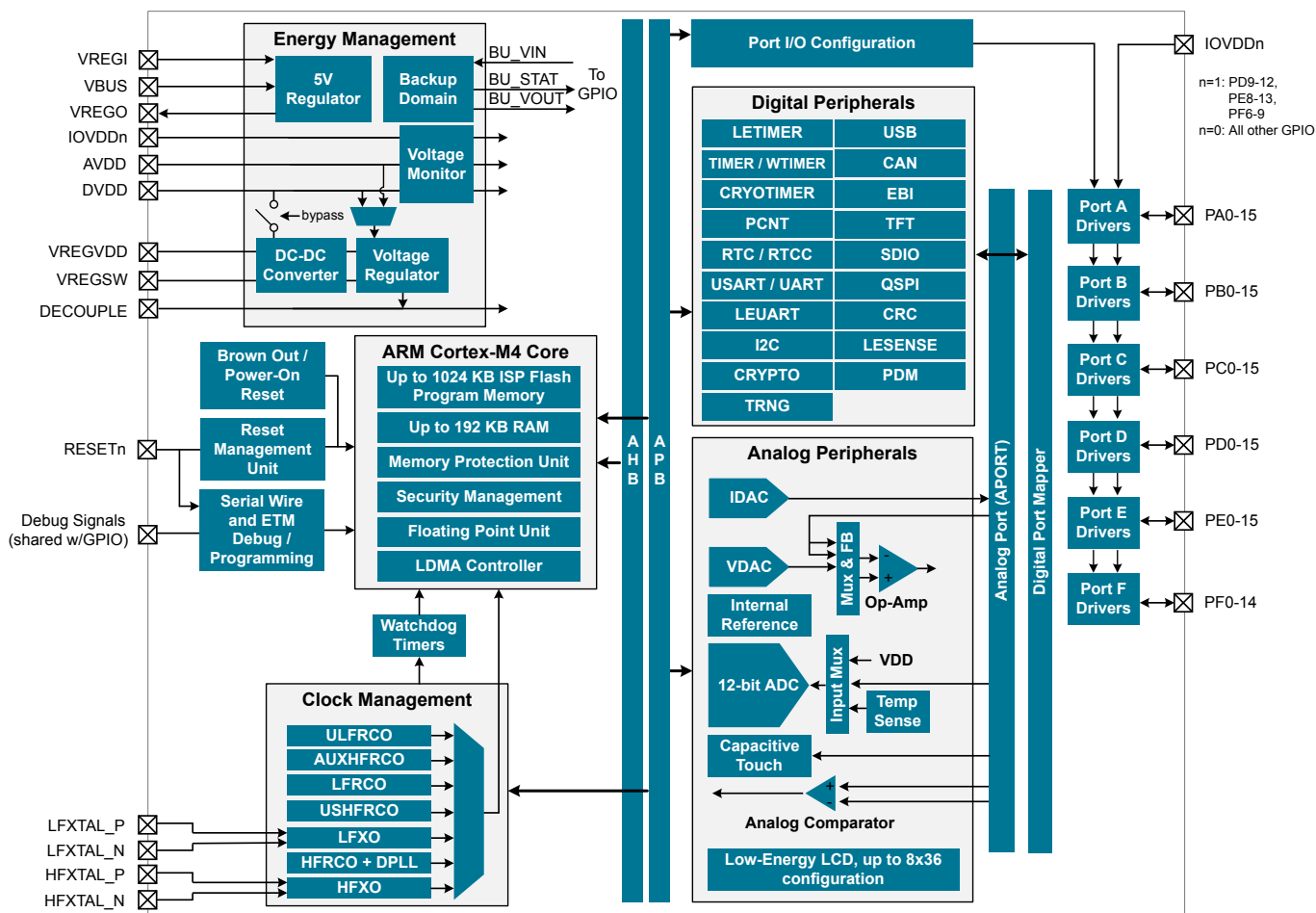


Figure 3.1. Detailed EFM32GG12 Block Diagram

3.2 Power

The EFM32GG12 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG12 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

3.2.4 EM2 and EM3 Power Domains

The EFM32GG12 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in [Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 13](#). If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

| Peripheral Power Domain 1 | Peripheral Power Domain 2 |
|---------------------------|---------------------------|
| ACMP0 | ACMP1 |
| PCNT0 | PCNT1 |
| ADC0 | PCNT2 |
| LETIMER0 | CSEN |
| LESENSE | VDAC0 |
| APOINT | LEUART0 |
| - | LEUART1 |
| - | LETIMER1 |
| - | I2C0 |
| - | I2C1 |
| - | IDAC |
| - | ADC1 |
| - | ACMP2 |
| - | LCD |
| - | RTC |

3.3 General Purpose Input/Output (GPIO)

EFM32GG12 has up to 95 General Purpose Input/Output pins. GPIO are organized on three independent supply rails, allowing for interface to multiple logic levels in the system simultaneously. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32GG12. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32GG12 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated universal high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be synchronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The peripheral may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART peripheral, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I²C)

The I²C interface enables communication between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C peripheral allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.5 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices. The interface is memory mapped into the address bus of the Cortex-M4. This enables seamless access from software without manually manipulating the I/O settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface to external devices. Timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

The EBI contains a TFT controller which can drive a TFT via an RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

3.6.6 Quad-SPI Flash Controller (QSPI)

The QSPI provides access to a wide range of flash devices with wide I/O busses. The I/O and clocking configuration is flexible and supports many types of devices. Up to 8-bit wide interfaces are supported. The QSPI handles opcodes, status flag polling, and timing configuration automatically.

The external flash memory is mapped directly to internal memory to allow random access to any word in the flash and direct code execution. An integrated instruction cache minimizes latency and allows efficient code execution. Execute in Place (XIP) is supported for devices with this feature.

Large data chunks can be transferred with DMA as efficiently as possible with high throughput and minimal bus load, utilizing an integrated 1 kB SRAM FIFO.

3.6.7 SDIO Host Controller (SDIO)

The SDIO is an SD3.01 / SDIO3.0 / eMMC4.51-compliant Host Controller interface for transferring data to and from SD/MMC/SDIO devices. The module conforms to the SD Host Controller Standard Specification Version 3.00. The Host Controller handles SDIO/SD/MMC Protocol at the transmission level, packing data, adding cyclic redundancy check (CRC), Start/End bits, and checking for transaction format correctness.

3.6.8 Universal Serial Bus (USB)

The USB is a full-speed/low-speed USB 2.0 compliant host/device controller. The USB can be used in device and host-only configurations, while a clock recovery mechanism allows crystal-less operation in device mode. The USB block supports both full speed (12 MBit/s) and low speed (1.5 MBit/s) operation. When operating as a device, a special Low Energy Mode ensures the current consumption is optimized, enabling USB communications on a strict power budget. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes internal pull-up and pull-down resistors, as well as voltage comparators for monitoring the VBUS voltage and A/B device identification using the ID line.

3.6.9 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmission may be disabled in order to support Time Triggered CAN applications.

3.6.10 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.11 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.6.12 Pulse Density Modulation (PDM) Interface

The PDM module provides a serial interface and decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-delta ADCs, digital sensors and other PDM or sigma delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports multiple channels of stereo or mono input data and DMA transfer.

3.7 Security Features

3.7.1 General Purpose Cyclic Redundancy Check (GPCRC)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Giant Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO peripheral allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN peripheral is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN peripheral uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The peripheral can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC peripheral or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.8 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32GG12. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor with FPU achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 1024 kB flash program memory
 - Dual-bank memory with read-while-write support
- Up to 192 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire or 4-pin JTAG debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the **[Documentation]** area.

3.11 Memory Map

The EFM32GG12 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

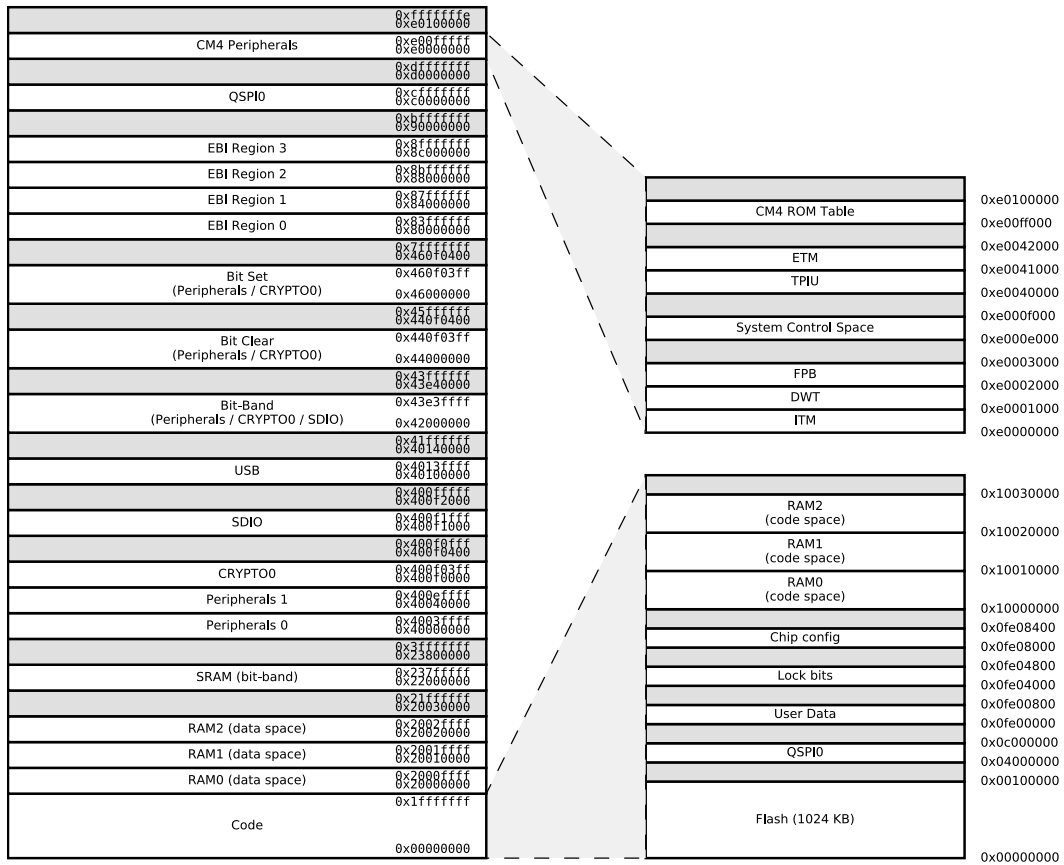


Figure 3.2. EFM32GG12 Memory Map — Core Peripherals and Code Space

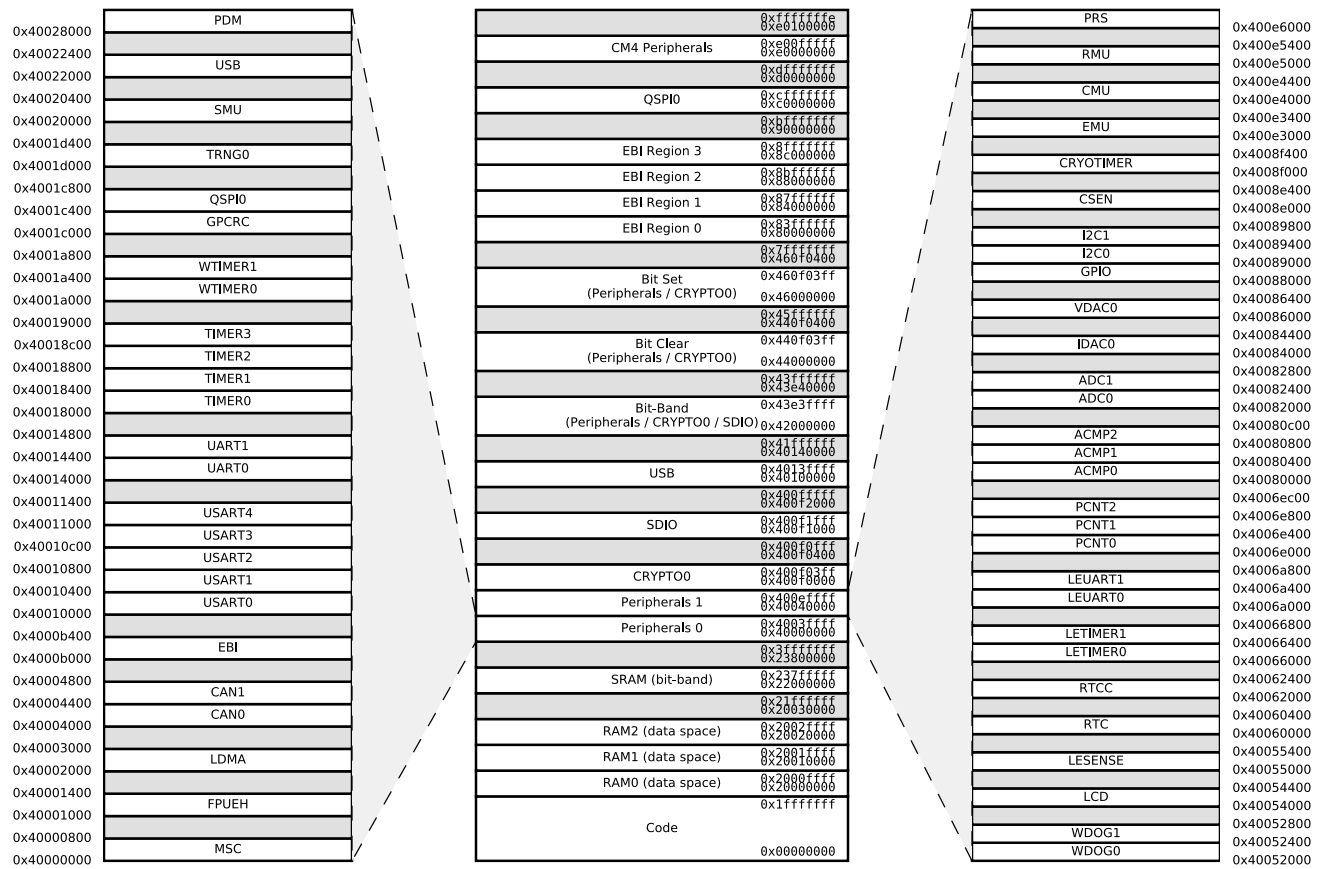


Figure 3.3. EFM32GG12 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32GG12 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining peripherals support full configuration.

Table 3.2. Configuration Summary

| Module | Configuration | Pin Connections |
|---------|-----------------------------|---------------------------------|
| USART0 | IrDA, SmartCard | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | I ² S, SmartCard | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | IrDA, SmartCard, High-Speed | US2_TX, US2_RX, US2_CLK, US2_CS |
| USART3 | I ² S, SmartCard | US3_TX, US3_RX, US3_CLK, US3_CS |
| USART4 | I ² S, SmartCard | US4_TX, US4_RX, US4_CLK, US4_CS |
| TIMER0 | with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | - | TIM1_CC[3:0] |
| TIMER2 | with DTI | TIM2_CC[2:0], TIM2_CDTI[2:0] |
| TIMER3 | - | TIM3_CC[2:0] |
| WTIMER0 | with DTI | WTIM0_CC[2:0], WTIM0_CDTI[2:0] |
| WTIMER1 | - | WTIM1_CC[3:0] |

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25\text{ }^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to [4.1.2.1 General Operating Conditions](#) for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|--|------|-----|--------------------------|-------------|
| Storage temperature range | T _{STG} | | -50 | — | 150 | °C |
| Voltage on supply pins other than VREGI and VBUS | V _{DDMAX} | | -0.3 | — | 3.8 | V |
| Voltage ramp rate on any supply pin | V _{DDRAMPMAX} | | — | — | 1 | V / μ s |
| DC voltage on any GPIO pin | V _{DIGPIN} | 5V tolerant GPIO pins ^{1 2 3} | -0.3 | — | Min of 5.25 and IOVDD +2 | V |
| | | LCD pins ³ | -0.3 | — | Min of 3.8 and IOVDD +2 | V |
| | | Standard GPIO pins | -0.3 | — | IOVDD+0.3 | V |
| Total current into VDD power lines | I _{VDDMAX} | Source | — | — | 200 | mA |
| Total current into VSS ground lines | I _{VSSMAX} | Sink | — | — | 200 | mA |
| Current per I/O pin | I _{IOMAX} | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | I _{IOALLMAX} | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |
| Junction temperature | T _J | -G grade devices | -40 | — | 105 | °C |
| | | -I grade devices | -40 | — | 125 | °C |
| Voltage on regulator supply pins VREGI and VBUS | V _{VREGI} | | -0.3 | — | 5.5 | V |

Note:

1. When a GPIO pin is routed to the analog block through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD \leq AVDD
- IOVDD \leq AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|---|------|-----|----------------------|------|
| Operating ambient temperature range ¹ | T _A | -G temperature grade | -40 | 25 | 85 | °C |
| | | -I temperature grade | -40 | 25 | 125 | °C |
| AVDD supply voltage ² | V _{AVDD} | | 1.8 | 3.3 | 3.8 | V |
| VREGVDD operating supply voltage ^{2 3} | V _{VREGVDD} | DCDC in regulation | 2.4 | 3.3 | 3.8 | V |
| | | DCDC in bypass, 50mA load | 1.8 | 3.3 | 3.8 | V |
| | | DCDC not in use. DVDD externally shorted to VREGVDD | 1.8 | 3.3 | 3.8 | V |
| VREGVDD current | I _{VREGVDD} | DCDC in bypass, T ≤ 85 °C | — | — | 200 | mA |
| | | DCDC in bypass, T > 85 °C | — | — | 100 | mA |
| DVDD operating supply voltage | V _{DVDD} | | 1.62 | — | V _{VREGVDD} | V |
| IOVDD operating supply voltage | V _{IOVDD} | All IOVDD pins ⁴ | 1.62 | — | V _{VREGVDD} | V |
| DECOUPLE output capacitor ^{5 6} | C _{DECOUPLE} | | 0.75 | 1.0 | 2.75 | μF |
| HFCORECLK frequency | f _{CORE} | VSCALE2, MODE = WS3 | — | — | 72 | MHz |
| | | VSCALE2, MODE = WS2 | — | — | 54 | MHz |
| | | VSCALE2, MODE = WS1 | — | — | 36 | MHz |
| | | VSCALE2, MODE = WS0 | — | — | 18 | MHz |
| | | VSCALE0, MODE = WS2 | — | — | 20 | MHz |
| | | VSCALE0, MODE = WS1 | — | — | 14 | MHz |
| | | VSCALE0, MODE = WS0 | — | — | 7 | MHz |
| HFCLK frequency | f _{HFCLK} | VSCALE2 | — | — | 72 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |
| HFSRCCLK frequency | f _{HFSRCCLK} | VSCALE2 | — | — | 72 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |
| HFBUSCLK frequency | f _{HFBUSCLK} | VSCALE2 | — | — | 50 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |
| HFPERCLK frequency | f _{HFPERCLK} | VSCALE2 | — | — | 50 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |
| HFPERBCLK frequency | f _{HFPERBCLK} | VSCALE2 | — | — | 72 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |
| HFPERCCLK frequency | f _{HFPERCCLK} | VSCALE2 | — | — | 50 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($\text{THETA}_{JA} \times \text{PowerDissipation}$). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and THETA_{JA} . | | | | | | |
| 2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate. | | | | | | |
| 3. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD_min} + I_{LOAD} * R_{BYP_max}$. | | | | | | |
| 4. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD. | | | | | | |
| 5. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias. | | | | | | |
| 6. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μ F capacitor) to 70 mA (with a 2.7 μ F capacitor). | | | | | | |

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|--------------------------------------|-----------------------------------|-----|------|-----|-----------------------------|
| Thermal resistance, QFN64 Package | THETA_{JA_QFN64} | 4-Layer PCB, Air velocity = 0 m/s | — | 17.8 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 15.4 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 13.8 | — | $^{\circ}\text{C}/\text{W}$ |
| Thermal resistance, TQFP64 Package | $\text{THE-}\text{TA}_{JA_TQFP64}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 33.9 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 32.1 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 30.1 | — | $^{\circ}\text{C}/\text{W}$ |
| Thermal resistance, TQFP100 Package | $\text{THE-}\text{TA}_{JA_TQFP100}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 44.1 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 37.7 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 35.5 | — | $^{\circ}\text{C}/\text{W}$ |
| Thermal resistance, BGA112 Package | $\text{THE-}\text{TA}_{JA_BGA112}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 42.0 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 37.0 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 35.3 | — | $^{\circ}\text{C}/\text{W}$ |
| Thermal resistance, BGA120 Package | $\text{THE-}\text{TA}_{JA_BGA120}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 47.9 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 41.8 | — | $^{\circ}\text{C}/\text{W}$ |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 39.6 | — | $^{\circ}\text{C}/\text{W}$ |

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 μ H (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 μ F (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|--|------|-----|--------------------------|------------------|
| Input voltage range | V _{DCDC_I} | Bypass mode, I _{DCDC_LOAD} = 50 mA | 1.8 | — | V _{VREGVDD_MAX} | V |
| | | Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I _{DCDC_LOAD} = 10 mA | 2.4 | — | V _{VREGVDD_MAX} | V |
| | | Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 200 mA | 2.6 | — | V _{VREGVDD_MAX} | V |
| Output voltage programmable range ¹ | V _{DCDC_O} | | 1.8 | — | V _{VREGVDD} | V |
| Regulation DC accuracy | ACC _{DC} | Low Noise (LN) mode, 1.8 V target output | 1.7 | — | 1.9 | V |
| Regulation window ² | WIN _{REG} | Low Power (LP) mode, LPCMPBIASEM _{xx} ³ = 0, 1.8 V target output, I _{DCDC_LOAD} \leq 75 μ A | 1.63 | — | 2.2 | V |
| | | Low Power (LP) mode, LPCMPBIASEM _{xx} ³ = 3, 1.8 V target output, I _{DCDC_LOAD} \leq 10 mA | 1.63 | — | 2.1 | V |
| Steady-state output ripple | V _R | | — | 3 | — | mV _{pp} |
| Output voltage under/overshoot | V _{OV} | CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA | — | 25 | 60 | mV |
| | | DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA | — | 45 | 90 | mV |
| | | Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode | — | 200 | — | mV |
| | | Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode | — | 40 | — | mV |
| | | Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode | — | 100 | — | mV |
| DC line regulation | V _{REG} | Input changes between V _{VREGVDD_MAX} and 2.4 V | — | 0.1 | — | % |
| DC load regulation | I _{REG} | Load changes between 0 mA and 100 mA in CCM mode | — | 0.1 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------|---|-----|-----|-----|------|
| Max load current | I _{LOAD_MAX} | Low noise (LN) mode, Heavy Drive ⁴ , T ≤ 85 °C | — | — | 200 | mA |
| | | Low noise (LN) mode, Heavy Drive ⁴ , T > 85 °C | — | — | 100 | mA |
| | | Low noise (LN) mode, Medium Drive ⁴ | — | — | 100 | mA |
| | | Low noise (LN) mode, Light Drive ⁴ | — | — | 50 | mA |
| | | Low power (LP) mode, LPCMPBIASEMxx ³ = 0 | — | — | 75 | μA |
| | | Low power (LP) mode, LPCMPBIASEMxx ³ = 3 | — | — | 10 | mA |
| DCDC nominal output capacitor ⁵ | C _{DCDC} | 25% tolerance | 1 | 4.7 | 4.7 | μF |
| DCDC nominal output inductor | L _{DCDC} | 20% tolerance | 4.7 | 4.7 | 4.7 | μH |
| Resistance in Bypass mode | R _{BYP} | | — | 1.2 | 2.5 | Ω |

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{REGVDD}.
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF. See Application Note AN0948 for details.

4.1.5 5V Regulator

$V_{VREGI} = 5\text{ V}$, $V_{VREGO} = 3.3\text{ V}$, $C_{VREGI} = 10\text{ }\mu\text{F}$, $C_{VREGO} = 4.7\text{ }\mu\text{F}$, unless otherwise specified.

Table 4.5. 5V Regulator

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------------|---|-----|------|------|---------------|
| VREGI or VBUS input voltage range | V_{VREGI} | Regulating output | 2.7 | — | 5.5 | V |
| | | Bypass mode enabled | 2.7 | — | 3.8 | V |
| VREGO output voltage | V_{VREGO} | Regulating output, 3.3 V setting ¹ | 3.1 | 3.3 | 3.5 | V |
| | | EM4S open-loop output, $I_{OUT} < 100\text{ }\mu\text{A}$ | 1.8 | — | 3.8 | V |
| Voltage output step size | V_{VREGO_SS} | | — | 0.1 | — | V |
| Resistance in Bypass Mode | R_{BYP} | Bypass mode enabled | — | 1.2 | 2.5 | Ω |
| Output current | I_{OUT} | EM0 or EM1, $V_{VREGI} > V_{VREGO} + 0.6\text{ V}$ | — | — | 200 | mA |
| | | EM0 or EM1, $V_{VREGI} > V_{VREGO} + 0.3\text{ V}$ | — | — | 100 | mA |
| | | EM2, EM3, or EM4H, $V_{VREGI} > V_{VREGO} + 0.6\text{ V}$ | — | — | 2 | mA |
| | | EM2, EM3, or EM4H, $V_{VREGI} > V_{VREGO} + 0.3\text{ V}$ | — | — | 0.5 | mA |
| | | EM4S | — | — | 20 | μA |
| Load regulation | LR_{VREGO} | EM0 or EM1 | — | 0.10 | — | mV/mA |
| | | EM2, EM3, or EM4H | — | 2.5 | — | mV/mA |
| DC power supply rejection | PSR_{DC} | | — | 40 | — | dB |
| VREGI or VBUS bypass capacitance | C_{VREGI} | | — | 10 | — | μF |
| VREGO bypass capacitance | C_{VREGO} | | 1 | 4.7 | 10 | μF |
| Supply current consumption | I_{VREGI} | EM0 or EM1, No load | — | 29 | — | μA |
| | | EM2, EM3, or EM4H, No load | — | 270 | — | nA |
| | | EM4S, No load | — | 70 | — | nA |
| VREGI and VBUS detection high threshold | V_{DET_H} | | 0.9 | 1.15 | — | V |
| VREGI and VBUS detection low threshold | V_{DET_L} | | — | 1.07 | 1.45 | V |
| Current monitor transfer ratio | $IMON_{XF}$ | Translation of current through VREGO path to voltage at ADC input | — | 0.35 | — | mA/mV |

Note:

- Output may be disturbed during DCDC mode transitions from BYPASS or OFF mode to LOWNOISE mode. Perturbation on VREGO can temporarily bring VREGO up beyond 3.5 V during these DCDC mode transitions. Refer to the EFM32GG12 Errata document, item EMU_E219 for more details.

4.1.6 Backup Supply Domain

Table 4.6. Backup Supply Domain

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|------|------|------|----------|
| Backup supply voltage range | V_{BU_VIN} | | 1.8 | — | 3.8 | V |
| PWRRES resistor | R_{PWRRES} | EMU_BUCTRL_PWRRES = RES0 | 3400 | 3900 | 4400 | Ω |
| | | EMU_BUCTRL_PWRRES = RES1 | 1450 | 1800 | 2150 | Ω |
| | | EMU_BUCTRL_PWRRES = RES2 | 1000 | 1350 | 1700 | Ω |
| | | EMU_BUCTRL_PWRRES = RES3 | 525 | 815 | 1100 | Ω |
| Output impedance between BU_VIN and BU_VOUT ¹ | R_{BU_VOUT} | EMU_BUCTRL_VOUTRES = STRONG | 35 | 110 | 185 | Ω |
| | | EMU_BUCTRL_VOUTRES = MED | 475 | 775 | 1075 | Ω |
| | | EMU_BUCTRL_VOUTRES = WEAK | 5600 | 6500 | 7400 | Ω |
| Supply current | I_{BU_VIN} | BU_VIN not powering backup domain, 25 °C | — | 11 | 70 | nA |
| | | BU_VIN powering backup domain, 25 °C ² | — | 550 | 2500 | nA |

Note:

1. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.
2. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.

4.1.7 Current Consumption

4.1.7.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.7. Current Consumption 3.3 V without DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|--|-----|-----|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled | I _{ACTIVE} | 72 MHz HFRCO, CPU running Prime from flash | — | 113 | — | μA/MHz |
| | | 72 MHz HFRCO, CPU running while loop from flash | — | 112 | 125 | μA/MHz |
| | | 72 MHz HFRCO, CPU running CoreMark loop from flash | — | 128 | — | μA/MHz |
| | | 50 MHz crystal, CPU running while loop from flash | — | 110 | — | μA/MHz |
| | | 48 MHz HFRCO, CPU running while loop from flash | — | 113 | 130 | μA/MHz |
| | | 32 MHz HFRCO, CPU running while loop from flash | — | 115 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 116 | 135 | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 122 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 308 | 400 | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled | I _{ACTIVE_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 99 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 255 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | I _{EM1} | 72 MHz HFRCO | — | 51 | 57 | μA/MHz |
| | | 50 MHz crystal | — | 49 | — | μA/MHz |
| | | 48 MHz HFRCO | — | 51 | 60 | μA/MHz |
| | | 32 MHz HFRCO | — | 54 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 55 | 64 | μA/MHz |
| | | 16 MHz HFRCO | — | 60 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 246 | 350 | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled | I _{EM1_VS} | 19 MHz HFRCO | — | 49 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 204 | — | μA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|---|-----|------|------|------|
| Current consumption in EM2 mode, with voltage scaling enabled | I _{EM2_VS} | Full 192 kB RAM retention and RTCC running from LFXO | — | 3.0 | — | μA |
| | | Full 192 kB RAM retention and RTCC running from LFRCO | — | 3.4 | — | μA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO ¹ | — | 2.4 | 4.7 | μA |
| Current consumption in EM3 mode, with voltage scaling enabled | I _{EM3_VS} | Full 192 kB RAM retention and CRYOTIMER running from ULFRCO | — | 2.7 | 7 | μA |
| Current consumption in EM4H mode, with voltage scaling enabled | I _{EM4H_VS} | 128 byte RAM retention, RTCC running from LFXO | — | 0.94 | — | μA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.59 | — | μA |
| | | 128 byte RAM retention, no RTCC | — | 0.59 | 1.15 | μA |
| Current consumption in EM4S mode | I _{EM4S} | No RAM retention, no RTCC | — | 0.08 | 0.16 | μA |
| Current consumption of peripheral power domain 1, with voltage scaling enabled | I _{PD1_VS} | Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ² | — | 0.73 | — | μA |
| Current consumption of peripheral power domain 2, with voltage scaling enabled | I _{PD2_VS} | Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ² | — | 0.32 | — | μA |

Note:

1. CMU_LFRCCOCTRL_ENVREF = 1, CMU_LFRCCOCTRL_VREFUPDATE = 1
2. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.4 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.

4.1.7.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.8. Current Consumption 3.3 V using DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|--|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹ | I _{ACTIVE_DCM} | 72 MHz HFRCO, CPU running Prime from flash | — | 76 | — | μA/MHz |
| | | 72 MHz HFRCO, CPU running while loop from flash | — | 75 | — | μA/MHz |
| | | 72 MHz HFRCO, CPU running CoreMark loop from flash | — | 85 | — | μA/MHz |
| | | 50 MHz crystal, CPU running while loop from flash | — | 76 | — | μA/MHz |
| | | 48 MHz HFRCO, CPU running while loop from flash | — | 78 | — | μA/MHz |
| | | 32 MHz HFRCO, CPU running while loop from flash | — | 85 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 89 | — | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 104 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 686 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode ² | I _{ACTIVE_CCM} | 72 MHz HFRCO, CPU running Prime from flash | — | 80 | — | μA/MHz |
| | | 72 MHz HFRCO, CPU running while loop from flash | — | 79 | — | μA/MHz |
| | | 72 MHz HFRCO, CPU running CoreMark loop from flash | — | 89 | — | μA/MHz |
| | | 50 MHz crystal, CPU running while loop from flash | — | 84 | — | μA/MHz |
| | | 48 MHz HFRCO, CPU running while loop from flash | — | 87 | — | μA/MHz |
| | | 32 MHz HFRCO, CPU running while loop from flash | — | 100 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 109 | — | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 139 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1290 | — | μA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode ³ | I _{ACTIVE_LPM} | 32 MHz HFRCO, CPU running while loop from flash | — | 76 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 77 | — | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 82 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 257 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ² | I _{ACTIVE_CCM_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 115 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1259 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode ³ | I _{ACTIVE_LPM_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 67 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 214 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹ | I _{EM1_DCM} | 72 MHz HFRCO | — | 38 | — | μA/MHz |
| | | 50 MHz crystal | — | 39 | — | μA/MHz |
| | | 48 MHz HFRCO | — | 42 | — | μA/MHz |
| | | 32 MHz HFRCO | — | 48 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 53 | — | μA/MHz |
| | | 16 MHz HFRCO | — | 68 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 652 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode ³ | I _{EM1_LPM} | 32 MHz HFRCO | — | 37 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 39 | — | μA/MHz |
| | | 16 MHz HFRCO | — | 43 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 209 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ¹ | I _{EM1_DCM_VS} | 19 MHz HFRCO | — | 56 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 627 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode ³ | I _{EM1_LPM_VS} | 19 MHz HFRCO | — | 35 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 185 | — | μA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode ³ | I _{EM2_VS} | Full 192 kB RAM retention and RTCC running from LFXO | — | 2.2 | — | μA |
| | | Full 192 kB RAM retention and RTCC running from LFRCO | — | 2.5 | — | μA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO ⁴ | — | 1.8 | — | μA |
| Current consumption in EM3 mode, with voltage scaling enabled | I _{EM3_VS} | Full 192 kB RAM retention and CRYOTIMER running from ULFR-CO | — | 1.9 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|---|-----|------|-----|------|
| Current consumption in EM4H mode, with voltage scaling enabled | I _{EM4H_VS} | 128 byte RAM retention, RTCC running from LFXO | — | 0.86 | — | μA |
| | | 128 byte RAM retention, CRYO-TIMER running from ULFRCO | — | 0.55 | — | μA |
| | | 128 byte RAM retention, no RTCC | — | 0.55 | — | μA |
| Current consumption in EM4S mode | I _{EM4S} | No RAM retention, no RTCC | — | 0.08 | — | μA |
| Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode ³ | I _{PD1_VS} | Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ⁵ | — | 0.76 | — | μA |
| Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode ³ | I _{PD2_VS} | Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ⁵ | — | 0.32 | — | μA |

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
2. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive, LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMLIMSEL=1, ANASW=DVDD.
4. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1
5. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.4 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.

4.1.7.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.9. Current Consumption 1.8 V without DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|---|-----|-----|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled | I _{ACTIVE} | 72 MHz HFRCO, CPU running Prime from flash | — | 113 | — | μA/MHz |
| | | 72 MHz HFRCO, CPU running while loop from flash | — | 112 | — | μA/MHz |
| | | 72 MHz HFRCO, CPU running CoreMark loop from flash | — | 128 | — | μA/MHz |
| | | 50 MHz crystal, CPU running while loop from flash | — | 110 | — | μA/MHz |
| | | 48 MHz HFRCO, CPU running while loop from flash | — | 112 | — | μA/MHz |
| | | 32 MHz HFRCO, CPU running while loop from flash | — | 115 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 116 | — | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 122 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 304 | — | μA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled | I _{ACTIVE_VS} | 19 MHz HFRCO, CPU running while loop from flash | — | 99 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 251 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | I _{EM1} | 72 MHz HFRCO | — | 51 | — | μA/MHz |
| | | 50 MHz crystal | — | 49 | — | μA/MHz |
| | | 48 MHz HFRCO | — | 51 | — | μA/MHz |
| | | 32 MHz HFRCO | — | 53 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 55 | — | μA/MHz |
| | | 16 MHz HFRCO | — | 60 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 242 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled | I _{EM1_VS} | 19 MHz HFRCO | — | 49 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 201 | — | μA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled | I _{EM2_VS} | Full 192 kB RAM retention and RTCC running from LFXO | — | 2.9 | — | μA |
| | | Full 192 kB RAM retention and RTCC running from LFRCO | — | 3.1 | — | μA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO ¹ | — | 2.1 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|-----|------|-----|---------------|
| Current consumption in EM3 mode, with voltage scaling enabled | I_{EM3_VS} | Full 192 kB RAM retention and CRYOTIMER running from ULFRCO | — | 2.6 | — | μA |
| Current consumption in EM4H mode, with voltage scaling enabled | I_{EM4H_VS} | 128 byte RAM retention, RTCC running from LFXO | — | 0.85 | — | μA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.48 | — | μA |
| | | 128 byte RAM retention, no RTCC | — | 0.48 | — | μA |
| Current consumption in EM4S mode | I_{EM4S} | No RAM retention, no RTCC | — | 0.06 | — | μA |
| Current consumption of peripheral power domain 1, with voltage scaling enabled | I_{PD1_VS} | Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ² | — | 0.75 | — | μA |
| Current consumption of peripheral power domain 2, with voltage scaling enabled | I_{PD2_VS} | Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ² | — | 0.32 | — | μA |

Note:

1. $CMU_LFRCOCTRL_ENVREF = 1$, $CMU_LFRCOCTRL_VREFUPDATE = 1$
2. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.4 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.

4.1.8 Wake Up Times

Table 4.10. Wake Up Times

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|-----|------|-----|---------------|
| Wake up time from EM1 | t_{EM1_WU} | | — | 3 | — | AHB Clocks |
| Wake up from EM2 | t_{EM2_WU} | Code execution from flash | — | 11.4 | — | μs |
| | | Code execution from RAM | — | 3.8 | — | μs |
| Wake up from EM3 | t_{EM3_WU} | Code execution from flash | — | 11.4 | — | μs |
| | | Code execution from RAM | — | 3.8 | — | μs |
| Wake up from EM4H ¹ | t_{EM4H_WU} | Executing from flash | — | 92 | — | μs |
| Wake up from EM4S ¹ | t_{EM4S_WU} | Executing from flash | — | 288 | — | μs |
| Time from release of reset source to first instruction execution | t_{RESET} | Soft Pin Reset released | — | 53 | — | μs |
| | | Any other reset released | — | 347 | — | μs |
| Power mode scaling time | t_{SCALE} | VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{2 3} | — | 31.8 | — | μs |
| | | VSCALE2 to VSCALE0, HFCLK = 19 MHz ⁴ | — | 4.3 | — | μs |

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. Scaling up from VSCALE0 to VSCALE2 requires approximately $30.3 \mu\text{s} + 28 \text{ HFCLKs}$.
3. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of $10 \text{ mV}/\mu\text{s}$ for approximately $20 \mu\text{s}$. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a $1 \mu\text{F}$ capacitor) to 70 mA (with a $2.7 \mu\text{F}$ capacitor).
4. Scaling down from VSCALE2 to VSCALE0 requires approximately $2.8 \mu\text{s} + 29 \text{ HFCLKs}$.

4.1.9 Brown Out Detector (BOD)

Table 4.11. Brown Out Detector (BOD)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------|----------------------------|------------------------------|------|-----|------|------|
| DVDD BOD threshold | V _{DVddbod} | DVDD rising | — | — | 1.62 | V |
| | | DVDD falling (EM0/EM1) | 1.35 | — | — | V |
| | | DVDD falling (EM2/EM3) | 1.3 | — | — | V |
| DVDD BOD hysteresis | V _{DVddbod_hyst} | | — | 18 | — | mV |
| DVDD BOD response time | t _{DVddbod_delay} | Supply drops at 0.1V/μs rate | — | 2.4 | — | μs |
| AVDD BOD threshold | V _{AVddbod} | AVDD rising | — | — | 1.8 | V |
| | | AVDD falling (EM0/EM1) | 1.62 | — | — | V |
| | | AVDD falling (EM2/EM3) | 1.53 | — | — | V |
| AVDD BOD hysteresis | V _{AVddbod_hyst} | | — | 20 | — | mV |
| AVDD BOD response time | t _{AVddbod_delay} | Supply drops at 0.1V/μs rate | — | 2.4 | — | μs |
| EM4 BOD threshold | V _{EM4dbod} | AVDD rising | — | — | 1.7 | V |
| | | AVDD falling | 1.45 | — | — | V |
| EM4 BOD hysteresis | V _{EM4bod_hyst} | | — | 25 | — | mV |
| EM4 BOD response time | t _{EM4bod_delay} | Supply drops at 0.1V/μs rate | — | 300 | — | μs |

4.1.10 Oscillators

4.1.10.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.12. Low-Frequency Crystal Oscillator (LFXO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|-----|--------|-----|------------|
| Crystal frequency | f_{LFXO} | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{LFXO} | | — | — | 70 | k Ω |
| Supported range of crystal load capacitance ¹ | C_{LFXO_CL} | | 6 | — | 18 | pF |
| On-chip tuning cap range ² | C_{LFXO_T} | On each of LFX TAL_N and LFX TAL_P pins | 8 | — | 40 | pF |
| On-chip tuning cap step size | SS_{LFXO} | | — | 0.25 | — | pF |
| Current consumption after startup ³ | I_{LFXO} | ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 2, AGC ⁴ = 1 | — | 273 | — | nA |
| Start-up time | t_{LFXO} | ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 2 | — | 308 | — | ms |

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{LFXO_T} / 2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.10.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.13. High-Frequency Crystal Oscillator (HFXO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|-------|------|---------------|
| Crystal frequency | f_{HFXO} | No clock doubling | 4 | — | 50 | MHz |
| | | Clock doubler enabled | 4 | — | 25 | MHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{HFXO} | 50 MHz crystal | — | — | 50 | Ω |
| | | 24 MHz crystal | — | — | 150 | Ω |
| | | 4 MHz crystal | — | — | 180 | Ω |
| Nominal on-chip tuning cap range ¹ | $C_{\text{HFXO_T}}$ | On each of HFXTAL_N and HFXTAL_P pins | 8.7 | — | 51.7 | pF |
| On-chip tuning capacitance step | SS_{HFXO} | | — | 0.084 | — | pF |
| Startup time | t_{HFXO} | 50 MHz crystal, ESR = 50 Ohm, $C_L = 8$ pF | — | 350 | — | μs |
| | | 24 MHz crystal, ESR = 150 Ohm, $C_L = 6$ pF | — | 700 | — | μs |
| | | 4 MHz crystal, ESR = 180 Ohm, $C_L = 18$ pF | — | 3 | — | ms |
| Current consumption after startup | I_{HFXO} | 50 MHz crystal | — | 660 | — | μA |
| | | 24 MHz crystal | — | 330 | — | μA |
| | | 4 MHz crystal | — | 70 | — | μA |

Note:

1. The effective load capacitance seen by the crystal will be $C_{\text{HFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.10.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.14. Low-Frequency RC Oscillator (LFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------|------------------------------------|------|--------|------|------|
| Oscillation frequency | f_{LFRCO} | ENVREF ¹ = 1, T ≤ 85 °C | 31.3 | 32.768 | 33.6 | kHz |
| | | ENVREF ¹ = 1, T > 85 °C | 31 | 32.768 | 36.8 | kHz |
| | | ENVREF ¹ = 0, T ≤ 85 °C | 31.3 | 32.768 | 33.4 | kHz |
| | | ENVREF ¹ = 0, T > 85 °C | 30 | 32.768 | 33.6 | kHz |
| Startup time | t_{LFRCO} | | — | 500 | — | μs |
| Current consumption ² | I_{LFRCO} | ENVREF = 1 in CMU_LFRCOCTRL | — | 370 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 520 | — | nA |

Note:

1. In CMU_LFRCOCTRL register.
2. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.

4.1.10.4 High-Frequency RC Oscillator (HFRCO)

Table 4.15. High-Frequency RC Oscillator (HFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-----------------------------|---|------|---------------|-----|---------------|
| Frequency accuracy | $f_{\text{HFRCO_ACC}}$ | At production calibrated frequencies, across supply voltage and temperature | -2.5 | — | 2.5 | % |
| Start-up time | t_{HFRCO} | $f_{\text{HFRCO}} \geq 19 \text{ MHz}$ | — | 300 | — | ns |
| | | $4 < f_{\text{HFRCO}} < 19 \text{ MHz}$ | — | 1 | — | μs |
| | | $f_{\text{HFRCO}} \leq 4 \text{ MHz}$ | — | 2.5 | — | μs |
| Maximum DPLL lock time ¹ | $t_{\text{DPLL_LOCK}}$ | $f_{\text{REF}} = 32.768 \text{ kHz}$, $f_{\text{HFRCO}} = 39.98 \text{ MHz}$, $N = 1219$, $M = 0$ | — | 183 | — | μs |
| Current consumption on all supplies | I_{HFRCO} | $f_{\text{HFRCO}} = 72 \text{ MHz}$ | — | 550 | 600 | μA |
| | | $f_{\text{HFRCO}} = 64 \text{ MHz}$ | — | 500 | 550 | μA |
| | | $f_{\text{HFRCO}} = 56 \text{ MHz}$ | — | 430 | 475 | μA |
| | | $f_{\text{HFRCO}} = 48 \text{ MHz}$ | — | 380 | 410 | μA |
| | | $f_{\text{HFRCO}} = 38 \text{ MHz}$ | — | 310 | 340 | μA |
| | | $f_{\text{HFRCO}} = 32 \text{ MHz}$ | — | 265 | 280 | μA |
| | | $f_{\text{HFRCO}} = 26 \text{ MHz}$ | — | 220 | 235 | μA |
| | | $f_{\text{HFRCO}} = 19 \text{ MHz}$ | — | 180 | 190 | μA |
| | | $f_{\text{HFRCO}} = 16 \text{ MHz}$ | — | 150 | 160 | μA |
| | | $f_{\text{HFRCO}} = 13 \text{ MHz}$ | — | 135 | 140 | μA |
| | | $f_{\text{HFRCO}} = 7 \text{ MHz}$ | — | 98 | 102 | μA |
| | | $f_{\text{HFRCO}} = 4 \text{ MHz}$ | — | 38 | 42 | μA |
| | | $f_{\text{HFRCO}} = 2 \text{ MHz}$ | — | 32 | 35 | μA |
| | | $f_{\text{HFRCO}} = 1 \text{ MHz}$ | — | 28 | 30 | μA |
| | | $f_{\text{HFRCO}} = 72 \text{ MHz}$, DPLL enabled | — | 580 | 650 | μA |
| | | $f_{\text{HFRCO}} = 40 \text{ MHz}$, DPLL enabled | — | 500 | 525 | μA |
| | | $f_{\text{HFRCO}} = 32 \text{ MHz}$, DPLL enabled | — | 400 | 420 | μA |
| | | $f_{\text{HFRCO}} = 16 \text{ MHz}$, DPLL enabled | — | 220 | 235 | μA |
| | | $f_{\text{HFRCO}} = 4 \text{ MHz}$, DPLL enabled | — | 56 | 60 | μA |
| $f_{\text{HFRCO}} = 1 \text{ MHz}$, DPLL enabled | — | 35 | 38 | μA | | |
| Coarse trim step size (% of period) | $SS_{\text{HFRCO_COARSE}}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{\text{HFRCO_FINE}}$ | | — | 0.1 | — | % |
| Period jitter | PJ_{HFRCO} | | — | 0.2 | — | % RMS |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|-------------------------|----------------------------------|-----|-----|-----|------|
| Frequency limits | f _{HFRCO_BAND} | FREQRANGE = 0, FINETUNINGEN = 0 | 1 | — | 10 | MHz |
| | | FREQRANGE = 3, FINETUNINGEN = 0 | 2 | — | 17 | MHz |
| | | FREQRANGE = 6, FINETUNINGEN = 0 | 4 | — | 30 | MHz |
| | | FREQRANGE = 7, FINETUNINGEN = 0 | 5 | — | 34 | MHz |
| | | FREQRANGE = 8, FINETUNINGEN = 0 | 7 | — | 42 | MHz |
| | | FREQRANGE = 10, FINETUNINGEN = 0 | 12 | — | 58 | MHz |
| | | FREQRANGE = 11, FINETUNINGEN = 0 | 15 | — | 68 | MHz |
| | | FREQRANGE = 12, FINETUNINGEN = 0 | 18 | — | 83 | MHz |
| | | FREQRANGE = 13, FINETUNINGEN = 0 | 24 | — | 100 | MHz |
| | | FREQRANGE = 14, FINETUNINGEN = 0 | 28 | — | 119 | MHz |
| | | FREQRANGE = 15, FINETUNINGEN = 0 | 33 | — | 138 | MHz |
| | | FREQRANGE = 16, FINETUNINGEN = 0 | 43 | — | 163 | MHz |

Note:

1. Maximum DPLL lock time $\sim 6 \times (M+1) \times t_{REF}$, where t_{REF} is the reference clock period.

4.1.10.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.16. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|--------------------------------|---|-----|---------------|-----|---------------|
| Frequency accuracy | $f_{\text{AUXHFRCO_ACC}}$ | At production calibrated frequencies, across supply voltage and temperature | -3 | — | 3 | % |
| Start-up time | t_{AUXHFRCO} | $f_{\text{AUXHFRCO}} \geq 19 \text{ MHz}$ | — | 400 | — | ns |
| | | $4 < f_{\text{AUXHFRCO}} < 19 \text{ MHz}$ | — | 1.4 | — | μs |
| | | $f_{\text{AUXHFRCO}} \leq 4 \text{ MHz}$ | — | 2.5 | — | μs |
| Current consumption on all supplies | I_{AUXHFRCO} | $f_{\text{AUXHFRCO}} = 50 \text{ MHz}$ | — | 270 | 285 | μA |
| | | $f_{\text{AUXHFRCO}} = 48 \text{ MHz}$ | — | 255 | 272 | μA |
| | | $f_{\text{AUXHFRCO}} = 38 \text{ MHz}$ | — | 212 | 225 | μA |
| | | $f_{\text{AUXHFRCO}} = 32 \text{ MHz}$ | — | 174 | 185 | μA |
| | | $f_{\text{AUXHFRCO}} = 26 \text{ MHz}$ | — | 148 | 158 | μA |
| | | $f_{\text{AUXHFRCO}} = 19 \text{ MHz}$ | — | 118 | 127 | μA |
| | | $f_{\text{AUXHFRCO}} = 16 \text{ MHz}$ | — | 108 | 116 | μA |
| | | $f_{\text{AUXHFRCO}} = 13 \text{ MHz}$ | — | 88 | 112 | μA |
| | | $f_{\text{AUXHFRCO}} = 7 \text{ MHz}$ | — | 59 | 72 | μA |
| | | $f_{\text{AUXHFRCO}} = 4 \text{ MHz}$ | — | 32 | 36 | μA |
| | | $f_{\text{AUXHFRCO}} = 2 \text{ MHz}$ | — | 27 | 30 | μA |
| $f_{\text{AUXHFRCO}} = 1 \text{ MHz}$ | — | 26 | 28 | μA | | |
| Coarse trim step size (% of period) | $SS_{\text{AUXHFRCO_COARSE}}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{\text{AUXHFRCO_FINE}}$ | | — | 0.1 | — | % |
| Period jitter | PJ_{AUXHFRCO} | | — | 0.2 | — | % RMS |

4.1.10.6 USB High-Frequency RC Oscillator (USHFRCO)

Table 4.17. USB High-Frequency RC Oscillator (USHFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|---|-------|-----|------|---------|
| Frequency accuracy | $f_{USHFRCO_ACC}$ | At production calibrated frequencies, across supply voltage and temperature | -2.5 | — | 2.5 | % |
| | | USB clock recovery enabled, Active connection as device, FINE-TUNINGEN ¹ = 1 | -0.25 | — | 0.25 | % |
| Start-up time | $t_{USHFRCO}$ | | — | 300 | — | ns |
| Current consumption on all supplies | $I_{USHFRCO}$ | $f_{USHFRCO} = 48$ MHz, FINETUNINGEN ¹ = 1 | — | 293 | 305 | μ A |
| | | $f_{USHFRCO} = 50$ MHz, FINETUNINGEN ¹ = 0 | — | 257 | 270 | μ A |
| | | $f_{USHFRCO} = 48$ MHz, FINETUNINGEN ¹ = 0 | — | 249 | 260 | μ A |
| | | $f_{USHFRCO} = 32$ MHz, FINETUNINGEN ¹ = 0 | — | 165 | 176 | μ A |
| | | $f_{USHFRCO} = 16$ MHz, FINETUNINGEN ¹ = 0 | — | 100 | 111 | μ A |
| Period jitter | $PJ_{USHFRCO}$ | | — | 0.2 | — | % RMS |
| Note: 1. In the CMU_USHFRCOCTRL register. | | | | | | |

4.1.10.7 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.18. Ultra-low Frequency RC Oscillator (ULFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------|--------------|----------------|------|-----|------|------|
| Oscillation frequency | f_{ULFRCO} | | 0.88 | 1 | 1.12 | kHz |

4.1.11 Flash Memory Characteristics¹

Table 4.19. Flash Memory Characteristics¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|---|-------|-----|-----|--------|
| Flash erase cycles before failure | EC _{FLASH} | | 10000 | — | — | cycles |
| Flash data retention | RET _{FLASH} | T ≤ 85 °C | 10 | — | — | years |
| | | T ≤ 125 °C | 10 | — | — | years |
| Word (32-bit) programming time | t _{W_PROG} | Burst write, 128 words, average time per word | 20 | 27 | 32 | µs |
| | | Single word | 59 | 68 | 80 | µs |
| Page erase time ² | t _{PERASE} | | 20 | 27 | 35 | ms |
| Mass erase time ³ | t _{MERASE} | | 20 | 27 | 35 | ms |
| Device erase time ^{4 5} | t _{DERASE} | T ≤ 85 °C | — | 80 | 95 | ms |
| | | T ≤ 125 °C | — | 80 | 100 | ms |
| Erase current ⁶ | I _{ERASE} | Page Erase | — | — | 1.6 | mA |
| | | Mass or Device Erase | — | — | 1.9 | mA |
| Write current ⁶ | I _{WRITE} | | — | — | 3.7 | mA |
| Supply voltage during flash erase and write | V _{FLASH} | | 1.62 | — | 3.6 | V |

Note:

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- Mass erase is issued by the CPU and erases all flash.
- Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
- From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- Measured at 25 °C.

4.1.12 General-Purpose I/O (GPIO)

Table 4.20. General-Purpose I/O (GPIO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------|--|-------------------|-----|-------------------|------------|
| Input low voltage ¹ | V_{IL} | GPIO pins | — | — | $IOVDD \cdot 0.3$ | V |
| Input high voltage ¹ | V_{IH} | GPIO pins | $IOVDD \cdot 0.7$ | — | — | V |
| Output high voltage relative to IOVDD | V_{OH} | Sourcing 3 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ² = WEAK | $IOVDD \cdot 0.8$ | — | — | V |
| | | Sourcing 1.2 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ² = WEAK | $IOVDD \cdot 0.6$ | — | — | V |
| | | Sourcing 20 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ² = STRONG | $IOVDD \cdot 0.8$ | — | — | V |
| | | Sourcing 8 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ² = STRONG | $IOVDD \cdot 0.6$ | — | — | V |
| Output low voltage relative to IOVDD | V_{OL} | Sinking 3 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ² = WEAK | — | — | $IOVDD \cdot 0.2$ | V |
| | | Sinking 1.2 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ² = WEAK | — | — | $IOVDD \cdot 0.4$ | V |
| | | Sinking 20 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ² = STRONG | — | — | $IOVDD \cdot 0.2$ | V |
| | | Sinking 8 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ² = STRONG | — | — | $IOVDD \cdot 0.4$ | V |
| Input leakage current | I_{IOLEAK} | All GPIO except LFXO pins, $GPIO \leq IOVDD$, $T \leq 85$ °C | — | 0.1 | 40 | nA |
| | | LFXO Pins, $GPIO \leq IOVDD$, $T \leq 85$ °C | — | 0.1 | 60 | nA |
| | | All GPIO except LFXO pins, $GPIO \leq IOVDD$, $T > 85$ °C | — | — | 150 | nA |
| | | LFXO Pins, $GPIO \leq IOVDD$, $T > 85$ °C | — | — | 300 | nA |
| Input leakage current on 5VTOL pads above IOVDD | $I_{5VTOLLEAK}$ | $IOVDD < GPIO \leq IOVDD + 2$ V | — | 3.3 | 15 | μ A |
| I/O pin pull-up/pull-down resistor ³ | R_{PUD} | | 30 | 40 | 65 | k Ω |
| Pulse width of pulses removed by the glitch suppression filter | $t_{IOGLITCH}$ | | 15 | 25 | 35 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|---|-----|-----------|-----|----------|
| Output fall time, From 70% to 30% of V_{IO} | t_{IOF} | $C_L = 50$ pF, DRIVESTRENGTH ² = STRONG, SLEWRATE ² = 0x6 | — | 1.8 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ² = WEAK, SLEWRATE ² = 0x6 | — | 4.5 | — | ns |
| Output rise time, From 30% to 70% of V_{IO} | t_{IOR} | $C_L = 50$ pF, DRIVESTRENGTH ² = STRONG, SLEWRATE = 0x6 ² | — | 2.2 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ² = WEAK, SLEWRATE ² = 0x6 | — | 7.4 | — | ns |
| Required external series resistor on USB D+ and D- | R_{USB} | | — | 33 +/-10% | — | Ω |

Note:

1. GPIO input threshold are proportional to the IOVDD supply, except for RESETn which is proportional to AVDD (or BU_VIN in backup mode).
2. In GPIO_Pn_CTRL register.
3. GPIO pull-ups are referenced to the IOVDD supply, except for RESETn, which connects to AVDD (or BU_VIN in backup mode).

4.1.13 Voltage Monitor (VMON)

Table 4.21. Voltage Monitor (VMON)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|---|------|-----|-----|------|
| Supply current (including I _{SENSE}) | I _{VMON} | In EM0 or EM1, 1 active channel, T ≤ 85 °C | — | 6 | 11 | μA |
| | | In EM0 or EM1, 1 active channel, T > 85 °C | — | — | 21 | μA |
| | | In EM0 or EM1, All channels active, T ≤ 85 °C | — | 15 | 20 | μA |
| | | In EM0 or EM1, All channels active, T > 85 °C | — | — | 32 | μA |
| | | In EM2, EM3 or EM4, 1 channel active and above threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 1 channel active and below threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, All channels active and above threshold | — | 99 | — | nA |
| | | In EM2, EM3 or EM4, All channels active and below threshold | — | 99 | — | nA |
| Loading of monitored supply | I _{SENSE} | In EM0 or EM1 | — | 2 | — | μA |
| | | In EM2, EM3 or EM4 | — | 2 | — | nA |
| Threshold range | V _{VMON_RANGE} | | 1.62 | — | 3.4 | V |
| Threshold step size | N _{VMON_STESP} | Coarse | — | 200 | — | mV |
| | | Fine | — | 20 | — | mV |
| Response time | t _{VMON_RES} | Supply drops at 1V/μs rate | — | 460 | — | ns |
| Hysteresis | V _{VMON_HYST} | | — | 26 | — | mV |

4.1.14 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.22. Analog to Digital Converter (ADC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------------------------|--|---------------------|-----|--------------------|------|
| Resolution | V _{RESOLUTION} | | 6 | — | 12 | Bits |
| Input voltage range ¹ | V _{ADCIN} | Single ended | — | — | V _{FS} | V |
| | | Differential | -V _{FS} /2 | — | V _{FS} /2 | V |
| Input range of external reference voltage, single ended and differential | V _{ADCREFIN_P} | | 1 | — | V _{AVDD} | V |
| Power supply rejection ² | PSRR _{ADC} | At DC | — | 80 | — | dB |
| Analog input common mode rejection ratio | CMRR _{ADC} | At DC | — | 80 | — | dB |
| Current from all supplies, using internal reference buffer. Continuous operation. WAR- MUPMODE ³ = KEEPADC- WARM | I _{ADC_CONTINU- OUS_LP} | 1 Msps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ⁴ | — | 270 | 350 | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 1 ⁴ | — | 125 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 1 ⁴ | — | 80 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR- MUPMODE ³ = NORMAL | I _{ADC_NORMAL_LP} | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ⁴ | — | 45 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 1 ⁴ | — | 8 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEP- INSTANDBY or KEEPIN- SLOWACC | I _{ADC_STAND- BY_LP} | 125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ⁴ | — | 105 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ⁴ | — | 70 | — | μA |
| Current from all supplies, using internal reference buffer. Continuous operation. WAR- MUPMODE ³ = KEEPADC- WARM | I _{ADC_CONTINU- OUS_HP} | 1 Msps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ⁴ | — | 325 | — | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 0 ⁴ | — | 175 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 0 ⁴ | — | 125 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR- MUPMODE ³ = NORMAL | I _{ADC_NORMAL_HP} | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ⁴ | — | 85 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 0 ⁴ | — | 16 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEP- INSTANDBY or KEEPIN- SLOWACC | I _{ADC_STAND- BY_HP} | 125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ⁴ | — | 160 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ⁴ | — | 125 | — | μA |
| Current from HFPERCLK | I _{ADC_CLK} | HFPERCLK = 16 MHz | — | 180 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|--|-----|-------|-----|---------------|
| ADC clock frequency | f_{ADCCLK} | | — | — | 16 | MHz |
| Throughput rate | f_{ADCRATE} | | — | — | 1 | Msp/s |
| Conversion time ⁵ | t_{ADCCONV} | 6 bit | — | 7 | — | cycles |
| | | 8 bit | — | 9 | — | cycles |
| | | 12 bit | — | 13 | — | cycles |
| Startup time of reference generator and ADC core | t_{ADCSTART} | WARMUPMODE ³ = NORMAL | — | — | 5 | μs |
| | | WARMUPMODE ³ = KEEPIN-STANDBY | — | — | 2 | μs |
| | | WARMUPMODE ³ = KEEPINSLOWACC | — | — | 1 | μs |
| SNDR at 1Msp/s and $f_{\text{IN}} = 10\text{kHz}$ | SNDR _{ADC} | Internal reference ⁶ , differential measurement | 58 | 67 | — | dB |
| | | External reference ⁷ , differential measurement | — | 68 | — | dB |
| Spurious-free dynamic range (SFDR) | SFDR _{ADC} | 1 MSamples/s, 10 kHz full-scale sine wave | — | 75 | — | dB |
| Differential non-linearity (DNL) | DNL _{ADC} | 12 bit resolution, No missing codes | -1 | — | 2 | LSB |
| Integral non-linearity (INL), End point method | INL _{ADC} | 12 bit resolution | -6 | — | 6 | LSB |
| Offset error | $V_{\text{ADCOFFSETERR}}$ | | -3 | 0 | 3 | LSB |
| Gain error in ADC | V_{ADCGAIN} | Using internal reference | — | -0.2 | 3.5 | % |
| | | Using external reference | — | -1 | — | % |
| Temperature sensor slope | $V_{\text{TS_SLOPE}}$ | | — | -1.84 | — | mV/°C |

Note:

- The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
- PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
- In ADCn_CTRL register.
- In ADCn_BIASPROG register.
- Derived from ADCCLK.
- Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is $\pm 1.25\text{ V}$. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.
- External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is $\pm 1.25\text{ V}$.

4.1.15 Analog Comparator (ACMP)

Table 4.23. Analog Comparator (ACMP)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------|--|-----|-----|--------------------|------|
| Input voltage range | V_{ACMPIN} | ACMPVDD = ACMPn_CTRL_PWRSEL ¹ | — | — | $V_{ACMPVDD}$ | V |
| Supply voltage | $V_{ACMPVDD}$ | BIASPROG ² ≤ 0x10 or FULL- BIAS ² = 0 | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | 0x10 < BIASPROG ² ≤ 0x20 and FULLBIAS ² = 1 | 2.1 | — | $V_{VREGVDD_MAX}$ | V |
| Active current not including voltage reference ³ | I_{ACMP} | BIASPROG ² = 1, FULLBIAS ² = 0 | — | 75 | — | nA |
| | | BIASPROG ² = 0x10, FULLBIAS ² = 0 | — | 350 | — | nA |
| | | BIASPROG ² = 0x02, FULLBIAS ² = 1 | — | 6.5 | — | μA |
| | | BIASPROG ² = 0x20, FULLBIAS ² = 1 | — | 65 | 100 | μA |
| Current consumption of inter- nal voltage reference ³ | $I_{ACMPREF}$ | VLP selected as input using 2.5 V Reference / 4 (0.625 V) | — | 50 | — | nA |
| | | VLP selected as input using VDD | — | 20 | — | nA |
| | | VBDIV selected as input using 1.25 V reference / 1 | — | 4.1 | — | μA |
| | | VADIV selected as input using VDD/1 | — | 2.4 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------|--|------|----------|------|---------------|
| Hysteresis ($V_{CM} = 1.25\text{ V}$, $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 1$) | $V_{ACMPHYST}$ | $HYSTSEL^4 = HYST0$ | -3 | 0 | 3 | mV |
| | | $HYSTSEL^4 = HYST1$ | 5 | 18 | 27 | mV |
| | | $HYSTSEL^4 = HYST2$ | 12 | 33 | 50 | mV |
| | | $HYSTSEL^4 = HYST3$ | 17 | 46 | 67 | mV |
| | | $HYSTSEL^4 = HYST4$ | 23 | 57 | 92 | mV |
| | | $HYSTSEL^4 = HYST5$ | 26 | 68 | 108 | mV |
| | | $HYSTSEL^4 = HYST6$ | 30 | 79 | 140 | mV |
| | | $HYSTSEL^4 = HYST7$ | 34 | 90 | 160 | mV |
| | | $HYSTSEL^4 = HYST8$ | -3 | 0 | 3 | mV |
| | | $HYSTSEL^4 = HYST9$ | -27 | -18 | -5 | mV |
| | | $HYSTSEL^4 = HYST10$ | -50 | -33 | -12 | mV |
| | | $HYSTSEL^4 = HYST11$ | -67 | -45 | -17 | mV |
| | | $HYSTSEL^4 = HYST12$ | -92 | -57 | -23 | mV |
| | | $HYSTSEL^4 = HYST13$ | -108 | -67 | -26 | mV |
| | | $HYSTSEL^4 = HYST14$ | -140 | -78 | -30 | mV |
| $HYSTSEL^4 = HYST15$ | -160 | -88 | -34 | mV | | |
| Comparator delay ⁵ | $t_{ACMPDELAY}$ | $BIASPROG^2 = 1$, $FULLBIAS^2 = 0$ | — | 30 | — | μs |
| | | $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 0$ | — | 3.7 | — | μs |
| | | $BIASPROG^2 = 0x02$, $FULLBIAS^2 = 1$ | — | 360 | — | ns |
| | | $BIASPROG^2 = 0x20$, $FULLBIAS^2 = 1$ | — | 35 | — | ns |
| Offset voltage | $V_{ACMPOFFSET}$ | $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 1$ | -35 | — | 35 | mV |
| Reference voltage | $V_{ACMPREF}$ | Internal 1.25 V reference | 1 | 1.25 | 1.47 | V |
| | | Internal 2.5 V reference | 1.98 | 2.5 | 2.8 | V |
| Capacitive sense internal resistance | R_{CSRES} | $CSRESSEL^6 = 0$ | — | infinite | — | k Ω |
| | | $CSRESSEL^6 = 1$ | — | 15 | — | k Ω |
| | | $CSRESSEL^6 = 2$ | — | 27 | — | k Ω |
| | | $CSRESSEL^6 = 3$ | — | 39 | — | k Ω |
| | | $CSRESSEL^6 = 4$ | — | 51 | — | k Ω |
| | | $CSRESSEL^6 = 5$ | — | 100 | — | k Ω |
| | | $CSRESSEL^6 = 6$ | — | 162 | — | k Ω |
| | | $CSRESSEL^6 = 7$ | — | 235 | — | k Ω |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. | | | | | | |
| 2. In ACMPn_CTRL register. | | | | | | |
| 3. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. | | | | | | |
| 4. In ACMPn_HYSTERESIS registers. | | | | | | |
| 5. ± 100 mV differential drive. | | | | | | |
| 6. In ACMPn_INPUTSEL register. | | | | | | |

4.1.16 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.24. Digital to Analog Converter (VDAC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|---|--------------------|------|-------------------|--------|
| Output voltage | V _{DACOUT} | Single-Ended | 0 | — | V _{VREF} | V |
| | | Differential ¹ | -V _{VREF} | — | V _{VREF} | V |
| Current consumption including references (2 channels) ² | I _{DAC} | 500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4 | — | 402 | — | μA |
| | | 44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4 | — | 88 | — | μA |
| | | 200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, REFSEL = 4, SETTLETIME = 0x02, WARMUP-TIME = 0x0A | — | 2 | — | μA |
| Current from HFPERCLK ³ | I _{DAC_CLK} | | — | 6.6 | — | μA/MHz |
| Sample rate | SR _{DAC} | | — | — | 500 | ksps |
| DAC clock frequency | f _{DAC} | | — | — | 1 | MHz |
| Conversion time | t _{DACCONV} | f _{DAC} = 1MHz | 2 | — | — | μs |
| Settling time | t _{DACSETTLE} | 50% fs step settling to 5 LSB | — | 2.5 | — | μs |
| Startup time | t _{DACSTARTUP} | Enable to 90% fs output, settling to 10 LSB | — | — | 12 | μs |
| Output impedance | R _{OUT} | DRIVESTRENGTH = 2, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 2, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Full supply range | — | 2 | — | Ω |
| Power supply rejection ratio ⁴ | PSRR | V _{out} = 50% fs. DC | — | 65.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|---|-------|------|------|------|
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz | SNDR _{DAC} | 500 ksps, single-ended, internal 1.25V reference | — | 60.4 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 61.6 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 64.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 63.3 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 64.4 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 65.8 | — | dB |
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz | SNDR _{DAC_BAND} | 500 ksps, single-ended, internal 1.25V reference | — | 65.3 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 66.7 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 70.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 67.8 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 69.0 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 68.5 | — | dB |
| Total harmonic distortion | THD | | — | 70.2 | — | dB |
| Differential non-linearity ⁵ | DNL _{DAC} | | -1.25 | — | 1.25 | LSB |
| Integral non-linearity | INL _{DAC} | | -4 | — | 4 | LSB |
| Offset error ⁶ | V _{OFFSET} | T = 25 °C | -8 | — | 8 | mV |
| | | Across operating temperature range | -25 | — | 25 | mV |
| Gain error ⁶ | V _{GAIN} | T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -2.5 | — | 2.5 | % |
| | | Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -3.5 | — | 3.5 | % |
| External load capacitance, OUTSCALE=0 | C _{LOAD} | | — | — | 75 | pF |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| <ol style="list-style-type: none"> 1. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range. 2. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load. 3. Current from HUPERCLK is dependent on HUPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC peripheral is enabled in the CMU. 4. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$, VDAC output at 90% of full scale 5. Entire range is monotonic and has no missing codes. 6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain. | | | | | | |

4.1.17 Current Digital to Analog Converter (IDAC)

Table 4.25. Current Digital to Analog Converter (IDAC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|--|------|------|-----|--------|
| Number of ranges | N_{IDAC_RANGES} | | — | 4 | — | ranges |
| Output current | I_{IDAC_OUT} | RANGESEL ¹ = RANGE0 | 0.05 | — | 1.6 | μA |
| | | RANGESEL ¹ = RANGE1 | 1.6 | — | 4.7 | μA |
| | | RANGESEL ¹ = RANGE2 | 0.5 | — | 16 | μA |
| | | RANGESEL ¹ = RANGE3 | 2 | — | 64 | μA |
| Linear steps within each range | N_{IDAC_STEPS} | | — | 32 | — | steps |
| Step size | SS_{IDAC} | RANGESEL ¹ = RANGE0 | — | 50 | — | nA |
| | | RANGESEL ¹ = RANGE1 | — | 100 | — | nA |
| | | RANGESEL ¹ = RANGE2 | — | 500 | — | nA |
| | | RANGESEL ¹ = RANGE3 | — | 2 | — | μA |
| Total accuracy, STEPSEL ¹ = 0x10 | ACC_{IDAC} | EM0 or EM1, AVDD=3.3 V, T = 25 °C | -3 | — | 3 | % |
| | | EM0 or EM1, Across operating temperature range | -18 | — | 22 | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -2.7 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -2.5 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -1.5 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -1.0 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -1.1 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -1.1 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.9 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.9 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|---|-----|------|-----|---------|
| Start up time | t_{IDAC_SU} | Output within 1% of steady state value | — | 5 | — | μs |
| Settling time, (output settled within 1% of steady state value), | t_{IDAC_SETTLE} | Range setting is changed | — | 5 | — | μs |
| | | Step value is changed | — | 1 | — | μs |
| Current consumption ² | I_{IDAC} | EM0 or EM1 Source mode, excluding output current, Across operating temperature range | — | 11 | 28 | μA |
| | | EM0 or EM1 Sink mode, excluding output current, Across operating temperature range | — | 13 | 30 | μA |
| | | EM2 or EM3 Source mode, excluding output current, T = 25 °C | — | 0.05 | — | μA |
| | | EM2 or EM3 Sink mode, excluding output current, T = 25 °C | — | 0.07 | — | μA |
| | | EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C | — | 11 | — | μA |
| | | EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C | — | 13 | — | μA |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | I_{COMP_SRC} | RANGESEL ¹ = RANGE0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$ | — | 0.11 | — | % |
| | | RANGESEL ¹ = RANGE1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$ | — | 0.06 | — | % |
| | | RANGESEL ¹ = RANGE2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$ | — | 0.04 | — | % |
| | | RANGESEL ¹ = RANGE3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$ | — | 0.03 | — | % |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD | I_{COMP_SINK} | RANGESEL ¹ = RANGE0, output voltage = 100 mV | — | 0.29 | — | % |
| | | RANGESEL ¹ = RANGE1, output voltage = 100 mV | — | 0.27 | — | % |
| | | RANGESEL ¹ = RANGE2, output voltage = 150 mV | — | 0.12 | — | % |
| | | RANGESEL ¹ = RANGE3, output voltage = 250 mV | — | 0.03 | — | % |

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.18 Capacitive Sense (CSEN)

Table 4.26. Capacitive Sense (CSEN)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|--|-----|------|-----|------|
| Single conversion time (1x accumulation) | t _{CNV} | 12-bit SAR Conversions | — | 20.2 | — | μs |
| | | 16-bit SAR Conversions | — | 26.4 | — | μs |
| | | Delta Modulation Conversion (single comparison) | — | 1.55 | — | μs |
| Maximum external capacitive load | C _{EXTMAX} | IREFPROG=7 (Gain = 1x), including routing parasitics | — | 68 | — | pF |
| | | IREFPROG=0 (Gain = 10x), including routing parasitics | — | 680 | — | pF |
| Maximum external series impedance | R _{EXTMAX} | | — | 1 | — | kΩ |
| Supply current, EM2 bonded conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0 | I _{CSEN_BOND} | 12-bit SAR conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 326 | — | nA |
| | | Delta Modulation conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 226 | — | nA |
| | | 12-bit SAR conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 33 | — | nA |
| | | Delta Modulation conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹ | — | 25 | — | nA |
| Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0 | I _{CSEN_EM2} | 12-bit SAR conversions, 20 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 690 | — | nA |
| | | Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 515 | — | nA |
| | | 12-bit SAR conversions, 200 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 79 | — | nA |
| | | Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹ | — | 57 | — | nA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------------|---|-----|------|-----|--------|
| Supply current, continuous conversions, WARMUP-MODE=KEEP_CSEN_WARM | I _{CSEN_ACTIVE} | SAR or Delta Modulation conversions of 33 pF capacitor, IRE-FPROG=0 (Gain = 10x), always on | — | 90.5 | — | μA |
| HFPERCLK supply current | I _{CSEN_HFPERCLK} | Current contribution from HFPERCLK when clock to CSEN block is enabled. | — | 2.25 | — | μA/MHz |

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the peripheral is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.19 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{1 2}.

Table 4.27. Operational Amplifier (OPAMP)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-------------------|--|------------------|------|-----------------------|------|
| Supply voltage (from AVDD) | V _{OPA} | HCMDIS = 0, Rail-to-rail input range | 2 | — | 3.8 | V |
| | | HCMDIS = 1 | 1.62 | — | 3.8 | V |
| Input voltage | V _{IN} | HCMDIS = 0, Rail-to-rail input range | V _{VSS} | — | V _{OPA} | V |
| | | HCMDIS = 1 | V _{VSS} | — | V _{OPA} -1.2 | V |
| Input impedance | R _{IN} | | 100 | — | — | MΩ |
| Output voltage | V _{OUT} | | V _{VSS} | — | V _{OPA} | V |
| Load capacitance ³ | C _{LOAD} | OUTSCALE = 0 | — | — | 75 | pF |
| | | OUTSCALE = 1 | — | — | 37.5 | pF |
| Output impedance | R _{OUT} | DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Buffer connection, Full supply range | — | 0.25 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Buffer connection, Full supply range | — | 0.6 | — | Ω |
| | | DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Buffer connection, Full supply range | — | 0.4 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Buffer connection, Full supply range | — | 1 | — | Ω |
| Internal closed-loop gain | G _{CL} | Buffer connection | 0.99 | 1 | 1.01 | - |
| | | 3x Gain connection | 2.93 | 2.99 | 3.05 | - |
| | | 16x Gain connection | 15.07 | 15.7 | 16.33 | - |
| Active current ⁴ | I _{OPA} | DRIVESTRENGTH = 3, OUTSCALE = 0 | — | 580 | — | μA |
| | | DRIVESTRENGTH = 2, OUTSCALE = 0 | — | 176 | — | μA |
| | | DRIVESTRENGTH = 1, OUTSCALE = 0 | — | 13 | — | μA |
| | | DRIVESTRENGTH = 0, OUTSCALE = 0 | — | 4.7 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|------------------|---|-----|------|-----|-------|
| Open-loop gain | G _{OL} | DRIVESTRENGTH = 3 | — | 135 | — | dB |
| | | DRIVESTRENGTH = 2 | — | 137 | — | dB |
| | | DRIVESTRENGTH = 1 | — | 121 | — | dB |
| | | DRIVESTRENGTH = 0 | — | 109 | — | dB |
| Loop unit-gain frequency ⁵ | UGF | DRIVESTRENGTH = 3, Buffer connection | — | 3.38 | — | MHz |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 0.9 | — | MHz |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 132 | — | kHz |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 34 | — | kHz |
| | | DRIVESTRENGTH = 3, 3x Gain connection | — | 2.57 | — | MHz |
| | | DRIVESTRENGTH = 2, 3x Gain connection | — | 0.71 | — | MHz |
| | | DRIVESTRENGTH = 1, 3x Gain connection | — | 113 | — | kHz |
| | | DRIVESTRENGTH = 0, 3x Gain connection | — | 28 | — | kHz |
| Phase margin | PM | DRIVESTRENGTH = 3, Buffer connection | — | 67 | — | ° |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 69 | — | ° |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 63 | — | ° |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 68 | — | ° |
| Output voltage noise | N _{OUT} | DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz | — | 146 | — | μVrms |
| | | DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz | — | 163 | — | μVrms |
| | | DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz | — | 170 | — | μVrms |
| | | DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz | — | 176 | — | μVrms |
| | | DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz | — | 313 | — | μVrms |
| | | DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz | — | 271 | — | μVrms |
| | | DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz | — | 247 | — | μVrms |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz | — | 245 | — | μVrms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|--|-----|-------|-----|------------|
| Slew rate ⁶ | SR | DRIVESTRENGTH = 3, INCBW=1 ⁷ | — | 4.7 | — | V/ μ s |
| | | DRIVESTRENGTH = 3, INCBW=0 | — | 1.5 | — | V/ μ s |
| | | DRIVESTRENGTH = 2, INCBW=1 ⁷ | — | 1.27 | — | V/ μ s |
| | | DRIVESTRENGTH = 2, INCBW=0 | — | 0.42 | — | V/ μ s |
| | | DRIVESTRENGTH = 1, INCBW=1 ⁷ | — | 0.17 | — | V/ μ s |
| | | DRIVESTRENGTH = 1, INCBW=0 | — | 0.058 | — | V/ μ s |
| | | DRIVESTRENGTH = 0, INCBW=1 ⁷ | — | 0.044 | — | V/ μ s |
| | | DRIVESTRENGTH = 0, INCBW=0 | — | 0.015 | — | V/ μ s |
| Startup time ⁸ | T _{START} | DRIVESTRENGTH = 2 | — | — | 12 | μ s |
| Input offset voltage | V _{OSI} | DRIVESTRENGTH = 2 or 3, T = 25 °C | -3 | — | 3 | mV |
| | | DRIVESTRENGTH = 1 or 0, T = 25 °C | -3 | — | 3 | mV |
| | | DRIVESTRENGTH = 2 or 3, across operating temperature range | -12 | — | 12 | mV |
| | | DRIVESTRENGTH = 1 or 0, across operating temperature range | -30 | — | 30 | mV |
| DC power supply rejection ratio ⁹ | PSRR _{DC} | Input referred | — | 70 | — | dB |
| DC common-mode rejection ratio ⁹ | CMRR _{DC} | Input referred | — | 70 | — | dB |
| Total harmonic distortion | THD _{OPA} | DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V | — | 90 | — | dB |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V | — | 90 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{INPUT} = 0.5\text{ V}$, $V_{OUTPUT} = 0.5\text{ V}$. | | | | | | |
| 2. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{INPUT} = 0.5\text{ V}$, $V_{OUTPUT} = 1.5\text{ V}$. Nominal voltage gain is 3. | | | | | | |
| 3. If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information. | | | | | | |
| 4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 μA current when the OPAMP drives 1.5 V between output and ground. | | | | | | |
| 5. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network. | | | | | | |
| 6. Step between 0.2V and $V_{OPA}-0.2\text{V}$, 10%-90% rising/falling range. | | | | | | |
| 7. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3 , or the OPAMP may not be stable. | | | | | | |
| 8. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV. | | | | | | |
| 9. When HCMDIS=1 and input common mode transitions the region from $V_{OPA}-1.4\text{V}$ to $V_{OPA}-1\text{V}$, input offset will change. PSRR and CMRR specifications do not apply to this transition region. | | | | | | |

4.1.20 LCD Driver

Table 4.28. LCD Driver

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|--|-----|------|----------------------|------|
| Frame rate | f_{LCDFR} | | 30 | — | 100 | Hz |
| LCD supply range ¹ | V_{LCDIN} | | 1.8 | — | 3.8 | V |
| LCD output voltage range | V_{LCD} | Current source mode, No external LCD capacitor | 2.0 | — | $V_{LCDIN}-0.4$ | V |
| | | Step-down mode with external LCD capacitor | 2.0 | — | V_{LCDIN} | V |
| | | Charge pump mode with external LCD capacitor | 2.0 | — | 1.9 * V_{LCDIN} | V |
| Contrast control step size | $STEP_{CONTRAST}$ | Current source mode | — | 64 | — | mV |
| | | Charge pump or Step-down mode | — | 43 | — | mV |
| Contrast control step accuracy ² | $ACC_{CONTRAST}$ | | — | +/-4 | — | % |
| Note: | | | | | | |
| 1. V_{LCDIN} is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW. | | | | | | |
| 2. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation. | | | | | | |

4.1.21 Pulse Counter (PCNT)

Table 4.29. Pulse Counter (PCNT)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------|-----------------|--|-----|-----|-----|------|
| Input frequency | F _{IN} | Asynchronous Single and Quadrature Modes | — | — | 20 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |

4.1.22 Analog Port (APORT)

Table 4.30. Analog Port (APORT)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|--------------------|----------------------|-----|-----|-----|------|
| Supply current ^{1 2} | I _{APORT} | Operation in EM0/EM1 | — | 7 | — | μA |
| | | Operation in EM2/EM3 | — | 63 | — | nA |

Note:

1. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported peripheral currents. Additional peripherals requesting access to APORT do not incur further current.
2. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.

4.1.23 I2C

4.1.23.1 I2C Standard-mode (Sm)¹Table 4.31. I2C Standard-mode (Sm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|-----|-----|------|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 100 | kHz |
| SCL clock low time | t _{LOW} | | 4.7 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 4 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 250 | — | — | ns |
| SDA hold time ³ | t _{HD_DAT} | | 100 | — | 3450 | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 4.7 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 4 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 4 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 4.7 | — | — | μs |

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.23.2 I2C Fast-mode (Fm)¹Table 4.32. I2C Fast-mode (Fm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|-----|-----|-----|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 400 | kHz |
| SCL clock low time | t _{LOW} | | 1.3 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.6 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 100 | — | — | ns |
| SDA hold time ³ | t _{HD_DAT} | | 100 | — | 900 | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 0.6 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 0.6 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 0.6 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 1.3 | — | — | μs |

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.23.3 I2C Fast-mode Plus (Fm+)¹

Table 4.33. I2C Fast-mode Plus (Fm+)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|------|-----|------|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 1000 | kHz |
| SCL clock low time | t _{LOW} | | 0.5 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.26 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 50 | — | — | ns |
| SDA hold time | t _{HD_DAT} | | 100 | — | — | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 0.26 | — | — | μs |
| (Repeated) START condition hold time | t _{HD_STA} | | 0.26 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 0.26 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 0.5 | — | — | μs |

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.24 USART SPI

SPI Master Timing

Table 4.34. SPI Master Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------------|---|-------------------------------|-----|-----|------|
| SCLK period ^{1 2 3} | t _{SCLK} | All USARTs except USART2 | 2 * t _{HFPERCLK} | — | — | ns |
| | | USART2 | 2 * t _{HFPERBCLK} | — | — | ns |
| CS to MOSI ^{1 2} | t _{CS_MO} | USART2, location 4, IOVDD = 1.8 V | -4 | — | 6 | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -2.5 | — | 5 | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -6.5 | — | 7.5 | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -5.5 | — | 6 | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -10.5 | — | 9 | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -8.5 | — | 7.5 | ns |
| SCLK to MOSI ^{1 2} | t _{SCLK_MO} | USART2, location 4, IOVDD = 1.8 V | -1 | — | 6 | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -1 | — | 5.5 | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -3 | — | 4 | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -2.5 | — | 2.5 | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -7 | — | 8.5 | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -6 | — | 9 | ns |
| MISO setup time ^{1 2} | t _{SU_MI} | USART2, location 4, IOVDD = 1.8 V | 41 | — | — | ns |
| | | USART2, location 4, IOVDD = 3.0 V | 32 | — | — | ns |
| | | USART2, location 5, IOVDD = 1.8 V | 49 | — | — | ns |
| | | USART2, location 5, IOVDD = 3.0 V | 30 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | 51 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | 32 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-------------|---|-------|-----|-----|------|
| MISO hold time ^{1 2} | t_{H_MI} | USART2, location 4, IOVDD = 1.8 V | -12 | — | — | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -12 | — | — | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -9.5 | — | — | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -9.5 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -10.5 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -10.5 | — | — | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.



Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.35. SPI Slave Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|-------------------|----------------|------------------------------|-----|------------------------------|------|
| SCLK period ^{1 2 3} | t_{SCLK} | | 6 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK high time ^{1 2 3} | t_{SCLK_HI} | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK low time ^{1 2 3} | t_{SCLK_LO} | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| CS active to MISO ^{1 2} | $t_{CS_ACT_MI}$ | | 22 | — | 54 | ns |
| CS disable to MISO ^{1 2} | $t_{CS_DIS_MI}$ | | 20 | — | 175 | ns |
| MOSI setup time ^{1 2} | t_{SU_MO} | | 6 | — | — | ns |
| MOSI hold time ^{1 2 3} | t_{H_MO} | | 7 | — | — | ns |
| SCLK to MISO ^{1 2 3} | t_{SCLK_MI} | | 17 + 1.5 * $t_{HFPERCLK}$ | — | 41 + 2.5 * $t_{HFPERCLK}$ | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

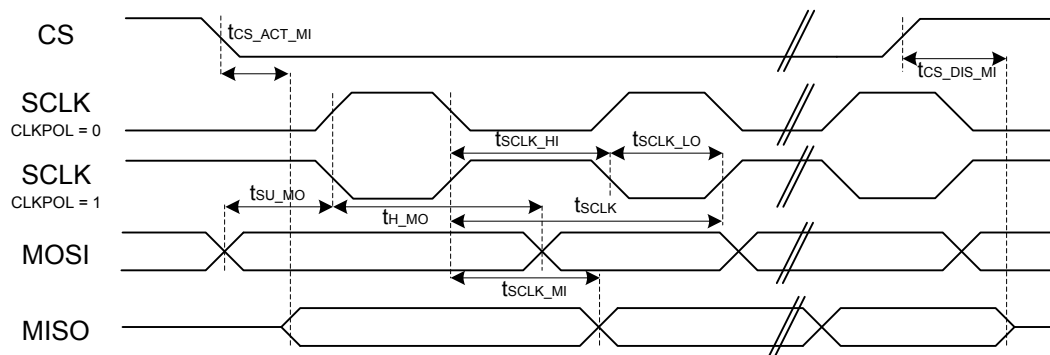


Figure 4.2. SPI Slave Timing Diagram

4.1.25 External Bus Interface (EBI)

EBI Write Enable Output Timing

Timing applies to both EBI_WEn and EBI_NANDWEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.36. EBI Write Enable Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|----------------|---|-----|-----|------|
| Output hold time, from trailing EBI_WEn / EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CS _n , EBI_BL _n invalid | t _{OH_WEn} | IOVDD ≥ 1.62 V | -22 + (WRHOLD * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -14 + (WRHOLD * t _{HFCOR-ECLK}) | — | — | ns |
| Output setup time, from EBI_AD, EBI_A, EBI_CS _n , EBI_BL _n valid to leading EBI_WEn / EBI_NANDWEn edge ¹ | t _{OSU_WEn} | IOVDD ≥ 1.62 V | -12 + (WRSET-UP * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -10 + (WRSET-UP * t _{HFCOR-ECLK}) | — | — | ns |
| EBI_WEn / EBI_NANDWEn pulse width ¹ | t _{WIDTH_WEn} | IOVDD ≥ 1.62 V | -6 + (MAX(1, WRSTRB) * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -5 + (MAX(1, WRSTRB) * t _{HFCOR-ECLK}) | — | — | ns |

Note:

- The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by 1/2 * t_{HCLKNODIV}.

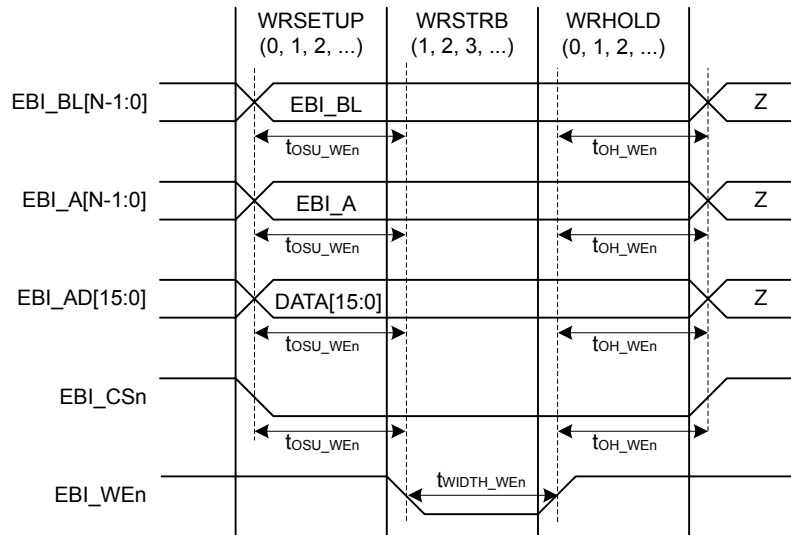


Figure 4.3. EBI Write Enable Output Timing Diagram

EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.37. EBI Address Latch Enable Output Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|---------------------|--|-----|-----|------|
| Output hold time, from trailing EBI_ALE edge to EBI_AD invalid ^{1 2} | t_{OH_ALEn} | IOVDD \geq 1.62 V | -22 + (ADDR-HOLD * $t_{HFCOR-ECLK}$) | — | — | ns |
| | | IOVDD \geq 3.0 V | -13 + (ADDR-HOLD * $t_{HFCOR-ECLK}$) | — | — | ns |
| Output setup time, from EBI_AD valid to leading EBI_ALE edge | t_{OSU_ALEn} | IOVDD \geq 1.62 V | -10 | — | — | ns |
| | | IOVDD \geq 3.0 V | -9 | — | — | ns |
| EBI_ALEn pulse width ¹ | t_{WIDTH_ALEn} | IOVDD \geq 1.62 V | -5 + ((ADDR-SETUP + 1) * $t_{HFCOR-ECLK}$) | — | — | ns |
| | | IOVDD \geq 3.0 V | -4 + ((ADDR-SETUP + 1) * $t_{HFCOR-ECLK}$) | — | — | ns |

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of t_{OSU_ALEn} by $t_{HFCORECLK} - 1/2 * t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

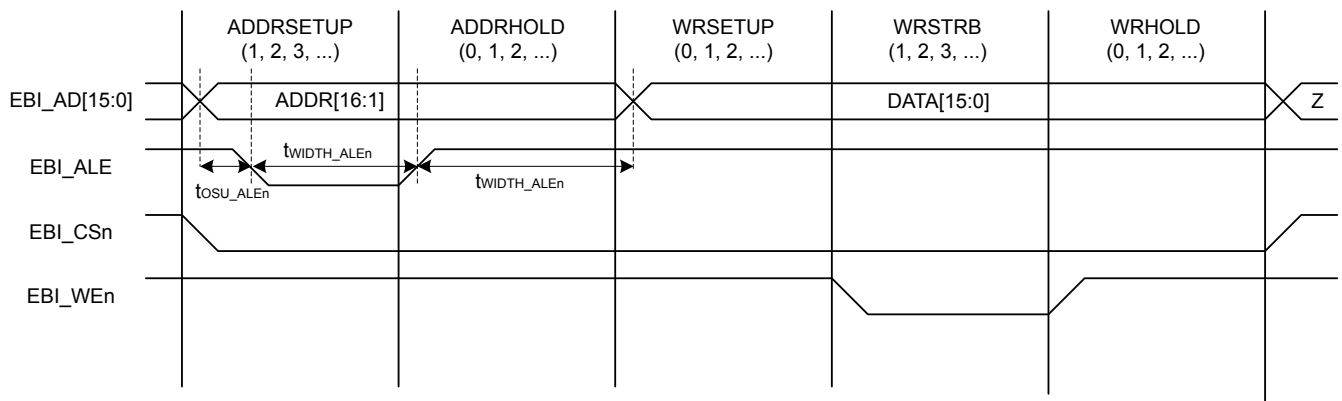


Figure 4.4. EBI Address Latch Enable Output Timing Diagram

EBI Read Enable Output Timing

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. Output timing for EBI_AD applies only to multiplexed addressing modes D8A24ALE and D16A16ALE. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.38. EBI Read Enable Output Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|----------------|--|-----|-----|------|
| Output hold time, from trailing EBI_REn / EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CS _n , EBI_BLn invalid | t _{OH_REn} | IOVDD ≥ 1.62 V | -21 + (RDHOLD * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -11 + (RDHOLD * t _{HFCOR-ECLK}) | — | — | ns |
| Output setup time, from EBI_AD, EBI_A, EBI_CS _n , EBI_BLn valid to leading EBI_REn / EBI_NANDREn edge ¹ | t _{OSU_REn} | IOVDD ≥ 1.62 V | -11 + (RDSETUP * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -10 + (RDSETUP * t _{HFCOR-ECLK}) | — | — | ns |
| EBI_REn pulse width ^{1 2} | t _{WIDTH_REn} | IOVDD ≥ 1.62 V | -6 + (MAX(1, RDSTRB) * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -4 + (MAX(1, RDSTRB) * t _{HFCOR-ECLK}) | — | — | ns |

Note:

- The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of t_{WIDTH_REn} and increases the length of t_{OSU_REn} by 1/2 * t_{HCLKNODIV}.
- When page mode is used, RDSTRB is replaced by RDPA for page hits.



Figure 4.5. EBI Read Enable Output Timing Diagram

EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.39. EBI TFT Output Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------|----------------|--|-----|-----|------|
| Output hold time, EBI_DCLK to EBI_AD invalid | t _{OH_DCLK} | IOVDD ≥ 1.62 V | -19 + (TFTHOLD * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -10 + (TFTHOLD * t _{HFCOR-ECLK}) | — | — | ns |
| Output setup time, EBI_AD valid to EBI_DCLK | t _{OSU_DCLK} | IOVDD ≥ 1.62 V | -12 + (TFTSET-UP * t _{HFCOR-ECLK}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -11 + (TFTSET-UP * t _{HFCOR-ECLK}) | — | — | ns |



Figure 4.6. EBI TFT Output Timing

EBI Read Enable Timing Requirements

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.40. EBI Read Enable Timing Requirements

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------|---------------------|-----|-----|-----|------|
| Setup time, from EBI_AD valid to trailing EBI_REn edge | t_{SU_REn} | IOVDD \geq 1.62 V | 50 | — | — | ns |
| | | IOVDD \geq 3.0 V | 29 | — | — | ns |
| Hold time, from trailing EBI_REn edge to EBI_AD invalid | t_{H_REn} | IOVDD \geq 1.62 V | -9 | — | — | ns |

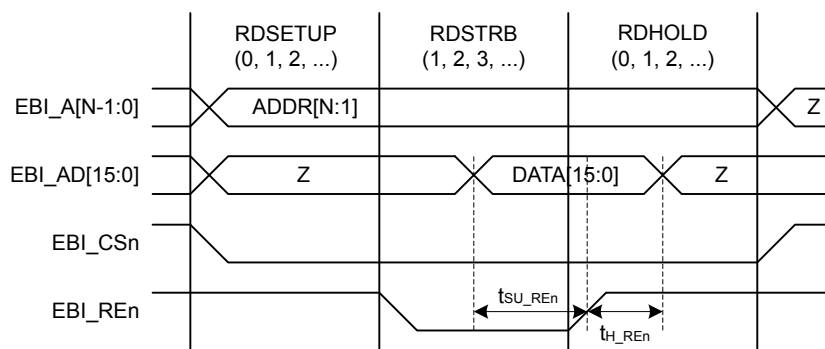


Figure 4.7. EBI Read Enable Timing Requirements

EBI Ready/Wait Timing Requirements

Timing applies to both EBI_REn and EBI_WEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.41. EBI Ready/Wait Timing Requirements

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---------------------|-----------------------------|-----|-----|------|
| Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge | t_{SU_ARDY} | IOVDD \geq 1.62 V | $52 + (3 * t_{HFCOR-ECLK})$ | — | — | ns |
| | | IOVDD \geq 3.0 V | $33 + (3 * t_{HFCOR-ECLK})$ | — | — | ns |
| Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid | t_{H_ARDY} | IOVDD \geq 1.62 V | -9 | — | — | ns |

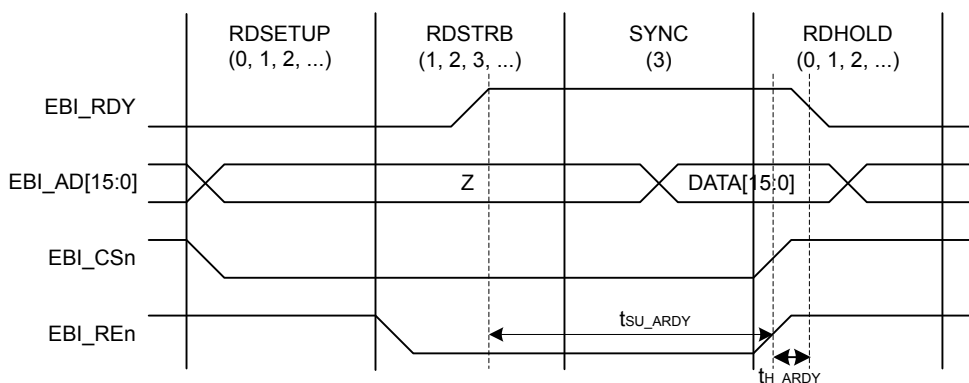


Figure 4.8. EBI Ready/Wait Timing Requirements

4.1.26 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.42. SDIO DS Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 25 | MHz |
| | | Using HF XO | — | — | 21 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HF XO | 18.14 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HF XO | 18.14 | — | — | ns |
| Clock rise time | t _R | | 1.49 | — | 4.86 | ns |
| Clock fall time | t _F | | 1.28 | — | 3.91 | ns |
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | t _{ISU} | | 5 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | t _{IH} | | 0 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | t _{ODLY} | | — | — | 14 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | t _{OH} | | 5 | — | — | ns |

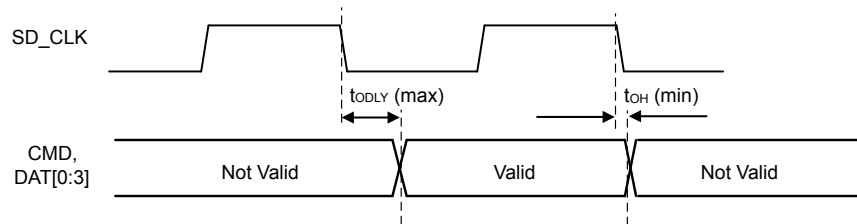
Table 4.43. SDIO DS Mode Timing (Location 1)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|---------------------|-----------------------------------|------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 19 | MHz |
| | | Using HF XO | — | — | 15 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 24.1 | — | — | ns |
| | | Using HF XO | 23.8 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 24.1 | — | — | ns |
| | | Using HF XO | 23.8 | — | — | ns |
| Clock rise time | t _R | | 1.49 | — | 4.86 | ns |
| Clock fall time | t _F | | 1.28 | — | 3.91 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|----------------|-----|-----|------|------|
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | t_{ISU} | | 5 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | t_{IH} | | 0 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | t_{ODLY} | | — | — | 19.1 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | t_{OH} | | 5 | — | — | ns |



Input Timing



Output Timing

Figure 4.9. SDIO DS Mode Timing

SDIO HS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.44. SDIO HS Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 45 | MHz |
| | | Using HFXO | — | — | 45 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 10.57 | — | — | ns |
| | | Using HFXO | 8.66 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 10.57 | — | — | ns |
| | | Using HFXO | 8.66 | — | — | ns |
| Clock rise time | t _R | | 0.83 | — | 3 | ns |
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | t _{ISU} | | 3.2 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | t _{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | t _{ODLY} | | — | — | 15.3 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | t _{OH} | | 2 | — | — | ns |

Table 4.45. SDIO HS Mode Timing (Location 1)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|-----------------------------------|-------|-----|-----|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 35 | MHz |
| | | Using HFXO | — | — | 35 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 13.11 | — | — | ns |
| | | Using HFXO | 10.88 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 13.11 | — | — | ns |
| | | Using HFXO | 10.88 | — | — | ns |
| Clock rise time | t _R | | 0.83 | — | 3 | ns |
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | t _{ISU} | | 3.5 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | t _{IH} | | 2.5 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|----------------|-----|-----|------|------|
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | t_{ODLY} | | — | — | 20.3 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | t_{OH} | | 2 | — | — | ns |



Input Timing



Output Timing

Figure 4.10. SDIO HS Mode Timing

SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.46. SDIO SDR Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 28 | MHz |
| | | Using HFXO | — | — | 28 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 16.4 | — | — | ns |
| | | Using HFXO | 13.61 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 16.4 | — | — | ns |
| | | Using HFXO | 13.61 | — | — | ns |
| Clock rise time | t _R | | 1.8 | — | 6.56 | ns |
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | t _{ISU} | | 5 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | t _{IH} | | 1.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | t _{ODLY} | | — | — | 20 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | t _{OH} | | 0.8 | — | — | ns |

Table 4.47. SDIO SDR Mode Timing (Location 1)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 25 | MHz |
| | | Using HFXO | — | — | 25 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.36 | — | — | ns |
| | | Using HFXO | 15.24 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.36 | — | — | ns |
| | | Using HFXO | 15.24 | — | — | ns |
| Clock rise time | t _R | | 1.8 | — | 6.56 | ns |
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | t _{ISU} | | 5 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | t _{IH} | | 1.5 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|----------------|-----|-----|------|------|
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | t_{ODLY} | | — | — | 24.3 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | t_{OH} | | 0.8 | — | — | ns |



Input Timing



Output Timing

Figure 4.11. SDIO SDR Mode Timing

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

Table 4.48. SDIO DDR Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|-----------------------------------|------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 14 | MHz |
| | | Using HFXO | — | — | 11.5 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 34.5 | — | — | ns |
| | | Using HFXO | 34.7 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 34.5 | — | — | ns |
| | | Using HFXO | 34.7 | — | — | ns |
| Clock rise time | t _R | | 1.79 | — | 6.56 | ns |
| Clock fall time | t _F | | 1.40 | — | 5.12 | ns |
| Input setup time, CMD valid to SD_CLK | t _{ISU} | | 6 | — | — | ns |
| Input hold time, SD_CLK to CMD change | t _{IH} | | 1.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | t _{ODLY} | | — | — | 21.1 | ns |
| Output hold time, SD_CLK to CMD change | t _{OH} | | 2 | — | — | ns |
| Input setup time, DAT[0:3] valid to SD_CLK | t _{ISU2X} | | 6.3 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:3] change | t _{IH2X} | | 1.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:3] valid | t _{ODLY2X} | | — | — | 30.8 | ns |
| Output hold time, SD_CLK to DAT[0:3] change | t _{OH2X} | | 2 | — | — | ns |

Table 4.49. SDIO DDR Mode Timing (Location 1)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|---------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 12.5 | MHz |
| | | Using HFXO | — | — | 10 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 36.72 | — | — | ns |
| | | Using HFXO | 38.1 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------|-----------------------------------|-------|-----|-------|------|
| Clock high time | t_{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 36.72 | — | — | ns |
| | | Using HFXO | 38.1 | — | — | ns |
| Clock rise time | t_R | | 1.79 | — | 6.56 | ns |
| Clock fall time | t_F | | 1.40 | — | 5.12 | ns |
| Input setup time, CMD valid to SD_CLK | t_{ISU} | | 7 | — | — | ns |
| Input hold time, SD_CLK to CMD change | t_{IH} | | 1.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | t_{ODLY} | | — | — | 24.81 | ns |
| Output hold time, SD_CLK to CMD change | t_{OH} | | 2 | — | — | ns |
| Input setup time, DAT[0:3] valid to SD_CLK | t_{ISU2X} | | 8.3 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:3] change | t_{IH2X} | | 1.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:3] valid | t_{ODLY2X} | | — | — | 35.1 | ns |
| Output hold time, SD_CLK to DAT[0:3] change | t_{OH2X} | | 2 | — | — | ns |



Input Timing



Output Timing

Figure 4.12. SDIO DDR Mode Timing

SDIO MMC Legacy Mode Timing

Timing is specified with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.50. SDIO MMC Legacy Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 28 | MHz |
| | | Using HFXO | — | — | 28 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 16.96 | — | — | ns |
| | | Using HFXO | 14.28 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 16.96 | — | — | ns |
| | | Using HFXO | 14.28 | — | — | ns |
| Clock rise time | t _R | | 1.8 | — | 5.6 | ns |
| Input setup time, CMD, DAT[0:7] valid to SD_CLK | t _{ISU} | | 4.8 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:7] change | t _{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:7] valid | t _{ODLY} | | — | — | 18.8 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:7] change | t _{OH} | | 3 | — | — | ns |

Table 4.51. SDIO MMC Legacy Mode Timing (Location 1)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|-----------------------------------|------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 25 | MHz |
| | | Using HFXO | — | — | 25 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HFXO | 15.2 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HFXO | 15.2 | — | — | ns |
| Clock rise time | t _R | | 1.8 | — | 5.6 | ns |
| Input setup time, CMD, DAT[0:7] valid to SD_CLK | t _{ISU} | | 4.8 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:7] change | t _{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:7] valid | t _{ODLY} | | — | — | 23.6 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------|----------------|-----|-----|-----|------|
| Output hold time, SD_CLK to CMD, DAT[0:7] change | t_{OH} | | 3 | — | — | ns |

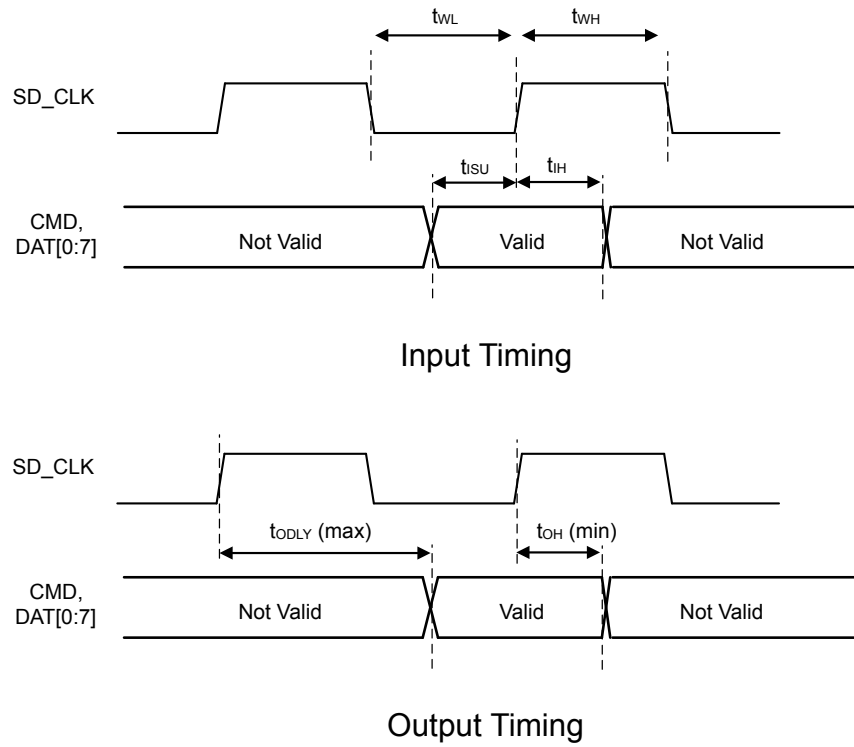


Figure 4.13. SDIO MMC Legacy Mode Timing

SDIO MMC SDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.52. SDIO MMC SDR Mode Timing (Location 0, 1.8V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 28 | MHz |
| | | Using HFXO | — | — | 28 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 16.96 | — | — | ns |
| | | Using HFXO | 14.28 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 16.96 | — | — | ns |
| | | Using HFXO | 14.28 | — | — | ns |
| Clock rise time | t _R | | 1.8 | — | 5.6 | ns |
| Input setup time, CMD, DAT[0:7] valid to SD_CLK | t _{ISU} | | 4.8 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:7] change | t _{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:7] valid | t _{ODLY} | | — | — | 18.8 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:7] change | t _{OH} | | 2.85 | — | — | ns |

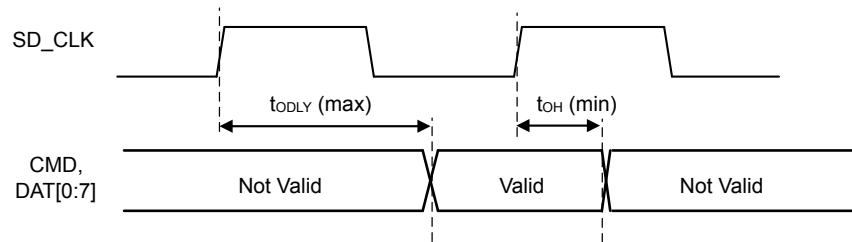
Table 4.53. SDIO MMC SDR Mode Timing (Location 1, 1.8V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|-----------------------------------|------|-----|-----|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 25 | MHz |
| | | Using HFXO | — | — | 25 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HFXO | 15.2 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HFXO | 15.2 | — | — | ns |
| Clock rise time | t _R | | 1.8 | — | 5.6 | ns |
| Input setup time, CMD, DAT[0:7] valid to SD_CLK | t _{ISU} | | 4.8 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:7] change | t _{IH} | | 2.5 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|----------------|-----|-----|------|------|
| Output delay time, SD_CLK to CMD, DAT[0:7] valid | t_{ODLY} | | — | — | 23.6 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:7] change | t_{OH} | | 3 | — | — | ns |



Input Timing



Output Timing

Figure 4.14. SDIO MMC SDR Mode Timing

SDIO MMC SDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.54. SDIO MMC SDR Mode Timing (Location 0, 3V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|-----------------------------------|------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 49 | MHz |
| | | Using HFXO | — | — | 49 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 9.7 | — | — | ns |
| | | Using HFXO | 7.8 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 9.7 | — | — | ns |
| | | Using HFXO | 7.8 | — | — | ns |
| Clock rise time | t _R | | 0.85 | — | 2.5 | ns |
| Input setup time, CMD, DAT[0:7] valid to SD_CLK | t _{ISU} | | 3.13 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:7] change | t _{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:7] valid | t _{ODLY} | | — | — | 15.2 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:7] change | t _{OH} | | 3 | — | — | ns |

Table 4.55. SDIO MMC SDR Mode Timing (Location 1, 3V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|-----------------------------------|------|-----|-----|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 38 | MHz |
| | | Using HFXO | — | — | 38 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 12 | — | — | ns |
| | | Using HFXO | 10 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 12 | — | — | ns |
| | | Using HFXO | 10 | — | — | ns |
| Clock rise time | t _R | | 0.85 | — | 2.5 | ns |
| Input setup time, CMD, DAT[0:7] valid to SD_CLK | t _{ISU} | | 3.4 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:7] change | t _{IH} | | 2.5 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|----------------|-----|-----|-------|------|
| Output delay time, SD_CLK to CMD, DAT[0:7] valid | t_{ODLY} | | — | — | 19.83 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:7] change | t_{OH} | | 3 | — | — | ns |



Input Timing



Output Timing

Figure 4.15. SDIO MMC SDR Mode Timing

SDIO MMC DDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.56. SDIO MMC DDR Mode Timing (Location 0, 1.8V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|-----------------------------------|------|-----|-------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 14.5 | MHz |
| | | Using HFXO | — | — | 12 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 31.6 | — | — | ns |
| | | Using HFXO | 31.2 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 31.6 | — | — | ns |
| | | Using HFXO | 31.2 | — | — | ns |
| Clock rise time | t _R | | 1.79 | — | 5.54 | ns |
| Clock fall time | t _F | | 1.40 | — | 4.21 | ns |
| Input setup time, CMD valid to SD_CLK | t _{ISU} | | 5.7 | — | — | ns |
| Input hold time, SD_CLK to CMD change | t _{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | t _{ODLY} | | — | — | 19.81 | ns |
| Output hold time, SD_CLK to CMD change | t _{OH} | | 3 | — | — | ns |
| Input setup time, DAT[0:7] valid to SD_CLK | t _{ISU2X} | | 7.6 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:7] change | t _{IH2X} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:7] valid | t _{ODLY2X} | | — | — | 30.3 | ns |
| Output hold time, SD_CLK to DAT[0:7] change | t _{OH2X} | | 3 | — | — | ns |

Table 4.57. SDIO MMC DDR Mode Timing (Location 1, 1.8V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|---------------------|-----------------------------------|------|-----|-----|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 12 | MHz |
| | | Using HFXO | — | — | 10 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 38.2 | — | — | ns |
| | | Using HFXO | 38 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------|-----------------------------------|------|-----|-------|------|
| Clock high time | t_{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 38.2 | — | — | ns |
| | | Using HFXO | 38 | — | — | ns |
| Clock rise time | t_R | | 1.79 | — | 5.54 | ns |
| Clock fall time | t_F | | 1.40 | — | 4.21 | ns |
| Input setup time, CMD valid to SD_CLK | t_{ISU} | | 7.1 | — | — | ns |
| Input hold time, SD_CLK to CMD change | t_{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | t_{ODLY} | | — | — | 23.87 | ns |
| Output hold time, SD_CLK to CMD change | t_{OH} | | 3 | — | — | ns |
| Input setup time, DAT[0:7] valid to SD_CLK | t_{ISU2X} | | 8.24 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:7] change | t_{IH2X} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:7] valid | t_{ODLY2X} | | — | — | 34.94 | ns |
| Output hold time, SD_CLK to DAT[0:7] change | t_{OH2X} | | 3 | — | — | ns |



Input Timing



Output Timing

Figure 4.16. SDIO MMC DDR Mode Timing

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

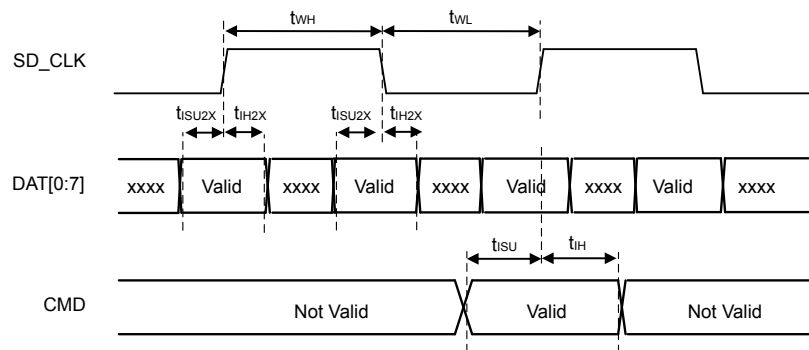
Table 4.58. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|-----------------------------------|-------|-----|-------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 16 | MHz |
| | | Using HFXO | — | — | 13.5 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 29.69 | — | — | ns |
| | | Using HFXO | 29.63 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 29.69 | — | — | ns |
| | | Using HFXO | 29.63 | — | — | ns |
| Clock rise time | t _R | | 0.84 | — | 2.5 | ns |
| Clock fall time | t _F | | 0.77 | — | 2.2 | ns |
| Input setup time, CMD valid to SD_CLK | t _{ISU} | | 4.3 | — | — | ns |
| Input hold time, SD_CLK to CMD change | t _{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | t _{ODLY} | | — | — | 16.47 | ns |
| Output hold time, SD_CLK to CMD change | t _{OH} | | 3 | — | — | ns |
| Input setup time, DAT[0:7] valid to SD_CLK | t _{ISU2X} | | 6 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:7] change | t _{IH2X} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:7] valid | t _{ODLY2X} | | — | — | 26.6 | ns |
| Output hold time, SD_CLK to DAT[0:7] change | t _{OH2X} | | 3 | — | — | ns |

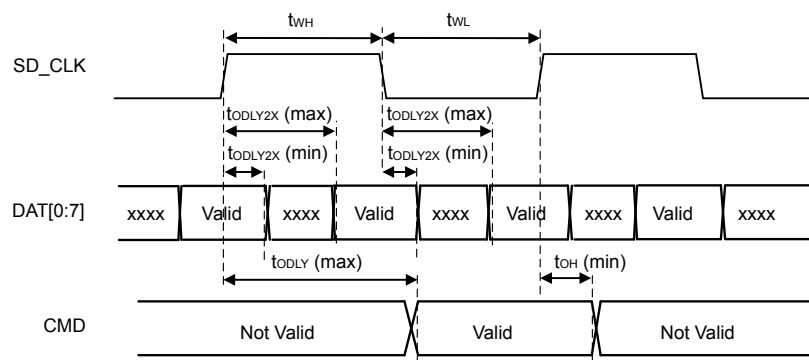
Table 4.59. SDIO MMC DDR Mode Timing (Location 1, 3V I/O)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|---------------------|-----------------------------------|------|-----|------|------|
| Clock frequency during data transfer | F _{SD_CLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 12.5 | MHz |
| | | Using HFXO | — | — | 11 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 36.7 | — | — | ns |
| | | Using HFXO | 34.6 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------|-----------------------------------|------|-----|-------|------|
| Clock high time | t_{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 36.7 | — | — | ns |
| | | Using HFXO | 34.6 | — | — | ns |
| Clock rise time | t_R | | 0.84 | — | 2.5 | ns |
| Clock fall time | t_F | | 0.77 | — | 2.2 | ns |
| Input setup time, CMD valid to SD_CLK | t_{ISU} | | 5.1 | — | — | ns |
| Input hold time, SD_CLK to CMD change | t_{IH} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | t_{ODLY} | | — | — | 20.9 | ns |
| Output hold time, SD_CLK to CMD change | t_{OH} | | 3 | — | — | ns |
| Input setup time, DAT[0:7] valid to SD_CLK | t_{ISU2X} | | 6.8 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:7] change | t_{IH2X} | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:7] valid | t_{ODLY2X} | | — | — | 31.37 | ns |
| Output hold time, SD_CLK to DAT[0:7] change | t_{OH2X} | | 3 | — | — | ns |



Input Timing



Output Timing

Figure 4.17. SDIO MMC DDR Mode Timing

SDIO SPI Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.60. SDIO SPI Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|-------------------|-----------------------------------|-------|-----|------|------|
| Clock frequency during data transfer | F _{SCLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 25 | MHz |
| | | Using HFXO | — | — | 21 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HFXO | 18.14 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 18.3 | — | — | ns |
| | | Using HFXO | 18.14 | — | — | ns |
| Clock rise time | t _R | | 1.49 | — | 4.86 | ns |
| Clock fall time | t _F | | 1.28 | — | 3.91 | ns |
| Input setup time, MISO valid to SCLK | t _{ISU} | | 5 | — | — | ns |
| Input hold time, SCLK to MISO change | t _{IH} | | 0 | — | — | ns |
| Output delay time, SCLK to MOSI valid | t _{ODLY} | | — | — | 14 | ns |
| Output hold time, SCLK to MOSI change | t _{OH} | | 5 | — | — | ns |

Table 4.61. SDIO SPI Mode Timing (Location 1)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|-------------------|-----------------------------------|------|-----|------|------|
| Clock frequency during data transfer | F _{SCLK} | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 19 | MHz |
| | | Using HFXO | — | — | 15 | MHz |
| Clock low time | t _{WL} | Using HFRCO, AUXHFRCO, or USHFRCO | 24.1 | — | — | ns |
| | | Using HFXO | 23.8 | — | — | ns |
| Clock high time | t _{WH} | Using HFRCO, AUXHFRCO, or USHFRCO | 24.1 | — | — | ns |
| | | Using HFXO | 23.8 | — | — | ns |
| Clock rise time | t _R | | 1.49 | — | 4.86 | ns |
| Clock fall time | t _F | | 1.28 | — | 3.91 | ns |
| Input setup time, MISO valid to SCLK | t _{ISU} | | 5 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|------------|----------------|-----|-----|------|------|
| Input hold time, SCLK to MISO change | t_{IH} | | 0 | — | — | ns |
| Output delay time, SCLK to MOSI valid | t_{ODLY} | | — | — | 19.1 | ns |
| Output hold time, SCLK to MOSI change | t_{OH} | | 5 | — | — | ns |

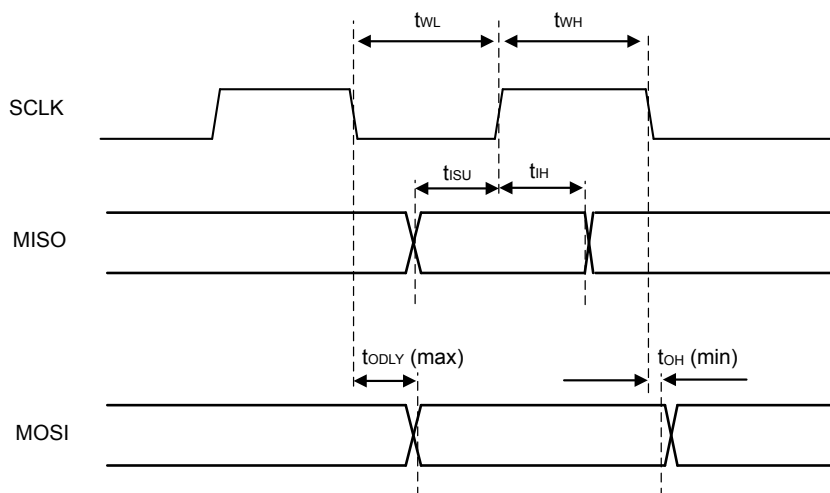


Figure 4.18. SDIO SPI Mode Timing

4.1.27 Quad SPI (QSPI)

4.1.27.1 QSPI SDR Mode

QSPI SDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 20, RX DLL = 45, 5-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.62. QSPI SDR Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|----------|----------------|------------------------|-----|-----------|------|
| Full SCLK period | T | | $(1/F_{SCLK})^* 0.965$ | — | — | ns |
| Output valid | t_{OV} | | — | — | T/2 - 3.0 | ns |
| Output hold | t_{OH} | | T/2 - 21.4 | — | — | ns |
| Input setup | t_{SU} | | 25.96 - T/2 | — | — | ns |
| Input hold | t_{H} | | T/2 - 1.0 | — | — | ns |

QSPI SDR Mode Timing (Optimal Conditions)

Timing is specified at IOVDD ≥ 3.0V, using internal HFRCO oscillator and with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 17, RX DLL = 29, 5-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.63. QSPI SDR Mode Timing (Optimized at 3.0V, Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|-----------------|----------------|---------------------------|-----|-----------|------|
| Full SCLK period | T | | $(1/F_{SCLK})^*$ 0.965 | — | — | ns |
| Output valid | t _{OV} | | — | — | T/2 - 2.2 | ns |
| Output hold | t _{OH} | | T/2 - 19.13 | — | — | ns |
| Input setup | t _{SU} | | 15.33 - T/2 | — | — | ns |
| Input hold | t _H | | T/2 - 4.1 | — | — | ns |

QSPI SDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 15, RX DLL = 47, 5-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.64. QSPI SDR Mode Timing (Locations 1, 2)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|----------|----------------|------------------------|-----|-----------|------|
| Full SCLK period | T | | $(1/F_{SCLK}) * 0.965$ | — | — | ns |
| Output valid | t_{OV} | | — | — | T/2 - 2.6 | ns |
| Output hold | t_{OH} | | T/2 - 19.26 | — | — | ns |
| Input setup | t_{SU} | | 25.47 - T/2 | — | — | ns |
| Input hold | t_H | | T/2 - 0.5 | — | — | ns |



Figure 4.19. QSPI SDR Timing Diagrams

QSPI SDR Flash Timing Example

This example uses timing values from SDR Mode Timing (Optimal Conditions) to demonstrate the calculation of allowable flash timing using the QSPI in SDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 40 MHz:
- The resulting minimum period, $T(\min) = (1/F_{SCLK}) * 0.965 = 24.125$ ns.
- Flash will see a minimum setup time of $T/2 - t_{OV} = T/2 - (T/2 - 2.2) = 2.4$ ns.
- Flash will see a minimum hold time of $T/2 + t_{OH} = T/2 + (T/2 - 19.13) = T - 19.13 = 24.125 - 19.13 = 4.9$ ns.
- Flash can have a maximum output valid time of $T/2 - t_{SU} = T/2 - (15.33 - T/2) = T - 15.33 = 24.125 - 15.33 = 8.8$ ns.
- Flash can have a minimum output hold time of $t_H - T/2 = (T/2 - 4.1) - T/2 = -4.1$ ns.

4.1.27.2 QSPI DDR Mode

QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 20, RX DLL = 52, 5-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.65. QSPI DDR Mode Timing (Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|----------|--------------------------|-------------------------------|-----|-----------|------|
| Half SCLK period | T/2 | HFXO | $(1/F_{SCLK})^*$ 0.4 - 0.4 | — | — | ns |
| | | HFRCO, AUXHFRCO, USHFRCO | $(1/F_{SCLK})^*$ 0.44 | — | — | ns |
| Output valid | t_{OV} | | — | — | T/2 - 2.3 | ns |
| Output hold | t_{OH} | | T/2 - 18.63 | — | — | ns |
| Input setup | t_{SU} | | 14.85 | — | — | ns |
| Input hold | t_{H} | | -2.2 | — | — | ns |

QSPI DDR Mode Timing (Optimal Conditions)

Timing is specified at IOVDD ≥ 3.0V, using internal HFRCO oscillator and with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 17, RX DLL = 37, 5-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.66. QSPI DDR Mode Timing (Optimized at 3.0V, Location 0)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|----------|--------------------------|--------------------------|-----|-----------|------|
| Half SCLK period | T/2 | HFRCO, AUXHFRCO, USHFRCO | $(1/F_{SCLK})^*$ 0.44 | — | — | ns |
| Output valid | t_{OV} | | — | — | T/2 - 2.4 | ns |
| Output hold | t_{OH} | | T/2 - 19.02 | — | — | ns |
| Input setup | t_{SU} | | 12.93 | — | — | ns |
| Input hold | t_{H} | | -0.8 | — | — | ns |

QSPI DDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 17, RX DLL = 50, 5-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.67. QSPI DDR Mode Timing (Locations 1, 2)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------|----------|--------------------------|----------------------------|-----|-----------|------|
| Half SCLK period | T/2 | HFXO | $(1/F_{SCLK})^* 0.4 - 0.4$ | — | — | ns |
| | | HFRCO, AUXHFRCO, USHFRCO | $(1/F_{SCLK})^* 0.44$ | — | — | ns |
| Output valid | t_{OV} | | — | — | T/2 - 2.8 | ns |
| Output hold | t_{OH} | | T/2 - 15.21 | — | — | ns |
| Input setup | t_{SU} | | 9.2 | — | — | ns |
| Input hold | t_H | | -0.38 | — | — | ns |

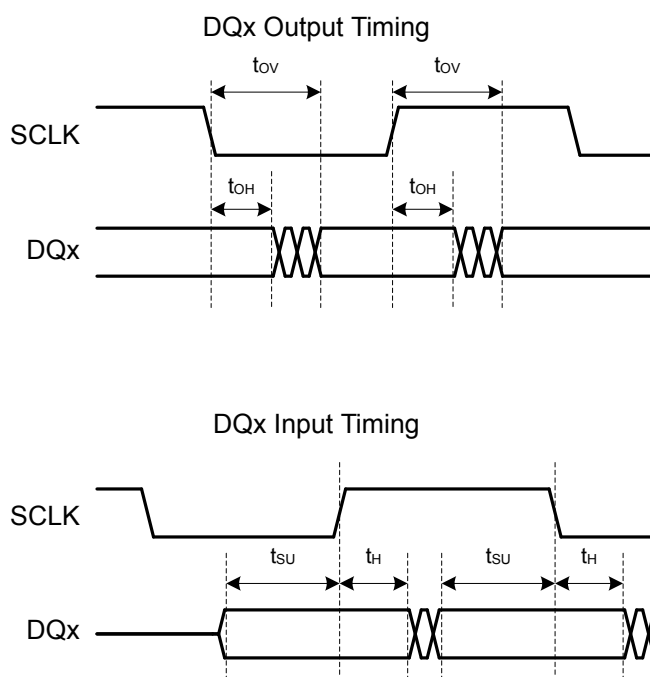


Figure 4.20. QSPI DDR Timing Diagrams

QSPI DDR Flash Timing Example

This example uses timing values for DDR Mode Timing (Optimal Conditions) to demonstrate the calculation of allowable flash timing using the QSPI in DDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 20 MHz from the HFXO clock source:
- The resulting minimum half-period, $T/2(\min) = (1/F_{SCLK}) * 0.44 = 22$ ns.
- Flash will see a minimum setup time of $T/2 - t_{OV} = T/2 - (T/2 - 2.2) = 2.4$ ns.
- Flash will see a minimum hold time of $t_{OH} = T/2 - 19.02 = 22 - 19.02 = 2.98$ ns.
- Flash can have a maximum output valid time of $T/2 - t_{SU} = T/2 - 12.93 = 22 - 12.93 = 9.07$ ns.
- Flash can have a minimum output hold time of $t_H = -0.8$ ns.

4.1.28 PDM

PDM Timing

Timing is specified for all route locations, 10 pF to 25 pF loading on PDM_CLK, and slew rate for PDM_CLK set to 7.

Table 4.68. Pulse Density Modulation (PDM) Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|-------------------------------------|------|-----|------|------|
| PDM_CLK frequency during data transfer | $F_{\text{PDM_CLK}}$ | Microphone mode, VSCALE2 or VSCALE0 | — | — | 4.8 | MHz |
| | | Sensor mode, VSCALE2 | — | — | 20 | MHz |
| | | Sensor mode, VSCALE0 | — | — | 10 | MHz |
| PDM_CLK duty cycle | $DC_{\text{PDM_CLK}}$ | | 47.5 | — | 52.5 | % |
| PDM_CLK rise time | t_{R} | | — | — | 7.5 | ns |
| PDM_CLK fall time | t_{F} | | — | — | 7.5 | ns |
| Input setup time | t_{ISU} | | 20 | — | — | ns |
| Input hold time | t_{IH} | VSCALE2 | 3 | — | — | ns |
| | | VSCALE0 | 4 | — | — | ns |



Figure 4.21. PDM Timing Diagrams

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current



Figure 4.22. EM0 Full Speed Active Mode Typical Supply Current vs. Temperature



Figure 4.23. EM0 Active Mode Typical Supply Current vs. Temperature

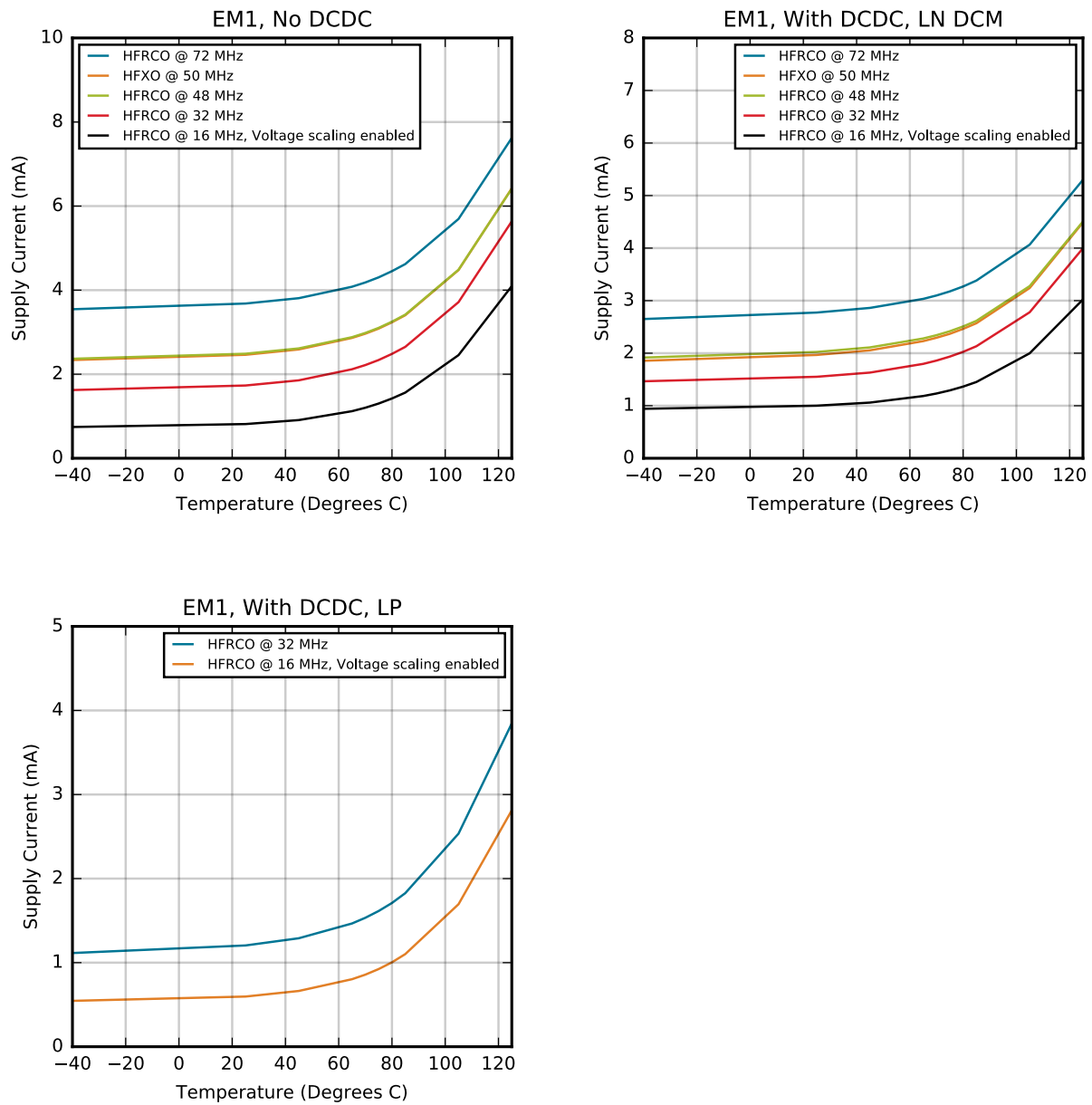


Figure 4.24. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

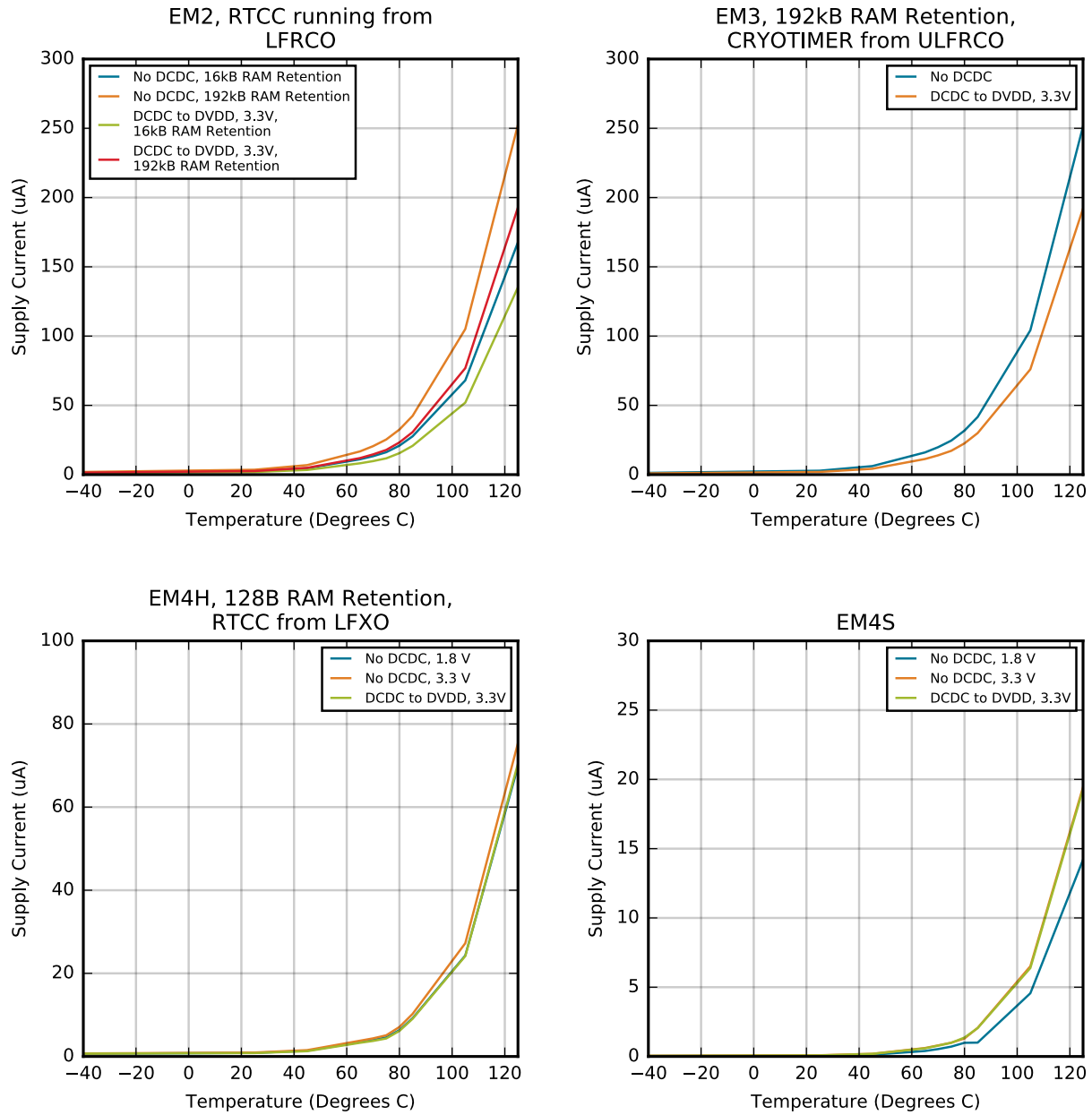


Figure 4.25. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature



Figure 4.26. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

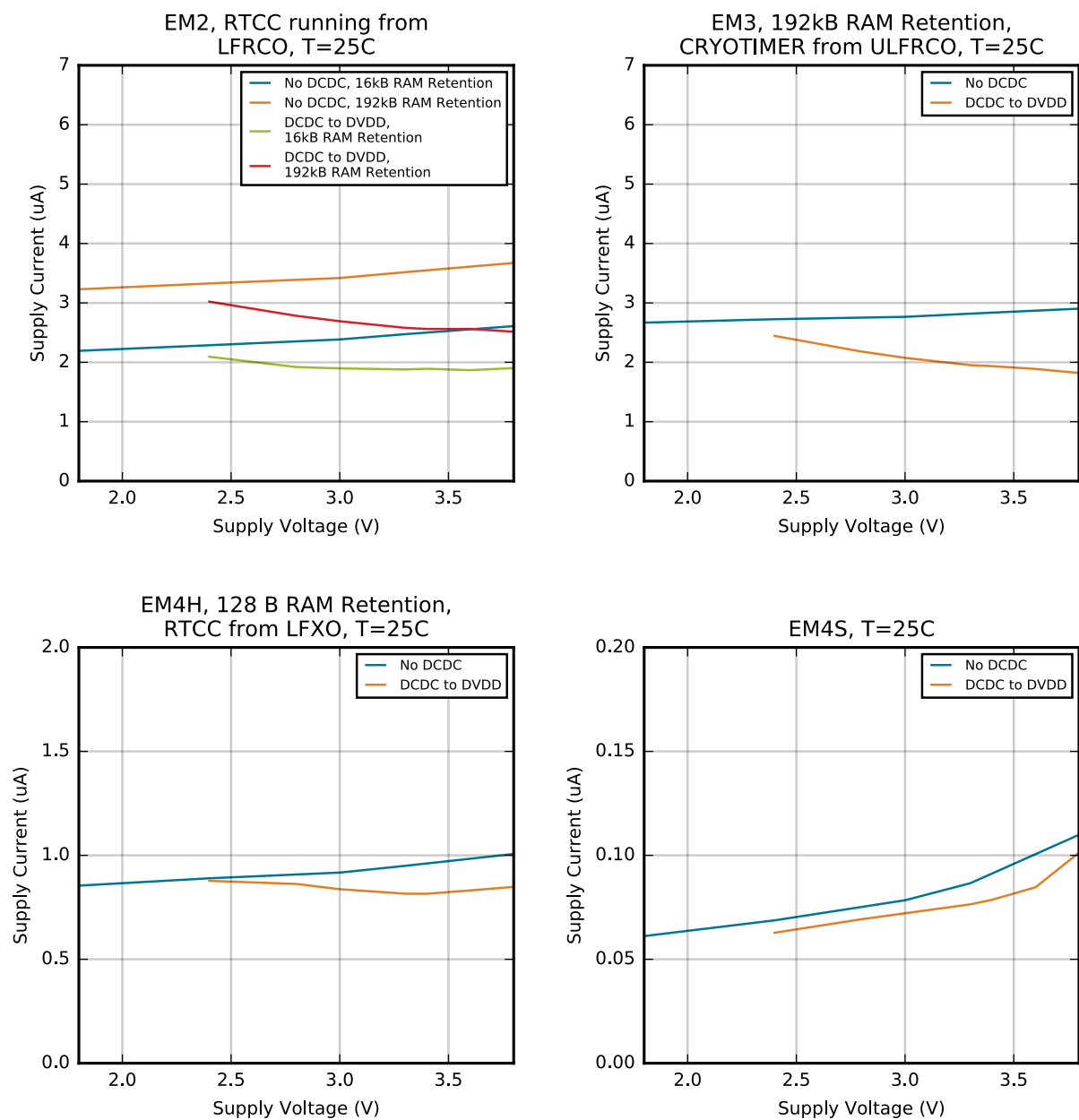


Figure 4.27. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 4.7 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

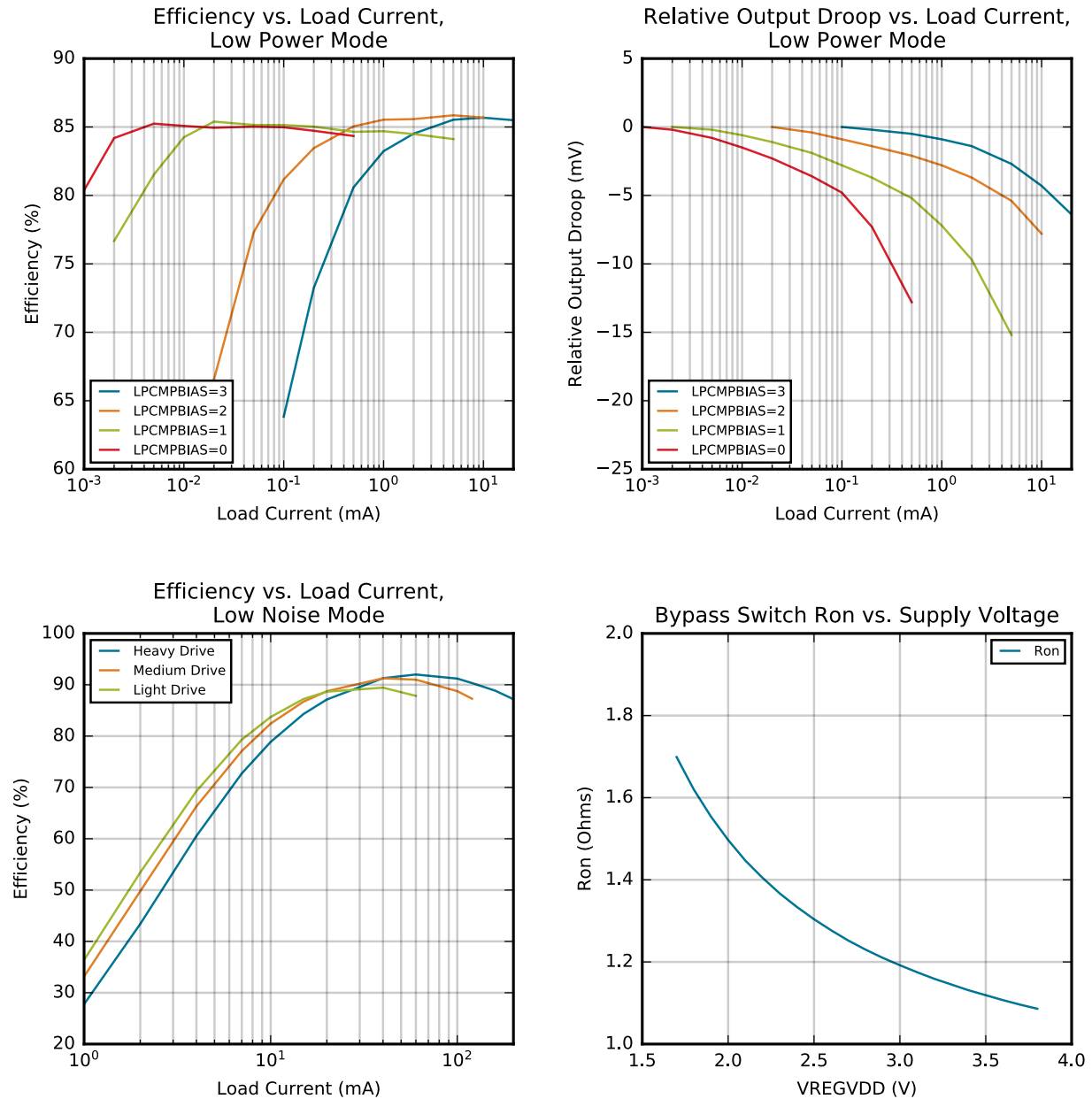


Figure 4.28. DC-DC Converter Typical Performance Characteristics



Figure 4.29. DC-DC Converter Transition Waveforms

5. Pin Definitions

5.1 EFM32GG12B8xx in BGA120 Device Pinout



Figure 5.1. EFM32GG12B8xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.1. EFM32GG12B8xx in BGA120 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PE15 | A1 | GPIO | PE14 | A2 | GPIO |
| PE12 | A3 | GPIO | PE9 | A4 | GPIO |
| PD11 | A5 | GPIO | PD9 | A6 | GPIO |
| PF7 | A7 | GPIO | PF5 | A8 | GPIO |
| PF14 | A9 | GPIO (5V) | PF12 | A10 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---|---|----------|-----------------------------------|--|
| VREGI | A11 | Input to 5 V regulator. | VREGO | A12 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |
| PF11 | A13 | GPIO (5V) | PA15 | B1 | GPIO |
| PE13 | B2 | GPIO | PE11 | B3 | GPIO |
| PE8 | B4 | GPIO | PD12 | B5 | GPIO |
| PD10 | B6 | GPIO | PF8 | B7 | GPIO |
| PF6 | B8 | GPIO | PF13 | B9 | GPIO (5V) |
| PF4 | B10 | GPIO | PF3 | B11 | GPIO |
| VBUS | B12 | USB VBUS signal and auxiliary input to 5 V regulator. | PF10 | B13 | GPIO (5V) |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| VSS | C5 C8 H3 J3 K11 L5 L8 | Ground | IOVDD1 | C6 | Digital IO power supply 1. |
| PF9 | C7 | GPIO | IOVDD0 | C9 G3 J11 K3 L4 L9 | Digital IO power supply 0. |
| PF2 | C10 | GPIO | PF1 | C11 | GPIO (5V) |
| PC14 | C12 | GPIO (5V) | PC15 | C13 | GPIO (5V) |
| PA3 | D1 | GPIO | PA2 | D2 | GPIO |
| PB15 | D3 | GPIO (5V) | PF0 | D11 | GPIO (5V) |
| PC12 | D12 | GPIO (5V) | PC13 | D13 | GPIO (5V) |
| PA6 | E1 | GPIO | PA5 | E2 | GPIO |
| PA4 | E3 | GPIO | PC9 | E11 | GPIO (5V) |
| PC10 | E12 | GPIO (5V) | PC11 | E13 | GPIO (5V) |
| PB0 | F1 | GPIO | PB1 | F2 | GPIO |
| PB2 | F3 | GPIO | PE6 | F11 | GPIO |
| PE7 | F12 | GPIO | PC8 | F13 | GPIO (5V) |
| PB3 | G1 | GPIO | PB4 | G2 | GPIO |
| PE3 | G11 | GPIO | PE4 | G12 | GPIO |
| PE5 | G13 | GPIO | PB5 | H1 | GPIO |
| PB6 | H2 | GPIO | DVDD | H11 | Digital power supply. |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|--------|---|
| PE2 | H12 | GPIO | DECOUPLE | H13 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PD14 | J1 | GPIO (5V) | PD15 | J2 | GPIO (5V) |
| PE1 | J12 | GPIO (5V) | VREGVDD | J13 | Voltage regulator VDD input |
| PC0 | K1 | GPIO (5V) | PC1 | K2 | GPIO (5V) |
| PE0 | K12 | GPIO (5V) | VREGSW | K13 | DCDC regulator switching node |
| PC2 | L1 | GPIO (5V) | PC3 | L2 | GPIO (5V) |
| PA7 | L3 | GPIO | PB9 | L6 | GPIO (5V) |
| PB10 | L7 | GPIO (5V) | PD1 | L10 | GPIO |
| PC6 | L11 | GPIO | PC7 | L12 | GPIO |
| VREGVSS | L13 | Voltage regulator VSS | PB7 | M1 | GPIO |
| PC4 | M2 | GPIO | PA8 | M3 | GPIO |
| PA10 | M4 | GPIO | PA13 | M5 | GPIO (5V) |
| PA14 | M6 | GPIO | RESETn | M7 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB12 | M8 | GPIO | PD0 | M9 | GPIO (5V) |
| PD2 | M10 | GPIO (5V) | PD3 | M11 | GPIO |
| PD4 | M12 | GPIO | PD8 | M13 | GPIO |
| PB8 | N1 | GPIO | PC5 | N2 | GPIO |
| PA9 | N3 | GPIO | PA11 | N4 | GPIO |
| PA12 | N5 | GPIO (5V) | PB11 | N6 | GPIO |
| BODEN | N7 | Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. | PB13 | N8 | GPIO |
| PB14 | N9 | GPIO | AVDD | N10 | Analog power supply. |
| PD5 | N11 | GPIO | PD6 | N12 | GPIO |
| PD7 | N13 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.2 EFM32GG12B5xx in BGA120 Device Pinout

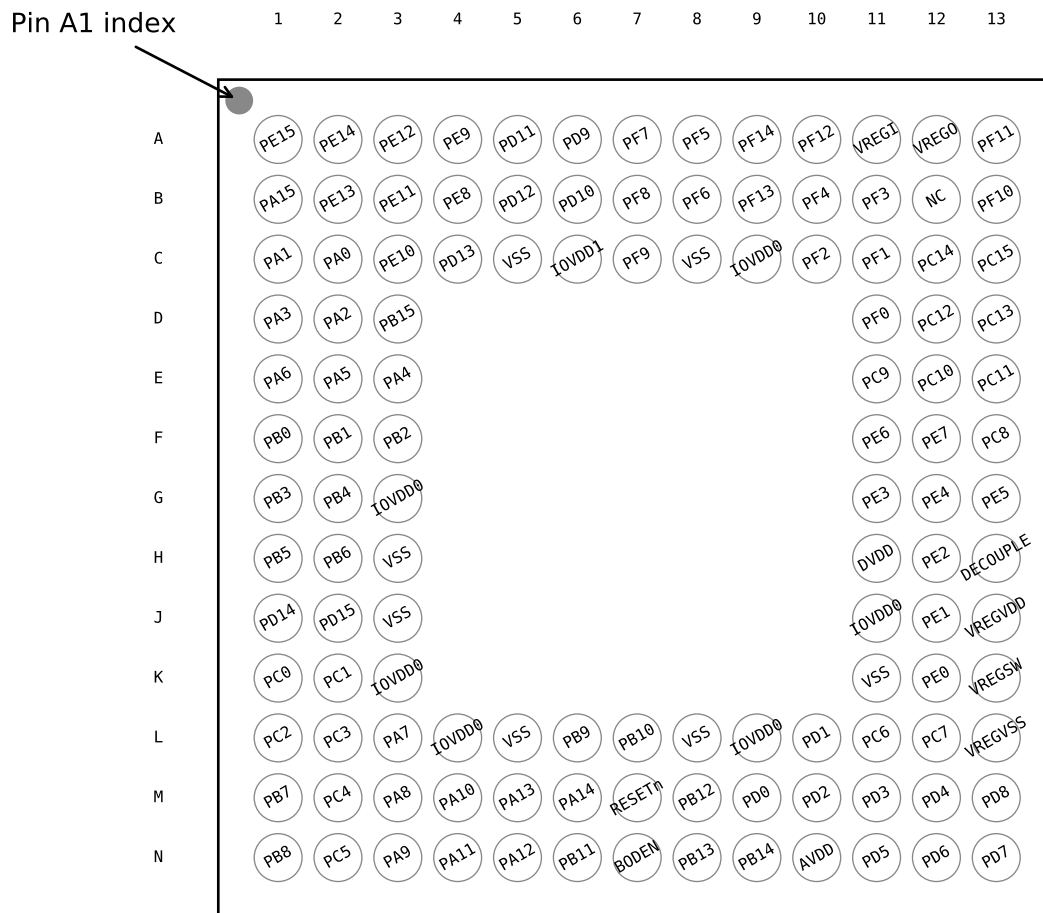


Figure 5.2. EFM32GG12B5xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.2. EFM32GG12B5xx in BGA120 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------|----------|--------|--|
| PE15 | A1 | GPIO | PE14 | A2 | GPIO |
| PE12 | A3 | GPIO | PE9 | A4 | GPIO |
| PD11 | A5 | GPIO | PD9 | A6 | GPIO |
| PF7 | A7 | GPIO | PF5 | A8 | GPIO |
| PF14 | A9 | GPIO (5V) | PF12 | A10 | GPIO (5V) |
| VREGI | A11 | Input to 5 V regulator. | VREGO | A12 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---|-------------|----------|-----------------------------------|--|
| PF11 | A13 | GPIO (5V) | PA15 | B1 | GPIO |
| PE13 | B2 | GPIO | PE11 | B3 | GPIO |
| PE8 | B4 | GPIO | PD12 | B5 | GPIO |
| PD10 | B6 | GPIO | PF8 | B7 | GPIO |
| PF6 | B8 | GPIO | PF13 | B9 | GPIO (5V) |
| PF4 | B10 | GPIO | PF3 | B11 | GPIO |
| NC | B12 | No Connect. | PF10 | B13 | GPIO (5V) |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| VSS | C5 C8 H3 J3 K11 L5 L8 | Ground | IOVDD1 | C6 | Digital IO power supply 1. |
| PF9 | C7 | GPIO | IOVDD0 | C9 G3 J11 K3 L4 L9 | Digital IO power supply 0. |
| PF2 | C10 | GPIO | PF1 | C11 | GPIO (5V) |
| PC14 | C12 | GPIO (5V) | PC15 | C13 | GPIO (5V) |
| PA3 | D1 | GPIO | PA2 | D2 | GPIO |
| PB15 | D3 | GPIO (5V) | PF0 | D11 | GPIO (5V) |
| PC12 | D12 | GPIO (5V) | PC13 | D13 | GPIO (5V) |
| PA6 | E1 | GPIO | PA5 | E2 | GPIO |
| PA4 | E3 | GPIO | PC9 | E11 | GPIO (5V) |
| PC10 | E12 | GPIO (5V) | PC11 | E13 | GPIO (5V) |
| PB0 | F1 | GPIO | PB1 | F2 | GPIO |
| PB2 | F3 | GPIO | PE6 | F11 | GPIO |
| PE7 | F12 | GPIO | PC8 | F13 | GPIO (5V) |
| PB3 | G1 | GPIO | PB4 | G2 | GPIO |
| PE3 | G11 | GPIO | PE4 | G12 | GPIO |
| PE5 | G13 | GPIO | PB5 | H1 | GPIO |
| PB6 | H2 | GPIO | DVDD | H11 | Digital power supply. |
| PE2 | H12 | GPIO | DECOUPLE | H13 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PD14 | J1 | GPIO (5V) | PD15 | J2 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|--------|---|
| PE1 | J12 | GPIO (5V) | VREGVDD | J13 | Voltage regulator VDD input |
| PC0 | K1 | GPIO (5V) | PC1 | K2 | GPIO (5V) |
| PE0 | K12 | GPIO (5V) | VREGSW | K13 | DCDC regulator switching node |
| PC2 | L1 | GPIO (5V) | PC3 | L2 | GPIO (5V) |
| PA7 | L3 | GPIO | PB9 | L6 | GPIO (5V) |
| PB10 | L7 | GPIO (5V) | PD1 | L10 | GPIO |
| PC6 | L11 | GPIO | PC7 | L12 | GPIO |
| VREGVSS | L13 | Voltage regulator VSS | PB7 | M1 | GPIO |
| PC4 | M2 | GPIO | PA8 | M3 | GPIO |
| PA10 | M4 | GPIO | PA13 | M5 | GPIO (5V) |
| PA14 | M6 | GPIO | RESETn | M7 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB12 | M8 | GPIO | PD0 | M9 | GPIO (5V) |
| PD2 | M10 | GPIO (5V) | PD3 | M11 | GPIO |
| PD4 | M12 | GPIO | PD8 | M13 | GPIO |
| PB8 | N1 | GPIO | PC5 | N2 | GPIO |
| PA9 | N3 | GPIO | PA11 | N4 | GPIO |
| PA12 | N5 | GPIO (5V) | PB11 | N6 | GPIO |
| BODEN | N7 | Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. | PB13 | N8 | GPIO |
| PB14 | N9 | GPIO | AVDD | N10 | Analog power supply. |
| PD5 | N11 | GPIO | PD6 | N12 | GPIO |
| PD7 | N13 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.3 EFM32GG12B4xx in BGA120 Device Pinout

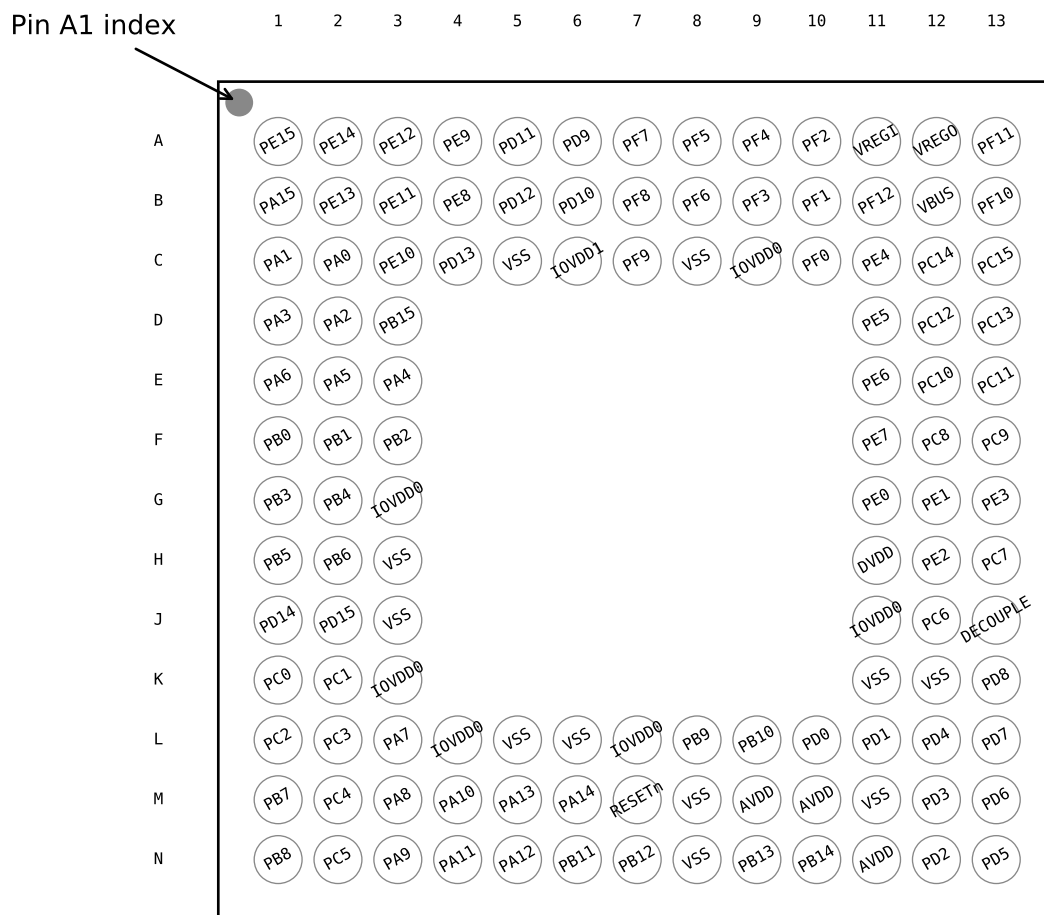


Figure 5.3. EFM32GG12B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.3. EFM32GG12B4xx in BGA120 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------|----------|--------|--|
| PE15 | A1 | GPIO | PE14 | A2 | GPIO |
| PE12 | A3 | GPIO | PE9 | A4 | GPIO |
| PD11 | A5 | GPIO | PD9 | A6 | GPIO |
| PF7 | A7 | GPIO | PF5 | A8 | GPIO |
| PF4 | A9 | GPIO | PF2 | A10 | GPIO |
| VREGI | A11 | Input to 5 V regulator. | VREGO | A12 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---|---|----------|-----------------------------------|----------------------------|
| PF11 | A13 | GPIO (5V) | PA15 | B1 | GPIO |
| PE13 | B2 | GPIO | PE11 | B3 | GPIO |
| PE8 | B4 | GPIO | PD12 | B5 | GPIO |
| PD10 | B6 | GPIO | PF8 | B7 | GPIO |
| PF6 | B8 | GPIO | PF3 | B9 | GPIO |
| PF1 | B10 | GPIO (5V) | PF12 | B11 | GPIO (5V) |
| VBUS | B12 | USB VBUS signal and auxiliary input to 5 V regulator. | PF10 | B13 | GPIO (5V) |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| VSS | C5 C8 H3 J3 K11 K12 L5 L6 M8 M11 N8 | Ground | IOVDD1 | C6 | Digital IO power supply 1. |
| PF9 | C7 | GPIO | IOVDD0 | C9 G3 J11 K3 L4 L7 | Digital IO power supply 0. |
| PF0 | C10 | GPIO (5V) | PE4 | C11 | GPIO |
| PC14 | C12 | GPIO (5V) | PC15 | C13 | GPIO (5V) |
| PA3 | D1 | GPIO | PA2 | D2 | GPIO |
| PB15 | D3 | GPIO (5V) | PE5 | D11 | GPIO |
| PC12 | D12 | GPIO (5V) | PC13 | D13 | GPIO (5V) |
| PA6 | E1 | GPIO | PA5 | E2 | GPIO |
| PA4 | E3 | GPIO | PE6 | E11 | GPIO |
| PC10 | E12 | GPIO (5V) | PC11 | E13 | GPIO (5V) |
| PB0 | F1 | GPIO | PB1 | F2 | GPIO |
| PB2 | F3 | GPIO | PE7 | F11 | GPIO |
| PC8 | F12 | GPIO (5V) | PC9 | F13 | GPIO (5V) |
| PB3 | G1 | GPIO | PB4 | G2 | GPIO |
| PE0 | G11 | GPIO (5V) | PE1 | G12 | GPIO (5V) |
| PE3 | G13 | GPIO | PB5 | H1 | GPIO |
| PB6 | H2 | GPIO | DVDD | H11 | Digital power supply. |
| PE2 | H12 | GPIO | PC7 | H13 | GPIO |
| PD14 | J1 | GPIO (5V) | PD15 | J2 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|------------------|--|
| PC6 | J12 | GPIO | DECOUPLE | J13 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PC0 | K1 | GPIO (5V) | PC1 | K2 | GPIO (5V) |
| PD8 | K13 | GPIO | PC2 | L1 | GPIO (5V) |
| PC3 | L2 | GPIO (5V) | PA7 | L3 | GPIO |
| PB9 | L8 | GPIO (5V) | PB10 | L9 | GPIO (5V) |
| PD0 | L10 | GPIO (5V) | PD1 | L11 | GPIO |
| PD4 | L12 | GPIO | PD7 | L13 | GPIO |
| PB7 | M1 | GPIO | PC4 | M2 | GPIO |
| PA8 | M3 | GPIO | PA10 | M4 | GPIO |
| PA13 | M5 | GPIO (5V) | PA14 | M6 | GPIO |
| RESETn | M7 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | AVDD | M9 M10 N11 | Analog power supply. |
| PD3 | M12 | GPIO | PD6 | M13 | GPIO |
| PB8 | N1 | GPIO | PC5 | N2 | GPIO |
| PA9 | N3 | GPIO | PA11 | N4 | GPIO |
| PA12 | N5 | GPIO (5V) | PB11 | N6 | GPIO |
| PB12 | N7 | GPIO | PB13 | N9 | GPIO |
| PB14 | N10 | GPIO | PD2 | N12 | GPIO (5V) |
| PD5 | N13 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.4 EFM32GG12B8xx in BGA112 Device Pinout

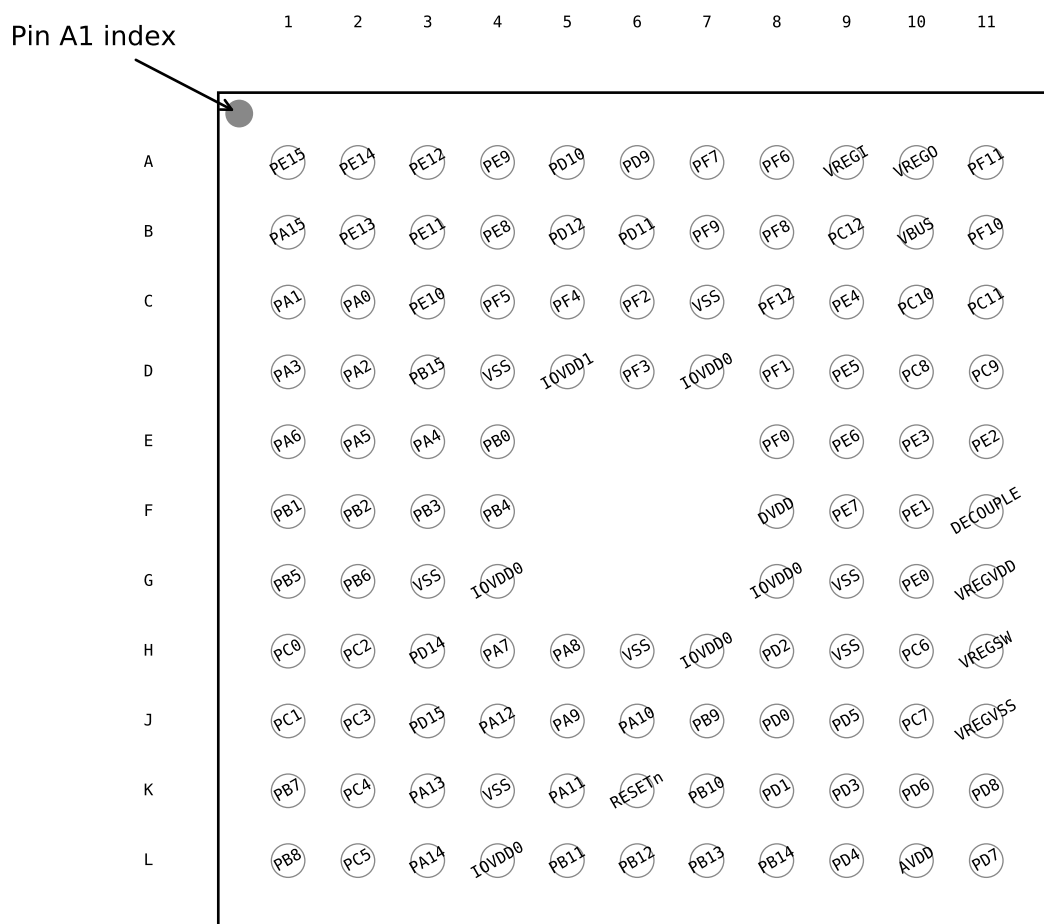


Figure 5.4. EFM32GG12B8xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.4. EFM32GG12B8xx in BGA112 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------|----------|--------|--|
| PE15 | A1 | GPIO | PE14 | A2 | GPIO |
| PE12 | A3 | GPIO | PE9 | A4 | GPIO |
| PD10 | A5 | GPIO | PD9 | A6 | GPIO |
| PF7 | A7 | GPIO | PF6 | A8 | GPIO |
| VREGI | A9 | Input to 5 V regulator. | VREGO | A10 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |
| PF11 | A11 | GPIO (5V) | PA15 | B1 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--|--|----------|--------|-----------------------|
| PE13 | B2 | GPIO | PE11 | B3 | GPIO |
| PE8 | B4 | GPIO | PD12 | B5 | GPIO |
| PD11 | B6 | GPIO | PF9 | B7 | GPIO |
| PF8 | B8 | GPIO | PC12 | B9 | GPIO (5V) |
| VBUS | B10 | USB VBUS signal and auxiliary input to 5 V regulator. | PF10 | B11 | GPIO (5V) |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PF5 | C4 | GPIO |
| PF4 | C5 | GPIO | PF2 | C6 | GPIO |
| VSS | C7 D4 G3 G9 H6 H9 K4 | Ground | PF12 | C8 | GPIO (5V) |
| PE4 | C9 | GPIO | PC10 | C10 | GPIO (5V) |
| PC11 | C11 | GPIO (5V) | PA3 | D1 | GPIO |
| PA2 | D2 | GPIO | PB15 | D3 | GPIO (5V) |
| IOVDD1 | D5 | Digital IO power supply 1. | PF3 | D6 | GPIO |
| IOVDD0 | D7 G4 G8 H7 L4 | Digital IO power supply 0. | PF1 | D8 | GPIO (5V) |
| PE5 | D9 | GPIO | PC8 | D10 | GPIO (5V) |
| PC9 | D11 | GPIO (5V) | PA6 | E1 | GPIO |
| PA5 | E2 | GPIO | PA4 | E3 | GPIO |
| PB0 | E4 | GPIO | PF0 | E8 | GPIO (5V) |
| PE6 | E9 | GPIO | PE3 | E10 | GPIO |
| PE2 | E11 | GPIO | PB1 | F1 | GPIO |
| PB2 | F2 | GPIO | PB3 | F3 | GPIO |
| PB4 | F4 | GPIO | DVDD | F8 | Digital power supply. |
| PE7 | F9 | GPIO | PE1 | F10 | GPIO (5V) |
| DECOUPLE | F11 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PB5 | G1 | GPIO |
| PB6 | G2 | GPIO | PE0 | G10 | GPIO (5V) |
| VREGVDD | G11 | Voltage regulator VDD input | PC0 | H1 | GPIO (5V) |
| PC2 | H2 | GPIO (5V) | PD14 | H3 | GPIO (5V) |
| PA7 | H4 | GPIO | PA8 | H5 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|--------|-----------------------|
| PD2 | H8 | GPIO (5V) | PC6 | H10 | GPIO |
| VREGSW | H11 | DCDC regulator switching node | PC1 | J1 | GPIO (5V) |
| PC3 | J2 | GPIO (5V) | PD15 | J3 | GPIO (5V) |
| PA12 | J4 | GPIO (5V) | PA9 | J5 | GPIO |
| PA10 | J6 | GPIO | PB9 | J7 | GPIO (5V) |
| PD0 | J8 | GPIO (5V) | PD5 | J9 | GPIO |
| PC7 | J10 | GPIO | VREGVSS | J11 | Voltage regulator VSS |
| PB7 | K1 | GPIO | PC4 | K2 | GPIO |
| PA13 | K3 | GPIO (5V) | PA11 | K5 | GPIO |
| RESETn | K6 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB10 | K7 | GPIO (5V) |
| PD1 | K8 | GPIO | PD3 | K9 | GPIO |
| PD6 | K10 | GPIO | PD8 | K11 | GPIO |
| PB8 | L1 | GPIO | PC5 | L2 | GPIO |
| PA14 | L3 | GPIO | PB11 | L5 | GPIO |
| PB12 | L6 | GPIO | PB13 | L7 | GPIO |
| PB14 | L8 | GPIO | PD4 | L9 | GPIO |
| AVDD | L10 | Analog power supply. | PD7 | L11 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.5 EFM32GG12B5xx in BGA112 Device Pinout

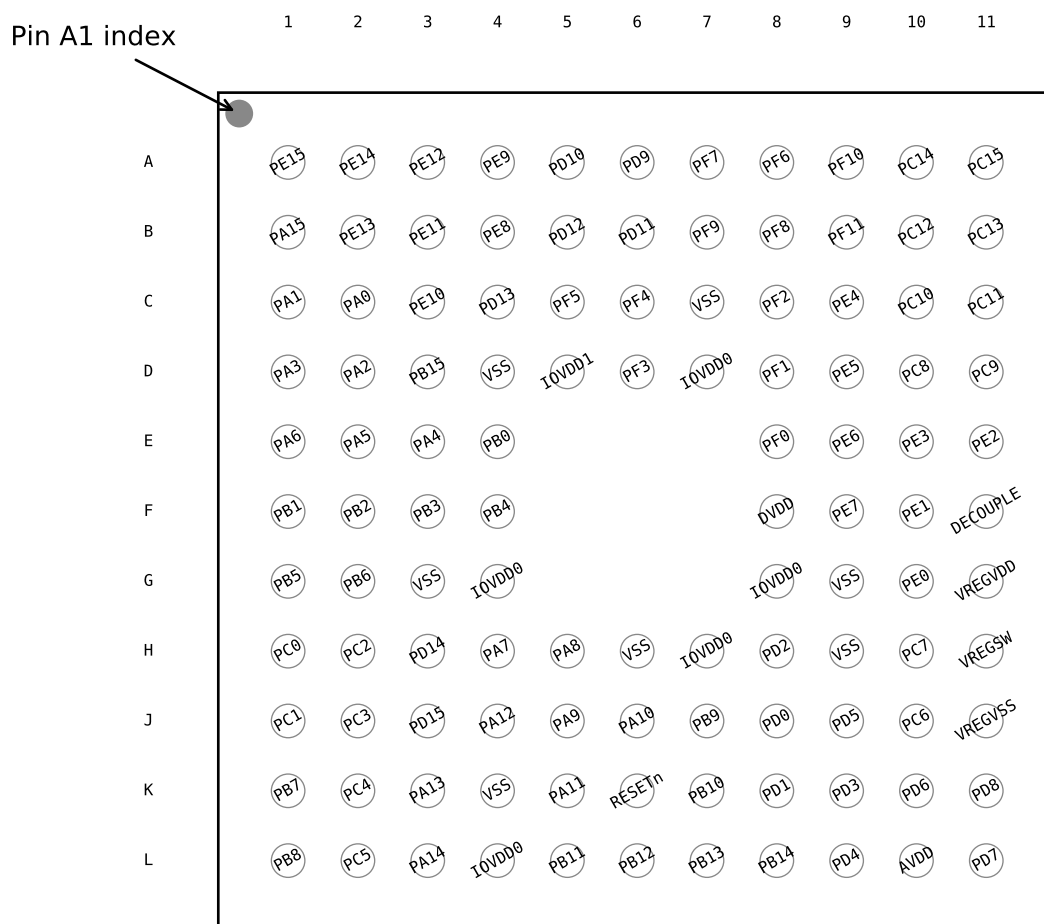


Figure 5.5. EFM32GG12B5xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.5. EFM32GG12B5xx in BGA112 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PE15 | A1 | GPIO | PE14 | A2 | GPIO |
| PE12 | A3 | GPIO | PE9 | A4 | GPIO |
| PD10 | A5 | GPIO | PD9 | A6 | GPIO |
| PF7 | A7 | GPIO | PF6 | A8 | GPIO |
| PF10 | A9 | GPIO (5V) | PC14 | A10 | GPIO (5V) |
| PC15 | A11 | GPIO (5V) | PA15 | B1 | GPIO |
| PE13 | B2 | GPIO | PE11 | B3 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--|--|----------|--------|-----------------------|
| PE8 | B4 | GPIO | PD12 | B5 | GPIO |
| PD11 | B6 | GPIO | PF9 | B7 | GPIO |
| PF8 | B8 | GPIO | PF11 | B9 | GPIO (5V) |
| PC12 | B10 | GPIO (5V) | PC13 | B11 | GPIO (5V) |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| PF5 | C5 | GPIO | PF4 | C6 | GPIO |
| VSS | C7 D4 G3 G9 H6 H9 K4 | Ground | PF2 | C8 | GPIO |
| PE4 | C9 | GPIO | PC10 | C10 | GPIO (5V) |
| PC11 | C11 | GPIO (5V) | PA3 | D1 | GPIO |
| PA2 | D2 | GPIO | PB15 | D3 | GPIO (5V) |
| IOVDD1 | D5 | Digital IO power supply 1. | PF3 | D6 | GPIO |
| IOVDD0 | D7 G4 G8 H7 L4 | Digital IO power supply 0. | PF1 | D8 | GPIO (5V) |
| PE5 | D9 | GPIO | PC8 | D10 | GPIO (5V) |
| PC9 | D11 | GPIO (5V) | PA6 | E1 | GPIO |
| PA5 | E2 | GPIO | PA4 | E3 | GPIO |
| PB0 | E4 | GPIO | PF0 | E8 | GPIO (5V) |
| PE6 | E9 | GPIO | PE3 | E10 | GPIO |
| PE2 | E11 | GPIO | PB1 | F1 | GPIO |
| PB2 | F2 | GPIO | PB3 | F3 | GPIO |
| PB4 | F4 | GPIO | DVDD | F8 | Digital power supply. |
| PE7 | F9 | GPIO | PE1 | F10 | GPIO (5V) |
| DECOUPLE | F11 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PB5 | G1 | GPIO |
| PB6 | G2 | GPIO | PE0 | G10 | GPIO (5V) |
| VREGVDD | G11 | Voltage regulator VDD input | PC0 | H1 | GPIO (5V) |
| PC2 | H2 | GPIO (5V) | PD14 | H3 | GPIO (5V) |
| PA7 | H4 | GPIO | PA8 | H5 | GPIO |
| PD2 | H8 | GPIO (5V) | PC7 | H10 | GPIO |
| VREGSW | H11 | DCDC regulator switching node | PC1 | J1 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|--------|-----------------------|
| PC3 | J2 | GPIO (5V) | PD15 | J3 | GPIO (5V) |
| PA12 | J4 | GPIO (5V) | PA9 | J5 | GPIO |
| PA10 | J6 | GPIO | PB9 | J7 | GPIO (5V) |
| PD0 | J8 | GPIO (5V) | PD5 | J9 | GPIO |
| PC6 | J10 | GPIO | VREGVSS | J11 | Voltage regulator VSS |
| PB7 | K1 | GPIO | PC4 | K2 | GPIO |
| PA13 | K3 | GPIO (5V) | PA11 | K5 | GPIO |
| RESETn | K6 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB10 | K7 | GPIO (5V) |
| PD1 | K8 | GPIO | PD3 | K9 | GPIO |
| PD6 | K10 | GPIO | PD8 | K11 | GPIO |
| PB8 | L1 | GPIO | PC5 | L2 | GPIO |
| PA14 | L3 | GPIO | PB11 | L5 | GPIO |
| PB12 | L6 | GPIO | PB13 | L7 | GPIO |
| PB14 | L8 | GPIO | PD4 | L9 | GPIO |
| AVDD | L10 | Analog power supply. | PD7 | L11 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.6 EFM32GG12B4xx in BGA112 Device Pinout

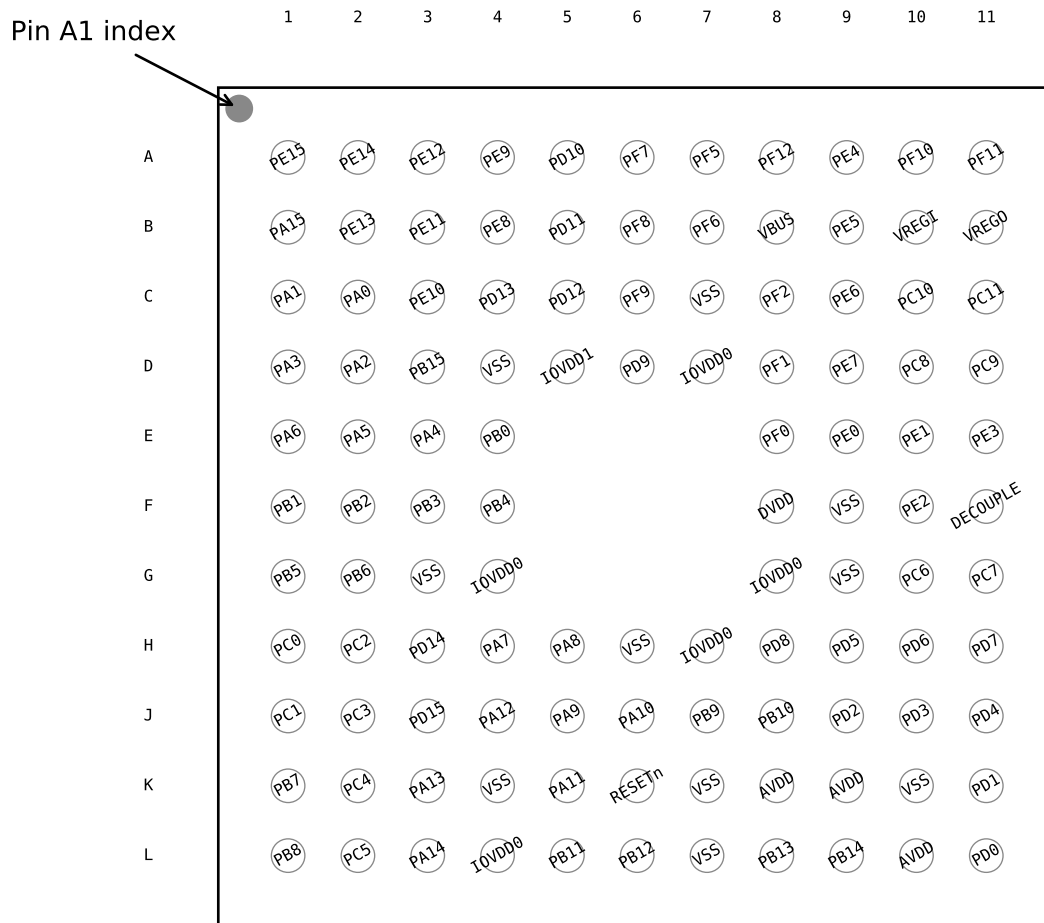


Figure 5.6. EFM32GG12B4xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.6. EFM32GG12B4xx in BGA112 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PE15 | A1 | GPIO | PE14 | A2 | GPIO |
| PE12 | A3 | GPIO | PE9 | A4 | GPIO |
| PD10 | A5 | GPIO | PF7 | A6 | GPIO |
| PF5 | A7 | GPIO | PF12 | A8 | GPIO (5V) |
| PE4 | A9 | GPIO | PF10 | A10 | GPIO (5V) |
| PF11 | A11 | GPIO (5V) | PA15 | B1 | GPIO |
| PE13 | B2 | GPIO | PE11 | B3 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---|---|----------|--------|--|
| PE8 | B4 | GPIO | PD11 | B5 | GPIO |
| PF8 | B6 | GPIO | PF6 | B7 | GPIO |
| VBUS | B8 | USB VBUS signal and auxiliary input to 5 V regulator. | PE5 | B9 | GPIO |
| VREGI | B10 | Input to 5 V regulator. | VREGO | B11 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| PD12 | C5 | GPIO | PF9 | C6 | GPIO |
| VSS | C7 D4 F9 G3 G9 H6 K4 K7 K10 L7 | Ground | PF2 | C8 | GPIO |
| PE6 | C9 | GPIO | PC10 | C10 | GPIO (5V) |
| PC11 | C11 | GPIO (5V) | PA3 | D1 | GPIO |
| PA2 | D2 | GPIO | PB15 | D3 | GPIO (5V) |
| IOVDD1 | D5 | Digital IO power supply 1. | PD9 | D6 | GPIO |
| IOVDD0 | D7 G4 G8 H7 L4 | Digital IO power supply 0. | PF1 | D8 | GPIO (5V) |
| PE7 | D9 | GPIO | PC8 | D10 | GPIO (5V) |
| PC9 | D11 | GPIO (5V) | PA6 | E1 | GPIO |
| PA5 | E2 | GPIO | PA4 | E3 | GPIO |
| PB0 | E4 | GPIO | PF0 | E8 | GPIO (5V) |
| PE0 | E9 | GPIO (5V) | PE1 | E10 | GPIO (5V) |
| PE3 | E11 | GPIO | PB1 | F1 | GPIO |
| PB2 | F2 | GPIO | PB3 | F3 | GPIO |
| PB4 | F4 | GPIO | DVDD | F8 | Digital power supply. |
| PE2 | F10 | GPIO | DECOUPLE | F11 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PB5 | G1 | GPIO | PB6 | G2 | GPIO |
| PC6 | G10 | GPIO | PC7 | G11 | GPIO |
| PC0 | H1 | GPIO (5V) | PC2 | H2 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|-----------------|----------------------|
| PD14 | H3 | GPIO (5V) | PA7 | H4 | GPIO |
| PA8 | H5 | GPIO | PD8 | H8 | GPIO |
| PD5 | H9 | GPIO | PD6 | H10 | GPIO |
| PD7 | H11 | GPIO | PC1 | J1 | GPIO (5V) |
| PC3 | J2 | GPIO (5V) | PD15 | J3 | GPIO (5V) |
| PA12 | J4 | GPIO (5V) | PA9 | J5 | GPIO |
| PA10 | J6 | GPIO | PB9 | J7 | GPIO (5V) |
| PB10 | J8 | GPIO (5V) | PD2 | J9 | GPIO (5V) |
| PD3 | J10 | GPIO | PD4 | J11 | GPIO |
| PB7 | K1 | GPIO | PC4 | K2 | GPIO |
| PA13 | K3 | GPIO (5V) | PA11 | K5 | GPIO |
| RESETn | K6 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | AVDD | K8 K9 L10 | Analog power supply. |
| PD1 | K11 | GPIO | PB8 | L1 | GPIO |
| PC5 | L2 | GPIO | PA14 | L3 | GPIO |
| PB11 | L5 | GPIO | PB12 | L6 | GPIO |
| PB13 | L8 | GPIO | PB14 | L9 | GPIO |
| PD0 | L11 | GPIO (5V) | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.7 EFM32GG12B3xx in BGA112 Device Pinout

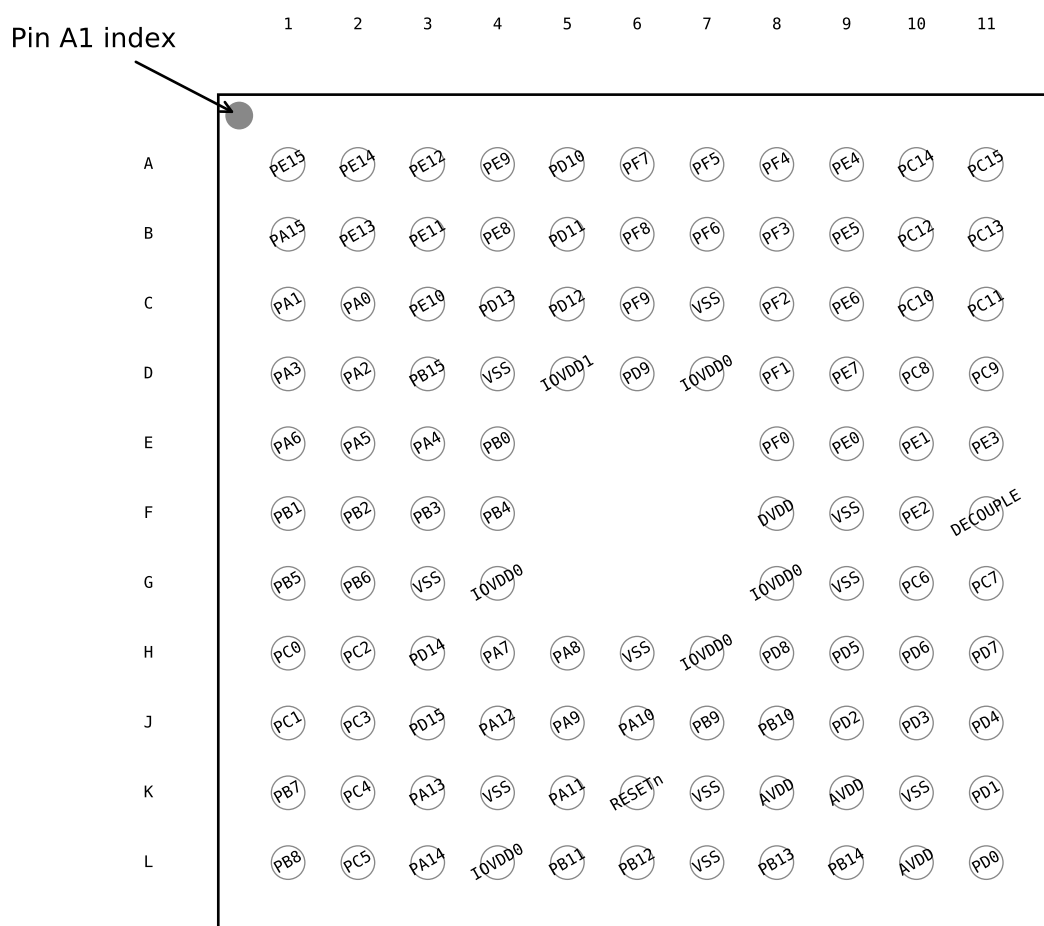


Figure 5.7. EFM32GG12B3xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.7. EFM32GG12B3xx in BGA112 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PE15 | A1 | GPIO | PE14 | A2 | GPIO |
| PE12 | A3 | GPIO | PE9 | A4 | GPIO |
| PD10 | A5 | GPIO | PF7 | A6 | GPIO |
| PF5 | A7 | GPIO | PF4 | A8 | GPIO |
| PE4 | A9 | GPIO | PC14 | A10 | GPIO (5V) |
| PC15 | A11 | GPIO (5V) | PA15 | B1 | GPIO |
| PE13 | B2 | GPIO | PE11 | B3 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---|----------------------------|----------|--------|--|
| PE8 | B4 | GPIO | PD11 | B5 | GPIO |
| PF8 | B6 | GPIO | PF6 | B7 | GPIO |
| PF3 | B8 | GPIO | PE5 | B9 | GPIO |
| PC12 | B10 | GPIO (5V) | PC13 | B11 | GPIO (5V) |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| PD12 | C5 | GPIO | PF9 | C6 | GPIO |
| VSS | C7 D4 F9 G3 G9 H6 K4 K7 K10 L7 | Ground | PF2 | C8 | GPIO |
| PE6 | C9 | GPIO | PC10 | C10 | GPIO (5V) |
| PC11 | C11 | GPIO (5V) | PA3 | D1 | GPIO |
| PA2 | D2 | GPIO | PB15 | D3 | GPIO (5V) |
| IOVDD1 | D5 | Digital IO power supply 1. | PD9 | D6 | GPIO |
| IOVDD0 | D7 G4 G8 H7 L4 | Digital IO power supply 0. | PF1 | D8 | GPIO (5V) |
| PE7 | D9 | GPIO | PC8 | D10 | GPIO (5V) |
| PC9 | D11 | GPIO (5V) | PA6 | E1 | GPIO |
| PA5 | E2 | GPIO | PA4 | E3 | GPIO |
| PB0 | E4 | GPIO | PF0 | E8 | GPIO (5V) |
| PE0 | E9 | GPIO (5V) | PE1 | E10 | GPIO (5V) |
| PE3 | E11 | GPIO | PB1 | F1 | GPIO |
| PB2 | F2 | GPIO | PB3 | F3 | GPIO |
| PB4 | F4 | GPIO | DVDD | F8 | Digital power supply. |
| PE2 | F10 | GPIO | DECOUPLE | F11 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PB5 | G1 | GPIO | PB6 | G2 | GPIO |
| PC6 | G10 | GPIO | PC7 | G11 | GPIO |
| PC0 | H1 | GPIO (5V) | PC2 | H2 | GPIO (5V) |
| PD14 | H3 | GPIO (5V) | PA7 | H4 | GPIO |
| PA8 | H5 | GPIO | PD8 | H8 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|-----------------|----------------------|
| PD5 | H9 | GPIO | PD6 | H10 | GPIO |
| PD7 | H11 | GPIO | PC1 | J1 | GPIO (5V) |
| PC3 | J2 | GPIO (5V) | PD15 | J3 | GPIO (5V) |
| PA12 | J4 | GPIO (5V) | PA9 | J5 | GPIO |
| PA10 | J6 | GPIO | PB9 | J7 | GPIO (5V) |
| PB10 | J8 | GPIO (5V) | PD2 | J9 | GPIO (5V) |
| PD3 | J10 | GPIO | PD4 | J11 | GPIO |
| PB7 | K1 | GPIO | PC4 | K2 | GPIO |
| PA13 | K3 | GPIO (5V) | PA11 | K5 | GPIO |
| RESETn | K6 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | AVDD | K8 K9 L10 | Analog power supply. |
| PD1 | K11 | GPIO | PB8 | L1 | GPIO |
| PC5 | L2 | GPIO | PA14 | L3 | GPIO |
| PB11 | L5 | GPIO | PB12 | L6 | GPIO |
| PB13 | L8 | GPIO | PB14 | L9 | GPIO |
| PD0 | L11 | GPIO (5V) | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.8 EFM32GG12B8xx in QFP100 Device Pinout



Figure 5.8. EFM32GG12B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.8. EFM32GG12B8xx in QFP100 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|-------------------|----------------------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| PA6 | 7 | GPIO | IOVDD0 | 8, 17, 31, 44, 82 | Digital IO power supply 0. |
| PB0 | 9 | GPIO | PB1 | 10 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|----------------------|--|
| PB2 | 11 | GPIO | PB3 | 12 | GPIO |
| PB4 | 13 | GPIO | PB5 | 14 | GPIO |
| PB6 | 15 | GPIO | VSS | 16 32 59 83 | Ground |
| PC0 | 18 | GPIO (5V) | PC1 | 19 | GPIO (5V) |
| PC2 | 20 | GPIO (5V) | PC3 | 21 | GPIO (5V) |
| PC4 | 22 | GPIO | PC5 | 23 | GPIO |
| PB7 | 24 | GPIO | PB8 | 25 | GPIO |
| PA7 | 26 | GPIO | PA8 | 27 | GPIO |
| PA9 | 28 | GPIO | PA10 | 29 | GPIO |
| PA11 | 30 | GPIO | PA12 | 33 | GPIO (5V) |
| PA13 | 34 | GPIO (5V) | PA14 | 35 | GPIO |
| RESETn | 36 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB9 | 37 | GPIO (5V) |
| PB10 | 38 | GPIO (5V) | PB11 | 39 | GPIO |
| PB12 | 40 | GPIO | AVDD | 41 | Analog power supply. |
| PB13 | 42 | GPIO | PB14 | 43 | GPIO |
| PD0 | 45 | GPIO (5V) | PD1 | 46 | GPIO |
| PD2 | 47 | GPIO (5V) | PD3 | 48 | GPIO |
| PD4 | 49 | GPIO | PD5 | 50 | GPIO |
| PD6 | 51 | GPIO | PD7 | 52 | GPIO |
| PD8 | 53 | GPIO | PC7 | 54 | GPIO |
| VREGVSS | 55 | Voltage regulator VSS | VREGSW | 56 | DCDC regulator switching node |
| VREGVDD | 57 | Voltage regulator VDD input | DVDD | 58 | Digital power supply. |
| DECOUPLE | 60 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PE1 | 61 | GPIO (5V) |
| PE2 | 62 | GPIO | PE3 | 63 | GPIO |
| PE4 | 64 | GPIO | PE5 | 65 | GPIO |
| PE6 | 66 | GPIO | PE7 | 67 | GPIO |
| PC8 | 68 | GPIO (5V) | PC9 | 69 | GPIO (5V) |
| PC10 | 70 | GPIO (5V) | PC11 | 71 | GPIO (5V) |
| VREGI | 72 | Input to 5 V regulator. | VREGO | 73 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|---|
| PF10 | 74 | GPIO (5V) | PF11 | 75 | GPIO (5V) |
| PF0 | 76 | GPIO (5V) | PF1 | 77 | GPIO (5V) |
| PF2 | 78 | GPIO | VBUS | 79 | USB VBUS signal and auxiliary input to 5 V regulator. |
| PF12 | 80 | GPIO (5V) | PF5 | 81 | GPIO |
| PF6 | 84 | GPIO | PF7 | 85 | GPIO |
| PF8 | 86 | GPIO | PF9 | 87 | GPIO |
| PD9 | 88 | GPIO | PD10 | 89 | GPIO |
| PD11 | 90 | GPIO | PD12 | 91 | GPIO |
| PE8 | 92 | GPIO | PE9 | 93 | GPIO |
| PE10 | 94 | GPIO | PE11 | 95 | GPIO |
| PE12 | 96 | GPIO | PE13 | 97 | GPIO |
| PE14 | 98 | GPIO | PE15 | 99 | GPIO |
| PA15 | 100 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.9 EFM32GG12B5xx in QFP100 Device Pinout

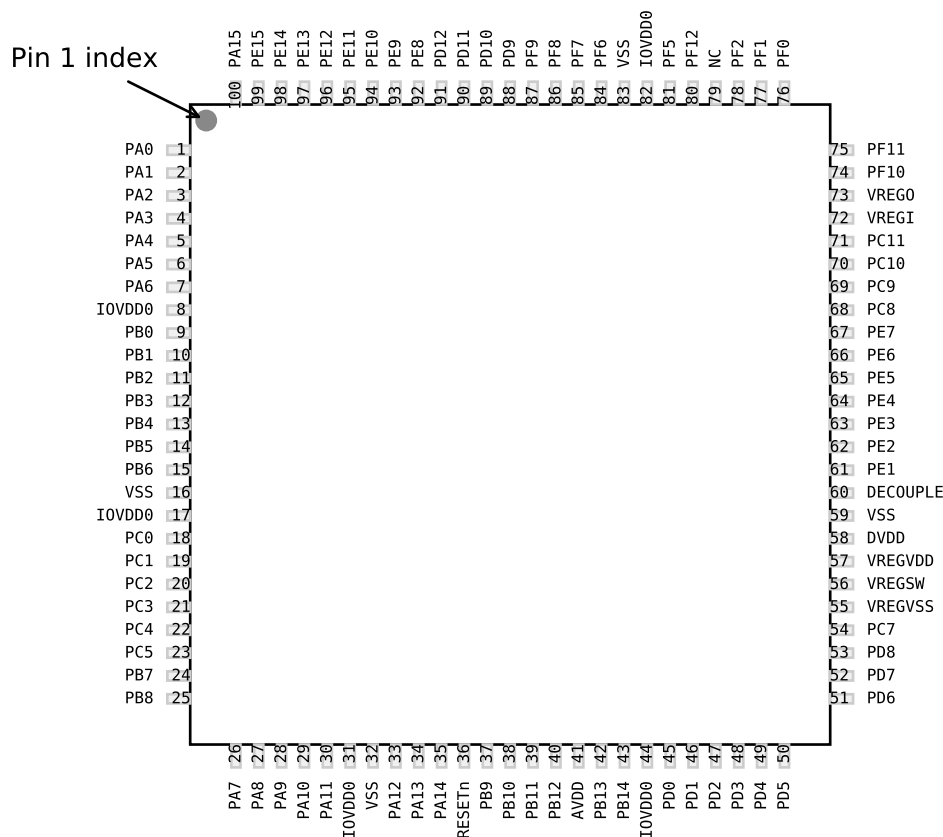


Figure 5.9. EFM32GG12B5xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.9. EFM32GG12B5xx in QFP100 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|-------------------|----------------------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| PA6 | 7 | GPIO | IOVDD0 | 8, 17, 31, 44, 82 | Digital IO power supply 0. |
| PB0 | 9 | GPIO | PB1 | 10 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|----------------------|--|
| PB2 | 11 | GPIO | PB3 | 12 | GPIO |
| PB4 | 13 | GPIO | PB5 | 14 | GPIO |
| PB6 | 15 | GPIO | VSS | 16 32 59 83 | Ground |
| PC0 | 18 | GPIO (5V) | PC1 | 19 | GPIO (5V) |
| PC2 | 20 | GPIO (5V) | PC3 | 21 | GPIO (5V) |
| PC4 | 22 | GPIO | PC5 | 23 | GPIO |
| PB7 | 24 | GPIO | PB8 | 25 | GPIO |
| PA7 | 26 | GPIO | PA8 | 27 | GPIO |
| PA9 | 28 | GPIO | PA10 | 29 | GPIO |
| PA11 | 30 | GPIO | PA12 | 33 | GPIO (5V) |
| PA13 | 34 | GPIO (5V) | PA14 | 35 | GPIO |
| RESETn | 36 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB9 | 37 | GPIO (5V) |
| PB10 | 38 | GPIO (5V) | PB11 | 39 | GPIO |
| PB12 | 40 | GPIO | AVDD | 41 | Analog power supply. |
| PB13 | 42 | GPIO | PB14 | 43 | GPIO |
| PD0 | 45 | GPIO (5V) | PD1 | 46 | GPIO |
| PD2 | 47 | GPIO (5V) | PD3 | 48 | GPIO |
| PD4 | 49 | GPIO | PD5 | 50 | GPIO |
| PD6 | 51 | GPIO | PD7 | 52 | GPIO |
| PD8 | 53 | GPIO | PC7 | 54 | GPIO |
| VREGVSS | 55 | Voltage regulator VSS | VREGSW | 56 | DCDC regulator switching node |
| VREGVDD | 57 | Voltage regulator VDD input | DVDD | 58 | Digital power supply. |
| DECOUPLE | 60 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PE1 | 61 | GPIO (5V) |
| PE2 | 62 | GPIO | PE3 | 63 | GPIO |
| PE4 | 64 | GPIO | PE5 | 65 | GPIO |
| PE6 | 66 | GPIO | PE7 | 67 | GPIO |
| PC8 | 68 | GPIO (5V) | PC9 | 69 | GPIO (5V) |
| PC10 | 70 | GPIO (5V) | PC11 | 71 | GPIO (5V) |
| VREGI | 72 | Input to 5 V regulator. | VREGO | 73 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PF10 | 74 | GPIO (5V) | PF11 | 75 | GPIO (5V) |
| PF0 | 76 | GPIO (5V) | PF1 | 77 | GPIO (5V) |
| PF2 | 78 | GPIO | NC | 79 | No Connect. |
| PF12 | 80 | GPIO (5V) | PF5 | 81 | GPIO |
| PF6 | 84 | GPIO | PF7 | 85 | GPIO |
| PF8 | 86 | GPIO | PF9 | 87 | GPIO |
| PD9 | 88 | GPIO | PD10 | 89 | GPIO |
| PD11 | 90 | GPIO | PD12 | 91 | GPIO |
| PE8 | 92 | GPIO | PE9 | 93 | GPIO |
| PE10 | 94 | GPIO | PE11 | 95 | GPIO |
| PE12 | 96 | GPIO | PE13 | 97 | GPIO |
| PE14 | 98 | GPIO | PE15 | 99 | GPIO |
| PA15 | 100 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.10 EFM32GG12B4xx in QFP100 Device Pinout

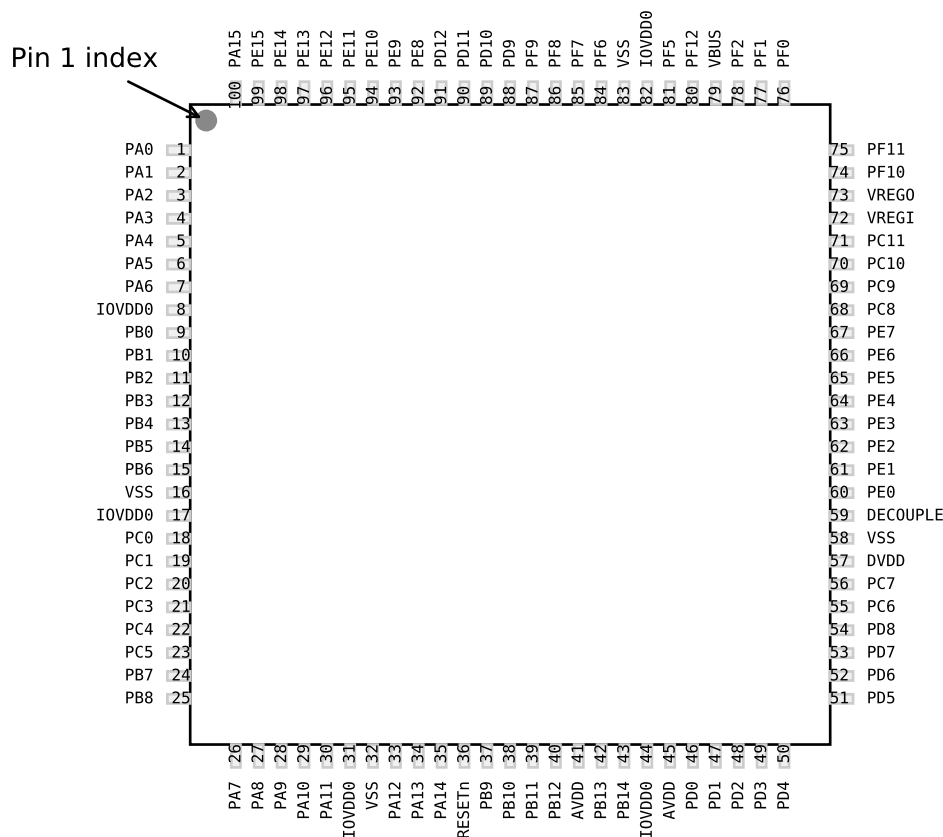


Figure 5.10. EFM32GG12B4xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.10. EFM32GG12B4xx in QFP100 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|-------------------|----------------------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| PA6 | 7 | GPIO | IOVDD0 | 8, 17, 31, 44, 82 | Digital IO power supply 0. |
| PB0 | 9 | GPIO | PB1 | 10 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|----------------------|-------------------------|
| PB2 | 11 | GPIO | PB3 | 12 | GPIO |
| PB4 | 13 | GPIO | PB5 | 14 | GPIO |
| PB6 | 15 | GPIO | VSS | 16 32 58 83 | Ground |
| PC0 | 18 | GPIO (5V) | PC1 | 19 | GPIO (5V) |
| PC2 | 20 | GPIO (5V) | PC3 | 21 | GPIO (5V) |
| PC4 | 22 | GPIO | PC5 | 23 | GPIO |
| PB7 | 24 | GPIO | PB8 | 25 | GPIO |
| PA7 | 26 | GPIO | PA8 | 27 | GPIO |
| PA9 | 28 | GPIO | PA10 | 29 | GPIO |
| PA11 | 30 | GPIO | PA12 | 33 | GPIO (5V) |
| PA13 | 34 | GPIO (5V) | PA14 | 35 | GPIO |
| RESETn | 36 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB9 | 37 | GPIO (5V) |
| PB10 | 38 | GPIO (5V) | PB11 | 39 | GPIO |
| PB12 | 40 | GPIO | AVDD | 41 45 | Analog power supply. |
| PB13 | 42 | GPIO | PB14 | 43 | GPIO |
| PD0 | 46 | GPIO (5V) | PD1 | 47 | GPIO |
| PD2 | 48 | GPIO (5V) | PD3 | 49 | GPIO |
| PD4 | 50 | GPIO | PD5 | 51 | GPIO |
| PD6 | 52 | GPIO | PD7 | 53 | GPIO |
| PD8 | 54 | GPIO | PC6 | 55 | GPIO |
| PC7 | 56 | GPIO | DVDD | 57 | Digital power supply. |
| DECOUPLE | 59 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PE0 | 60 | GPIO (5V) |
| PE1 | 61 | GPIO (5V) | PE2 | 62 | GPIO |
| PE3 | 63 | GPIO | PE4 | 64 | GPIO |
| PE5 | 65 | GPIO | PE6 | 66 | GPIO |
| PE7 | 67 | GPIO | PC8 | 68 | GPIO (5V) |
| PC9 | 69 | GPIO (5V) | PC10 | 70 | GPIO (5V) |
| PC11 | 71 | GPIO (5V) | VREGI | 72 | Input to 5 V regulator. |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|--|----------|--------|-------------|
| VREGO | 73 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs | PF10 | 74 | GPIO (5V) |
| PF11 | 75 | GPIO (5V) | PF0 | 76 | GPIO (5V) |
| PF1 | 77 | GPIO (5V) | PF2 | 78 | GPIO |
| VBUS | 79 | USB VBUS signal and auxiliary input to 5 V regulator. | PF12 | 80 | GPIO (5V) |
| PF5 | 81 | GPIO | PF6 | 84 | GPIO |
| PF7 | 85 | GPIO | PF8 | 86 | GPIO |
| PF9 | 87 | GPIO | PD9 | 88 | GPIO |
| PD10 | 89 | GPIO | PD11 | 90 | GPIO |
| PD12 | 91 | GPIO | PE8 | 92 | GPIO |
| PE9 | 93 | GPIO | PE10 | 94 | GPIO |
| PE11 | 95 | GPIO | PE12 | 96 | GPIO |
| PE13 | 97 | GPIO | PE14 | 98 | GPIO |
| PE15 | 99 | GPIO | PA15 | 100 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.11 EFM32GG12B3xx in QFP100 Device Pinout

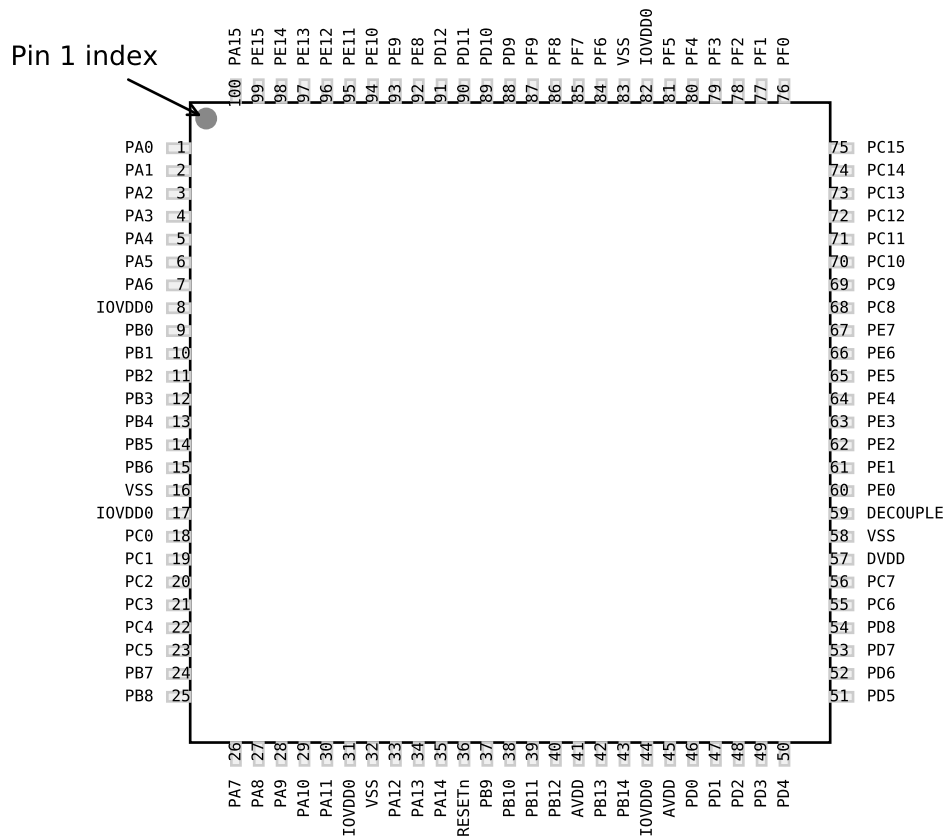


Figure 5.11. EFM32GG12B3xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.11. EFM32GG12B3xx in QFP100 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|-------------------|----------------------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| PA6 | 7 | GPIO | IOVDD0 | 8, 17, 31, 44, 82 | Digital IO power supply 0. |
| PB0 | 9 | GPIO | PB1 | 10 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|----------------------|-----------------------|
| PB2 | 11 | GPIO | PB3 | 12 | GPIO |
| PB4 | 13 | GPIO | PB5 | 14 | GPIO |
| PB6 | 15 | GPIO | VSS | 16 32 58 83 | Ground |
| PC0 | 18 | GPIO (5V) | PC1 | 19 | GPIO (5V) |
| PC2 | 20 | GPIO (5V) | PC3 | 21 | GPIO (5V) |
| PC4 | 22 | GPIO | PC5 | 23 | GPIO |
| PB7 | 24 | GPIO | PB8 | 25 | GPIO |
| PA7 | 26 | GPIO | PA8 | 27 | GPIO |
| PA9 | 28 | GPIO | PA10 | 29 | GPIO |
| PA11 | 30 | GPIO | PA12 | 33 | GPIO (5V) |
| PA13 | 34 | GPIO (5V) | PA14 | 35 | GPIO |
| RESETn | 36 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB9 | 37 | GPIO (5V) |
| PB10 | 38 | GPIO (5V) | PB11 | 39 | GPIO |
| PB12 | 40 | GPIO | AVDD | 41 45 | Analog power supply. |
| PB13 | 42 | GPIO | PB14 | 43 | GPIO |
| PD0 | 46 | GPIO (5V) | PD1 | 47 | GPIO |
| PD2 | 48 | GPIO (5V) | PD3 | 49 | GPIO |
| PD4 | 50 | GPIO | PD5 | 51 | GPIO |
| PD6 | 52 | GPIO | PD7 | 53 | GPIO |
| PD8 | 54 | GPIO | PC6 | 55 | GPIO |
| PC7 | 56 | GPIO | DVDD | 57 | Digital power supply. |
| DECOUPLE | 59 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PE0 | 60 | GPIO (5V) |
| PE1 | 61 | GPIO (5V) | PE2 | 62 | GPIO |
| PE3 | 63 | GPIO | PE4 | 64 | GPIO |
| PE5 | 65 | GPIO | PE6 | 66 | GPIO |
| PE7 | 67 | GPIO | PC8 | 68 | GPIO (5V) |
| PC9 | 69 | GPIO (5V) | PC10 | 70 | GPIO (5V) |
| PC11 | 71 | GPIO (5V) | PC12 | 72 | GPIO (5V) |
| PC13 | 73 | GPIO (5V) | PC14 | 74 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PC15 | 75 | GPIO (5V) | PF0 | 76 | GPIO (5V) |
| PF1 | 77 | GPIO (5V) | PF2 | 78 | GPIO |
| PF3 | 79 | GPIO | PF4 | 80 | GPIO |
| PF5 | 81 | GPIO | PF6 | 84 | GPIO |
| PF7 | 85 | GPIO | PF8 | 86 | GPIO |
| PF9 | 87 | GPIO | PD9 | 88 | GPIO |
| PD10 | 89 | GPIO | PD11 | 90 | GPIO |
| PD12 | 91 | GPIO | PE8 | 92 | GPIO |
| PE9 | 93 | GPIO | PE10 | 94 | GPIO |
| PE11 | 95 | GPIO | PE12 | 96 | GPIO |
| PE13 | 97 | GPIO | PE14 | 98 | GPIO |
| PE15 | 99 | GPIO | PA15 | 100 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.12 EFM32GG12B8xx in QFP64 Device Pinout

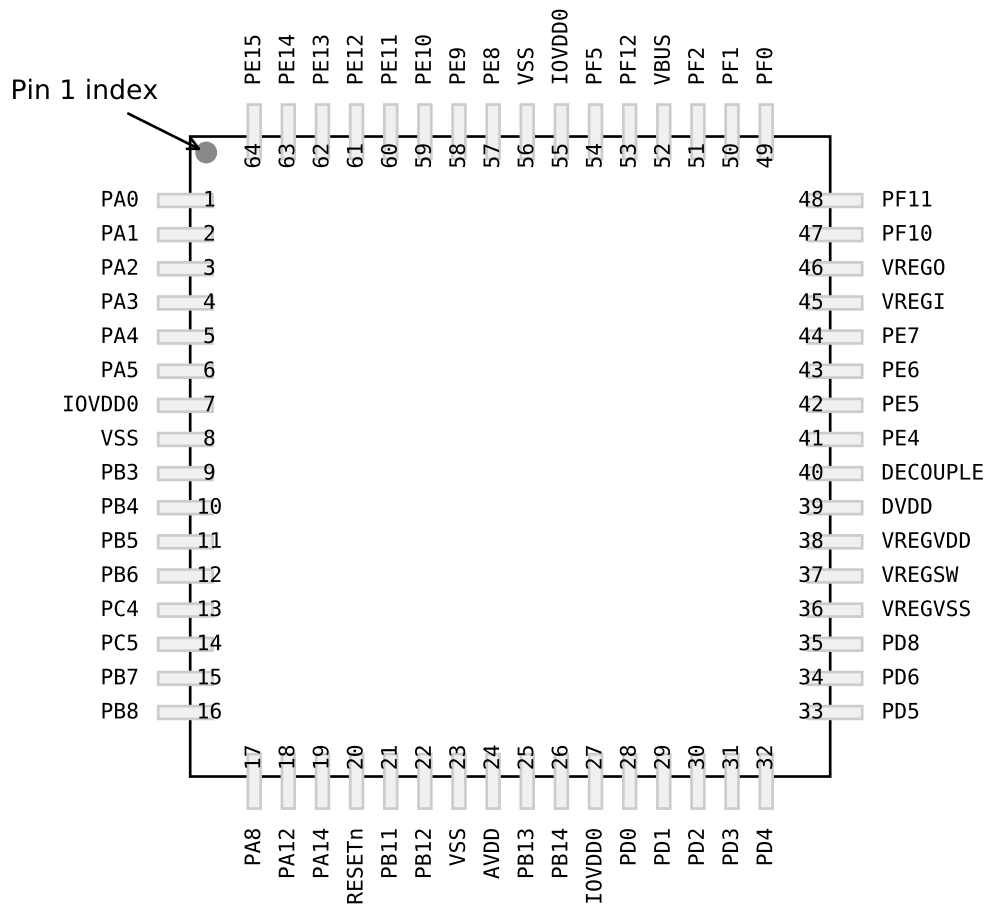


Figure 5.12. EFM32GG12B8xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.12. EFM32GG12B8xx in QFP64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|---------------|-------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| IOVDD0 | 7 27 55 | Digital IO power supply 0. | VSS | 8 23 56 | Ground |
| PB3 | 9 | GPIO | PB4 | 10 | GPIO |
| PB5 | 11 | GPIO | PB6 | 12 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------------|----------|--------|---|
| PC4 | 13 | GPIO | PC5 | 14 | GPIO |
| PB7 | 15 | GPIO | PB8 | 16 | GPIO |
| PA8 | 17 | GPIO | PA12 | 18 | GPIO (5V) |
| PA14 | 19 | GPIO | RESETn | 20 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB11 | 21 | GPIO | PB12 | 22 | GPIO |
| AVDD | 24 | Analog power supply. | PB13 | 25 | GPIO |
| PB14 | 26 | GPIO | PD0 | 28 | GPIO (5V) |
| PD1 | 29 | GPIO | PD2 | 30 | GPIO (5V) |
| PD3 | 31 | GPIO | PD4 | 32 | GPIO |
| PD5 | 33 | GPIO | PD6 | 34 | GPIO |
| PD8 | 35 | GPIO | VREGVSS | 36 | Voltage regulator VSS |
| VREGSW | 37 | DCDC regulator switching node | VREGVDD | 38 | Voltage regulator VDD input |
| DVDD | 39 | Digital power supply. | DECOUPLE | 40 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PE4 | 41 | GPIO | PE5 | 42 | GPIO |
| PE6 | 43 | GPIO | PE7 | 44 | GPIO |
| VREGI | 45 | Input to 5 V regulator. | VREGO | 46 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |
| PF10 | 47 | GPIO (5V) | PF11 | 48 | GPIO (5V) |
| PF0 | 49 | GPIO (5V) | PF1 | 50 | GPIO (5V) |
| PF2 | 51 | GPIO | VBUS | 52 | USB VBUS signal and auxiliary input to 5 V regulator. |
| PF12 | 53 | GPIO (5V) | PF5 | 54 | GPIO |
| PE8 | 57 | GPIO | PE9 | 58 | GPIO |
| PE10 | 59 | GPIO | PE11 | 60 | GPIO |
| PE12 | 61 | GPIO | PE13 | 62 | GPIO |
| PE14 | 63 | GPIO | PE15 | 64 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.13 EFM32GG12B5xx in QFP64 Device Pinout

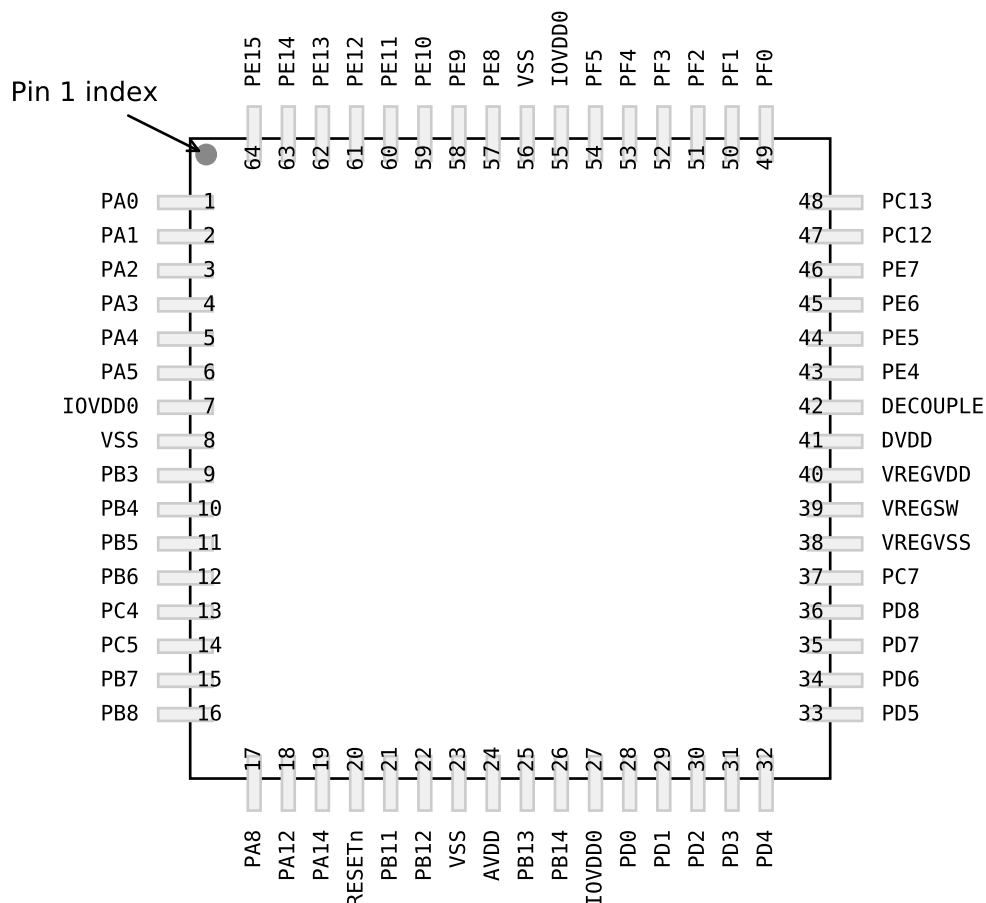


Figure 5.13. EFM32GG12B5xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.13. EFM32GG12B5xx in QFP64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|---------------|-------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| IOVDD0 | 7 27 55 | Digital IO power supply 0. | VSS | 8 23 56 | Ground |
| PB3 | 9 | GPIO | PB4 | 10 | GPIO |
| PB5 | 11 | GPIO | PB6 | 12 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------------|----------|--------|---|
| PC4 | 13 | GPIO | PC5 | 14 | GPIO |
| PB7 | 15 | GPIO | PB8 | 16 | GPIO |
| PA8 | 17 | GPIO | PA12 | 18 | GPIO (5V) |
| PA14 | 19 | GPIO | RESETn | 20 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB11 | 21 | GPIO | PB12 | 22 | GPIO |
| AVDD | 24 | Analog power supply. | PB13 | 25 | GPIO |
| PB14 | 26 | GPIO | PD0 | 28 | GPIO (5V) |
| PD1 | 29 | GPIO | PD2 | 30 | GPIO (5V) |
| PD3 | 31 | GPIO | PD4 | 32 | GPIO |
| PD5 | 33 | GPIO | PD6 | 34 | GPIO |
| PD7 | 35 | GPIO | PD8 | 36 | GPIO |
| PC7 | 37 | GPIO | VREGVSS | 38 | Voltage regulator VSS |
| VREGSW | 39 | DCDC regulator switching node | VREGVDD | 40 | Voltage regulator VDD input |
| DVDD | 41 | Digital power supply. | DECOUPLE | 42 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PE4 | 43 | GPIO | PE5 | 44 | GPIO |
| PE6 | 45 | GPIO | PE7 | 46 | GPIO |
| PC12 | 47 | GPIO (5V) | PC13 | 48 | GPIO (5V) |
| PF0 | 49 | GPIO (5V) | PF1 | 50 | GPIO (5V) |
| PF2 | 51 | GPIO | PF3 | 52 | GPIO |
| PF4 | 53 | GPIO | PF5 | 54 | GPIO |
| PE8 | 57 | GPIO | PE9 | 58 | GPIO |
| PE10 | 59 | GPIO | PE11 | 60 | GPIO |
| PE12 | 61 | GPIO | PE13 | 62 | GPIO |
| PE14 | 63 | GPIO | PE15 | 64 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.14 EFM32GG12B4xx in QFP64 Device Pinout



Figure 5.14. EFM32GG12B4xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.14. EFM32GG12B4xx in QFP64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|---------------|-------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| IOVDD0 | 7 26 55 | Digital IO power supply 0. | VSS | 8 22 56 | Ground |
| PB3 | 9 | GPIO | PB4 | 10 | GPIO |
| PB5 | 11 | GPIO | PB6 | 12 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|--|----------|----------|---|
| PC4 | 13 | GPIO | PC5 | 14 | GPIO |
| PB7 | 15 | GPIO | PB8 | 16 | GPIO |
| PA12 | 17 | GPIO (5V) | PA13 | 18 | GPIO (5V) |
| PA14 | 19 | GPIO | RESETn | 20 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB11 | 21 | GPIO | AVDD | 23 27 | Analog power supply. |
| PB13 | 24 | GPIO | PB14 | 25 | GPIO |
| PD0 | 28 | GPIO (5V) | PD1 | 29 | GPIO |
| PD2 | 30 | GPIO (5V) | PD3 | 31 | GPIO |
| PD4 | 32 | GPIO | PD5 | 33 | GPIO |
| PD6 | 34 | GPIO | PD7 | 35 | GPIO |
| PD8 | 36 | GPIO | PC6 | 37 | GPIO |
| PC7 | 38 | GPIO | DVDD | 39 | Digital power supply. |
| DECOUPLE | 40 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PE4 | 41 | GPIO |
| PE5 | 42 | GPIO | PE6 | 43 | GPIO |
| PE7 | 44 | GPIO | VREGI | 45 | Input to 5 V regulator. |
| VREGO | 46 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs | PF10 | 47 | GPIO (5V) |
| PF11 | 48 | GPIO (5V) | PF0 | 49 | GPIO (5V) |
| PF1 | 50 | GPIO (5V) | PF2 | 51 | GPIO |
| VBUS | 52 | USB VBUS signal and auxiliary input to 5 V regulator. | PF12 | 53 | GPIO (5V) |
| PF5 | 54 | GPIO | PE8 | 57 | GPIO |
| PE9 | 58 | GPIO | PE10 | 59 | GPIO |
| PE11 | 60 | GPIO | PE12 | 61 | GPIO |
| PE13 | 62 | GPIO | PE14 | 63 | GPIO |
| PE15 | 64 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.15 EFM32GG12B1xx in QFP64 Device Pinout

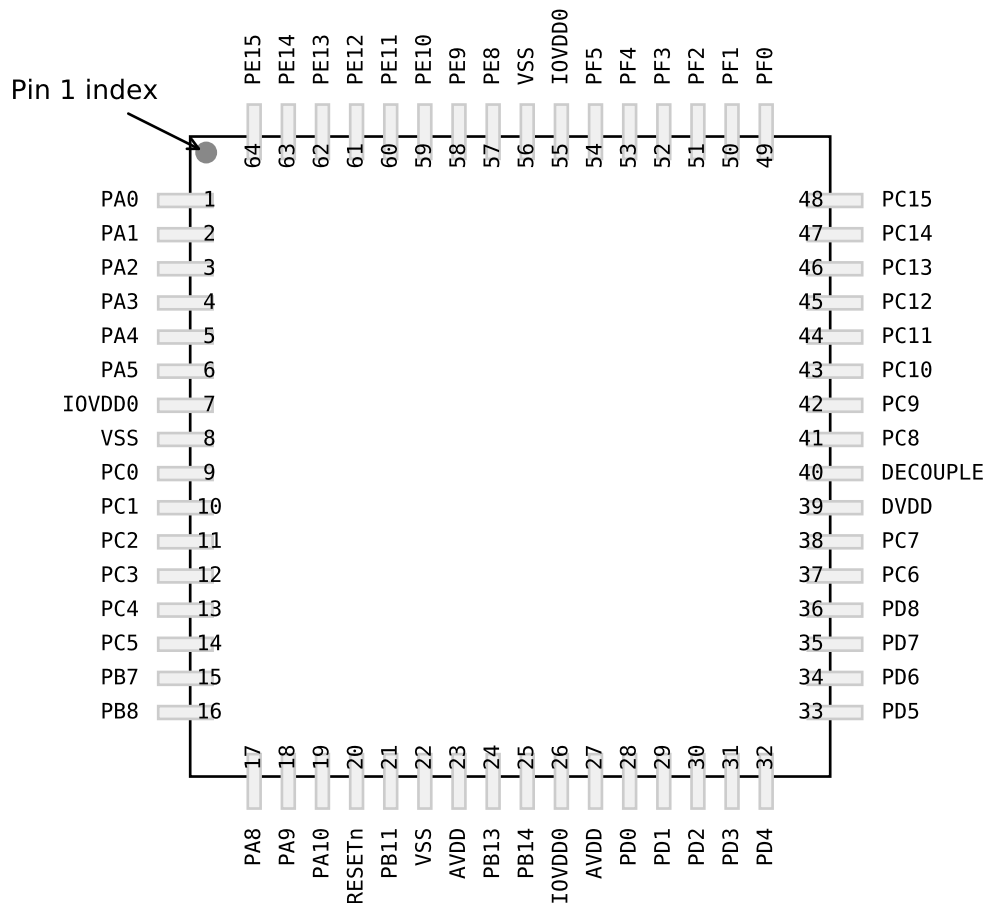


Figure 5.15. EFM32GG12B1xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.15. EFM32GG12B1xx in QFP64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|---------------|-------------|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| IOVDD0 | 7 26 55 | Digital IO power supply 0. | VSS | 8 22 56 | Ground |
| PC0 | 9 | GPIO (5V) | PC1 | 10 | GPIO (5V) |
| PC2 | 11 | GPIO (5V) | PC3 | 12 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|--|----------|----------|---|
| PC4 | 13 | GPIO | PC5 | 14 | GPIO |
| PB7 | 15 | GPIO | PB8 | 16 | GPIO |
| PA8 | 17 | GPIO | PA9 | 18 | GPIO |
| PA10 | 19 | GPIO | RESETn | 20 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB11 | 21 | GPIO | AVDD | 23 27 | Analog power supply. |
| PB13 | 24 | GPIO | PB14 | 25 | GPIO |
| PD0 | 28 | GPIO (5V) | PD1 | 29 | GPIO |
| PD2 | 30 | GPIO (5V) | PD3 | 31 | GPIO |
| PD4 | 32 | GPIO | PD5 | 33 | GPIO |
| PD6 | 34 | GPIO | PD7 | 35 | GPIO |
| PD8 | 36 | GPIO | PC6 | 37 | GPIO |
| PC7 | 38 | GPIO | DVDD | 39 | Digital power supply. |
| DECOUPLE | 40 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PC8 | 41 | GPIO (5V) |
| PC9 | 42 | GPIO (5V) | PC10 | 43 | GPIO (5V) |
| PC11 | 44 | GPIO (5V) | PC12 | 45 | GPIO (5V) |
| PC13 | 46 | GPIO (5V) | PC14 | 47 | GPIO (5V) |
| PC15 | 48 | GPIO (5V) | PF0 | 49 | GPIO (5V) |
| PF1 | 50 | GPIO (5V) | PF2 | 51 | GPIO |
| PF3 | 52 | GPIO | PF4 | 53 | GPIO |
| PF5 | 54 | GPIO | PE8 | 57 | GPIO |
| PE9 | 58 | GPIO | PE10 | 59 | GPIO |
| PE11 | 60 | GPIO | PE12 | 61 | GPIO |
| PE13 | 62 | GPIO | PE14 | 63 | GPIO |
| PE15 | 64 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.16 EFM32GG12B8xx in QFN64 Device Pinout

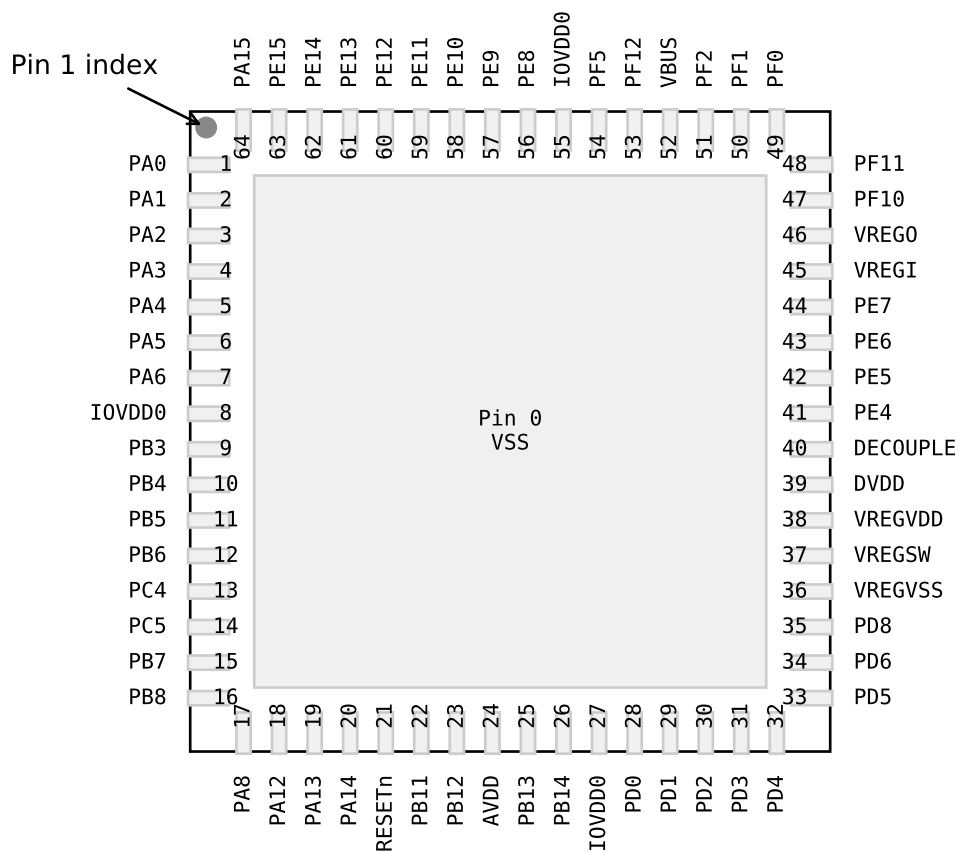


Figure 5.16. EFM32GG12B8xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.16. EFM32GG12B8xx in QFN64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|--------|-------------|
| VSS | 0 | Ground | PA0 | 1 | GPIO |
| PA1 | 2 | GPIO | PA2 | 3 | GPIO |
| PA3 | 4 | GPIO | PA4 | 5 | GPIO |
| PA5 | 6 | GPIO | PA6 | 7 | GPIO |
| IOVDD0 | 8 27 55 | Digital IO power supply 0. | PB3 | 9 | GPIO |
| PB4 | 10 | GPIO | PB5 | 11 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------------|----------|--------|---|
| PB6 | 12 | GPIO | PC4 | 13 | GPIO |
| PC5 | 14 | GPIO | PB7 | 15 | GPIO |
| PB8 | 16 | GPIO | PA8 | 17 | GPIO |
| PA12 | 18 | GPIO (5V) | PA13 | 19 | GPIO (5V) |
| PA14 | 20 | GPIO | RESETn | 21 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB11 | 22 | GPIO | PB12 | 23 | GPIO |
| AVDD | 24 | Analog power supply. | PB13 | 25 | GPIO |
| PB14 | 26 | GPIO | PD0 | 28 | GPIO (5V) |
| PD1 | 29 | GPIO | PD2 | 30 | GPIO (5V) |
| PD3 | 31 | GPIO | PD4 | 32 | GPIO |
| PD5 | 33 | GPIO | PD6 | 34 | GPIO |
| PD8 | 35 | GPIO | VREGVSS | 36 | Voltage regulator VSS |
| VREGSW | 37 | DCDC regulator switching node | VREGVDD | 38 | Voltage regulator VDD input |
| DVDD | 39 | Digital power supply. | DECOUPLE | 40 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PE4 | 41 | GPIO | PE5 | 42 | GPIO |
| PE6 | 43 | GPIO | PE7 | 44 | GPIO |
| VREGI | 45 | Input to 5 V regulator. | VREGO | 46 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |
| PF10 | 47 | GPIO (5V) | PF11 | 48 | GPIO (5V) |
| PF0 | 49 | GPIO (5V) | PF1 | 50 | GPIO (5V) |
| PF2 | 51 | GPIO | VBUS | 52 | USB VBUS signal and auxiliary input to 5 V regulator. |
| PF12 | 53 | GPIO (5V) | PF5 | 54 | GPIO |
| PE8 | 56 | GPIO | PE9 | 57 | GPIO |
| PE10 | 58 | GPIO | PE11 | 59 | GPIO |
| PE12 | 60 | GPIO | PE13 | 61 | GPIO |
| PE14 | 62 | GPIO | PE15 | 63 | GPIO |
| PA15 | 64 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.17 EFM32GG12B5xx in QFN64 Device Pinout

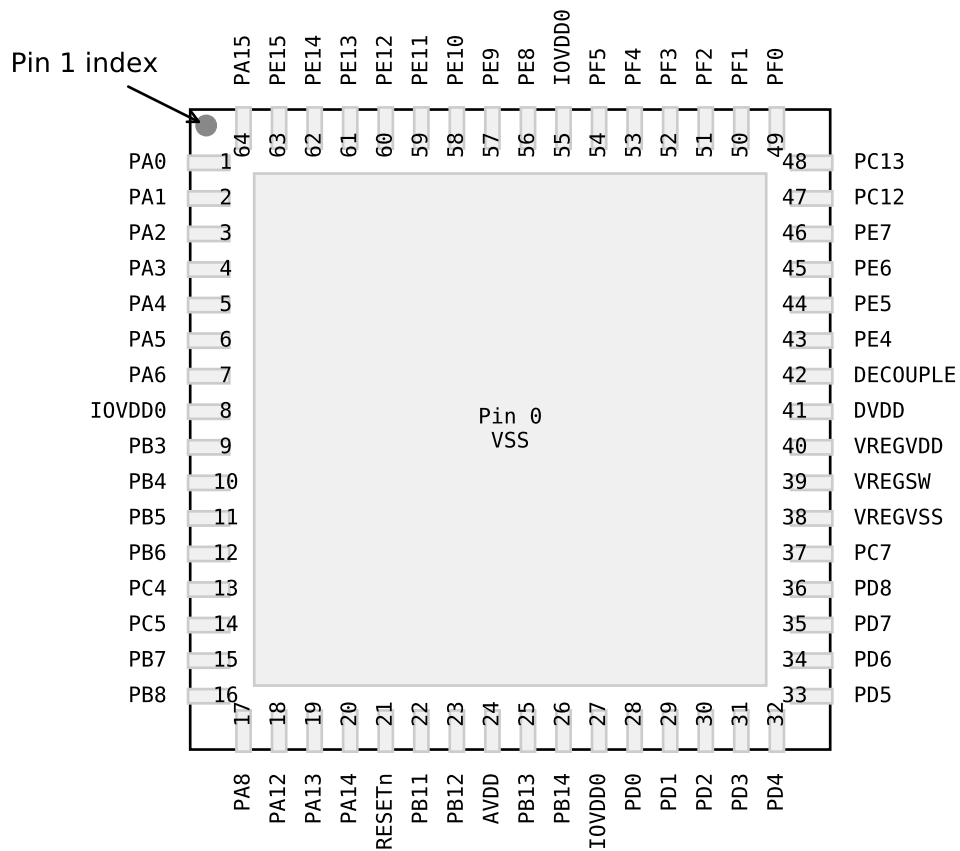


Figure 5.17. EFM32GG12B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.17. EFM32GG12B5xx in QFN64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|--------|-------------|
| VSS | 0 | Ground | PA0 | 1 | GPIO |
| PA1 | 2 | GPIO | PA2 | 3 | GPIO |
| PA3 | 4 | GPIO | PA4 | 5 | GPIO |
| PA5 | 6 | GPIO | PA6 | 7 | GPIO |
| IOVDD0 | 8 27 55 | Digital IO power supply 0. | PB3 | 9 | GPIO |
| PB4 | 10 | GPIO | PB5 | 11 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------------|----------|--------|---|
| PB6 | 12 | GPIO | PC4 | 13 | GPIO |
| PC5 | 14 | GPIO | PB7 | 15 | GPIO |
| PB8 | 16 | GPIO | PA8 | 17 | GPIO |
| PA12 | 18 | GPIO (5V) | PA13 | 19 | GPIO (5V) |
| PA14 | 20 | GPIO | RESETn | 21 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB11 | 22 | GPIO | PB12 | 23 | GPIO |
| AVDD | 24 | Analog power supply. | PB13 | 25 | GPIO |
| PB14 | 26 | GPIO | PD0 | 28 | GPIO (5V) |
| PD1 | 29 | GPIO | PD2 | 30 | GPIO (5V) |
| PD3 | 31 | GPIO | PD4 | 32 | GPIO |
| PD5 | 33 | GPIO | PD6 | 34 | GPIO |
| PD7 | 35 | GPIO | PD8 | 36 | GPIO |
| PC7 | 37 | GPIO | VREGVSS | 38 | Voltage regulator VSS |
| VREGSW | 39 | DCDC regulator switching node | VREGVDD | 40 | Voltage regulator VDD input |
| DVDD | 41 | Digital power supply. | DECOUPLE | 42 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. |
| PE4 | 43 | GPIO | PE5 | 44 | GPIO |
| PE6 | 45 | GPIO | PE7 | 46 | GPIO |
| PC12 | 47 | GPIO (5V) | PC13 | 48 | GPIO (5V) |
| PF0 | 49 | GPIO (5V) | PF1 | 50 | GPIO (5V) |
| PF2 | 51 | GPIO | PF3 | 52 | GPIO |
| PF4 | 53 | GPIO | PF5 | 54 | GPIO |
| PE8 | 56 | GPIO | PE9 | 57 | GPIO |
| PE10 | 58 | GPIO | PE11 | 59 | GPIO |
| PE12 | 60 | GPIO | PE13 | 61 | GPIO |
| PE14 | 62 | GPIO | PE15 | 63 | GPIO |
| PA15 | 64 | GPIO | | | |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.18 EFM32GG12B4xx in QFN64 Device Pinout

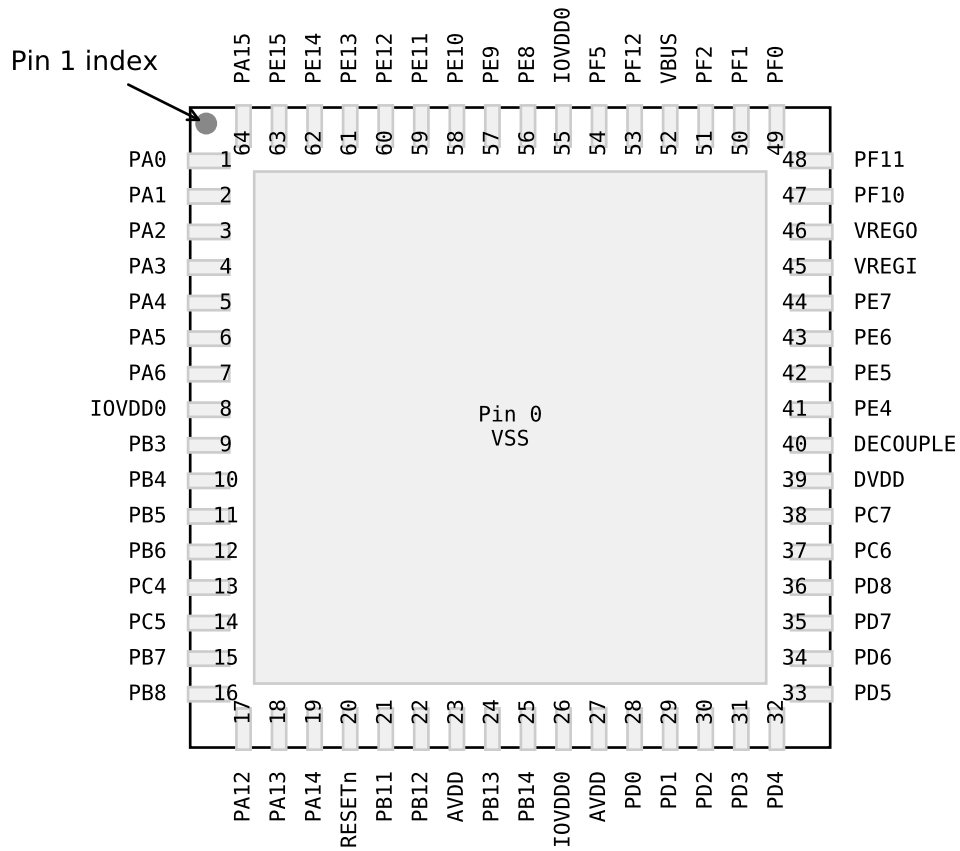


Figure 5.18. EFM32GG12B4xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.18. EFM32GG12B4xx in QFN64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|--------|-------------|
| VSS | 0 | Ground | PA0 | 1 | GPIO |
| PA1 | 2 | GPIO | PA2 | 3 | GPIO |
| PA3 | 4 | GPIO | PA4 | 5 | GPIO |
| PA5 | 6 | GPIO | PA6 | 7 | GPIO |
| IOVDD0 | 8 26 55 | Digital IO power supply 0. | PB3 | 9 | GPIO |
| PB4 | 10 | GPIO | PB5 | 11 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|----------|-------------------------|
| PB6 | 12 | GPIO | PC4 | 13 | GPIO |
| PC5 | 14 | GPIO | PB7 | 15 | GPIO |
| PB8 | 16 | GPIO | PA12 | 17 | GPIO (5V) |
| PA13 | 18 | GPIO (5V) | PA14 | 19 | GPIO |
| RESETn | 20 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB11 | 21 | GPIO |
| PB12 | 22 | GPIO | AVDD | 23 27 | Analog power supply. |
| PB13 | 24 | GPIO | PB14 | 25 | GPIO |
| PD0 | 28 | GPIO (5V) | PD1 | 29 | GPIO |
| PD2 | 30 | GPIO (5V) | PD3 | 31 | GPIO |
| PD4 | 32 | GPIO | PD5 | 33 | GPIO |
| PD6 | 34 | GPIO | PD7 | 35 | GPIO |
| PD8 | 36 | GPIO | PC6 | 37 | GPIO |
| PC7 | 38 | GPIO | DVDD | 39 | Digital power supply. |
| DECOUPLE | 40 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PE4 | 41 | GPIO |
| PE5 | 42 | GPIO | PE6 | 43 | GPIO |
| PE7 | 44 | GPIO | VREGI | 45 | Input to 5 V regulator. |
| VREGO | 46 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs | PF10 | 47 | GPIO (5V) |
| PF11 | 48 | GPIO (5V) | PF0 | 49 | GPIO (5V) |
| PF1 | 50 | GPIO (5V) | PF2 | 51 | GPIO |
| VBUS | 52 | USB VBUS signal and auxiliary input to 5 V regulator. | PF12 | 53 | GPIO (5V) |
| PF5 | 54 | GPIO | PE8 | 56 | GPIO |
| PE9 | 57 | GPIO | PE10 | 58 | GPIO |
| PE11 | 59 | GPIO | PE12 | 60 | GPIO |
| PE13 | 61 | GPIO | PE14 | 62 | GPIO |
| PE15 | 63 | GPIO | PA15 | 64 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.19 EFM32GG12B1xx in QFN64 Device Pinout



Figure 5.19. EFM32GG12B1xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.19. EFM32GG12B1xx in QFN64 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|---------------|----------------------------|----------|--------|-------------|
| VSS | 0 | Ground | PA0 | 1 | GPIO |
| PA1 | 2 | GPIO | PA2 | 3 | GPIO |
| PA3 | 4 | GPIO | PA4 | 5 | GPIO |
| PA5 | 6 | GPIO | PA6 | 7 | GPIO |
| IOVDD0 | 8 26 55 | Digital IO power supply 0. | PC0 | 9 | GPIO (5V) |
| PC1 | 10 | GPIO (5V) | PC2 | 11 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|----------|-----------------------|
| PC3 | 12 | GPIO (5V) | PC4 | 13 | GPIO |
| PC5 | 14 | GPIO | PB7 | 15 | GPIO |
| PB8 | 16 | GPIO | PA8 | 17 | GPIO |
| PA9 | 18 | GPIO | PA10 | 19 | GPIO |
| RESETn | 20 | Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB11 | 21 | GPIO |
| PB12 | 22 | GPIO | AVDD | 23 27 | Analog power supply. |
| PB13 | 24 | GPIO | PB14 | 25 | GPIO |
| PD0 | 28 | GPIO (5V) | PD1 | 29 | GPIO |
| PD2 | 30 | GPIO (5V) | PD3 | 31 | GPIO |
| PD4 | 32 | GPIO | PD5 | 33 | GPIO |
| PD6 | 34 | GPIO | PD7 | 35 | GPIO |
| PD8 | 36 | GPIO | PC6 | 37 | GPIO |
| PC7 | 38 | GPIO | DVDD | 39 | Digital power supply. |
| DECOUPLE | 40 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits. | PC8 | 41 | GPIO (5V) |
| PC9 | 42 | GPIO (5V) | PC10 | 43 | GPIO (5V) |
| PC11 | 44 | GPIO (5V) | PC12 | 45 | GPIO (5V) |
| PC13 | 46 | GPIO (5V) | PC14 | 47 | GPIO (5V) |
| PC15 | 48 | GPIO (5V) | PF0 | 49 | GPIO (5V) |
| PF1 | 50 | GPIO (5V) | PF2 | 51 | GPIO |
| PF3 | 52 | GPIO | PF4 | 53 | GPIO |
| PF5 | 54 | GPIO | PE8 | 56 | GPIO |
| PE9 | 57 | GPIO | PE10 | 58 | GPIO |
| PE11 | 59 | GPIO | PE12 | 60 | GPIO |
| PE13 | 61 | GPIO | PE14 | 62 | GPIO |
| PE15 | 63 | GPIO | PA15 | 64 | GPIO |

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [5.21 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 5.20. GPIO Functionality Table

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|-----------------------------|--|---|---|
| | Analog | EBI | Timers | Communication | Other |
| PA0 | BUSBY BUSAX LCD_SEG13 | EBI_AD09 #0 EBI_CSTFT #3 | TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4 | SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0 | PDM_CLK #0 CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0 |
| PA1 | BUSAY BUSBX LCD_SEG14 | EBI_AD10 #0 EBI_DCLK #3 | TIM0_CC0 #7 TIM0_CC1 #0 TIM3_CC1 #4 PCNT0_S1IN #4 | SDIO_DAT1 #1 US3_RX #0 QSPI0_CS1 #1 I2C0_SCL #0 | PDM_DAT0 #0 CMU_CLK1 #0 PRS_CH1 #0 |
| PA2 | BUSBY BUSAX LCD_SEG15 | EBI_AD11 #0 EBI_DTEN #3 | TIM0_CC2 #0 TIM3_CC2 #4 | SDIO_DAT2 #1 US1_RX #6 US3_CLK #0 QSPI0_DQ0 #1 | PDM_DAT1 #0 CMU_CLK0 #0 PRS_CH8 #1 ETM_TD0 #3 |
| PA3 | BUSAY BUSBX LCD_SEG16 | EBI_AD12 #0 EBI_VSNC #3 | TIM0_CDTI0 #0 TIM3_CC0 #5 | SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1 | CMU_CLK2 #1 CMU_CLKI0 #1 PDM_DAT2 #0 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3 |
| PA4 | BUSBY BUSAX LCD_SEG17 | EBI_AD13 #0 EBI_HSNC #3 | TIM0_CDTI1 #0 TIM3_CC1 #5 | SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1 | PDM_DAT3 #0 LES_ALTEX3 ETM_TD2 #3 |
| PA5 | BUSAY BUSBX LCD_SEG18 | EBI_AD14 #0 | TIM0_CDTI2 #0 TIM3_CC2 #5 PCNT1_S0IN #0 | SDIO_DAT5 #1 US3_RTS #0 U0_CTS #2 QSPI0_DQ3 #1 LEU1_TX #1 | LES_ALTEX4 ACMP1_O #7 ETM_TD3 #3 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|--|---|--|--|
| | Analog | EBI | Timers | Communication | Other |
| PA6 | BUSBY BUSAX LCD_SEG19 | EBI_AD15 #0 | TIM3_CC0 #6 WTIM0_CC0 #1 LETIM1_OUT1 #0 PCNT1_S1IN #0 | SDIO_CD #2 U0_RTS #2 LEU1_RX #1 | PRS_CH6 #0 ACMP0_O #4 ETM_TCLK #3 GPIO_EM4WU1 |
| PA7 | BUSAY BUSBX LCD_SEG35 | EBI_AD13 #1 EBI_A01 #3 EBI_CSTFT #0 | TIM0_CC2 #5 LETIM1_OUT0 #0 PCNT1_S0IN #4 | US2_TX #2 US4_CTS #0 | PRS_CH7 #1 |
| PA8 | BUSBY BUSAX LCD_SEG36 | EBI_AD14 #1 EBI_A02 #3 EBI_DCLK #0 | TIM2_CC0 #0 TIM0_CC0 #6 LETIM0_OUT0 #6 PCNT1_S1IN #4 | US2_RX #2 US4_RTS #0 | PRS_CH8 #0 |
| PA9 | BUSAY BUSBX LCD_SEG37 | EBI_AD15 #1 EBI_A03 #3 EBI_DTEN #0 | TIM2_CC1 #0 TIM0_CC1 #6 LETIM0_OUT1 #6 | US2_CLK #2 | PRS_CH9 #0 |
| PA10 | BUSBY BUSAX LCD_SEG38 | EBI_CS0 #1 EBI_A04 #3 EBI_VSNC #0 | TIM2_CC2 #0 TIM0_CC2 #6 | US2_CS #2 | PRS_CH10 #0 |
| PA11 | BUSAY BUSBX LCD_SEG39 | EBI_CS1 #1 EBI_A05 #3 EBI_HSNC #0 | LETIM1_OUT0 #1 | US2_CTS #2 | PRS_CH11 #0 |
| PA12 | BUSBY BUSAX | EBI_CS2 #1 EBI_REn #2 EBI_A00 #0 EBI_A06 #3 | TIM2_CC0 #1 WTIM0_CDT10 #2 LETIM1_OUT0 #2 PCNT1_S0IN #5 | CAN1_RX #5 US0_CLK #5 US2_RTS #2 | CMU_CLK0 #5 PRS_CH12 #0 ACMP1_O #3 |
| PA13 | BUSAY BUSBX | EBI_WEn #1 EBI_NANDWEn #2 EBI_A01 #0 EBI_A07 #3 | TIM0_CC2 #7 TIM2_CC1 #1 WTIM0_CDT11 #2 LETIM1_OUT1 #1 PCNT1_S1IN #5 | CAN1_TX #5 US0_CS #5 US2_TX #3 | PDM_DAT3 #3 PRS_CH13 #0 |
| PA14 | BUSBY BUSAX LCD_BEXT | EBI_REn #1 EBI_A02 #0 EBI_A08 #3 | TIM2_CC2 #1 WTIM0_CDT12 #2 LETIM1_OUT1 #2 | US1_TX #6 US2_RX #3 US3_RTS #2 | PRS_CH14 #0 ACMP1_O #4 |
| PA15 | BUSAY BUSBX LCD_SEG12 | EBI_AD08 #0 | TIM3_CC2 #0 | US2_CLK #3 | PRS_CH15 #0 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|--|---|--|--------------------------|
| | Analog | EBI | Timers | Communication | Other |
| PB0 | BUSBY BUSAX LCD_SEG32 | EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0 | TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2 | LEU1_TX #3 | PRS_CH4 #1 ACMP0_O #5 |
| PB1 | BUSAY BUSBX LCD_SEG33 | EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0 | TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LETIM1_OUT1 #5 PCNT0_S1IN #5 | LEU1_RX #3 | PRS_CH5 #1 |
| PB2 | BUSBY BUSAX LCD_SEG34 | EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0 | TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LETIM1_OUT0 #5 | US1_CS #6 | ACMP0_O #6 |
| PB3 | BUSAY BUSBX LCD_SEG20 / LCD_COM4 | EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0 | TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1 | SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1 | ACMP0_O #7 |
| PB4 | BUSBY BUSAX LCD_SEG21 / LCD_COM5 | EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0 | WTIM0_CC1 #6 PCNT1_S1IN #1 | SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4 | |
| PB5 | BUSAY BUSBX LCD_SEG22 / LCD_COM6 | EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0 | WTIM0_CC2 #6 LETIM1_OUT0 #4 PCNT0_S0IN #6 | US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4 | |
| PB6 | BUSBY BUSAX LCD_SEG23 / LCD_COM7 | EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0 | TIM0_CC0 #3 TIM2_CC0 #4 LETIM1_OUT1 #4 PCNT0_S1IN #6 | US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1 | PRS_CH12 #1 |
| PB7 | LFXTAL_P | | TIM0_CDTI0 #4 TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 US3_RX #2 US4_TX #0 U0_CTS #4 | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|--|--|---|---|
| | Analog | EBI | Timers | Communication | Other |
| PB8 | LFXTAL_N | | TIM0_CDTI1 #4 TIM1_CC1 #3 | US0_RX #4 US1_CS #0 US4_RX #0 U0_RTS #4 | CMU_CLKI0 #2 |
| PB9 | BUSAY BUSBX | EBI_ALE #1 EBI_NANDREn #2 EBI_A00 #1 EBI_A03 #0 EBI_A09 #3 | LETIM0_OUT0 #7 | SDIO_WP #3 CAN0_RX #3 US1_CTS #0 U1_TX #2 | PDM_DAT2 #3 PRS_CH13 #1 ACMP1_O #5 |
| PB10 | BUSBY BUSAX | EBI_BL0 #2 EBI_A01 #1 EBI_A04 #0 EBI_A10 #3 | LETIM0_OUT1 #7 | SDIO_CD #3 CAN0_TX #3 US1_RTS #0 US2_CTS #3 U1_RX #2 | PDM_DAT1 #3 PRS_CH9 #2 ACMP1_O #6 |
| PB11 | BUSAY BUSBX VDAC0_OUT0 / OPA0_OUT IDAC0_OUT | EBI_BL1 #2 EBI_A02 #1 EBI_A11 #3 | TIM0_CDTI2 #4 TIM1_CC2 #3 LETIM0_OUT0 #1 PCNT0_S1IN #7 PCNT1_S0IN #6 | US0_CTS #5 US1_CLK #5 US2_CS #3 U1_CTS #2 I2C1_SDA #1 | CMU_CLK1 #5 CMU_CLKI0 #7 PDM_DAT0 #3 ACMP0_O #3 GPIO_EM4WU7 |
| PB12 | BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT | EBI_A03 #1 EBI_A12 #3 | TIM1_CC3 #3 LETIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6 | US2_CTS #1 U1_RTS #2 I2C1_SCL #1 | PDM_CLK #3 |
| PB13 | BUSAY BUSBX HFXTAL_P | | WTIM1_CC0 #0 PCNT2_S0IN #2 | US0_CLK #4 US1_CTS #5 LEU0_TX #1 | CMU_CLKI0 #3 PRS_CH7 #0 |
| PB14 | BUSBY BUSAX HFXTAL_N | | WTIM1_CC1 #0 PCNT2_S1IN #2 | US0_CS #4 US1_RTS #5 LEU0_RX #1 | PRS_CH6 #1 |
| PB15 | BUSAY BUSBX | EBI_CS3 #1 EBI_ARDY #2 | TIM3_CC1 #7 | SDIO_WP #2 US2_RTS #1 | ETM_TD2 #1 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|--|--|--|--|------------------------|
| | Analog | EBI | Timers | Communication | Other |
| PC0 | VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X | EBI_AD07 #1 EBI_CS0 #2 EBI_REn #3 EBI_A23 #0 | TIM0_CC1 #3 TIM2_CC1 #4 PCNT0_S0IN #2 | CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4 | LES_CH0 PRS_CH2 #0 |
| PC1 | VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X | EBI_AD08 #1 EBI_CS1 #2 EBI_BL0 #3 EBI_A24 #0 | TIM0_CC2 #3 TIM2_CC2 #4 WTIM0_CC0 #7 PCNT0_S1IN #2 | CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4 | LES_CH1 PRS_CH3 #0 |
| PC2 | VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X | EBI_AD09 #1 EBI_CS2 #2 EBI_NANDWEEn #3 EBI_A25 #0 | TIM0_CDTI0 #3 TIM2_CC0 #5 WTIM0_CC1 #7 LETIM1_OUT0 #3 | CAN1_RX #0 US1_RX #4 US2_TX #0 QSPIO_RST0 #1 | LES_CH2 PRS_CH10 #1 |
| PC3 | VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BUSACMP0X | EBI_AD10 #1 EBI_CS3 #2 EBI_BL1 #3 EBI_NANDREn #0 | TIM0_CDTI1 #3 TIM2_CC1 #5 WTIM0_CC2 #7 LETIM1_OUT1 #3 | CAN1_TX #0 US1_CLK #4 US2_RX #0 QSPIO_RST1 #1 | LES_CH3 PRS_CH11 #1 |
| PC4 | BUSACMP0Y BUSACMP0X OPA0_P | EBI_AD11 #1 EBI_ALE #2 EBI_NANDREn #3 EBI_A26 #0 | TIM0_CC0 #5 TIM0_CDTI2 #3 TIM2_CC2 #5 LETIM0_OUT0 #3 PCNT1_S0IN #3 | SDIO_CD #1 US2_CLK #0 US4_CLK #0 U0_TX #4 U1_CTS #4 I2C1_SDA #0 | LES_CH4 GPIO_EM4WU6 |
| PC5 | BUSACMP0Y BUSACMP0X OPA0_N | EBI_AD12 #1 EBI_WEn #2 EBI_NANDWEEn #0 EBI_A00 #3 | TIM0_CC1 #5 LETIM0_OUT1 #3 PCNT1_S1IN #3 | SDIO_WP #1 US2_CS #0 US4_CS #0 U0_RX #4 U1_RTS #4 I2C1_SCL #0 | LES_CH5 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|--|---|---|---------------------------------------|
| | Analog | EBI | Timers | Communication | Other |
| PC6 | BUSACMP0Y BUSACMP0X OPA3_P | EBI_A05 #0 | WTIM1_CC3 #2 | US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2 | LES_CH6 PRS_CH14 #1 ETM_TCLK #2 |
| PC7 | BUSACMP0Y BUSACMP0X OPA3_N | EBI_A06 #0 EBI_A13 #1 EBI_A21 #3 | WTIM1_CC0 #3 | US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2 | LES_CH7 PRS_CH15 #1 ETM_TD0 #2 |
| PC8 | BUSACMP1Y BUSACMP1X | EBI_A15 #0 EBI_A20 #1 EBI_A26 #3 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 PRS_CH4 #0 |
| PC9 | BUSACMP1Y BUSACMP1X | EBI_A21 #1 EBI_A27 #3 | TIM2_CC1 #2 | CAN1_RX #3 US0_CLK #2 | LES_CH9 PRS_CH5 #0 GPIO_EM4WU2 |
| PC10 | BUSACMP1Y BUSACMP1X | EBI_A22 #1 | TIM2_CC2 #2 | CAN1_TX #3 US0_RX #2 | LES_CH10 |
| PC11 | BUSACMP1Y BUSACMP1X | EBI_ALE #4 EBI_ALE #5 EBI_A23 #1 | | CAN1_TX #4 US0_TX #2 I2C1_SDA #4 | LES_CH11 |
| PC12 | VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BUSACMP1X | | TIM1_CC3 #0 PCNT2_S0IN #4 | CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 | CMU_CLK0 #1 LES_CH12 |
| PC13 | VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BUSACMP1X | EBI_ARDY #4 | TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 PCNT2_S1IN #4 | US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 | LES_CH13 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|--|--|--|--|--|
| | Analog | EBI | Timers | Communication | Other |
| PC14 | VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSACMP1Y BUSACMP1X | EBI_NANDWE _n #4 | TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 LETIM0_OUT0 #5 PCNT0_S1IN #0 | US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 U1_CTS #0 LEU0_TX #5 | LES_CH14 PRS_CH0 #2 |
| PC15 | VDAC0_OUT1ALT / OPA1_OUTALT #3 BUSACMP1Y BUSACMP1X | EBI_NANDRE _n #4 | TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LETIM0_OUT1 #5 | US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 U1_RTS #0 LEU0_RX #5 | LES_CH15 PRS_CH1 #2 DBG_SWO #1 |
| PD0 | VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BUSADC0Y BUSADC0X | EBI_A04 #1 EBI_A13 #3 | WTIM1_CC2 #0 PCNT2_S0IN #0 | CAN0_RX #2 US1_TX #1 USB_VBUSEN #2 | PDM_CLK #4 |
| PD1 | VDAC0_OUT1ALT / OPA1_OUTALT #4 BUSADC0Y BUSADC0X OPA3_OUT | EBI_A05 #1 EBI_A14 #3 | TIM0_CC0 #2 WTIM1_CC3 #0 PCNT2_S1IN #0 | CAN0_TX #2 US1_RX #1 | PDM_DAT0 #4 DBG_SWO #2 |
| PD2 | BUSADC0Y BUSADC0X | EBI_A06 #1 EBI_A15 #3 EBI_A27 #0 | TIM0_CC1 #2 WTIM1_CC0 #1 | US1_CLK #1 LEU1_TX #2 | PDM_DAT1 #4 DBG_SWO #3 |
| PD3 | BUSADC0Y BUSADC0X OPA2_N | EBI_A07 #1 EBI_A16 #3 | TIM0_CC2 #2 WTIM1_CC1 #1 | CAN1_RX #2 US1_CS #1 LEU1_RX #2 | PDM_DAT2 #4 ETM_TD1 #0 ETM_TD1 #2 |
| PD4 | BUSADC0Y BUSADC0X OPA2_P | EBI_A08 #1 EBI_A17 #3 | WTIM0_CDTI0 #4 WTIM1_CC2 #1 | CAN1_TX #2 US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3 | CMU_CLKI0 #0 PDM_DAT3 #4 PRS_CH10 #2 ETM_TD2 #0 ETM_TD2 #2 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|----------------------------|--|---|---|
| | Analog | EBI | Timers | Communication | Other |
| PD5 | BUSADC0Y BUSADC0X OPA2_OUT | EBI_A09 #1 EBI_A18 #3 | WTIM0_CDTI1 #4 WTIM1_CC3 #1 | US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3 | PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2 |
| PD6 | BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT ADC1_EXTP OPA1_P | EBI_A10 #1 EBI_A19 #3 | TIM1_CC0 #4 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1 | CMU_CLK2 #2 LES_ALTEX0 PRS_CH5 #2 ACMP0_O #2 ETM_TD0 #0 |
| PD7 | BUSADC0Y BUSADC0X ADC0_EXTN ADC1_EXTN OPA1_N | EBI_A11 #1 EBI_A20 #3 | TIM1_CC1 #4 WTIM1_CC1 #2 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 ACMP1_O #2 ETM_TCLK #0 |
| PD8 | BU_VIN | EBI_A12 #1 | WTIM1_CC2 #2 | US2_RTS #5 | CMU_CLK1 #1 PRS_CH12 #2 ACMP2_O #0 |
| PD9 | LCD_SEG28 | EBI_CS0 #0 EBI_DTEN #1 | | SDIO_DAT7 #0 QSPI0_DQ0 #0 US4_TX #1 | PDM_DAT3 #2 |
| PD10 | LCD_SEG29 | EBI_CS1 #0 EBI_VSNC #1 | | SDIO_DAT6 #0 QSPI0_DQ1 #0 US4_RX #1 | CMU_CLK2 #5 CMU_CLKI0 #5 |
| PD11 | LCD_SEG30 | EBI_CS2 #0 EBI_HSNC #1 | | SDIO_DAT5 #0 QSPI0_DQ2 #0 US4_CLK #1 | |
| PD12 | LCD_SEG31 | EBI_CS3 #0 | | SDIO_DAT4 #0 QSPI0_DQ3 #0 US4_CS #1 | |
| PD13 | | EBI_ARDY #1 | TIM2_CDTI0 #1 TIM3_CC1 #6 WTIM0_CC1 #1 | US4_CTS #1 | ETM_TD1 #1 |
| PD14 | | EBI_NANDWE _n #1 | TIM2_CDTI1 #1 TIM3_CC2 #6 WTIM0_CC2 #1 | CAN0_RX #5 US4_RTS #1 I2C0_SDA #3 | |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|--|---|--|----------------------------|
| | Analog | EBI | Timers | Communication | Other |
| PD15 | | EBI_NANDREn #1 | TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2 | CAN0_TX #5 I2C0_SCL #3 | |
| PE0 | BUSDY BUSCX | EBI_A07 #0 | TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1 | CAN0_RX #6 U0_TX #1 I2C1_SDA #2 | ACMP2_O #1 |
| PE1 | BUSCY BUSDX | EBI_A08 #0 | TIM3_CC1 #1 WTIM1_CC2 #3 PCNT0_S1IN #1 | CAN0_TX #6 U0_RX #1 I2C1_SCL #2 | CMU_CLKI0 #4 ACMP2_O #2 |
| PE2 | BU_VOUT | EBI_A09 #0 EBI_A14 #1 | TIM3_CC2 #1 WTIM1_CC3 #3 | US0_RTS #1 U0_CTS #1 U1_TX #3 | ACMP0_O #1 |
| PE3 | BU_STAT | EBI_A10 #0 EBI_A15 #1 | TIM3_CC0 #2 WTIM1_CC0 #4 | US0_CTS #1 U0_RTS #1 U1_RX #3 | ACMP1_O #1 |
| PE4 | BUSDY BUSCX LCD_COM0 | EBI_A11 #0 EBI_A16 #1 EBI_A22 #3 | TIM3_CC1 #2 WTIM0_CC0 #0 WTIM1_CC1 #4 | US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 U1_CTS #3 I2C0_SDA #7 USB_VBUSEN #1 | |
| PE5 | BUSCY BUSDX LCD_COM1 | EBI_A12 #0 EBI_A17 #1 EBI_A23 #3 | TIM3_CC0 #3 TIM3_CC2 #2 WTIM0_CC1 #0 WTIM1_CC2 #4 | US0_CLK #1 US1_CLK #6 US3_CTS #1 U1_RTS #3 I2C0_SCL #7 | |
| PE6 | BUSDY BUSCX LCD_COM2 | EBI_A13 #0 EBI_A18 #1 EBI_A24 #3 | TIM3_CC1 #3 WTIM0_CC2 #0 WTIM1_CC3 #4 | US0_RX #1 US3_TX #1 | PRS_CH6 #2 |
| PE7 | BUSCY BUSDX LCD_COM3 | EBI_A14 #0 EBI_A19 #1 EBI_A25 #3 | TIM3_CC2 #3 WTIM1_CC0 #5 | US0_TX #1 US3_RX #1 | PRS_CH7 #2 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|---------------------------|--|---|--|
| | Analog | EBI | Timers | Communication | Other |
| PE8 | BUSDY BUSCX LCD_SEG4 | EBI_AD00 #0 EBI_CS0 #4 | TIM2_CDTI0 #2 PCNT2_S0IN #1 | SDIO_DAT3 #0 QSPIO_DQ4 #0 | PDM_CLK #1 PRS_CH3 #1 |
| PE9 | BUSCY BUSDX LCD_SEG5 | EBI_AD01 #0 EBI_CS1 #4 | PCNT2_S1IN #1 | SDIO_DAT2 #0 QSPIO_DQ5 #0 | PDM_DAT0 #1 PRS_CH8 #2 |
| PE10 | BUSDY BUSCX LCD_SEG6 | EBI_AD02 #0 EBI_CS2 #4 | TIM1_CC0 #1 WTIM0_CDTI0 #0 | SDIO_DAT1 #0 QSPIO_DQ6 #0 US0_TX #0 | PDM_DAT1 #1 PRS_CH2 #2 GPIO_EM4WU9 |
| PE11 | BUSCY BUSDX LCD_SEG7 | EBI_AD03 #0 EBI_CS3 #4 | TIM1_CC1 #1 WTIM0_CDTI1 #0 | SDIO_DAT0 #0 QSPIO_DQ7 #0 US0_RX #0 | LES_ALTEX5 PDM_DAT2 #1 PRS_CH3 #2 ETM_TCLK #4 |
| PE12 | BUSDY BUSCX LCD_SEG8 | EBI_AD04 #0 | TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4 | SDIO_CMD #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6 | CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PDM_DAT3 #1 PRS_CH1 #3 ETM_TD0 #4 |
| PE13 | BUSCY BUSDX LCD_SEG9 | EBI_AD05 #0 | TIM1_CC3 #1 TIM2_CC2 #3 LETIM0_OUT1 #4 | SDIO_CLK #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6 | LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5 |
| PE14 | BUSDY BUSCX LCD_SEG10 | EBI_AD06 #0 | TIM2_CDTI1 #2 TIM3_CC0 #0 | QSPIO_RST0 #0 SDIO_CLK #1 US0_CTS #0 QSPIO_SCLK #1 LEU0_TX #2 | PRS_CH13 #2 ETM_TD2 #4 |
| PE15 | BUSCY BUSDX LCD_SEG11 | EBI_AD07 #0 | TIM2_CDTI2 #2 TIM3_CC1 #0 | QSPIO_RST1 #0 SDIO_CMD #1 US0_RTS #0 QSPIO_DQS #1 LEU0_RX #2 | PRS_CH14 #2 ETM_TD3 #4 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|--|---|--|---|
| | Analog | EBI | Timers | Communication | Other |
| PF0 | BUSDY BUSCX | EBI_A24 #1 | TIM0_CC0 #4 WTIM0_CC1 #4 LETIM0_OUT0 #2 | US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | PRS_CH15 #2 DBG_SWCLKTCK BOOT_TX |
| PF1 | BUSCY BUSDX | EBI_A25 #1 | TIM0_CC1 #4 WTIM0_CC2 #4 LETIM0_OUT1 #2 | US2_RX #5 CAN1_RX #1 US1_CS #2 U0_TX #5 LEU0_RX #3 I2C0_SCL #5 | PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX |
| PF2 | BUSDY BUSCX LCD_SEG0 | EBI_ARDY #0 EBI_A26 #1 | TIM0_CC2 #4 TIM1_CC0 #5 TIM2_CC0 #3 | US2_CLK #5 CAN0_TX #1 US1_TX #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4 | CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO DBG_SWO #0 GPIO_EM4WU4 |
| PF3 | BUSCY BUSDX LCD_SEG1 | EBI_ALE #0 | TIM0_CDTI0 #2 TIM1_CC1 #5 | CAN1_TX #1 US1_CTS #2 | CMU_CLK1 #4 PRS_CH0 #1 ETM_TD3 #1 |
| PF4 | BUSDY BUSCX LCD_SEG2 | EBI_WEn #0 EBI_WEn #5 | TIM0_CDTI1 #2 TIM1_CC2 #5 | US1_RTS #2 | PRS_CH1 #1 |
| PF5 | BUSCY BUSDX LCD_SEG3 | EBI_REn #0 EBI_REn #5 EBI_A27 #1 | TIM0_CDTI2 #2 TIM1_CC3 #6 | US2_CS #5 USB_VBUSEN #0 | PRS_CH2 #1 DBG_TDI |
| PF6 | BUSDY BUSCX LCD_SEG24 | EBI_BL0 #0 EBI_BL0 #4 EBI_BL0 #5 EBI_CSTFT #1 | TIM0_CC0 #1 | US2_TX #4 QSPIO_SCLK #0 US1_TX #3 U0_TX #0 | PDM_CLK #2 |
| PF7 | BUSCY BUSDX LCD_SEG25 | EBI_BL1 #0 EBI_BL1 #4 EBI_BL1 #5 EBI_DCLK #1 | TIM0_CC1 #1 | US2_RX #4 QSPIO_CS0 #0 US1_RX #3 U0_RX #0 | PDM_DAT0 #2 |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|-----------|---|--------------------------|---------------|--|---|
| | Analog | EBI | Timers | Communication | Other |
| PF8 | BUSDY BUSCX LCD_SEG26 | EBI_WEn #4 EBI_BL0 #1 | TIM0_CC2 #1 | US2_CLK #4 QSPIO_CS1 #0 SDIO_CD #0 U0_CTS #0 U1_RTS #1 | PDM_DAT1 #2 ETM_TCLK #1 GPIO_EM4WU8 |
| PF9 | BUSCY BUSDX LCD_SEG27 | EBI_REn #4 EBI_BL1 #1 | | US2_CS #4 QSPIO_DQS #0 SDIO_WP #0 U0_RTS #0 U1_CTS #1 | PDM_DAT2 #2 ETM_TD0 #1 |
| PF10 | BUSDY BUSCX | EBI_ARDY #5 | PCNT2_S0IN #3 | U1_TX #1 USB_DM | |
| PF11 | BUSCY BUSDX | EBI_NANDWEn #5 | PCNT2_S1IN #3 | U1_RX #1 USB_DP | |
| PF12 | BUSDY BUSCX | EBI_NANDREn #5 | TIM1_CC3 #5 | USB_ID | |
| PF13 | BUSCY BUSDX | | TIM1_CC0 #6 | | |
| PF14 | BUSDY BUSCX | | TIM1_CC1 #6 | | |

5.21 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to [5.20 GPIO Functionality Table](#) for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.21. Alternate Functionality Overview

| Alternate Functionality | LOCATION | | Description |
|----------------------------|--|--|--|
| | 0 - 3 | 4 - 7 | |
| ACMP0_O | 0: PE13 1: PE2 2: PD6 3: PB11 | 4: PA6 5: PB0 6: PB2 7: PB3 | Analog comparator ACMP0, digital output. |
| ACMP1_O | 0: PF2 1: PE3 2: PD7 3: PA12 | 4: PA14 5: PB9 6: PB10 7: PA5 | Analog comparator ACMP1, digital output. |
| ACMP2_O | 0: PD8 1: PE0 2: PE1 | | Analog comparator ACMP2, digital output. |
| ADC0_EXTN | 0: PD7 | | Analog to digital converter ADC0 external reference input negative pin. |
| ADC0_EXTP | 0: PD6 | | Analog to digital converter ADC0 external reference input positive pin. |
| ADC1_EXTN | 0: PD7 | | Analog to digital converter ADC1 external reference input negative pin. |
| ADC1_EXTP | 0: PD6 | | Analog to digital converter ADC1 external reference input positive pin. |
| BOOT_RX | 0: PF1 | | Bootloader RX. |
| BOOT_TX | 0: PF0 | | Bootloader TX. |
| BU_STAT | 0: PE3 | | Backup Power Domain status, whether or not the system is in backup mode. |
| BU_VIN | 0: PD8 | | Battery input for Backup Power Domain. |
| BU_VOUT | 0: PE2 | | Power output for Backup Power Domain. |
| CAN0_RX | 0: PC0 1: PF0 2: PD0 3: PB9 | 5: PD14 6: PE0 | CAN0 RX. |
| CAN0_TX | 0: PC1 1: PF2 2: PD1 3: PB10 | 5: PD15 6: PE1 | CAN0 TX. |

| Alternate | LOCATION | | Description |
|--------------|---------------------------------------|---|---|
| | 0 - 3 | 4 - 7 | |
| CAN1_RX | 0: PC2 1: PF1 2: PD3 3: PC9 | 4: PC12 5: PA12 | CAN1 RX. |
| CAN1_TX | 0: PC3 1: PF3 2: PD4 3: PC10 | 4: PC11 5: PA13 | CAN1 TX. |
| CMU_CLK0 | 0: PA2 1: PC12 2: PD7 | 4: PF2 5: PA12 | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | 0: PA1 1: PD8 2: PE12 | 4: PF3 5: PB11 | Clock Management Unit, clock output number 1. |
| CMU_CLK2 | 0: PA0 1: PA3 2: PD6 | 4: PA3 5: PD10 | Clock Management Unit, clock output number 2. |
| CMU_CLKI0 | 0: PD4 1: PA3 2: PB8 3: PB13 | 4: PE1 5: PD10 6: PE12 7: PB11 | Clock Management Unit, clock input number 0. |
| DBG_SWCLKTCK | 0: PF0 | | Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down. |
| DBG_SWDIOTMS | 0: PF1 | | Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up. |
| DBG_SWO | 0: PF2 1: PC15 2: PD1 3: PD2 | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| DBG_TDI | 0: PF5 | | Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active. |
| DBG_TDO | 0: PF2 | | Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received. |

| Alternate | LOCATION | | Description |
|-----------|------------------------------|-------|---|
| | 0 - 3 | 4 - 7 | |
| EBI_A00 | 0: PA12 1: PB9 3: PC5 | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | 0: PA13 1: PB10 3: PA7 | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | 0: PA14 1: PB11 3: PA8 | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | 0: PB9 1: PB12 3: PA9 | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | 0: PB10 1: PD0 3: PA10 | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | 0: PC6 1: PD1 3: PA11 | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | 0: PC7 1: PD2 3: PA12 | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | 0: PE0 1: PD3 3: PA13 | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | 0: PE1 1: PD4 3: PA14 | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | 0: PE2 1: PD5 3: PB9 | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | 0: PE3 1: PD6 3: PB10 | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | 0: PE4 1: PD7 3: PB11 | | External Bus Interface (EBI) address output pin 11. |

| Alternate | LOCATION | | Description |
|-----------|-----------------------------|-------|---|
| | 0 - 3 | 4 - 7 | |
| EBI_A12 | 0: PE5 1: PD8 3: PB12 | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | 0: PE6 1: PC7 3: PD0 | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | 0: PE7 1: PE2 3: PD1 | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | 0: PC8 1: PE3 3: PD2 | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | 0: PB0 1: PE4 3: PD3 | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | 0: PB1 1: PE5 3: PD4 | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | 0: PB2 1: PE6 3: PD5 | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | 0: PB3 1: PE7 3: PD6 | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | 0: PB4 1: PC8 3: PD7 | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | 0: PB5 1: PC9 3: PC7 | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | 0: PB6 1: PC10 3: PE4 | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | 0: PC0 1: PC11 3: PE5 | | External Bus Interface (EBI) address output pin 23. |

| Alternate | LOCATION | | Description |
|-----------|----------------------------|-------|--|
| | 0 - 3 | 4 - 7 | |
| EBI_A24 | 0: PC1 1: PF0 3: PE6 | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | 0: PC2 1: PF1 3: PE7 | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | 0: PC4 1: PF2 3: PC8 | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | 0: PD2 1: PF5 3: PC9 | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | 0: PE8 1: PB0 | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | 0: PE9 1: PB1 | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | 0: PE10 1: PB2 | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | 0: PE11 1: PB3 | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | 0: PE12 1: PB4 | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | 0: PE13 1: PB5 | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | 0: PE14 1: PB6 | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | 0: PE15 1: PC0 | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | 0: PA15 1: PC1 | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | 0: PA0 1: PC2 | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | 0: PA1 1: PC3 | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | 0: PA2 1: PC4 | | External Bus Interface (EBI) address and data input / output pin 11. |

| Alternate | LOCATION | | |
|---------------|--|--------------------|--|
| Functionality | 0 - 3 | 4 - 7 | Description |
| EBI_AD12 | 0: PA3 1: PC5 | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | 0: PA4 1: PA7 | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | 0: PA5 1: PA8 | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | 0: PA6 1: PA9 | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | 0: PF3 1: PB9 2: PC4 3: PB5 | 4: PC11 5: PC11 | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | 0: PF2 1: PD13 2: PB15 3: PB4 | 4: PC13 5: PF10 | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | 0: PF6 1: PF8 2: PB10 3: PC1 | 4: PF6 5: PF6 | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | 0: PF7 1: PF9 2: PB11 3: PC3 | 4: PF7 5: PF7 | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | 0: PD9 1: PA10 2: PC0 3: PB0 | 4: PE8 | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | 0: PD10 1: PA11 2: PC1 3: PB1 | 4: PE9 | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | 0: PD11 1: PA12 2: PC2 3: PB2 | 4: PE10 | External Bus Interface (EBI) Chip Select output 2. |

| Alternate | LOCATION | | |
|---------------|--|--------------------|--|
| Functionality | 0 - 3 | 4 - 7 | Description |
| EBI_CS3 | 0: PD12 1: PB15 2: PC3 3: PB3 | 4: PE11 | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | 0: PA7 1: PF6 3: PA0 | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | 0: PA8 1: PF7 3: PA1 | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | 0: PA9 1: PD9 3: PA2 | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | 0: PA11 1: PD11 3: PA4 | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | 0: PC3 1: PD15 2: PB9 3: PC4 | 4: PC15 5: PF12 | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | 0: PC5 1: PD14 2: PA13 3: PC2 | 4: PC14 5: PF11 | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | 0: PF5 1: PA14 2: PA12 3: PC0 | 4: PF9 5: PF5 | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | 0: PA10 1: PD10 3: PA3 | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | 0: PF4 1: PA13 2: PC5 3: PB6 | 4: PF8 5: PF4 | External Bus Interface (EBI) Write Enable output. |

| Alternate | LOCATION | | |
|---------------|---------------------------------------|---------------------------------------|--|
| Functionality | 0 - 3 | 4 - 7 | Description |
| ETM_TCLK | 0: PD7 1: PF8 2: PC6 3: PA6 | 4: PE11 | Embedded Trace Module ETM clock . |
| ETM_TD0 | 0: PD6 1: PF9 2: PC7 3: PA2 | 4: PE12 | Embedded Trace Module ETM data 0. |
| ETM_TD1 | 0: PD3 1: PD13 2: PD3 3: PA3 | 4: PE13 | Embedded Trace Module ETM data 1. |
| ETM_TD2 | 0: PD4 1: PB15 2: PD4 3: PA4 | 4: PE14 | Embedded Trace Module ETM data 2. |
| ETM_TD3 | 0: PD5 1: PF3 2: PD5 3: PA5 | 4: PE15 | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | 0: PA0 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | 0: PA6 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | 0: PC9 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | 0: PF1 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | 0: PF2 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | 0: PE13 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU6 | 0: PC4 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU7 | 0: PB11 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU8 | 0: PF8 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU9 | 0: PE10 | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | 0: PB14 | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | 0: PB13 | | High Frequency Crystal positive pin. |
| I2C0_SCL | 0: PA1 1: PD7 2: PC7 3: PD15 | 4: PC1 5: PF1 6: PE13 7: PE5 | I2C0 Serial Clock Line input / output. |

| Alternate | LOCATION | | Description |
|-----------|---------------------------------------|---------------------------------------|---|
| | 0 - 3 | 4 - 7 | |
| I2C0_SDA | 0: PA0 1: PD6 2: PC6 3: PD14 | 4: PC0 5: PF0 6: PE12 7: PE4 | I2C0 Serial Data input / output. |
| I2C1_SCL | 0: PC5 1: PB12 2: PE1 3: PD5 | 4: PF2 | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | 0: PC4 1: PB11 2: PE0 3: PD4 | 4: PC11 | I2C1 Serial Data input / output. |
| IDAC0_OUT | 0: PB11 | | IDAC0 output. |
| LCD_BEXT | 0: PA14 | | LCD external supply bypass in step down or charge pump mode. If using the LCD in step-down or charge pump mode, a 1 uF (minimum) capacitor between this pin and VSS is required. To reduce supply ripple, a larger capacitor of approximately 1000 times the total LCD segment capacitance may be used. If using the LCD with the internal supply source, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | 0: PE4 | | LCD driver common line number 0. |
| LCD_COM1 | 0: PE5 | | LCD driver common line number 1. |
| LCD_COM2 | 0: PE6 | | LCD driver common line number 2. |
| LCD_COM3 | 0: PE7 | | LCD driver common line number 3. |
| LCD_SEG0 | 0: PF2 | | LCD segment line 0. |
| LCD_SEG1 | 0: PF3 | | LCD segment line 1. |
| LCD_SEG2 | 0: PF4 | | LCD segment line 2. |
| LCD_SEG3 | 0: PF5 | | LCD segment line 3. |
| LCD_SEG4 | 0: PE8 | | LCD segment line 4. |
| LCD_SEG5 | 0: PE9 | | LCD segment line 5. |
| LCD_SEG6 | 0: PE10 | | LCD segment line 6. |
| LCD_SEG7 | 0: PE11 | | LCD segment line 7. |
| LCD_SEG8 | 0: PE12 | | LCD segment line 8. |
| LCD_SEG9 | 0: PE13 | | LCD segment line 9. |
| LCD_SEG10 | 0: PE14 | | LCD segment line 10. |
| LCD_SEG11 | 0: PE15 | | LCD segment line 11. |
| LCD_SEG12 | 0: PA15 | | LCD segment line 12. |

| Alternate | LOCATION | | Description |
|-------------------------|----------|-------|--|
| | 0 - 3 | 4 - 7 | |
| LCD_SEG13 | 0: PA0 | | LCD segment line 13. |
| LCD_SEG14 | 0: PA1 | | LCD segment line 14. |
| LCD_SEG15 | 0: PA2 | | LCD segment line 15. |
| LCD_SEG16 | 0: PA3 | | LCD segment line 16. |
| LCD_SEG17 | 0: PA4 | | LCD segment line 17. |
| LCD_SEG18 | 0: PA5 | | LCD segment line 18. |
| LCD_SEG19 | 0: PA6 | | LCD segment line 19. |
| LCD_SEG20 / LCD_COM4 | 0: PB3 | | LCD segment line 20. This pin may also be used as LCD COM line 4 |
| LCD_SEG21 / LCD_COM5 | 0: PB4 | | LCD segment line 21. This pin may also be used as LCD COM line 5 |
| LCD_SEG22 / LCD_COM6 | 0: PB5 | | LCD segment line 22. This pin may also be used as LCD COM line 6 |
| LCD_SEG23 / LCD_COM7 | 0: PB6 | | LCD segment line 23. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | 0: PF6 | | LCD segment line 24. |
| LCD_SEG25 | 0: PF7 | | LCD segment line 25. |
| LCD_SEG26 | 0: PF8 | | LCD segment line 26. |
| LCD_SEG27 | 0: PF9 | | LCD segment line 27. |
| LCD_SEG28 | 0: PD9 | | LCD segment line 28. |
| LCD_SEG29 | 0: PD10 | | LCD segment line 29. |
| LCD_SEG30 | 0: PD11 | | LCD segment line 30. |
| LCD_SEG31 | 0: PD12 | | LCD segment line 31. |
| LCD_SEG32 | 0: PB0 | | LCD segment line 32. |
| LCD_SEG33 | 0: PB1 | | LCD segment line 33. |
| LCD_SEG34 | 0: PB2 | | LCD segment line 34. |
| LCD_SEG35 | 0: PA7 | | LCD segment line 35. |
| LCD_SEG36 | 0: PA8 | | LCD segment line 36. |
| LCD_SEG37 | 0: PA9 | | LCD segment line 37. |
| LCD_SEG38 | 0: PA10 | | LCD segment line 38. |
| LCD_SEG39 | 0: PA11 | | LCD segment line 39. |
| LES_ALTEX0 | 0: PD6 | | LESENSE alternate excite output 0. |
| LES_ALTEX1 | 0: PD7 | | LESENSE alternate excite output 1. |
| LES_ALTEX2 | 0: PA3 | | LESENSE alternate excite output 2. |
| LES_ALTEX3 | 0: PA4 | | LESENSE alternate excite output 3. |
| LES_ALTEX4 | 0: PA5 | | LESENSE alternate excite output 4. |
| LES_ALTEX5 | 0: PE11 | | LESENSE alternate excite output 5. |
| LES_ALTEX6 | 0: PE12 | | LESENSE alternate excite output 6. |

| Alternate | LOCATION | | Description |
|-------------|--|---|--|
| | 0 - 3 | 4 - 7 | |
| LES_ALTEX7 | 0: PE13 | | LESENSE alternate excite output 7. |
| LES_CH0 | 0: PC0 | | LESENSE channel 0. |
| LES_CH1 | 0: PC1 | | LESENSE channel 1. |
| LES_CH2 | 0: PC2 | | LESENSE channel 2. |
| LES_CH3 | 0: PC3 | | LESENSE channel 3. |
| LES_CH4 | 0: PC4 | | LESENSE channel 4. |
| LES_CH5 | 0: PC5 | | LESENSE channel 5. |
| LES_CH6 | 0: PC6 | | LESENSE channel 6. |
| LES_CH7 | 0: PC7 | | LESENSE channel 7. |
| LES_CH8 | 0: PC8 | | LESENSE channel 8. |
| LES_CH9 | 0: PC9 | | LESENSE channel 9. |
| LES_CH10 | 0: PC10 | | LESENSE channel 10. |
| LES_CH11 | 0: PC11 | | LESENSE channel 11. |
| LES_CH12 | 0: PC12 | | LESENSE channel 12. |
| LES_CH13 | 0: PC13 | | LESENSE channel 13. |
| LES_CH14 | 0: PC14 | | LESENSE channel 14. |
| LES_CH15 | 0: PC15 | | LESENSE channel 15. |
| LETIM0_OUT0 | 0: PD6 1: PB11 2: PF0 3: PC4 | 4: PE12 5: PC14 6: PA8 7: PB9 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | 0: PD7 1: PB12 2: PF1 3: PC5 | 4: PE13 5: PC15 6: PA9 7: PB10 | Low Energy Timer LETIM0, output channel 1. |
| LETIM1_OUT0 | 0: PA7 1: PA11 2: PA12 3: PC2 | 4: PB5 5: PB2 | Low Energy Timer LETIM1, output channel 0. |
| LETIM1_OUT1 | 0: PA6 1: PA13 2: PA14 3: PC3 | 4: PB6 5: PB1 | Low Energy Timer LETIM1, output channel 1. |

| Alternate | LOCATION | | Description |
|-------------|--|---------------------------------------|---|
| | 0 - 3 | 4 - 7 | |
| LEU0_RX | 0: PD5 1: PB14 2: PE15 3: PF1 | 4: PA0 5: PC15 | LEUART0 Receive input. |
| LEU0_TX | 0: PD4 1: PB13 2: PE14 3: PF0 | 4: PF2 5: PC14 | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | 0: PC7 1: PA6 2: PD3 3: PB1 | 4: PB5 | LEUART1 Receive input. |
| LEU1_TX | 0: PC6 1: PA5 2: PD2 3: PB0 | 4: PB4 | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | 0: PB8 | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | 0: PB7 | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| OPA0_N | 0: PC5 | | Operational Amplifier 0 external negative input. |
| OPA0_P | 0: PC4 | | Operational Amplifier 0 external positive input. |
| OPA1_N | 0: PD7 | | Operational Amplifier 1 external negative input. |
| OPA1_P | 0: PD6 | | Operational Amplifier 1 external positive input. |
| OPA2_N | 0: PD3 | | Operational Amplifier 2 external negative input. |
| OPA2_OUT | 0: PD5 | | Operational Amplifier 2 output. |
| OPA2_OUTALT | 0: PD0 | | Operational Amplifier 2 alternative output. |
| OPA2_P | 0: PD4 | | Operational Amplifier 2 external positive input. |
| OPA3_N | 0: PC7 | | Operational Amplifier 3 external negative input. |
| OPA3_OUT | 0: PD1 | | Operational Amplifier 3 output. |
| OPA3_P | 0: PC6 | | Operational Amplifier 3 external positive input. |
| PCNT0_S0IN | 0: PC13 1: PE0 2: PC0 3: PD6 | 4: PA0 5: PB0 6: PB5 7: PB12 | Pulse Counter PCNT0 input number 0. |

| Alternate | LOCATION | | |
|---------------|--|---------------------------------------|-------------------------------------|
| Functionality | 0 - 3 | 4 - 7 | Description |
| PCNT0_S1IN | 0: PC14 1: PE1 2: PC1 3: PD7 | 4: PA1 5: PB1 6: PB6 7: PB11 | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | 0: PA5 1: PB3 2: PD15 3: PC4 | 4: PA7 5: PA12 6: PB11 | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | 0: PA6 1: PB4 2: PB0 3: PC5 | 4: PA8 5: PA13 6: PB12 | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | 0: PD0 1: PE8 2: PB13 3: PF10 | 4: PC12 | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | 0: PD1 1: PE9 2: PB14 3: PF11 | 4: PC13 | Pulse Counter PCNT2 input number 1. |
| PDM_CLK | 0: PA0 1: PE8 2: PF6 3: PB12 | 4: PD0 | PDM Clock Output. |
| PDM_DAT0 | 0: PA1 1: PE9 2: PF7 3: PB11 | 4: PD1 | PDM Data 0. |
| PDM_DAT1 | 0: PA2 1: PE10 2: PF8 3: PB10 | 4: PD2 | PDM Data 1. |
| PDM_DAT2 | 0: PA3 1: PE11 2: PF9 3: PB9 | 4: PD3 | PDM Data 2. |

| Alternate | LOCATION | | Description |
|-----------|--|--------|--|
| | 0 - 3 | 4 - 7 | |
| PDM_DAT3 | 0: PA4 1: PE12 2: PD9 3: PA13 | 4: PD4 | PDM Data 3. |
| PRS_CH0 | 0: PA0 1: PF3 2: PC14 3: PF2 | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | 0: PA1 1: PF4 2: PC15 3: PE12 | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | 0: PC0 1: PF5 2: PE10 3: PE13 | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | 0: PC1 1: PE8 2: PE11 3: PA0 | | Peripheral Reflex System PRS, channel 3. |
| PRS_CH4 | 0: PC8 1: PB0 2: PF1 | | Peripheral Reflex System PRS, channel 4. |
| PRS_CH5 | 0: PC9 1: PB1 2: PD6 | | Peripheral Reflex System PRS, channel 5. |
| PRS_CH6 | 0: PA6 1: PB14 2: PE6 | | Peripheral Reflex System PRS, channel 6. |
| PRS_CH7 | 0: PB13 1: PA7 2: PE7 | | Peripheral Reflex System PRS, channel 7. |
| PRS_CH8 | 0: PA8 1: PA2 2: PE9 | | Peripheral Reflex System PRS, channel 8. |

| Alternate | LOCATION | | Description |
|-----------|------------------------------|-------|---|
| | 0 - 3 | 4 - 7 | |
| PRS_CH9 | 0: PA9 1: PA3 2: PB10 | | Peripheral Reflex System PRS, channel 9. |
| PRS_CH10 | 0: PA10 1: PC2 2: PD4 | | Peripheral Reflex System PRS, channel 10. |
| PRS_CH11 | 0: PA11 1: PC3 2: PD5 | | Peripheral Reflex System PRS, channel 11. |
| PRS_CH12 | 0: PA12 1: PB6 2: PD8 | | Peripheral Reflex System PRS, channel 12. |
| PRS_CH13 | 0: PA13 1: PB9 2: PE14 | | Peripheral Reflex System PRS, channel 13. |
| PRS_CH14 | 0: PA14 1: PC6 2: PE15 | | Peripheral Reflex System PRS, channel 14. |
| PRS_CH15 | 0: PA15 1: PC7 2: PF0 | | Peripheral Reflex System PRS, channel 15. |
| QSPI0_CS0 | 0: PF7 1: PA0 | | Quad SPI 0 Chip Select 0. |
| QSPI0_CS1 | 0: PF8 1: PA1 | | Quad SPI 0 Chip Select 1. |
| QSPI0_DQ0 | 0: PD9 1: PA2 | | Quad SPI 0 Data 0. |
| QSPI0_DQ1 | 0: PD10 1: PA3 | | Quad SPI 0 Data 1. |
| QSPI0_DQ2 | 0: PD11 1: PA4 | | Quad SPI 0 Data 2. |
| QSPI0_DQ3 | 0: PD12 1: PA5 | | Quad SPI 0 Data 3. |
| QSPI0_DQ4 | 0: PE8 1: PB3 | | Quad SPI 0 Data 4. |

| Alternate | LOCATION | | Description |
|------------|---------------------------------------|-------|--------------------------|
| | 0 - 3 | 4 - 7 | |
| QSPI0_DQ5 | 0: PE9 1: PB4 | | Quad SPI 0 Data 5. |
| QSPI0_DQ6 | 0: PE10 1: PB5 | | Quad SPI 0 Data 6. |
| QSPI0_DQ7 | 0: PE11 1: PB6 | | Quad SPI 0 Data 7. |
| QSPI0_DQS | 0: PF9 1: PE15 | | Quad SPI 0 Data S. |
| QSPI0_RST0 | 0: PE14 1: PC2 | | Quad SPI 0 Reset 0. |
| QSPI0_RST1 | 0: PE15 1: PC3 | | Quad SPI 0 Reset 1. |
| QSPI0_SCLK | 0: PF6 1: PE14 | | Quad SPI 0 Serial Clock. |
| SDIO_CD | 0: PF8 1: PC4 2: PA6 3: PB10 | | SDIO Card Detect. |
| SDIO_CLK | 0: PE13 1: PE14 | | SDIO Serial Clock. |
| SDIO_CMD | 0: PE12 1: PE15 | | SDIO Command. |
| SDIO_DAT0 | 0: PE11 1: PA0 | | SDIO Data 0. |
| SDIO_DAT1 | 0: PE10 1: PA1 | | SDIO Data 1. |
| SDIO_DAT2 | 0: PE9 1: PA2 | | SDIO Data 2. |
| SDIO_DAT3 | 0: PE8 1: PA3 | | SDIO Data 3. |
| SDIO_DAT4 | 0: PD12 1: PA4 | | SDIO Data 4. |
| SDIO_DAT5 | 0: PD11 1: PA5 | | SDIO Data 5. |
| SDIO_DAT6 | 0: PD10 1: PB3 | | SDIO Data 6. |

| Alternate | LOCATION | | |
|---------------|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | Description |
| SDIO_DAT7 | 0: PD9 1: PB4 | | SDIO Data 7. |
| SDIO_WP | 0: PF9 1: PC5 2: PB15 3: PB9 | | SDIO Write Protect. |
| TIM0_CC0 | 0: PA0 1: PF6 2: PD1 3: PB6 | 4: PF0 5: PC4 6: PA8 7: PA1 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | 0: PA1 1: PF7 2: PD2 3: PC0 | 4: PF1 5: PC5 6: PA9 7: PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | 0: PA2 1: PF8 2: PD3 3: PC1 | 4: PF2 5: PA7 6: PA10 7: PA13 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDT10 | 0: PA3 1: PC13 2: PF3 3: PC2 | 4: PB7 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDT11 | 0: PA4 1: PC14 2: PF4 3: PC3 | 4: PB8 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDT12 | 0: PA5 1: PC15 2: PF5 3: PC4 | 4: PB11 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | 0: PC13 1: PE10 2: PB0 3: PB7 | 4: PD6 5: PF2 6: PF13 | Timer 1 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | |
|---------------|--|------------------------------|--|
| Functionality | 0 - 3 | 4 - 7 | Description |
| TIM1_CC1 | 0: PC14 1: PE11 2: PB1 3: PB8 | 4: PD7 5: PF3 6: PF14 | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | 0: PC15 1: PE12 2: PB2 3: PB11 | 4: PC13 5: PF4 | Timer 1 Capture Compare input / output channel 2. |
| TIM1_CC3 | 0: PC12 1: PE13 2: PB3 3: PB12 | 4: PC14 5: PF12 6: PF5 | Timer 1 Capture Compare input / output channel 3. |
| TIM2_CC0 | 0: PA8 1: PA12 2: PC8 3: PF2 | 4: PB6 5: PC2 | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | 0: PA9 1: PA13 2: PC9 3: PE12 | 4: PC0 5: PC3 | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | 0: PA10 1: PA14 2: PC10 3: PE13 | 4: PC1 5: PC4 | Timer 2 Capture Compare input / output channel 2. |
| TIM2_CDT10 | 0: PB0 1: PD13 2: PE8 | | Timer 2 Complimentary Dead Time Insertion channel 0. |
| TIM2_CDT11 | 0: PB1 1: PD14 2: PE14 | | Timer 2 Complimentary Dead Time Insertion channel 1. |
| TIM2_CDT12 | 0: PB2 1: PD15 2: PE15 | | Timer 2 Complimentary Dead Time Insertion channel 2. |

| Alternate | LOCATION | | Description |
|-----------|--|--|---|
| | 0 - 3 | 4 - 7 | |
| TIM3_CC0 | 0: PE14 1: PE0 2: PE3 3: PE5 | 4: PA0 5: PA3 6: PA6 7: PD15 | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | 0: PE15 1: PE1 2: PE4 3: PE6 | 4: PA1 5: PA4 6: PD13 7: PB15 | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | 0: PA15 1: PE2 2: PE5 3: PE7 | 4: PA2 5: PA5 6: PD14 7: PB0 | Timer 3 Capture Compare input / output channel 2. |
| U0_CTS | 0: PF8 1: PE2 2: PA5 3: PC13 | 4: PB7 5: PD5 | UART0 Clear To Send hardware flow control input. |
| U0_RTS | 0: PF9 1: PE3 2: PA6 3: PC12 | 4: PB8 5: PD6 | UART0 Request To Send hardware flow control output. |
| U0_RX | 0: PF7 1: PE1 2: PA4 3: PC15 | 4: PC5 5: PF2 6: PE4 | UART0 Receive input. |
| U0_TX | 0: PF6 1: PE0 2: PA3 3: PC14 | 4: PC4 5: PF1 6: PD7 | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_CTS | 0: PC14 1: PF9 2: PB11 3: PE4 | 4: PC4 | UART1 Clear To Send hardware flow control input. |
| U1_RTS | 0: PC15 1: PF8 2: PB12 3: PE5 | 4: PC5 | UART1 Request To Send hardware flow control output. |

| Alternate | LOCATION | | |
|---------------|---|-----------------------------|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| U1_RX | 0: PC13 1: PF11 2: PB10 3: PE3 | 4: PE13 | UART1 Receive input. |
| U1_TX | 0: PC12 1: PF10 2: PB9 3: PE2 | 4: PE12 | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | 0: PE12 1: PE5 2: PC9 3: PC15 | 4: PB13 5: PA12 | USART0 clock input / output. |
| US0_CS | 0: PE13 1: PE4 2: PC8 3: PC14 | 4: PB14 5: PA13 | USART0 chip select input / output. |
| US0_CTS | 0: PE14 1: PE3 2: PC7 3: PC13 | 4: PB6 5: PB11 | USART0 Clear To Send hardware flow control input. |
| US0_RTS | 0: PE15 1: PE2 2: PC6 3: PC12 | 4: PB5 5: PD6 | USART0 Request To Send hardware flow control output. |
| US0_RX | 0: PE11 1: PE6 2: PC10 3: PE12 | 4: PB8 5: PC1 | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | 0: PE10 1: PE7 2: PC11 3: PE13 | 4: PB7 5: PC0 | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | 0: PB7 1: PD2 2: PF0 3: PC15 | 4: PC3 5: PB11 6: PE5 | USART1 clock input / output. |

| Alternate | LOCATION | | |
|---------------|---|-----------------------------|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| US1_CS | 0: PB8 1: PD3 2: PF1 3: PC14 | 4: PC0 5: PE4 6: PB2 | USART1 chip select input / output. |
| US1_CTS | 0: PB9 1: PD4 2: PF3 3: PC6 | 4: PC12 5: PB13 | USART1 Clear To Send hardware flow control input. |
| US1_RTS | 0: PB10 1: PD5 2: PF4 3: PC7 | 4: PC13 5: PB14 | USART1 Request To Send hardware flow control output. |
| US1_RX | 0: PC1 1: PD1 2: PD6 3: PF7 | 4: PC2 5: PA0 6: PA2 | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | 0: PC0 1: PD0 2: PD7 3: PF6 | 4: PC1 5: PF2 6: PA14 | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | 0: PC4 1: PB5 2: PA9 3: PA15 | 4: PF8 5: PF2 | USART2 clock input / output. |
| US2_CS | 0: PC5 1: PB6 2: PA10 3: PB11 | 4: PF9 5: PF5 | USART2 chip select input / output. |
| US2_CTS | 0: PC1 1: PB12 2: PA11 3: PB10 | 4: PC12 5: PD6 | USART2 Clear To Send hardware flow control input. |
| US2_RTS | 0: PC0 1: PB15 2: PA12 3: PC14 | 4: PC13 5: PD8 | USART2 Request To Send hardware flow control output. |

| Alternate | LOCATION | | Description |
|---------------|--|------------------|---|
| Functionality | 0 - 3 | 4 - 7 | |
| US2_RX | 0: PC3 1: PB4 2: PA8 3: PA14 | 4: PF7 5: PF1 | USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | 0: PC2 1: PB3 2: PA7 3: PA13 | 4: PF6 5: PF0 | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| US3_CLK | 0: PA2 1: PD7 2: PD4 | | USART3 clock input / output. |
| US3_CS | 0: PA3 1: PE4 2: PC14 3: PC0 | | USART3 chip select input / output. |
| US3_CTS | 0: PA4 1: PE5 2: PD6 | | USART3 Clear To Send hardware flow control input. |
| US3_RTS | 0: PA5 1: PC1 2: PA14 3: PC15 | | USART3 Request To Send hardware flow control output. |
| US3_RX | 0: PA1 1: PE7 2: PB7 | | USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO). |
| US3_TX | 0: PA0 1: PE6 2: PB3 | | USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI). |
| US4_CLK | 0: PC4 1: PD11 | | USART4 clock input / output. |
| US4_CS | 0: PC5 1: PD12 | | USART4 chip select input / output. |
| US4_CTS | 0: PA7 1: PD13 | | USART4 Clear To Send hardware flow control input. |
| US4_RTS | 0: PA8 1: PD14 | | USART4 Request To Send hardware flow control output. |

| Alternate | LOCATION | | Description |
|-----------------------------|----------|---------|--|
| | 0 - 3 | 4 - 7 | |
| US4_RX | 0: PB8 | | USART4 Asynchronous Receive. |
| | 1: PD10 | | USART4 Synchronous mode Master Input / Slave Output (MISO). |
| US4_TX | 0: PB7 | | USART4 Asynchronous Transmit. Also used as receive input in half duplex communication. |
| | 1: PD9 | | USART4 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | 0: PF10 | | USB D- pin. |
| USB_DP | 0: PF11 | | USB D+ pin. |
| USB_ID | 0: PF12 | | USB ID pin. |
| USB_VBUSEN | 0: PF5 | | USB 5 V VBUS enable. |
| | 1: PE4 | | |
| | 2: PD0 | | |
| VDAC0_EXT | 0: PD6 | | Digital to analog converter VDAC0 external reference input pin. |
| VDAC0_OUT0 / OPA0_OUT | 0: PB11 | | Digital to Analog Converter DAC0 output channel number 0. |
| VDAC0_OUT0ALT / OPA0_OUTALT | 0: PC0 | 4: PD0 | Digital to Analog Converter DAC0 alternative output for channel 0. |
| | 1: PC1 | | |
| | 2: PC2 | | |
| | 3: PC3 | | |
| VDAC0_OUT1 / OPA1_OUT | 0: PB12 | | Digital to Analog Converter DAC0 output channel number 1. |
| VDAC0_OUT1ALT / OPA1_OUTALT | 0: PC12 | 4: PD1 | Digital to Analog Converter DAC0 alternative output for channel 1. |
| | 1: PC13 | | |
| | 2: PC14 | | |
| | 3: PC15 | | |
| WTIM0_CC0 | 0: PE4 | 4: PC15 | Wide timer 0 Capture Compare input / output channel 0. |
| | 1: PA6 | 5: PB0 | |
| | | 6: PB3 | |
| | | 7: PC1 | |
| WTIM0_CC1 | 0: PE5 | 4: PF0 | Wide timer 0 Capture Compare input / output channel 1. |
| | 1: PD13 | 5: PB1 | |
| | | 6: PB4 | |
| | | 7: PC2 | |
| WTIM0_CC2 | 0: PE6 | 4: PF1 | Wide timer 0 Capture Compare input / output channel 2. |
| | 1: PD14 | 5: PB2 | |
| | | 6: PB5 | |
| | | 7: PC3 | |

| Alternate | LOCATION | | Description |
|-------------|---------------------------------------|------------------|---|
| | 0 - 3 | 4 - 7 | |
| WTIM0_CDTI0 | 0: PE10 1: PD15 2: PA12 | 4: PD4 | Wide timer 0 Complimentary Dead Time Insertion channel 0. |
| WTIM0_CDTI1 | 0: PE11 2: PA13 | 4: PD5 | Wide timer 0 Complimentary Dead Time Insertion channel 1. |
| WTIM0_CDTI2 | 0: PE12 2: PA14 | 4: PD6 | Wide timer 0 Complimentary Dead Time Insertion channel 2. |
| WTIM1_CC0 | 0: PB13 1: PD2 2: PD6 3: PC7 | 4: PE3 5: PE7 | Wide timer 1 Capture Compare input / output channel 0. |
| WTIM1_CC1 | 0: PB14 1: PD3 2: PD7 3: PE0 | 4: PE4 | Wide timer 1 Capture Compare input / output channel 1. |
| WTIM1_CC2 | 0: PD0 1: PD4 2: PD8 3: PE1 | 4: PE5 | Wide timer 1 Capture Compare input / output channel 2. |
| WTIM1_CC3 | 0: PD1 1: PD5 2: PC6 3: PE2 | 4: PE6 | Wide timer 1 Capture Compare input / output channel 3. |

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 5.22. Alternate Functionality Priority

| Alternate Functionality | Location | Priority |
|-------------------------|-------------------|--------------------------|
| CMU_CLK2 | 1: PA3 5: PD10 | High Speed High Speed |
| CMU_CLKI0 | 1: PA3 5: PD10 | High Speed High Speed |
| PDM_CLK | 0: PA0 | High Speed |
| PDM_DAT0 | 0: PA1 | High Speed |

| Alternate Functionality | Location | Priority |
|-------------------------|----------|------------------|
| PDM_DAT1 | 0: PA2 | High Speed |
| PDM_DAT2 | 0: PA3 | High Speed |
| PDM_DAT3 | 0: PA4 | High Speed |
| QSPI0_CS0 | 0: PF7 | High Speed |
| QSPI0_CS1 | 0: PF8 | High Speed |
| QSPI0_DQ0 | 0: PD9 | High Speed |
| QSPI0_DQ1 | 0: PD10 | High Speed |
| QSPI0_DQ2 | 0: PD11 | High Speed |
| QSPI0_DQ3 | 0: PD12 | High Speed |
| QSPI0_DQ4 | 0: PE8 | High Speed |
| QSPI0_DQ5 | 0: PE9 | High Speed |
| QSPI0_DQ6 | 0: PE10 | High Speed |
| QSPI0_DQ7 | 0: PE11 | High Speed |
| QSPI0_DQS | 0: PF9 | High Speed |
| QSPI0_RST0 | 0: PE14 | High Speed |
| QSPI0_RST1 | 0: PE15 | High Speed |
| QSPI0_SCLK | 0: PF6 | High Speed |
| SDIO_CLK | 0: PE13 | High Speed |
| SDIO_CMD | 0: PE12 | High Speed |
| SDIO_DAT0 | 0: PE11 | High Speed |
| SDIO_DAT1 | 0: PE10 | High Speed |
| SDIO_DAT2 | 0: PE9 | High Speed |
| SDIO_DAT3 | 0: PE8 | High Speed |
| SDIO_DAT4 | 0: PD12 | High Speed |
| SDIO_DAT5 | 0: PD11 | High Speed |
| SDIO_DAT6 | 0: PD10 | High Speed |
| SDIO_DAT7 | 0: PD9 | High Speed |
| TIM0_CC0 | 3: PB6 | Non-interference |
| TIM0_CC1 | 3: PC0 | Non-interference |
| TIM0_CC2 | 3: PC1 | Non-interference |
| TIM0_CDTI0 | 1: PC13 | Non-interference |
| TIM0_CDTI1 | 1: PC14 | Non-interference |
| TIM0_CDTI2 | 1: PC15 | Non-interference |
| TIM2_CC0 | 0: PA8 | Non-interference |
| TIM2_CC1 | 0: PA9 | Non-interference |
| TIM2_CC2 | 0: PA10 | Non-interference |
| TIM2_CDTI0 | 0: PB0 | Non-interference |

| Alternate Functionality | Location | Priority |
|-------------------------|------------------|--------------------------|
| TIM2_CDT11 | 0: PB1 | Non-interference |
| TIM2_CDT12 | 0: PB2 | Non-interference |
| US2_CLK | 4: PF8 5: PF2 | High Speed High Speed |
| US2_CS | 4: PF9 5: PF5 | High Speed High Speed |
| US2_RX | 4: PF7 5: PF1 | High Speed High Speed |
| US2_TX | 4: PF6 5: PF0 | High Speed High Speed |

5.22 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. [Figure 5.20 APORT Connection Diagram on page 204](#) shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

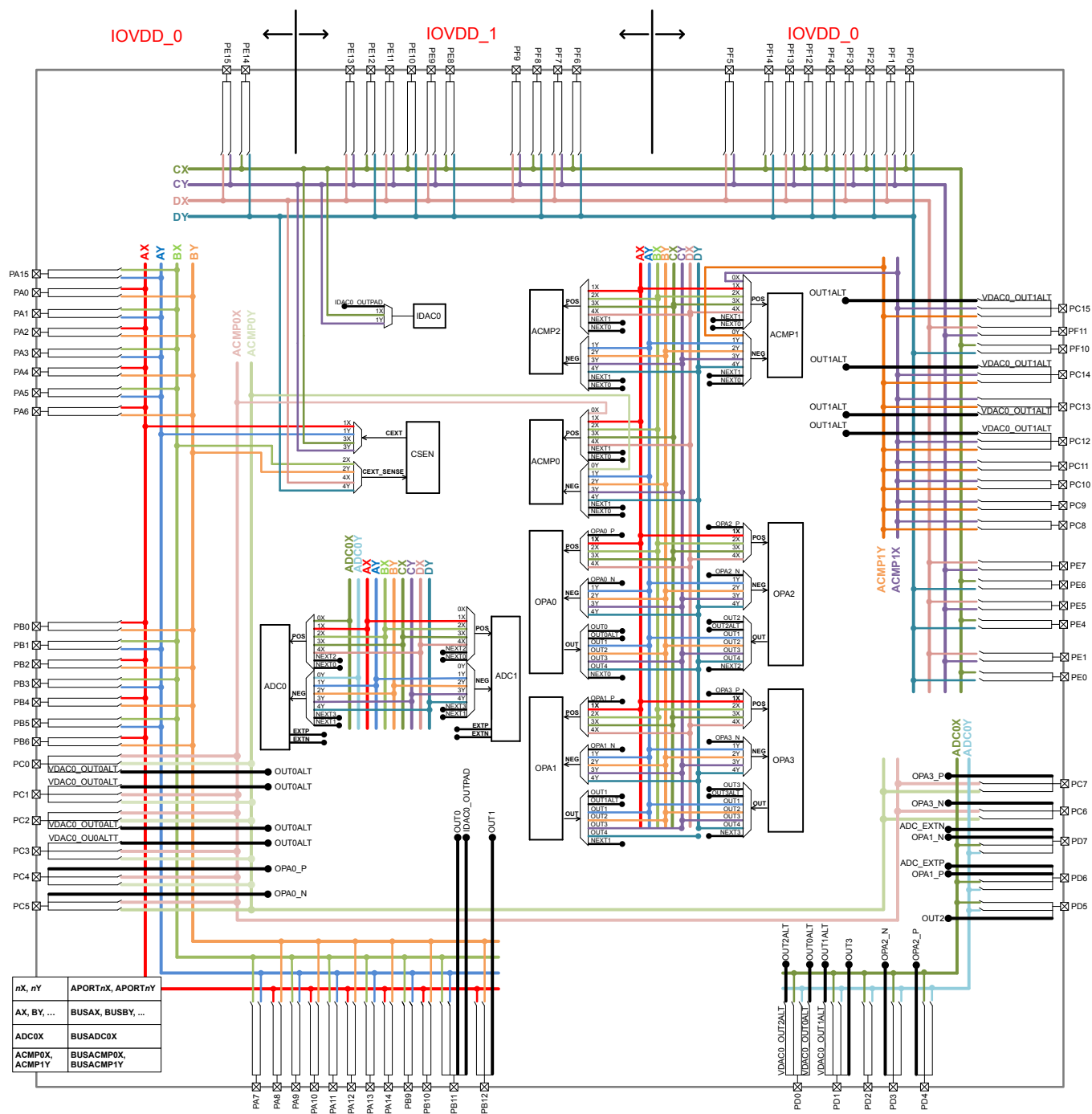


Figure 5.20. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 5.23. ACMP0 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | APORT0Y | APORT0X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|-----------|-----------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | BUSACMP0Y | BUSACMP0X | Bus |
| PF14 | | | PF14 | PB14 | PB15 | PB15 | PB14 | | | CH31 |
| | PF13 | PF13 | | | | | | | | CH30 |
| PF12 | | | PF12 | PB12 | PB13 | PB13 | PB12 | | | CH29 |
| | PF11 | PF11 | | | | PB11 | | | | CH28 |
| PF10 | | | PF10 | PB10 | | | PB10 | | | CH27 |
| | PF9 | PF9 | | | | PB9 | | | | CH26 |
| PF8 | | | PF8 | | | | | | | CH25 |
| | PF7 | PF7 | | | | | | | | CH24 |
| PF6 | | | PF6 | PB6 | | | PB6 | | | CH23 |
| | PF5 | PF5 | | | | PB5 | | | | CH22 |
| PF4 | | | PF4 | PB4 | | | PB4 | | | CH21 |
| | PF3 | PF3 | | | | PB3 | | | | CH20 |
| PF2 | | | PF2 | PB2 | | | PB2 | | | CH19 |
| | PF1 | PF1 | | | | PB1 | | | | CH18 |
| PF0 | | | PF0 | PB0 | | | PB0 | | | CH17 |
| | PE15 | PE15 | | | | PA15 | | | | CH16 |
| PE14 | | | PE14 | PA14 | | | PA14 | | | CH15 |
| | PE13 | PE13 | | | | PA13 | | | | CH14 |
| PE12 | | | PE12 | PA12 | | | PA12 | | | CH13 |
| | PE11 | PE11 | | | | PA11 | | | | CH12 |
| PE10 | | | PE10 | PA10 | | | PA10 | | | CH11 |
| | PE9 | PE9 | | | | PA9 | | | | CH10 |
| PE8 | | | PE8 | PA8 | | | PA8 | | | CH9 |
| | PE7 | PE7 | | | | PA7 | | | | CH8 |
| PE6 | | | PE6 | PA6 | | | PA6 | PC7 | PC7 | CH7 |
| | PE5 | PE5 | | | | PA5 | | PC6 | PC6 | CH6 |
| PE4 | | | PE4 | PA4 | | PA5 | | PC5 | PC5 | CH5 |
| | | | | | | PA3 | | PC4 | PC4 | CH4 |
| | | | | | | PA3 | | PC3 | PC3 | CH3 |
| | | | | | | | PA2 | PC2 | PC2 | CH2 |
| | PE1 | PE1 | | | | PA1 | | PC1 | PC1 | CH1 |
| PE0 | | | PE0 | PA0 | | | PA0 | PC0 | PC0 | CH0 |

Table 5.24. ACMP1 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | APORT0Y | APORT0X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|-----------|-----------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | BUSACMP1Y | BUSACMP1X | Bus |
| PF14 | | | PF14 | PB14 | | PB15 | PB14 | | | CH31 |
| | PF13 | PF13 | | | | | | | | CH30 |
| PF12 | | | PF12 | PB12 | | PB13 | PB12 | | | CH29 |
| | PF11 | PF11 | | | | PB11 | PB11 | | | CH28 |
| PF10 | | | PF10 | PB10 | | | PB10 | | | CH27 |
| | PF9 | PF9 | | | | PB9 | | | | CH26 |
| PF8 | | | PF8 | | | | | | | CH25 |
| | PF7 | PF7 | | | | | | | | CH24 |
| PF6 | | | PF6 | PB6 | | | PB6 | | | CH23 |
| | PF5 | PF5 | | | | PB5 | | | | CH22 |
| PF4 | | | PF4 | PB4 | | | PB4 | | | CH21 |
| | PF3 | PF3 | | | | PB3 | | | | CH20 |
| PF2 | | | PF2 | PB2 | | | PB2 | | | CH19 |
| | PF1 | PF1 | | | | PB1 | | | | CH18 |
| PF0 | | | PF0 | PB0 | | | PB0 | | | CH17 |
| | PE15 | PE15 | | | | PA15 | | | | CH16 |
| PE14 | | | PE14 | PA14 | | | PA14 | | | CH15 |
| | PE13 | PE13 | | | | PA13 | | | | CH14 |
| PE12 | | | PE12 | PA12 | | | PA12 | | | CH13 |
| | PE11 | PE11 | | | | PA11 | | | | CH12 |
| PE10 | | | PE10 | PA10 | | | PA10 | | | CH11 |
| | PE9 | PE9 | | | | PA9 | | | | CH10 |
| PE8 | | | PE8 | PA8 | | | PA8 | | | CH9 |
| | PE7 | PE7 | | | | PA7 | | | | CH8 |
| PE6 | | | PE6 | PA6 | | | PA6 | PC15 | PC15 | CH7 |
| | PE5 | PE5 | | | | | PA6 | PC14 | PC14 | CH6 |
| PE4 | | | PE4 | PA4 | | | PA4 | PC13 | PC13 | CH5 |
| | | | | | | | PA4 | PC12 | PC12 | CH4 |
| | | | | | | | PA2 | PC11 | PC11 | CH3 |
| | PE1 | PE1 | | PA2 | | | PA2 | PC10 | PC10 | CH2 |
| | | | | | | | | PC9 | PC9 | CH1 |
| PE0 | | | PE0 | PA0 | | | PA0 | PC8 | PC8 | CH0 |

Table 5.25. ACMP2 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | Bus |
| PF14 | | | PF14 | PB14 | PB15 | PB15 | PB14 | CH31 |
| | PF13 | PF13 | | | PB13 | PB13 | | CH30 |
| PF12 | | | PF12 | PB12 | | | PB12 | CH29 |
| | PF11 | PF11 | | | PB11 | PB11 | | CH28 |
| PF10 | | | PF10 | PB10 | | | PB10 | CH27 |
| | PF9 | PF9 | | | PB9 | PB9 | | CH26 |
| PF8 | | | PF8 | | | | | CH25 |
| | PF7 | PF7 | | | | | | CH24 |
| PF6 | | | PF6 | PB6 | | | PB6 | CH23 |
| | PF5 | PF5 | | | PB5 | PB5 | | CH22 |
| PF4 | | | PF4 | PB4 | | | PB4 | CH21 |
| | PF3 | PF3 | | | PB3 | PB3 | | CH20 |
| PF2 | | | PF2 | PB2 | | | PB2 | CH19 |
| | PF1 | PF1 | | | PB1 | PB1 | | CH18 |
| PF0 | | | PF0 | PB0 | | | PB0 | CH17 |
| | PE15 | PE15 | | | PA15 | PA15 | | CH16 |
| PE14 | | | PE14 | PA14 | | | PA14 | CH15 |
| | PE13 | PE13 | | | PA13 | PA13 | | CH14 |
| PE12 | | | PE12 | PA12 | | | PA12 | CH13 |
| | PE11 | PE11 | | | PA11 | PA11 | | CH12 |
| PE10 | | | PE10 | PA10 | | | PA10 | CH11 |
| | PE9 | PE9 | | | PA9 | PA9 | | CH10 |
| PE8 | | | PE8 | PA8 | | | PA8 | CH9 |
| | PE7 | PE7 | | | PA7 | PA7 | | CH8 |
| PE6 | | | PE6 | PA6 | | | PA6 | CH7 |
| | PE5 | PE5 | | | PA5 | PA5 | | CH6 |
| PE4 | | | PE4 | PA4 | | | PA4 | CH5 |
| | | | | | PA3 | PA3 | | CH4 |
| | | | | PA2 | | | PA2 | CH3 |
| | PE1 | PE1 | | | PA1 | PA1 | | CH2 |
| PE0 | | | PE0 | PA0 | | | PA0 | CH1 |
| | | | | | | | | CH0 |

Table 5.26. ADC0 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | APORT0Y | APORT0X | Port Bus |
|---------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | BUSADC0Y | BUSADC0X | CH31 |
| PF14 | | | PF14 | PB14 | | PB15 | PB14 | | | CH30 |
| | PF13 | PF13 | | | PB13 | PB13 | | | | CH29 |
| PF12 | | | PF12 | PB12 | | PB11 | PB12 | | | CH28 |
| | PF11 | PF11 | | | PB11 | PB11 | | | | CH27 |
| PF10 | | | PF10 | PB10 | | | PB10 | | | CH26 |
| | PF9 | PF9 | | | PB9 | PB9 | | | | CH25 |
| PF8 | | | PF8 | | | | | | | CH24 |
| | PF7 | PF7 | | | | | | | | CH23 |
| PF6 | | | PF6 | PB6 | | | PB6 | | | CH22 |
| | PF5 | PF5 | | | PB5 | PB5 | | | | CH21 |
| PF4 | | | PF4 | PB4 | | | PB4 | | | CH20 |
| | PF3 | PF3 | | | PB3 | PB3 | | | | CH19 |
| PF2 | | | PF2 | PB2 | | | PB2 | | | CH18 |
| | PF1 | PF1 | | | PB1 | PB1 | | | | CH17 |
| PF0 | | | PF0 | PB0 | | | PB0 | | | CH16 |
| | PE15 | PE15 | | | PA15 | PA15 | | | | CH15 |
| PE14 | | | PE14 | PA14 | | | PA14 | | | CH14 |
| | PE13 | PE13 | | | PA13 | PA13 | | | | CH13 |
| PE12 | | | PE12 | PA12 | | | PA12 | | | CH12 |
| | PE11 | PE11 | | | PA11 | PA11 | | | | CH11 |
| PE10 | | | PE10 | PA10 | | | PA10 | | | CH10 |
| | PE9 | PE9 | | | PA9 | PA9 | | | | CH9 |
| PE8 | | | PE8 | PA8 | | | PA8 | | | CH8 |
| | PE7 | PE7 | | | PA7 | PA7 | | PD7 | PD7 | CH7 |
| PE6 | | | PE6 | PA6 | | | PA6 | PD6 | PD6 | CH6 |
| | PE5 | PE5 | | | PA5 | PA5 | | PD5 | PD5 | CH5 |
| PE4 | | | PE4 | PA4 | | | PA4 | PD4 | PD4 | CH4 |
| | | | | | PA3 | PA3 | | PD3 | PD3 | CH3 |
| | | | | PA2 | | | PA2 | PD2 | PD2 | CH2 |
| | PE1 | PE1 | | | PA1 | PA1 | | PD1 | PD1 | CH1 |
| PE0 | | | PE0 | PA0 | | | PA0 | PD0 | PD0 | CH0 |

Table 5.27. ADC1 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | Bus |
| PF14 | | | PF14 | PB14 | PB15 | PB15 | PB14 | CH31 |
| | PF13 | PF13 | | | PB13 | PB13 | | CH30 |
| PF12 | | | PF12 | PB12 | | | PB12 | CH29 |
| | PF11 | PF11 | | | PB11 | PB11 | | CH28 |
| PF10 | | | PF10 | PB10 | | | PB10 | CH27 |
| | PF9 | PF9 | | | PB9 | PB9 | | CH26 |
| PF8 | | | PF8 | | | | | CH25 |
| | PF7 | PF7 | | | | | | CH24 |
| PF6 | | | PF6 | PB6 | | | PB6 | CH23 |
| | PF5 | PF5 | | | PB5 | PB5 | | CH22 |
| PF4 | | | PF4 | PB4 | | | PB4 | CH21 |
| | PF3 | PF3 | | | PB3 | PB3 | | CH20 |
| PF2 | | | PF2 | PB2 | | | PB2 | CH19 |
| | PF1 | PF1 | | | PB1 | PB1 | | CH18 |
| PF0 | | | PF0 | PB0 | | | PB0 | CH17 |
| | PE15 | PE15 | | | PA15 | PA15 | | CH16 |
| PE14 | | | PE14 | PA14 | | | PA14 | CH15 |
| | PE13 | PE13 | | | PA13 | PA13 | | CH14 |
| PE12 | | | PE12 | PA12 | | | PA12 | CH13 |
| | PE11 | PE11 | | | PA11 | PA11 | | CH12 |
| PE10 | | | PE10 | PA10 | | | PA10 | CH11 |
| | PE9 | PE9 | | | PA9 | PA9 | | CH10 |
| PE8 | | | PE8 | PA8 | | | PA8 | CH9 |
| | PE7 | PE7 | | | PA7 | PA7 | | CH8 |
| PE6 | | | PE6 | PA6 | | | PA6 | CH7 |
| | PE5 | PE5 | | | PA5 | PA5 | | CH6 |
| PE4 | | | PE4 | PA4 | | | PA4 | CH5 |
| | | | | | PA3 | PA3 | | CH4 |
| | | | | PA2 | | | PA2 | CH3 |
| | PE1 | PE1 | | | PA1 | PA1 | | CH2 |
| PE0 | | | PE0 | PA0 | | | PA0 | CH1 |
| | | | | | | | | CH0 |

Table 5.30. VDACC0 / OPA Bus and Pin Mapping

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | | |
|---------------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| OPA0_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | BUSBY | BUSCY | BUSDY | PF14 | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| APORT2Y | BUSBY | BUSBY | BUSCY | BUSDY | PF14 | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| APORT3Y | BUSBY | BUSBY | BUSCY | BUSDY | PF14 | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| APORT4Y | BUSBY | BUSBY | BUSCY | BUSDY | PF14 | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| OPA0_P | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | BUSBX | BUSCX | BUSDY | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 | |
| APORT2X | BUSBX | BUSBX | BUSCX | BUSDY | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 | |
| APORT3X | BUSCX | BUSCX | BUSCX | BUSDY | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 | |
| APORT4X | BUSDX | BUSDX | BUSDX | BUSDY | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 | |

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---------------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| OPA1_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 |
| APORT3Y | BUSCY | | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | PE3 | | PE1 | |
| APORT4Y | BUSDY | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | PE0 | | | | | PE0 |
| OPA1_P | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT2X | BUSBX | PB15 | | PB13 | | PB11 | | PB9 | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | | PA0 | |
| APORT3X | BUSCX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | PE2 | | PE0 |
| APORT4X | BUSDX | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | PE3 | | PE1 | | PE0 |
| OPA2_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | | | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT3Y | BUSCY | | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | PE3 | | PE1 | |
| APORT4Y | BUSDY | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | PE0 | | | | | PE0 |

6. BGA120 Package Specifications

6.1 BGA120 Package Dimensions

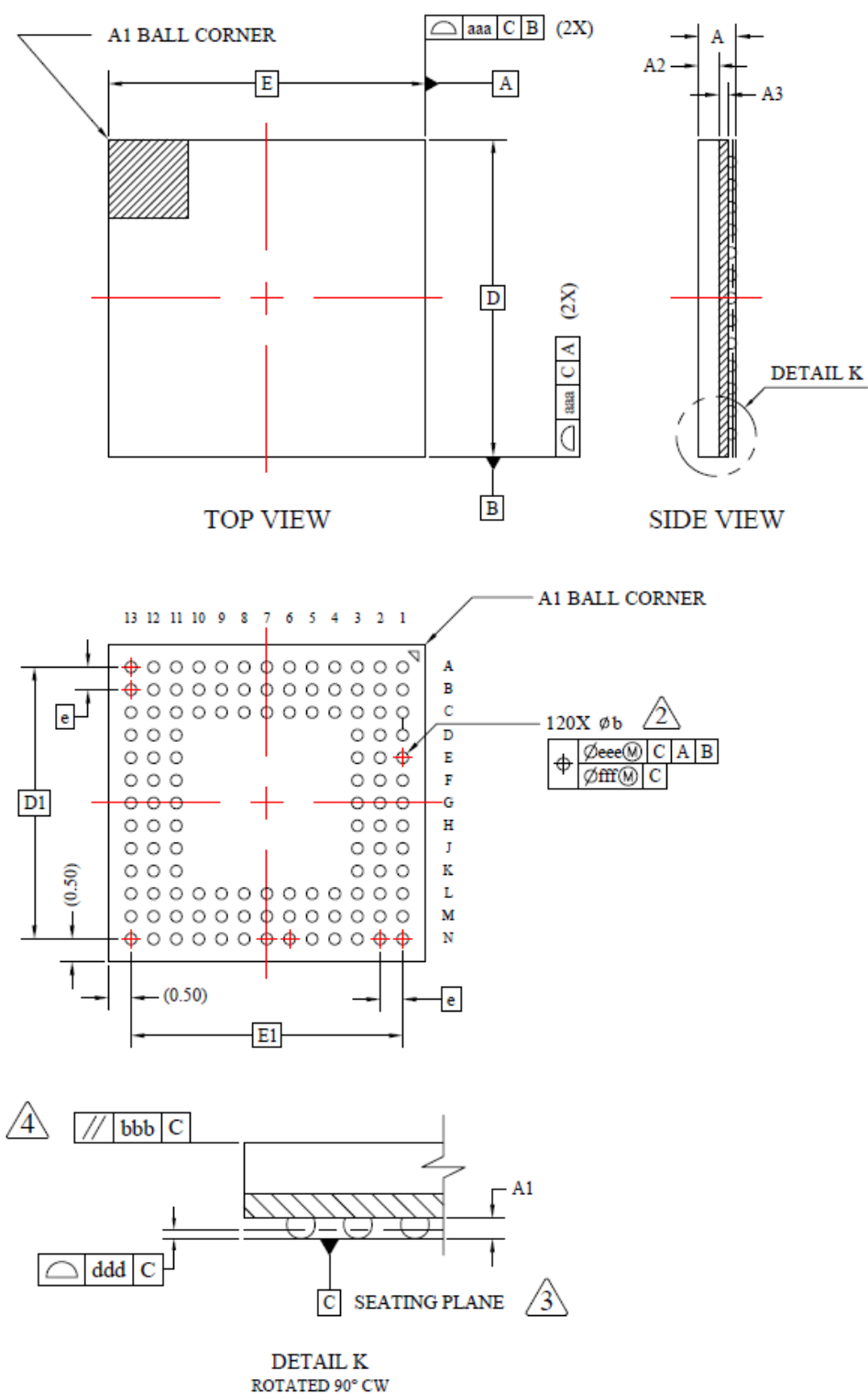


Figure 6.1. BGA120 Package Drawing

Table 6.1. BGA120 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 0.78 | 0.84 | 0.90 |
| A1 | 0.13 | 0.18 | 0.23 |
| A3 | 0.17 | 0.21 | 0.25 |
| A2 | 0.45 REF | | |
| D | 7.00 BSC | | |
| e | 0.50 BSC | | |
| E | 7.00 BSC | | |
| D1 | 6.00 BSC | | |
| E1 | 6.00 BSC | | |
| b | 0.20 | 0.25 | 0.30 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ddd | 0.08 | | |
| eee | 0.15 | | |
| fff | 0.05 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 BGA120 PCB Land Pattern

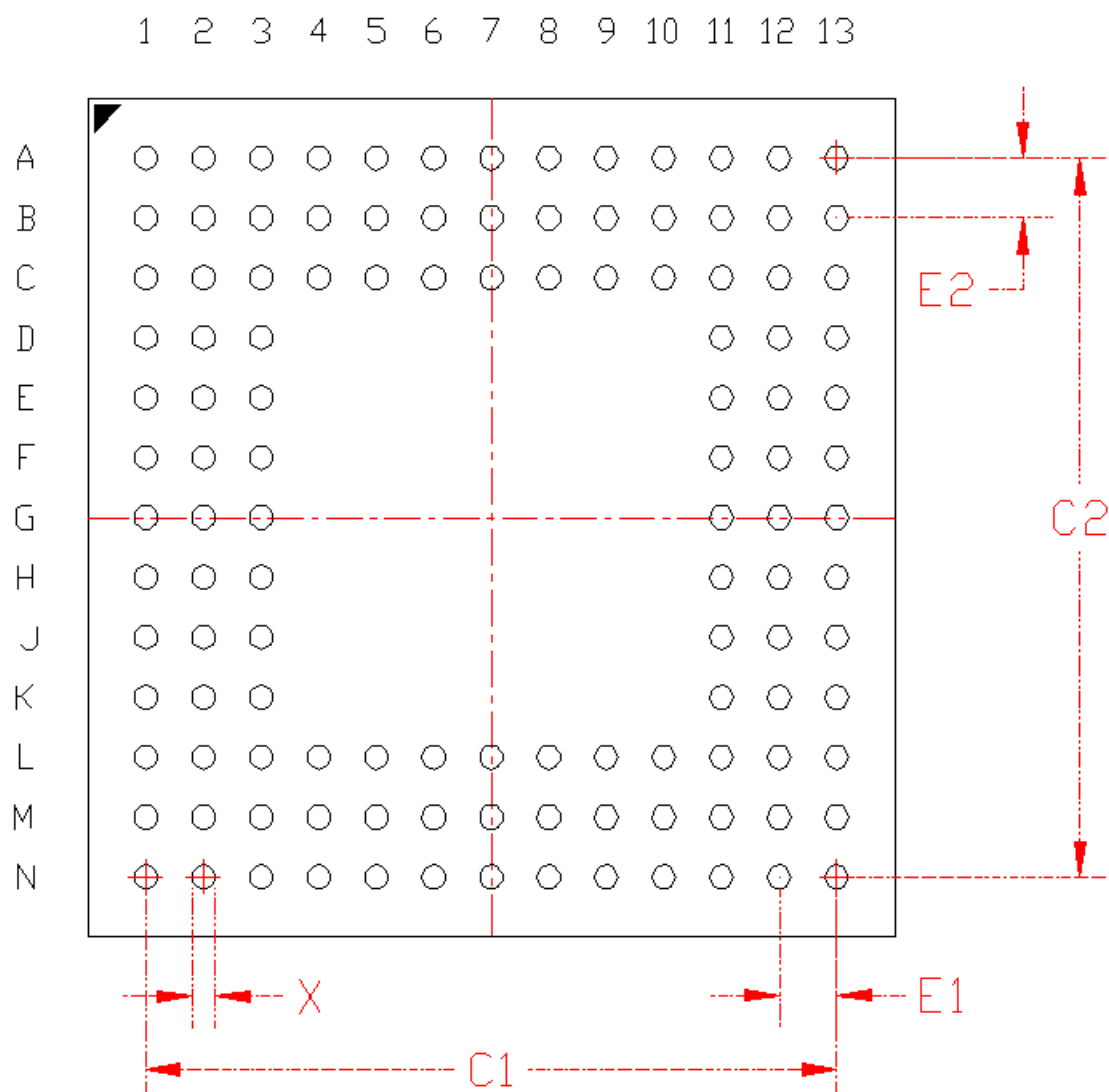


Figure 6.2. BGA120 PCB Land Pattern Drawing

Table 6.2. BGA120 PCB Land Pattern Dimensions

| Dimension | Min | Nom | Max |
|-----------|-----|------|-----|
| X | | 0.20 | |
| C1 | | 6.00 | |
| C2 | | 6.00 | |
| E1 | | 0.5 | |
| E2 | | 0.5 | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6.3 BGA120 Package Marking



Figure 6.3. BGA120 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

7. BGA112 Package Specifications

7.1 BGA112 Package Dimensions

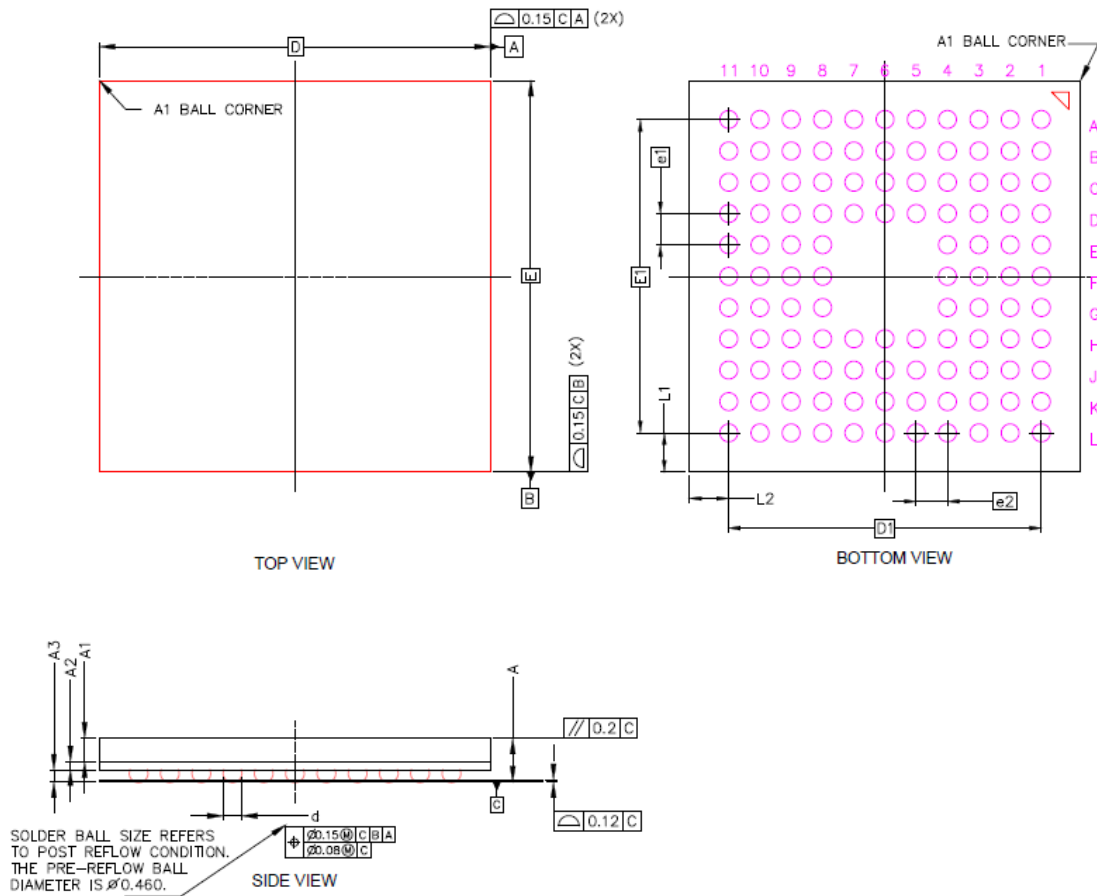


Figure 7.1. BGA112 Package Drawing

Table 7.1. BGA112 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|-----------|------|------|
| A | - | - | 1.30 |
| A1 | 0.55 | 0.60 | 0.65 |
| A2 | 0.21 BSC | | |
| A3 | 0.30 | 0.35 | 0.40 |
| d | 0.43 | 0.48 | 0.53 |
| D | 10.00 BSC | | |
| D1 | 8.00 BSC | | |
| E | 10.00 BSC | | |
| E1 | 8.00 BSC | | |
| e1 | 0.80 BSC | | |
| e2 | 0.80 BSC | | |
| L1 | 1.00 REF | | |
| L2 | 1.00 REF | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 BGA112 PCB Land Pattern



Figure 7.2. BGA112 PCB Land Pattern Drawing

Table 7.2. BGA112 PCB Land Pattern Dimensions

| Dimension | Min | Nom | Max |
|-----------|-----|------|-----|
| X | | 0.45 | |
| C1 | | 8.00 | |
| C2 | | 8.00 | |
| E1 | | 0.8 | |
| E2 | | 0.8 | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 BGA112 Package Marking



Figure 7.3. BGA112 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

8. TQFP100 Package Specifications

8.1 TQFP100 Package Dimensions



Figure 8.1. TQFP100 Package Drawing

Table 8.1. TQFP100 Package Dimensions

| Dimension | Min | Typ | Max |
|------------|----------|------|------|
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.09 | - | 0.20 |
| c1 | 0.09 | - | 0.16 |
| D | 16.0 BSC | | |
| E | 16.0 BSC | | |
| D1 | 14.0 BSC | | |
| E1 | 14.0 BSC | | |
| e | 0.50 BSC | | |
| L1 | 1 REF | | |
| L | 0.45 | 0.60 | 0.75 |
| Θ | 0 | 3.5 | 7 |
| Θ 1 | 0 | - | - |
| Θ 2 | 11 | 12 | 13 |
| Θ 3 | 11 | 12 | 13 |
| R1 | 0.08 | - | - |
| R2 | 0.08 | - | 0.2 |
| S | 0.2 | - | - |
| aaa | 0.2 | | |
| bbb | 0.2 | | |
| ccc | 0.08 | | |
| ddd | 0.08 | | |
| eee | 0.05 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 TQFP100 PCB Land Pattern



Figure 8.2. TQFP100 PCB Land Pattern Drawing

Table 8.2. TQFP100 PCB Land Pattern Dimensions

| Dimension | Min | Nom | Max |
|-----------|-----|----------|-----|
| C1 | | 15.4 | |
| C2 | | 15.4 | |
| E | | 0.50 BSC | |
| X | | 0.30 | |
| Y | | 1.50 | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.3 TQFP100 Package Marking



Figure 8.3. TQFP100 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

9. TQFP64 Package Specifications

9.1 TQFP64 Package Dimensions

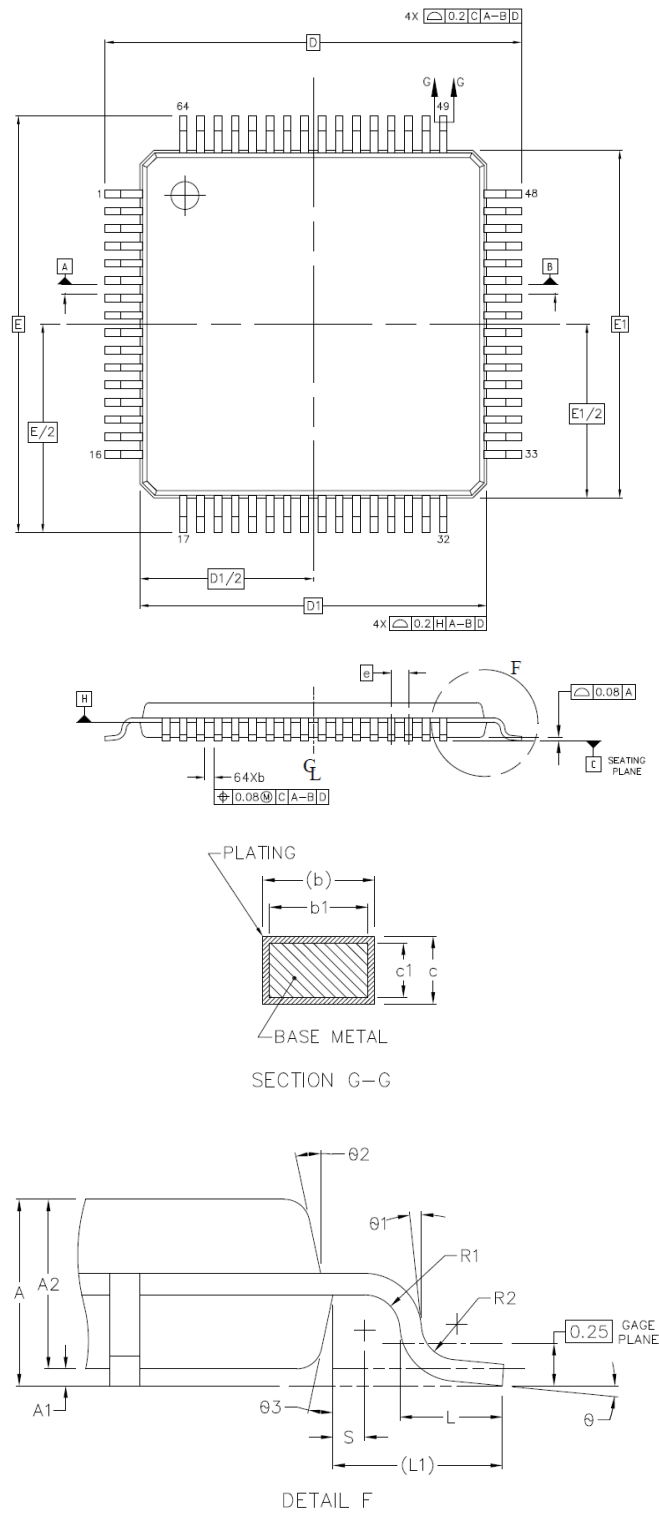


Figure 9.1. TQFP64 Package Drawing

Table 9.1. TQFP64 Package Dimensions

| Dimension | Min | Typ | Max |
|------------|-----------|------|------|
| A | — | 1.15 | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.09 | — | 0.20 |
| c1 | 0.09 | — | 0.16 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| e | 0.50 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| R1 | 0.08 | — | — |
| R2 | 0.08 | — | 0.20 |
| S | 0.20 | — | — |
| θ | 0 | 3.5 | 7 |
| $\theta 1$ | 0 | — | 0.10 |
| $\theta 2$ | 11 | 12 | 13 |
| $\theta 3$ | 11 | 12 | 13 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 TQFP64 PCB Land Pattern

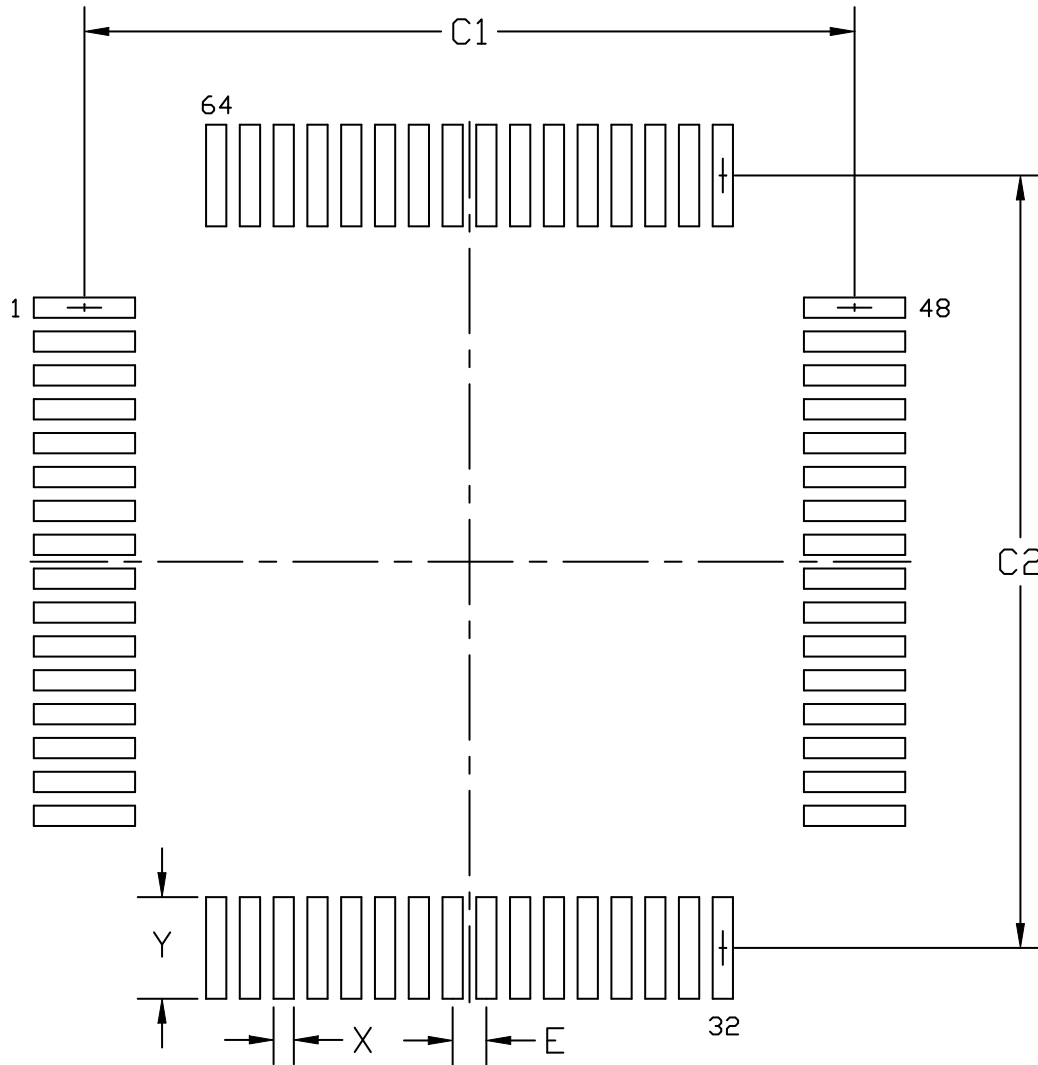


Figure 9.2. TQFP64 PCB Land Pattern Drawing

Table 9.2. TQFP64 PCB Land Pattern Dimensions

| Dimension | Min | Max |
|-----------|----------|-------|
| C1 | 11.30 | 11.40 |
| C2 | 11.30 | 11.40 |
| E | 0.50 BSC | |
| X | 0.20 | 0.30 |
| Y | 1.40 | 1.50 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 TQFP64 Package Marking



Figure 9.3. TQFP64 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

10. QFN64 Package Specifications

10.1 QFN64 Package Dimensions



Figure 10.1. QFN64 Package Drawing

Table 10.1. QFN64 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|-----------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | — | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| A3 | 0.203 REF | | |
| D | 9.00 BSC | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| D2 | 7.10 | 7.20 | 7.30 |
| E2 | 7.10 | 7.20 | 7.30 |
| L | 0.40 | 0.45 | 0.50 |
| L1 | 0.00 | — | 0.10 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 QFN64 PCB Land Pattern



Figure 10.2. QFN64 PCB Land Pattern Drawing

Table 10.2. QFN64 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| C1 | 8.90 |
| C2 | 8.90 |
| E | 0.50 |
| X1 | 0.30 |
| Y1 | 0.85 |
| X2 | 7.30 |
| Y2 | 7.30 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 QFN64 Package Marking



Figure 10.3. QFN64 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

11. Revision History

Revision 1.0

July, 2019

- [4.1 Electrical Characteristics](#) updated with final production test limits.
- RESETn pin pullup connection to AVDD clarified in pinout tables.
- [Table 5.20 GPIO Functionality Table on page 166](#) formatting updated for translation.

Revision 0.6

February, 2019

- Updated [2. Ordering Information](#) with new high temperature range BGA part numbers.
- [4.1 Electrical Characteristics](#) updated with notes distinguishing RESETn reference (AVDD) from all other GPIO reference (IOVDD).
- Added to pin description of DECOUPLE - decouple output for on-chip voltage should not be used to power external circuits.
- [5.20 GPIO Functionality Table](#): re-ordered to show pins in alphabetical order by GPIO name.

Revision 0.5

December, 2018

- [4.1 Electrical Characteristics](#) updated with latest characterization data and production test limits.
- [4.1 Electrical Characteristics](#) added SDIO location 1 and SDIO SPI mode timing details.
- [4.1 Electrical Characteristics](#) sorted all table footnotes in order of appearance.
- [Table 5.21 Alternate Functionality Overview on page 178](#) changed vertical white space.

Revision 0.1

May, 2018

Initial release.

Silicon Labs

Simplicity Studio™4



Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!



IoT Portfolio
www.silabs.com/IoT



SW/HW
www.silabs.com/simplicity



Quality
www.silabs.com/quality



Support and Community
community.silabs.com

Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, ClockBuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, ISOModem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>