



EFP01 Energy Friendly PMIC Family Data Sheet

The EFP01 Energy Friendly Power Management IC (PMIC) is an extremely flexible, highly efficient, multi-output power management IC, providing complete system power and primary cell battery Coulomb counting for EFM32 and EFR32 devices. The EFP01 can operate over a wide input voltage range (0.8 to 5.5 V) with quiescent current as low as 300 nA (EM2 mode, single output enabled).

EFP01 can be configured to support the following battery types:

- Single alkaline (Zn/MnO₂), zinc-carbon or lithium iron-disulfide (Li/FeS₂) primary cells, or NiMH/NiCd rechargeable cells (0.8 to 1.8 V)
- Dual alkaline, zinc-carbon or lithium iron-disulfide (Li/FeS₂) primary cells, or NiMH/NiCd rechargeable cells (1.6 to 3.6 V)
- Single lithium (Li/MnO₂) primary cells (1.8 to 3.2 V)
- Single lithium thionyl chloride (Li/SOCl₂) primary cell (3.0 to 3.65 V)
- Single lithium ion/lithium polymer (typically LiCoO₂) rechargeable batteries (2.7 to 4.35 V)
- Single lithium iron phosphate (LiFePO₄) rechargeable battery (2.5 to 3.65 V)
- USB (≤ 5.5 V)

EFP01 applications include the following:

- IoT Sensors and End Devices
- Metering
- Home and Building Automation and Security
- Health and Wellness
- Wearables
- Smart Accessories
- Human Interface Devices

ENERGY FRIENDLY FEATURES

- Provides 4 supply outputs:
 - One Buck/Boost DC-DC Converter
 - One Buck-only DC-DC Converter + LDO
 - One LDO
 - One Switched Output
- Up to 94% efficiency

1. Feature List

The EFP01 highlighted features are listed below.

- **VOA**
 - Output Voltage: 1.7 V to 5.2 V
 - DCDC A can be configured in Buck/Boost, Buck-only, or Boost-only
 - DCDC A output be combined with the VOC linear regulator for more efficient regulation as the input voltage approaches the output voltage
 - Firmware-programmable switched output (VOA_SW) allows complete powerdown of high leakage external circuitry in low power modes
- **VOB**
 - Output Voltage:
 - 0.8 V to 3.3 V (EFP0101/03/06/09/11)
 - 0.8 V to 1.26 V (EFP0102/04/07/08/10)
 - DCDC B can be used only in Buck configuration
 - Dedicated internal linear regulator in parallel provides more efficient regulation as the input voltage approaches the output voltage
- **VOC**
 - Output Voltage: 1.7 V to 3.3 V
 - Linear regulator only
 - Can be used either to create an independent third output supply or in conjunction with DCDC A
- **Coulomb Counter**
 - Lossless (i.e. no sense resistor) measurement of charge in- to the load
- **Communication & Control**
 - Fully configurable I²C
 - Direct Mode supports fast transitions between energy modes
 - IRQ pin to notify host processor
- **Ultra-low EM2 Quiescent Current**
 - 150 nA with no outputs enabled
 - 300 nA with a single output enabled
 - +125 nA for each additional output enabled
- **Safety**
 - Programmable inrush current
 - Short-circuit tolerant outputs
 - Under-voltage lock-out (UVLO) circuitry holds device in lowest power reset state when VDDDB is below 1.2 V
 - Over-temperature monitoring and IRQ assertion
- **Wide Operating Range**
 - 0.8 V to 5.5 V input power supply
 - -40 to 100 °C junction temperature
- **QFN20 3x3 mm Package**

2. Ordering Information

Additional OPN-specific features & limitations can be found in [• OPN-Specific Features](#).

Table 2.1. Ordering Information

| Orderable Part Number (OPN) | Supported Input Voltage Range | Device Configuration | VOB Configuration at Startup | Temp Code | Package | Top Mark Line 1 |
|-----------------------------|---|-----------------------|------------------------------|-----------|---------|-----------------|
| EFP0101GM20-E | 1.8 V–5.5 V | Wired Buck | 1.858 V | G | QFN20 | P01G |
| EFP0102GM20-E | 1.8 V–5.5 V | Wired Buck | OFF | G | QFN20 | P02G |
| EFP0103GM20-E | 1.8 V–5.5 V | Wired Buck with LDO C | 1.858 V | G | QFN20 | P03G |
| EFP0104GM20-E | 1.8 V–5.5 V | Wired Buck with LDO C | OFF | G | QFN20 | P04G |
| EFP0106GM20-E | 1.8 V–5.5 V | Buck/Boost | 1.858 V | G | QFN20 | P06G |
| EFP0107GM20-E | 1.8 V–5.5 V | Buck/Boost | OFF | G | QFN20 | P07G |
| EFP0108GM20-E | 0.8 V–1.8 V | Single-Cell Boost | OFF | G | QFN20 | P08G |
| EFP0109GM20-E | 1.8 V - 3.6 V | Wired Boost | 1.858 V | G | QFN20 | P09G |
| EFP0110GM20-E | 1.8 V - 3.6 V | Wired Boost | OFF | G | QFN20 | P10G |
| EFP0111GM20-E | 1.5 V–5.5 V (after startup), 2.5–5.5 V (at startup) | Boost Bootstrap | 1.858 V | G | QFN20 | P11G |

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3. System Overview

3.1 Introduction

The EFP01 Energy Friendly PMIC product family is designed to support a range of battery-powered applications, as well as other systems requiring high performance and low energy consumption.

A block diagram of the EFP01 family is shown in [Figure 3.1 EFP01 Block Diagram on page 7](#). The diagram shows a superset of features available on the family, which vary by part number. For more information about specific device features, consult [Ordering Information](#).

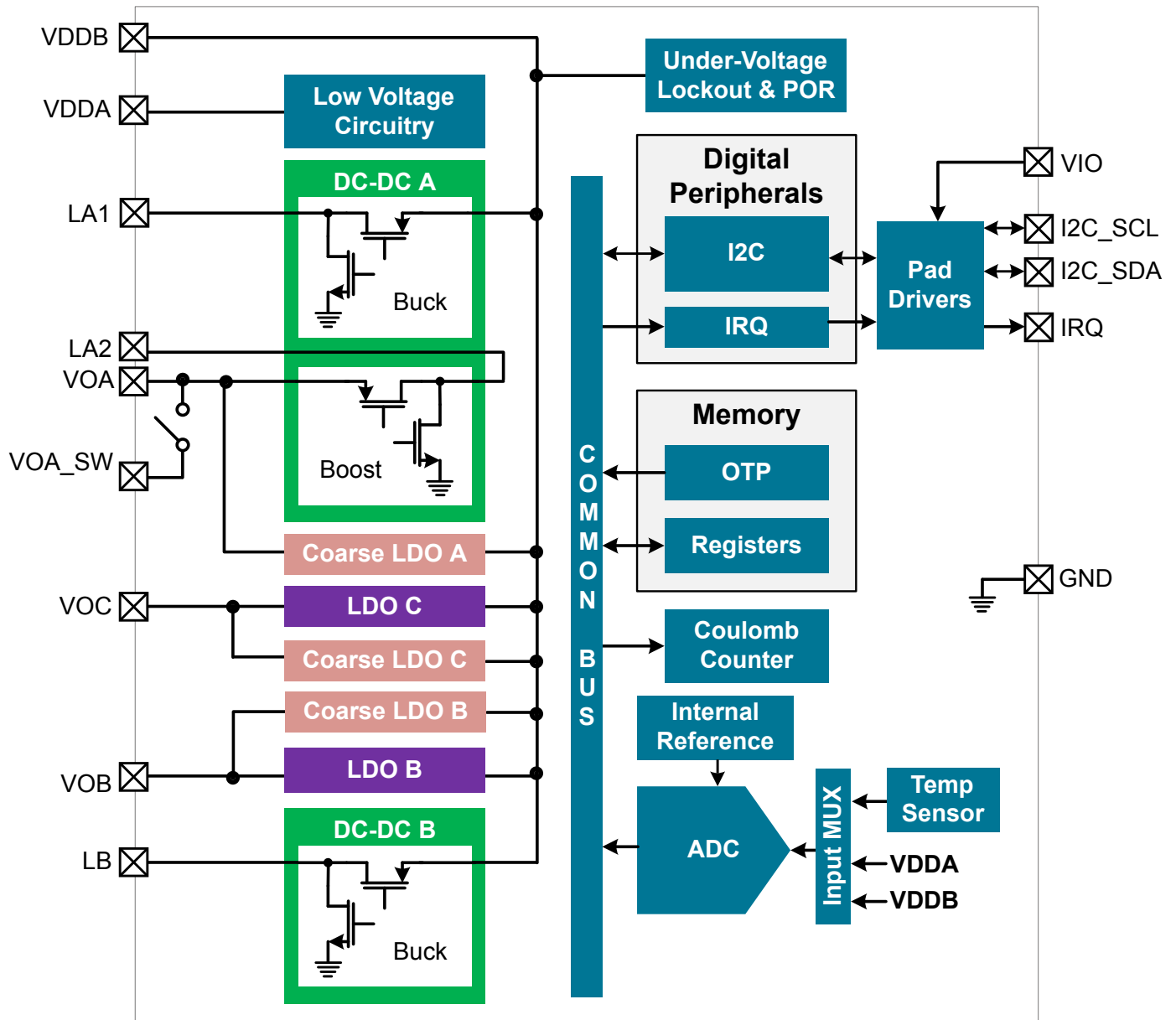


Figure 3.1. EFP01 Block Diagram

Table 3.1. OPN-Specific Features

| OPN | Supported Input Voltage Range | VOA Output at Startup | VOA DCDC Mode at Startup | VOB Output at Startup | VOB Programmable Range | VOC Output at Startup | EM4 Support | Battery Voltage Monitoring |
|----------------------------------|--|-----------------------|--------------------------------------|-----------------------|------------------------|---------------------------------|---|----------------------------|
| EFP0101 Wired Buck | 1.8 V-5.5 V | 1.860 V | Wired Buck | 1.858 V | 0.8 V -3.3 V | 1.870 V | Supported | Yes, on VDDB |
| EFP0102 Wired Buck | 1.8 V-5.5 V | 1.860 V | Wired Buck | OFF | 0.8 V -1.26 V | 1.870 V | Supported, VOB Coarse Regulator disabled | Yes, on VDDB |
| EFP0103 Wired Buck with LDO C | 1.8 V-5.5 V | 1.860 V | Wired Buck with LDO | 1.858 V | 0.8 V -3.3 V | Not available (Paired with VOA) | Supported | Yes, on VDDB |
| EFP0104 Wired Buck with LDO C | 1.8 V-5.5 V | 1.860 V | Wired Buck with LDO | OFF | 0.8 V -1.26 V | Not available (Paired with VOA) | Supported, VOB Coarse Regulator disabled | Yes, on VDDB |
| EFP0106 Buck/Boost | 1.8 V-5.5 V | 1.860 V | Buck/Boost | 1.858 V | 0.8 V -3.3 V | 1.870 V | Supported | Yes, on VDDB |
| EFP0107 Buck/Boost | 1.8 V-5.5 V | 1.860 V | Buck/Boost | OFF | 0.8 V -1.26 V | 1.870 V | Supported, VOB Coarse Regulator disabled | Yes, on VDDB |
| EFP0108 Single-Cell Boost | 0.8 V-1.8 V | 1.860 V | Wired Boost | OFF | 0.8 V -1.26 V | OFF | Not supported | Yes, on VDDB |
| EFP0109 Wired Boost | 1.8 V-3.6 V | 3.327 V | Wired Boost | 1.858 V | 0.8 V -3.3 V | 1.870 V | Supported | Yes, on VDDB |
| EFP0110 Wired Boost | 1.8 V-3.6 V | 3.327 V | Wired Boost | OFF | 0.8 V -1.26 V | 1.870 V | Supported, VOB Coarse Regulator disabled | Yes, on VDDB |
| EFP0111 Boost Bootstrap | 1.5 V-5.5 V (after start-up), 2.5V-5.5V (at startup) | 5.222 V | Wired Boost, Current Limited Enabled | 1.858 V | 0.8 V -3.3 V | 1.870 V | Supported when supply voltage $\geq 2.5V$. | Not supported |

3.2 Power

The EFP01 can provide up to three voltage rails for EFR32 and EFM32 devices from a single input supply voltage.

The EFP01 has two independent DCDC converters: DCDC A and DCDC B, each requiring an external inductor. DCDC A can use buck/boost, wired buck, or wired boost configurations, while DCDC B only supports buck configuration.

In addition, the EFP01 has two integrated LDOs supplied from the VDDB pin: LDO B and LDO C. LDO B is internally wired in parallel with DCDC B. LDO C can be used independently or externally wired in parallel with DCDC A.

Finally, each EFP01 output (VOA, VOB, VOC) has its own coarse regulator in parallel for use in [EM4](#). The coarse regulators have very low quiescent current draw, but have poor output regulation (e.g., the output may range from ~1.7 to 3.4 V) and can only support very light loads (~100 μ A).

The EFP01 Configuration Tool in Simplicity Studio can generate recommended settings and a configuration header file to simplify development.

3.2.1 DCDC A Overview

The EFP01's DCDC A can be configured for buck/boost, wired buck, or wired boost modes.

Table 3.2. DCDC A Configuration and Modes Summary

| Hardware Configuration | DCDC A Operating Mode | Required Register Setting | Compatible OPNs |
|-----------------------------------|-------------------------|----------------------------------|-------------------|
| Buck | Wired Buck | BB_CTRL3.BB_MODE = 6 | EFP0101 / EFP0102 |
| Buck with LDO | Wired Buck with LDO | BB_CTRL3.BB_MODE = 5 | EFP0103 / EFP0104 |
| Buck/Boost | Autonomous (Buck/Boost) | BB_CTRL3.BB_MODE = 1 (typically) | EFP0106 / EFP0107 |
| Single-Cell Boost | Wired Boost | BB_CTRL3.BB_MODE = 7 | EFP0108 |
| Wired Boost | Wired Boost | BB_CTRL3.BB_MODE = 7 | EFP0109 / EFP0110 |
| Boost Bootstrap | Wired Boost | BB_CTRL3.BB_MODE = 7 | EFP0111 |

3.2.1.1 Output Voltage Configuration

The DCDC A output target voltage is set by the VOA_V register according to the below equation:

$$VOA (V) = 1.7374V + (VOA_V \times 0.0306V)$$

Unlike DCDC B, there is only a single VOA output voltage register that is used in both EM0 and EM2 modes.

Note that in Boost modes it is possible to program the VOA output voltage to a voltage higher than the Maximum Output Voltage in the Electrical Characteristics table. Firmware should ensure that the Maximum Output Voltage isn't exceeded.

3.2.1.2 Peak Current Configuration

DCDC A has a configurable peak current adjustment set by the BB_IPK and BB_IPK_EM2 fields of the BB_IPK register. The BB_IPK and BB_IPK_EM2 settings are used differently depending on the operating mode of the DCDC A converter (as shown below), but the resulting peak currents for all modes are derived from the following base peak current (IPK_BASE) equations.

In EM0, IPK_BASE is determined by: $IPK_BASE = 0.090A + (0.009A \times BB_IPK)$

In EM2, IPK_BASE is determined by: $IPK_BASE = 0.090A + 0.009A \times (4 \times BB_IPK_EM2 + 2)$

Typically, the peak current can be lowered in EM2 for greater efficiency. However, unlike DCDC B there is only a single Coulomb counter for DCDC A that is used in both EM0 and EM2 modes. Therefore, if Coulomb counting is used with DCDC A, BB_IPK_EM2 must be set such that the peak current in EM2 is the same as the peak current in EM0 to ensure the charge per pulse is the same in both energy modes. Roughly equivalent peak currents in EM2 and EM0 can be achieved by setting $BB_IPK_EM2 = (BB_IPK - 2) / 4$.

Note: The Maximum Output Current formulas below provide useful guidance but are not a guarantee of performance. The final authority for the Maximum Output Current will be the Output Load Current specifications in the Electrical Characteristics tables.

Buck Mode

- Register Programming: BB_CTRL3.BB_MODE = WiredBuck or Autonomous
- $Peak\ Current\ (A) = IPK_BASE + \frac{25ns \times (VDDB - VOA)}{L_A}$
- $Maximum\ Output\ Current\ (A) = 0.5 \times IPK_BASE$

Buck/Boost Mode (NTM Operation)

- Register Programming: BB_CTRL3.BB_MODE = Autonomous
- $Peak\ Current\ (A) = 1.15 \times IPK_BASE + \frac{25ns \times VDDB}{L_A}$
- $Maximum\ Output\ Current\ (A) = 0.5 \times 1.15 \times IPK_BASE$

Boost Mode (with no peak current adjustment)

- Register Programming: BB_CTRL3.BB_MODE = WiredBoost or Autonomous, BB_CTRL6.BB_IPK_NOADJ = 1
- $Peak\ Current\ (A) = 2.35 \times IPK_BASE + \frac{25ns \times VBOOST}{L_A}$
- $Maximum\ Output\ Current\ (A) = efficiency \times 0.5 \times 2.35 \times IPK_BASE \times \frac{VBOOST}{VOA}$

Boost Mode (with peak current adjustment)

- Register Programming: BB_CTRL3.BB_MODE = WiredBoost or Autonomous, BB_CTRL6.BB_IPK_NOADJ = 0, BB_CTRL5.BB_IPK_BOOST_ADJ is programmed as recommended in its register description, ADC_CC_CTRL.ADC_INTERVAL > 0 to enable ADC operations.
- When operating in Boost Mode with peak current adjustment, the peak current will be adjusted to maintain a near constant output load current over the battery voltage range. Note that peak current adjustment only affects EM0 operation. In EM2, the Boost Mode (with no peak current adjustment) equations apply.
- $Peak\ Current\ (A) = 2.35 \times MIN\left(\frac{IPK_BASE \times VOA}{2 \times VBOOST}, 385mA\right) + \frac{25ns \times VBOOST}{L_A}$
- $Maximum\ Output\ Current\ (A) = efficiency \times 0.5 \times 2.35 \times MIN\left(\frac{IPK_BASE \times VOA}{2 \times VBOOST}, 385mA\right) \times \frac{VBOOST}{VOA}$

3.2.1.3 Peak Current Adjustment

In boost mode, the EFP01 can be configured to automatically adjust the DCDC A peak current based on the battery voltage to support a near-constant maximum output load current (where the maximum output load current is $\sim IPK_BASE / 2$). This feature allows the boost converter to lower the peak current at higher battery voltages, resulting in more efficient operation and lower output ripple voltage, as shown in [Figure 3.2 Peak Current Adjustment Comparison on page 11](#).

Because the peak current adjustment feature requires battery voltage monitoring, the ADC must be enabled (i.e., the ADC_INTERVAL field of the ADC_CC_CTRL register is set to a non-zero value). This also means that peak current adjustment is not available in the [Boost Bootstrap](#) configuration, because battery monitoring is not support in that configuration.

If peak current adjustment is enabled, it will only affect peak current in EM0, and not EM2.

To use peak current adjustment:

1. Set BB_IPK_NOADJ = 0 in the BB_CTRL6 register
2. Program BB_IPK_BOOST_ADJ in the BB_CTRL5 register as recommended in its register description. Note that because the BB_IPK_BOOST_ADJ value is dependent on both the VOA target voltage and the BB_IPK setting, the BB_IPK_BOOST_ADJ value should be updated whenever the VOA target or the peak current settings are changed.
3. Set ADC_INTERVAL in the ADC_CC_CTRL register to a non-zero value to enable ADC operations

To disable peak current adjustment, set BB_IPK_NOADJ = 1 in the BB_CTRL6 register.



Figure 3.2. Peak Current Adjustment Comparison

3.2.1.4 Current Limiting

When powering EFP01 from weak power sources or sources with a high internal impedance, peak load currents at the converter output can cause a large supply voltage droop at the input, increasing the risk of an unintended power-on reset. To alleviate these issues, it may be necessary to limit the input current.

Note: EFP0111 is the only OPN that has its current limit enabled by default (on DCDC A).

Note: Because enabling the current limit will essentially current-starve the output, the system designer should validate the application under the worst-case output load current.

On EFP01, the current limit is controlled by forcing a minimum time between the start of pulse events (T_{SW_MIN}) and is configured by BB_IRI_CON in the BB_CTRL6 register. BB_IRI_CON can be calculated based on the mode, the input voltage (V_{DDB}), output voltage (V_{OA}), DCDC A inductor value (L_A), peak current (I_{PK} , set by BB_IPK), and the desired limited battery current (I_{BATT_LIMIT}) as follows:

$$\text{In buck mode: } I_{BATT_LIMIT} = \frac{L \times I_{PK}^2}{2 \times T_{SW_MIN}} \times \frac{1}{(V_{DDB} - V_{OA})}$$

$$\text{In boost mode: } I_{BATT_LIMIT} = \frac{L \times I_{PK}^2}{2 \times T_{SW_MIN}} \times \left(\frac{1}{V_{OA} - V_{BOOST}} + \frac{1}{V_{BOOST}} \right)$$

where T_{SW_MIN} is programmed by BB_IRI_CON as follows:

$$T_{SW_MIN} = 300ns \times (2 \times BB_IRI_CON + 1)$$

Note that the required BB_IRI_CON setting for a given current limit varies with the V_{DDB} or V_{BOOST} voltages and the peak current, both variables that can change over battery voltage. An application requiring a fixed current limit over the entire range of the battery may need to occasionally measure the V_{DDB} voltage and recalculate / reprogram the BB_IRI_CON setting.

Note also that in configurations where the VOC LDO is used in parallel with the VOA output (e.g., Buck with LDO configuration), the BB_IRI_CON bitfield in the BB_CTRL6 register will control the current limit when the converter is in DCDC mode and the VOC_IRI_CON bitfield in the $LDOC_BB_CTRL$ register will control the current limit when the converter is in LDO mode.

3.2.1.5 T_{ON} Maximum Limiting

Buck Mode T_{ON_MAX}

In Buck mode, the pulse frequency modulation (PFM) pulse on time (T_{ON}) required to charge the inductor is given by:

$$T_{ON} = \frac{L \times I_{PK}}{V_{DDB} - V_{OA}}$$
 As V_{DDB} approaches V_{OA} , the resulting T_{ON} can become quite large, resulting in sizable output ripple voltage or, in the worst case, the DCDC stalling altogether.

When the BB_TON_MAX field in the $LDOC_BB_CTRL$ register is set to a non-zero value, the PFM pulse T_{ON} will be limited as shown:
$$T_{ON_MAX} = 70 \text{ ns} + (1 + (4 \times BB_TON_MAX))$$
 A limited T_{ON} will terminate the inductor charging before the programmed peak current value is reached, and limit the maximum available load current and the actual peak current values.

Because the time-measuring circuitry required to limit T_{ON} costs some small amount of power, BB_TON_MAX should be set to set a nonzero value only under specific conditions:

- If the subsequent reduction in max available load current can be tolerated and the reduction in ripple voltage is desired.
- When operating with low input voltage headroom (i.e., $V_{DDB} - V_{OA}$ is very small) and there is no LDO enabled in parallel with the DCDC output.



Figure 3.3. Buck Mode TON_MAX Limiting Example

Boost Mode T_{ON_MAX}

In Boost mode, the BB_TON_MAX field in the $LDOC_BB_CTRL$ register should be set to a non-zero value to ensure a finite on-time under all conditions. Without this protection, in certain scenarios (e.g., where the inductor peak current may be limited by battery impedances and inductor and power train resistances), the inductor current may not reach the threshold of the peak current detector and the Boost converter power train NMOS will not turn off.

3.2.1.6 Boost Mode T_{OFF} Maximum Limiting

In certain scenarios, the battery voltage at the input to the EFP01 in boost mode can be as high as, or higher than, the desired output. For example:

- A Li/FeS₂ battery can have an output voltage as high as 1.8 V at the very start of its life, which would be problematic in an application where the regulated output needs to be 1.8 V.
- Two alkaline or Li/FeS₂ batteries in series can provide a voltage as high as 3.6 V. If a 3.3 V regulated output is desired, the buck/boost configuration can be used, but the buck/boost configuration efficiency is ~5-8% less than the wired boost configuration.

A PFM converter, such as the EFP01, cannot typically operate in a boost mode with an input voltage even slightly higher than the output. In this scenario, the inductor current during the T_{OFF} interval may never reach zero (a requirement for the converter to signal the end of the discharge phase), resulting in an inaccurate and poorly regulated output voltage.

To address this issue, the EFP01 has a T_{OFF} maximum limiting feature to enforce a maximum discharge interval time. When the BB_TOFF_MAX field in the BB_CTRL6 register is set to a nonzero value, the T_{OFF} discharge interval is ended after a set period of time, even if the inductor current has not reached zero, with any residual inductor current is discharged into the VOA pin.

To avoid extremely large ripple voltage, T_{OFF} maximum limiting should only be enabled when the maximum battery voltage is no higher than 0.3V above the programmed VOA voltage.

3.2.1.7 NTM Buck/Boost Transitional Mode

When DCDC A is in the Buck/Boost configuration and programmed to Autonomous (or Buck/Boost) mode, (i.e., BB_CTRL3.BB_MODE = 1), the DCDC converter will automatically switch between one of three operating modes:

- Buck: Traditional Buck operation used when VDDDB is much greater than VOA
- Boost: Traditional Boost operation used when VDDDB is much lower than VOA
- NTM: Transitional mode between Buck and Boost modes, used when VDDDB is close to VOA

The Boost-to-NTM and NTM-to-Buck mode transition voltage thresholds are controlled by the NTM_LDO_THRSH bit field in the BB_CTRL3 register. For example, the figures below show the DCDC A operating mode versus the battery voltage for various NTM_LDO_THRSH settings for a Buck/Boost application with a 3.3V output.

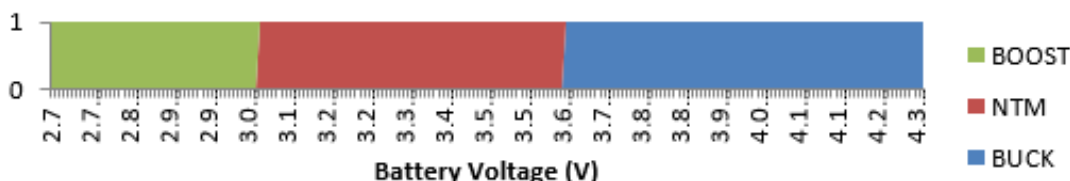


Figure 3.4. Operating Mode vs Battery Voltage, NTM_LDO_THRSH=3

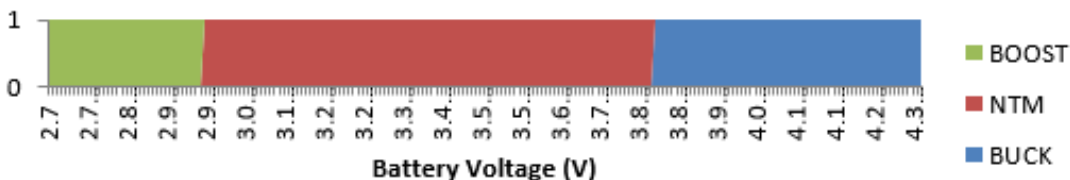


Figure 3.5. Operating Mode vs Battery Voltage, NTM_LDO_THRSH=5

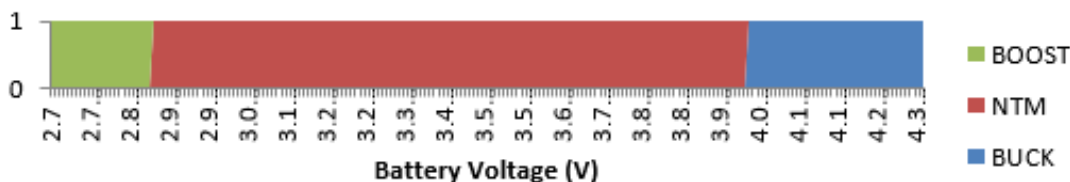


Figure 3.6. Operating Mode vs Battery Voltage, NTM_LDO_THRSH=7

3.2.1.8 VOA Switch (VOA_SW)

The VOA output has an internal switch connecting it to the VOA_SW pin. This optional VOA_SW output can be used to completely power down high-leakage external circuitry when entering the 3.3.3 EM2 and/or 3.3.4 EM4 modes. The VOA_SW state is controlled by the VOA_SW_CON bitfield in the BIAS_SW register.

Note that if a large capacitive load is attached to the VOA_SW output, the VOA output may see momentary voltage droops when VOA_SW is enabled.

3.2.1.9 DCDC A with LDO C in Parallel

In certain configurations, DCDC A is connected in parallel with LDO C on the printed circuit board, such as [4.1.2 Wired Buck with LDO C Configuration \(EFP0103 & EFP0104\)](#). This configuration is advantageous when the minimum input supply voltage approaches the VOA output voltage (e.g., $V_{DDB_{MIN}} - VOA \leq 300\text{mV}$) as it allows EFP01 to continue to regulate the output voltage over a wider input voltage range than is possible with DCDC A alone.

When LDO C is used in parallel with DCDC A:

- The DCDC mode must be set to WIREDBUCKLDO (i.e., `BB_MODE = 3` in the `BB_CTRL3` register)
- The input voltage threshold for transition from Buck-to-LDO mode can be adjusted by the `NTM_LDO_THRSH` bitfield in the `BB_CTRL3` register.
- If inrush current limiting is desired, the `BB_IRI_CON` bitfield in the `BB_CTRL6` register controls the current limit when the converter is in DCDC mode and the `VOC_IRI_CON` bitfield in the `LDOC_BB_CTRL` register controls the current limit when the converter is in LDO mode.
- When Coulomb counting is enabled, the resulting pulse counts will be split between the `CCA_MSBY/LSBY` result registers (when the converter is in DCDC mode) and the `CCC_MSBY/LSBY` result registers (when the converter is in LDO mode).

Note that when using LDO C in parallel with DCDC A, LDO C is not available as an independent LDO.

3.2.1.10 Low Voltage Charge Pump

The EFP0108 Single-Cell Boost mode enables the use of battery voltages between 0.8V and 1.8V. Because this is below the 1.8V minimum `V_{DDB}` operating voltage, the EFP0108 must temporarily generate an internal voltage sufficient to supply `V_{DDB}`. To do this, the EFP0108 enables a charge pump supplied from its `V_{DDA}` pin at startup. Once the internal charge pump output reaches a level sufficient to supply `V_{DDB}`, the regular DCDC A Boost powertrain circuitry is enabled and the VOA output is boosted to its target voltage. At that point, `V_{DDB}` will be powered from the DCDC A output (VOA is externally connected to `V_{DDB}` as shown in [Figure 4.4 Single-Cell Boost Configuration on page 33](#)). At this point, the low voltage charge pump is no longer needed and is automatically disabled.

For all other OPNs, the low voltage charge pump is not used, and the `V_{DDA}` input can safely be grounded.

3.2.2 DCDC B Overview

The EFP01's DCDC B can only be configured for buck mode.

Table 3.3. DCDC B Configuration and Modes Summary

| Mode | Required Register Configurations |
|-----------------------------|-----------------------------------|
| Buck with LDO B in parallel | <code>BK_CTRL1.BK_MODE = 3</code> |
| Buck | <code>BK_CTRL1.BK_MODE = 1</code> |

3.2.2.1 Output Voltage Configuration

The DCDC B output target voltage in EM0 is set by `VOB_EM0_V` in the `VOB_EM0_V` register according to the below equation:

$$VOB \text{ in } EM0 (V) = 0.8095V + (VOB_EM0_V \times 0.0223V)$$

In EM2, the DCDC B output target voltage will be automatically set to value specified in the `VOB_EM2_V` register according to the below equation:

$$VOB \text{ in } EM2 (V) = 0.8095V + (VOB_EM2_V \times 0.0223V)$$

3.2.2.2 Peak Current Configuration

DCDC B has configurable peak current adjustment, set by the BK_IPK and BK_IPK_EM2 fields in the BK_IPK register.

In EM0, IPK_BASE is determined by: $IPK_BASE = 0.090A + (0.009A \times BK_IPK)$

In EM2, IPK_BASE is determined by: $IPK_BASE = 0.090A + 0.009A \times (4 \times BK_IPK_EM2 + 2)$

The DCDC B buck converter peak current is determined by: $Peak\ Current\ (A) = IPK_BASE + \frac{25ns \times (VDDDB - VOB)}{L_B}$

Typically, the peak current can be lowered in EM2 for improved efficiency.

Note: The Maximum Output Current formula below provides useful guidance but is not a guarantee of performance. The final authority for the Maximum Output Current will be the Output Load Current specifications in the Electrical Characteristics tables.

The DCDC B buck converter maximum output current is determined by: $Maximum\ Output\ Current\ (A) = 0.5 \times IPK_BASE$

3.2.2.3 Current Limiting

When powering EFP01 from weak power sources or sources with a high internal impedance, peak load currents at the converter output can cause a large supply voltage droop at the input, increasing the risk of an unintended power-on reset. To alleviate these issues, it may be necessary to limit the input current.

Note: Because enabling the current limit will essentially current-starve the output, the system designer should validate the application under the worst-case output load current.

On EFP01, the current limit is controlled by forcing a minimum time between the start of pulse events and is configured by the BK_IRI_CON field in BK_CTRL2. BK_IRI_CON can be calculated based on the mode, the input voltage (VDDDB), output voltage (VOB), DCDC B inductor value (L_B), peak current (I_{PK}, set by BK_IPK), and the desired limited battery current (I_{BATT_LIMIT}) as follows:

$$I_{BATT_LIMIT} = \frac{L \times I_{PK}^2}{2 \times T_{SW} \times (VDDDB - VOB)}$$

where T_{SW} is programmed by BK_IRI_CON as follows:

$$T_{SW} = 300ns \times (2 \times BK_IRI_CON + 1)$$

The maximum output load current is going to be limited accordingly, and can be determined by:

$$I_{LOAD_MAX} = \frac{VDDDB}{VOB} \times efficiency \times I_{BATT_LIMIT}$$

Note that the required BK_IRI_CON setting for a given current limit varies with the VDDDB voltage and the peak current, both variables that can change over battery voltage. An application requiring a fixed current limit over the entire range of the battery may need to occasionally measure the VDDDB voltage and recalculate / reprogram the BK_IRI_CON setting.

3.2.2.4 T_{ON} Maximum Limiting

In Buck mode, the pulse frequency modulation (PFM) pulse on time (T_{ON}) required to charge the inductor is roughly (L × IPK)/(VDDDB - VOB). As VDDDB approaches VOB, the resulting T_{ON} can become quite large, resulting in large output ripple voltage or, in the worst case, the DCDC stalling altogether.

When the BK_TON_MAX field in the BK_CTRL1 register is set to a non-zero value, the PFM pulse T_{ON} is limited to no more than 70 ns × (1 + 4 × BK_TON_MAX), which terminates the inductor charging before the programmed peak current value is reached. When operating in this T_{ON} limiting mode, the maximum available load current and the actual peak current values are reduced from the otherwise expected value.

Because the time measuring mechanism costs some power, BK_TON_MAX should be set to set a nonzero value only under specific conditions:

- If the subsequent reduction in max available load current can be tolerated and the reduction in ripple voltage is desired.
- When operating with low input voltage headroom (i.e., VDDDB - VOB is very small) and there is no LDO enabled in parallel with the DCDC output.

Comparison plots of T_{ON} limiting can be found in [Figure 3.3 DCDC A TON Max Limiting Example on page 14](#).

3.2.2.5 DCDC B with LDO B in Parallel

DCDC B is internally connected in parallel with LDO B, and the two can optionally be used in parallel. This configuration is advantageous when the minimum input supply voltage (VDDB) approaches the VOB output voltage (e.g., $VDDB_{MIN} - VOB \leq 300\text{mV}$) as it allows EFP01 to continue to regulate the output voltage over a wider input voltage range than is possible with DCDC B alone.

When LDO B is used in parallel with DCDC B:

- The DCDC mode must be set to BUCKLDO (i.e., BK_MODE = 3 in the BK_CTRL1 register).
- The input voltage threshold for transition from Buck-to-LDO mode can be adjusted by the BK_LDO_THRESH bit field in the BB_CTRL2 register. It is recommended that this setting be left at power-on default value.

3.2.3 LDO B and LDO C Overview

The EFP01 has two integrated LDOs supplied from the VDDB pin. Instead of being continuously on, each LDO operates in a pulsed-current mode that minimizes quiescent current and is compatible with the internal Coulomb counter.

3.2.3.1 LDO B

LDO B is hard-wired in parallel with DCDC B, with an output sharing the VOB pin. When used in parallel with DCDC B, DCDC B will automatically switch to LDO B to provide better efficiency as the input voltage approaches the output voltage. LDO B can also be used as a standalone LDO (i.e. without DCDC B).

LDO B shares the DCDC B output voltage target registers, VOB_EM0_V and VOB_EM2_V.

Table 3.4. LDO B Summary

| Mode | Required Register Configuration(s) | Output Pin | Output Target Voltage Registers |
|-------------------------|------------------------------------|------------|---------------------------------|
| In parallel with DCDC B | BK_CTRL1.BK_MODE = 3 | VOB | VOB_EM0_V and VOB_EM2_V |
| Standalone, no DCDC | BK_CTRL1.BK_MODE = 2 | | |

3.2.3.2 LDO C

Similar to LDO B, LDO C can be used as an independent standalone supply (with the LDO output on the VOC pin) or may be connected in parallel with DCDC A (with the LDO output sharing the VOA pin with DCDC A). When used in parallel with DCDC A, DCDC A will automatically switch to LDO C to provide better efficiency as the input voltage approaches the output voltage.

LDO C's output voltage register depends on the mode:

- In standalone mode, the output voltage target is set in the VOC_V register.
- In parallel mode, the LDO C shares DCDC A's output voltage register, VOA_V.

Table 3.5. LDO C Summary

| Mode | Required Register Configuration(s) | Output Pin | Output Target Voltage Register |
|-------------------------|---|---|--------------------------------|
| In parallel with DCDC A | BB_CTRL3.BB_MODE = 5 | VOA = VOC (must be shorted together on PCB) | VOA_V |
| Standalone, no DCDC | LDOC_CTRL.LDOC_ENA_SA = 1 and BB_CTRL3.BB_MODE != 5 | VOC | VOC_V |

3.2.3.3 Maximum Output Current

After startup, the maximum output current for LDO B and LDO C is set by the LDOB_IGAIN and LDOC_IGAIN fields in the LDOB_CTRL and LDOC_CTRL registers, respectively. The LDOx_IGAIN fields should be set to the required output current plus margin, but no higher than necessary. LDOx_IGAIN can be computed as follows:

Note: The Maximum Output Current formula below provides useful guidance but is not a guarantee of performance. The final authority for the Maximum Output Current will be the Output Load Current specifications in the Electrical Characteristics tables.

$$LDOx_IGAIN = ROUND\left(17 - \frac{V_{OUT}}{2.76 \times I_{OUT_MAX}}\right)$$

At startup, and prior to the LDO reaching its target voltage, the available output current for LDO B and LDO C is determined by the LDOB_VMIN and LDOC_VMIN fields in the LDOB_CTRL and LDOC_CTRL registers, respectively. To ensure the LDO output current at startup is always at least the desired amount (as configured by LDOx_IGAIN, above), the settings for the LDOx_VMIN fields should be programmed based on the output target voltage as shown below:

Table 3.6. LDOx_VMIN Settings

| V _{OUT} Range | LDOx_VMIN Setting |
|--------------------------------|-------------------|
| V _{OUT} ≥ 2.7V | 3 |
| 2.4V ≤ V _{OUT} < 2.7V | 2 |
| 2.0V ≤ V _{OUT} < 2.4V | 1 |
| V _{OUT} < 2.0V | 0 |

Table 3.7 Example LDOx_IGAIN and LDOx_VMIN settings on page 20 shows the recommended LDOx_IGAIN and LDOx_VMIN settings for some example applications. Note that in the calculations below, I_{OUT_MAX} has been increased by 20% to provide some margin.

Table 3.7. Example LDOx_IGAIN and LDOx_VMIN settings

| V _{OUT} (V) | I _{OUT_MAX} (mA) | LDOx_IGAIN | LDOx_VMIN |
|----------------------|---------------------------|------------|-----------|
| 1.8 | 50 | 6 | 0 |
| 1.8 | 100 | 12 | 0 |
| 3.0 | 50 | 0 | 3 |
| 3.0 | 100 | 8 | 3 |
| 1.2 (LDO B only) | 50 | 10 | 0 |

3.2.3.4 LDO Current Limiting

On EFP01, the current limit is controlled by forcing a minimum time between the start of pulse events (T_{SW_MIN}) and is configured by the BK_IRI_CON bitfield in the BK_CTRL2 register (for LDO B) or the VOC_IRI_CON bitfield in the LDOC_BB_CTRL register (for LDO C). The (I_{BATT_LIMIT}) can be determined from the IRI_CON setting as follows:

$$I_{BATT_LIMIT} = \frac{I_{OUT_MAX}}{(2 \times IRI_CON + 1)}$$

where I_{OUT_MAX} is determined by LDOx_IGAIN as shown in 3.2.3.3 Maximum Output Current.

Because the current limit is essentially current-starving the output, most applications will likely want to disable the current limit after the output is stable (which can be determined by polling the STATUS_LIVE.VOx_INREG_LIVE bits).

3.2.3.5 LDO Startup

In some configurations, the LDO input supply (i.e., the VDDB pin) is powered from the VOA output. The VOA output may see momentary voltage droops when the LDO is enabled due to instantaneous current required to charge the 10 μ F capacitors on the LDO outputs. To avoid this, the current limit can be enabled before the LDO is enabled and then disabled after the LDO output is stable. Consult [3.2.3.4 LDO Current Limiting](#) for more information.

3.2.3.6 DCDC to LDO Transition

When DCDC A or B is operating with a LDO in parallel, at some point the VDDB input supply voltage approaches the LDO output voltage causing the controller to switch from DCDC mode to LDO mode. The dropout voltage (VDDB-VOB for LDO B or VDDB-VOC for LDO C) at which this transition from DCDC to LDO occurs is controlled by the BK_LDO_THRESH bit field in the BK_CTRL2 register for DCDC B / LDO B, and by the NTM_LDO_THRSH bit field in the BB_CTRL3 register for DCDC A / LDO C.

3.2.3.7 Bypass Mode

Both LDO B and LDO C support a bypass mode, in which the VDDB pin input voltage is shorted directly to the corresponding output pin (VOB and VOC, respectively). By default, both LDOs automatically enter bypass mode when the input supply voltage at VDDB drops too low to maintain regulation accuracy. This behavior can be disabled for both LDOs by setting the LDO_NO_AUTO_BYP bit in the LDOB_CTRL register.

In addition, both LDO B and LDO C can be forced into bypass mode by setting the BYP bit in the LDOB_CTRL and LDOC_CTRL registers, respectively. When forcing bypass mode, care must be taken to ensure that any loads attached to the LDO output pins (VOB and VOC) are tolerant of the VDDB pin input voltage.

3.2.4 Coarse Regulators

Each EFP01 output (VOA, VOB, VOC) has its own coarse regulator in parallel for use in EM4. The coarse regulators have very low quiescent current draw but poor output regulation — the outputs may range from 1.69V to 3.4V — and can only support very light loads (100 μ A).

The coarse regulator for each output can be enabled by setting the corresponding CRSREG_EN_x bit in the EM_CRSSREG_CTRL register. If the CRSREG_BYP bit is set, any enabled coarse regulator's output (VOA, VOB, or VOC pin) is shorted to its input (the VDDB pin).

For certain OPNs (EFP0102/04/07/08/10) the maximum VOB output is limited to 1.26V, which is incompatible with both the coarse regulator and the bypass mode. For this reason, the VOB coarse regulator and VOB coarse regulator bypass features are disabled on these OPNs.

3.3 Energy Modes

The EFP01 operates in 3 different energy modes to optimize efficiency based on the expected load.

Table 3.8. Energy Modes Overview

| Energy Mode | Maximum Output Current (per output) | BIAS_SW Register Programming | Coarse Regulator | DCDCs and LDOs | ADC | Coulomb Counter |
|-------------|---|------------------------------|--|--|-----------|-----------------|
| EM0 | Full Output Current (value depends on mode and configuration) | BIAS0 = 7 | Disabled | On, if enabled | Available | Available |
| EM2 | ~20 mA (value depends on mode and configuration) | BIAS2 = 1 | Disabled | On, if enabled. Note that if BB_CTRL6.BB_I PK_NOADJ is set in Boost modes, no peak current adjustment will occur in EM2. | Available | Available |
| EM4 | ~100 uA | N/A | Enabled according to setting of CRSREG_EN_X bits in EM_CRSREG_CTRL | All DCDCs and LDOs disabled | Disabled | Not supported |

3.3.1 Energy Mode Control

The energy mode state of EFP01 can be changed either by I²C or via direct pin control.

3.3.1.1 I²C Control

Using standard I²C control, the EFP01's energy mode can be set by writing the EM_STSEL bitfield in the EM_CRSREG_CTRL register. The EFP01's internal pull up resistors on I2C_SDA and I2C_SCL pins will continue to be enabled in EM2 and EM4 modes when using this method.

3.3.1.2 Direct Mode Control

In direct mode, the internal pull-ups on the I2C_SDA and I2C_SCL pins are disabled, and the pins become high-impedance inputs that the host processor can drive to quickly change energy modes.

Once enabled by setting the EM_DIRECTEN bit in the EM_CRISREG_CTRL register, direct mode allows the energy mode to be selected by driving the I2C_SDA and I2C_SCL pins according to [Table 3.9 Direct Mode Energy Mode States on page 23](#). When I2C_SCL and I2C_SDA enter the I²C Start Condition, direct mode is automatically disabled, and the EFP01 optionally enters EM0 if FORCE_EM0 = 1 in the EM_CRISREG_CTRL register.

Note: Use of Direct Mode is not recommended unless the host processor has dedicated hardware support for EFP01 (e.g., EFR32xG22 and later devices). Although Direct Mode state control can be bit-banged, there can be some undesirable side effects. For example, if the host processor receives a system reset (hard or soft) while in the Direct Mode EM0 or EM2 state, the host's I²C outputs can be disabled and can float to logic low levels (because the EFP01's internal pull-ups are disabled in Direct Mode). Because I2C_SCL = I2C_SDA = 0 is recognized by EFP01 as the EM4 state in Direct Mode, EFP01 disables its DCDC converters and LDO outputs and enters EM4 where it can only supply ~100 µA. This low current output is insufficient for a host processor to boot, resulting in an unusable state from which recovery is not possible without disconnecting and then reconnecting the power supply.

Note: Direct Mode is primarily intended for applications where the EFP01 is the only device on the I²C bus; other I²C devices may not tolerate the non-standard I²C states used by Direct Mode.

Table 3.9. Direct Mode Energy Mode States

| Direct Mode State | I2C_SCL Level | I2C_SDA Level | Allowed State Transitions |
|--|---------------|---------------|---|
| EM0 | 1 | 1 | <ul style="list-style-type: none"> EM2¹ I²C Start Condition |
| EM2 | 0 | 1 | <ul style="list-style-type: none"> EM0 EM4 |
| EM4 | 0 | 0 | <ul style="list-style-type: none"> EM2¹ |
| I ² C Start Condition | 1 | 0 | <ul style="list-style-type: none"> EM0² |
| <p>Note:</p> <ol style="list-style-type: none"> Direct mode transitions between EM0 and EM4 are not allowed. The system must briefly go through the EM2 state on EM4 exit or entrance. If the FORCE_EM0 bit in the EM_CRISREG_CTRL register is set, the internal device state will be set to EM0 automatically whenever the I²C start condition appears. | | | |

3.3.2 EM0

The EFP01 defaults to EM0 out of reset. In EM0, all features are enabled, and the maximum output current can be supported on any enabled DCDC converters.

3.3.3 EM2

Functionally, EM2 is very similar to EM0, with the proviso that in EM2 bias currents are reduced for improved efficiency at the expense of maximum supported output current.

DCDC A and DCDC B have independent peak current configuration bit fields for EM2 (in BB_IPK_EM2 and BK_IPK_EM2, respectively). In addition, the VOB output target voltage has its own independent configuration in EM2 (VOB_EM2_V).

DCDC B has an independent result register for storing the Coulomb counter result in EM2 (CCB2_MSBY/LSBY). However, DCDC A shares one set of registers for Coulomb counting in both EM0 and EM2. Because of this, DCDC A must should use the same peak current setting in both EM0 and EM2 in order for the Coulomb count to be accurate.

3.3.4 EM4

In EM4, the EFP01 disables all enabled DCDCs and LDOs, and enables any desired coarse regulators (i.e., those with their CRSREG_EN_x bits set in the EM_CRSREG_CTRL register). ADC voltage and temperature measurements are disabled in EM4. Coulomb counting is not supported in EM4.

While in EM4, the EFP01's registers can be read or written via I²C transactions, but the EFP01 will not generate any IRQs in EM4.

Several device configurations have restrictions on EM4 operation:

- In [Figure 4.4 Single-Cell Boost Configuration on page 33](#), EM4 is not supported at all.
- In [Figure 4.6 Boost Bootstrap Configuration on page 35](#), EM4 is supported only when the supply voltage > 2.5V

Note: Unless the host processor has dedicated EM4 hardware support for [3.3.1.2 Direct Mode Control](#), EM4 should not be used. Once the EFP01 is in EM4, it is only able to source 100 μ A per output, which may not be sufficient to power the host while it exits EM4 and sends the necessary I²C command to place the EFP01 in EM2 or EM0. Dedicated EFP01 EM4 hardware support is available on EFR32xG22 and later devices.

3.4 Measurement

3.4.1 Coulomb Counter

Note:

Refer to AN1188: EFP01 Coulomb Counting for a more detailed discussion of the Coulomb counter and example code.

The EFP01 has an integrated Coulomb counter that can losslessly measure the charge drawn from the battery for each DCDC and LDO.

Before normal operation can begin, the Coulomb counter must go through a calibration phase. Periodically, recalibration may be necessary due to changes in operating conditions (e.g., battery voltage or operating temperature).

3.4.1.1 Calibration

Overview

During calibration, a known internal current load is applied to the selected output, and the device counts the number of 10 MHz clock cycles required for a fixed number of pulse-frequency modulation (PFM) pulses to occur. The CC_CAL register CCL_SEL, CC_CAL_NREQ, and CCL_LVL fields respectively determine the output used (VOA, VOB, or VOC), the number of PFM pulses to count, and the current load applied to the output. The CCC_MSBY and CCC_LSBY registers are retasked during calibration to store the resulting number of 10 MHz clock cycles counted (note that only the CCC_MSBY and CCC_LSBY registers are used regardless of which output is being calibrated). Based on these results, the charge-per-pulse (CPP) can be determined.

After configuration, calibration is initiated by setting the CC_CAL_STRT bit in the CMD register. If enabled, the Coulomb counter should be disabled prior to calibration by setting writing a 0 to the CC_EN bit in the CC_CTRL register.

For accurate calibration, any devices or loads powered by the EFP01's outputs are expected to be in a stable, steady-state of operation during this calibration phase. In practice, occasional recalibration of the Coulomb counter is expected, particularly when either the input voltage or the temperature has changed significantly.

Factors Affecting the Charge-Per-Pulse

The charge-per-pulse (CPP) may vary depending on the operating mode of the converter. For example, if DCDC B is configured in buck with LDO mode (i.e., the converter automatically switches between buck and LDO modes depending on input voltage), the CPP when the converter is in buck can differ from the CPP when the converter is operating in LDO mode. For this reason, it may be necessary to calibrate a given DCDC converter in each of its expected operating modes. Thus if DCDC B is in buck with LDO mode, and the battery voltage is sufficiently close to the output voltage such that the converter may switch to LDO mode, calibration should be performed on DCDC B once in buck mode and again in LDO mode.

The current DCDC operating modes of DCDC A and DCDC B are reported by the CCA_MODE and CCB_MODE fields of the CC_MODE register, respectively. For calibration purposes, the operating modes can be temporarily forced using the BB_MODE and BK_MODE fields in the BB_CTRL3 and BK_CTRL1 registers for DCDC A and DCDC B, respectively. Host firmware is expected to maintain a CPP for each operating mode of the converter.

In addition, the energy mode can affect the charge-per-pulse. The VOB output has independent result registers for EM0 and EM2, and will need to be calibrated in each energy mode. The VOA and VOC outputs each have only a single result register pair used in both EM0 and EM2. If Coulomb Counting is used with VOA, the BB_IPK and BB_IPK_EM2 peak current values are expected to be the same to ensure an accurate count on VOA regardless of energy mode.

3.4.1.2 Recalibration

In addition, certain changes in external conditions may affect the charge-per-pulse. The below list contains conditions that may necessitate a recalibration event:

- Significant change in input supply voltage
- Significant change in temperature

3.4.1.3 Operation

Note:

Refer to AN1188: EFP01 Coulomb Counting for a more detailed discussion of the Coulomb counter and example code.

PFM pulse counts for the VOA, VOB (separately for EM0 and EM2), and VOC outputs are stored in the CCA_MSBY/CCA_LSBY (VOA), CCB0_MSBY/CCB_LSBY (VOB in EM0), CCB2_MSBY/CCB2_LSBY (VOB in EM2), and CCC_MSBY/CCC_LSBY (VOC) most significant/least significant byte register pairs, respectively, during normal operation. Note that when DCDC A is operating with LDO C in parallel, the resulting counts will be split between the CCA result registers (when the DCDC A is powering the load) and the CCC result registers (when LDO C is powering the load).

Prescaler

The actual value stored in a given Coulomb counter result register pair is scaled according to the CC_PRESCAL field in the CC_CTRL register. This setting applies globally such that the count in a given result register pair represents $2^{(16-2 \times \text{CC_PRESCAL})}$ PFM pulses. Note that the prescaler setting does not affect the CCC_MSBY/LSBY registers during calibration.

Enabling / Disabling

Start Coulomb counting by writing a 1 to the CC_EN bit in the CC_CTRL register; stop counting by writing a 0 to CC_EN.

Servicing

Once enabled, the Coulomb counter result registers will eventually overflow, so some amount of firmware maintenance is required. The CC_THRSH field in the CC_CTRL register sets the desired threshold (50%, 62.5%, 75%, or 87%) for setting the STATUS_G register CC_FULL flag. Note that the CC_FULL_UNMASK bit in the STATUS_GM register must be written to 1 so that an interrupt can be requested when the CC_FULL flag is set. When firmware receives an interrupt, and discovers that CC_FULL is set, all relevant Coulomb counter result registers should be read and added to local variable counts. Additionally, each converter's operating mode should be determined (by reading the CCA_MODE or CCB_MODE field in the CC_MODE register for DCDC A or DCDC B, respectively) in order to perform battery life calculations using the relevant CPP value. Clear the Coulomb counter result registers after reading them by writing a 1 to the CC_CLR bit in the CMD register.

3.4.2 Analog to Digital Converter (ADC)

An internal ADC can monitor the internal die temperature and the battery voltage. The battery voltage is determined by reading the voltage at either the VDDA or VDDDB pins of the device. The determination of which pin to read is made automatically by hardware - if a valid voltage is present on VDDA (e.g., `CC_MODE.SC_MODE==1`), VDDA will be measured; otherwise, VDDDB will be measured.

ADC Result Registers

The measured 12-bit ADC readings are automatically loaded into 8-bit register pairs, divided into the most significant nibble and the least significant byte. Because these ADC results are spread over two registers and the result may be continuously updated, addressing any of these ADC result registers causes an inhibition in the updating of the register to prevent corruption. To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.

There are three ADC voltage result register pairs and one ADC temperature result register pair, as described below:

- `VDD_AVG_MSN`, `VDD_AVG_LSBY`: These registers hold the 12-bit filtered average voltage reading. The IIR averaging low-pass filter time constant is set by the `ADC_CC_CTRL.ADC_IIR_TAU` bitfield (time constant = $2^{\text{ADC_IIR_TAU}}$). It is recommended to set `ADC_IIR_TAU = 7` to provide the slowest filtering.
- `VDD_MIN_MSN`, `VDD_MIN_LSBY`: These registers hold the 12-bit minimum voltage reading since the device was powered on or since the last `ADC_CLR` event.
- `VDD_MAX_MSN`, `VDD_MAX_LSBY`: These registers hold the 12-bit maximum voltage reading since the device was powered on, or since the last `ADC_CLR` event.
- `TEMP_MSN`, `TEMP_LSBY`: These registers hold the last 12-bit temperature reading.

When the `CMD.ADC_CLR` bit is set, on the next subsequent ADC trigger (whether manual or automatic), all three of the ADC result register pairs will be set to the same read value.

ADC Triggering

Each ADC triggering will cause a reading of both the voltage and temperature. The ADC readings can be triggered manually or automatically:

- The `CMD.ADC_START` bit can be set to manually trigger an ADC reading.
- The ADC can be configured to trigger automatically based off the number of counted pulse events in all enabled converters by configuring `ADC_CC_CTRL.ADC_INTERVAL`. If `ADC_INTERVAL > 0`, the rate of automatic ADC readings is determined by the number of counted pulse events ($2^{(\text{ADC_INTERVAL} + 3)}$). Note in certain scenarios (e.g., EM2 with very light loading) it is possible to have very long periods of time with few or no pulse events. For that reason, whenever `ADC_INTERVAL > 0`, the ADC readings will be updated at a minimum period of four refresh cycles (approximately ~400 msec at room temperature), regardless of the number of counted pulse events. It is recommended to set `ADC_INTERVAL=7`.
- If `ADC_CC_CTRL.ADC_INTERVAL = 0`, no automatic ADC readings will occur.

Because the ADC has multiple uses (both internally and at the application level) and ADC readings consume very little power, it is recommended to always set `ADC_INTERVAL=7` to ensure that ADC readings are always triggered periodically automatically. Some of the uses of the ADC include the following:

- If `BB_CTRL2.BB_IPK_NOADJ=0`, the ADC is used internally to adjust the boost converter peak current as the battery voltage drops, providing a near-constant output load current over the entire battery range.
- The ADC is used to determine whether a Low Battery Fault (`STATUS_G.VDD_LOW`) has occurred. The threshold for a Low Battery Fault is set in `ADC_LIMITS.ADC_V_LIM`.
- The battery voltage reading is used to determine the charge per pulse during Coulomb counting.
- The ADC temperature readings are used to optimize the internal bias refresh rate over temperature and to determine whether an Over Temperature Fault (`STATUS_G.TEMP_FAULT`) has occurred (where the threshold for the Over Temperature condition is set by `ADC_LIMITS.ADC_T_LIM`).

If enabled (i.e., `ADC_CC_CTRL.ADC_INTERVAL > 0`), the ADC will continue to take measurements in EM0 and EM2 energy modes. In EM4, the ADC will be automatically disabled and no measurement updates will occur.

ADC Calculations

To convert from the result register values to usable units:

- $\text{VDDDB (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.49$
- $\text{VDDA (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.01$
- $\text{Temperature (C)} = 40 + (\text{convert_from_2s_complement}((\text{TEMP_MSN} \ll 8) + \text{TEMP_LSBY}) + 2) / 6.04236$

3.5 Memory

3.5.1 OTP

The EFP01 contains OTP memory that is programmed at the factory to load calibration constants and configuration defaults into the registers. The default configuration may be modified after power-up by overwriting the corresponding register via I²C write. Additionally, any OTP address can be directly read through register I²C accesses.

The out-of-reset default OTP configuration can be restored by three methods:

1. A VDDA/VDDDB/VBOOST power-cycle, resulting in a [POR](#)
2. Setting the CMD.OTP_REREAD bit. This will cause the EFP01 registers to be overwritten with the OTP defaults.
3. Setting the CMD.RESET bit. This will cause the EFP01 registers to be momentarily cleared to 0, and then overwritten with the OTP defaults.

Note: When the converter mode bitfields are cleared to 0, any enabled converters or LDOs will be disabled for ~400us, which can result in a supply brown-out. For this reason, use of CMD.OTP_REREAD is recommended instead.

Note: When the EFP01 DCDC B is powering the EFR32 DECOUPLE supply, the out-of-reset mode for DCDC B is Disabled. If the EFR32 is not also getting reset, the EFR32 internal LDO must be re-enabled before resetting the OTP to its default values.

Refer to the [OTP Definition](#) section for more details and default OTP programming.

3.5.2 Registers

The EFP01 is controlled and configured via access to its Registers. Register access is supported in all of EFP01's energy modes (i.e., EM0, EM2, and EM4).

Default configuration and calibration register values are automatically loaded from OTP at boot (see [7.2 OTP Defaults](#)).

Refer to the [Register Definitions](#) section for more details.

3.6 Communications and Other Digital Peripherals

3.6.1 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the EFP01 and the host MCU. It is capable of operating in I²C secondary/device mode only, with transmission rates from 10 kbit/s up to 5 Mbit/s, and can function in EM0, EM2, and EM4. The EFP01 uses a fixed I²C address of 0x60.

The I²C module has internal pull ups on its SDA and SCL pins that are enabled automatically at startup. These internal pull ups can be disabled using the I2C_PU bit in the I2C_CTRL register.

In addition, the I²C module provides an optional, non-standard Direct Mode feature to allow fast transitions between Energy Modes (described in [3.3.1 Energy Mode Control](#)). EFP01's internal pull ups are automatically disabled when Direct Mode is enabled.

Note: Direct Mode is primarily intended for applications where the EFP01 is the only device on the I²C bus - other I²C devices may not tolerate the non-standard I²C states used by Direct Mode.

3.6.2 Interrupt Output (IRQ)

The EFP01 has an open-drain Interrupt Output (IRQ) that can be used to notify the host processor. Out of reset, an internal pull-up will be enabled on the IRQ pin - this pull-up will always remain enabled and cannot be disabled.

An IRQ will be generated whenever both of the following conditions are true:

- A status flag is set in either the STATUS_G or STATUS_V registers
- The flag's corresponding UNMASK bit in either the STATUS_GM or STATUS_VM registers is also set to one.

When an IRQ is generated, the IRQ pin will be driven low until any flags that are both unmasked and set are cleared.

By default, only the STATUS_GM.OTP_READ_UNMASK bit is set, which results in an IRQ whenever the OTP is read. Because the OTP is read on every EFP01 power-up and/or reset, the host firmware can use this OTP_READ flag and resulting IRQ as an indication that an unexpected reset condition has occurred on the EFP01, and that any post-startup configuration needs to be rewritten to its registers.

3.7 System Protection

3.7.1 Under-voltage Lockout (UVLO)

When the VDDDB voltage falls below the UVLO trip point (consult Electrical Specifications table for the typical value), the EFP01 automatically transitions to an extremely low-power state to minimize power consumption. In this state, only the Power-On Reset (POR) is enabled.

3.7.2 Power-on Reset (POR)

When the VDDDB voltage rises above the Rising POR threshold (consult Electrical Specifications table), the EFP01 automatically loads its OTP programmed defaults into the corresponding registers, at which point any enabled converters will begin regulation. If the VDDDB voltage falls below the Falling POR threshold, the EFP01 will go into reset and all outputs will be disabled.

3.7.3 Over-Voltage Protection

By default in EM0 and EM2 modes, each output has overvoltage protection enabled. When the output voltage on a specific converter is more than ~180 mV higher than the programmed value, an internal ~2 mA load is enabled on the output until the overvoltage condition clears. This feature can be disabled on the VOB output by setting the BK_CTRL0.BK_DIS_OV_PROT bit.

In OPNs where DCDC B is providing an output that must stay between 1.1 V to 1.2 V, the coarse regulator cannot be enabled in EM4 (as the coarse LDO output can be much higher than 1.2 V). To ensure the supply voltage in EM4 does not increase beyond an acceptable level due to leakage, a simple voltage clamp can be enabled on the VOB output by setting the BK_CTRL0.CLAMPB bit.

3.7.4 Short Circuit Tolerance

The PFM operation of the DCDC converters along with the programmable peak current limit provide some inherent protection against an output short circuit. In the buck or buck/boost configuration, any output short condition will result in that DCDC output dropping out of regulation, with a maximum output current that is approximately $IPK_BASE/2$ (where IPK_BASE is defined for DCDC A in [3.2.1.2 Peak Current Configuration](#) and DCDC B in [3.2.2.2 Peak Current Configuration](#)).

Similarly, LDO C and LDO B under an output short condition are limited to the configured maximum output current (as defined in [3.2.3.3 Maximum Output Current](#)).

Note: Depending on the converter programming, an output short circuit condition for either the DCDC or the LDO output current may still result in an unacceptable rise in on-die temperature. To minimize on-die temperature rise, the PCB designer should maximize thermal connections from the package to the PCB ground planes to optimize heat flow from the package and minimize the θ_{JA} .

Note: There is no inherent output short circuit protection for DCDC A when it is configured in wired boost mode as described in the [4.1.5 Wired Boost Configuration \(EFP0109 & EFP0110\)](#), [4.1.4 Single-Cell Boost Configuration \(EFP0108\)](#), or [4.1.6 Boost Bootstrap Configuration \(EFP0111\)](#). Shorting the VOA output to ground in one of these configurations will result in an uncontrolled battery discharge through the body diode in the boost powertrain PFET. The current, in this case, is limited only by the system impedances, such as the internal body diode resistance, the inductor resistance, and the battery internal resistance. Any desired short circuit protection for wired boost modes must be implemented in external circuitry.

Firmware can detect and manage an output short condition through the following mechanisms:

- An output short should cause the output to drop out of regulation, resulting in the corresponding VOx_ISLOW flag being set in the $STATUS_V$ register.
- In the worst case, where the output short current has resulted in excessive on-chip power dissipation, the $TEMP_FAULT$ flag in the $STATUS_G$ register will be set to indicate an over temperature condition.

It is recommended that firmware unmask these bits in the $STATUS_VM$ and $STATUS_GM$ registers at start-up so that they can generate interrupt requests. Firmware can then respond appropriately to the VOx_ISLOW and/or $TEMP_FAULT$ condition(s), e.g. by lowering the peak current or $LDOx_IGAIN$ setting, increasing the inrush current limit, or disabling the output altogether.

3.8 Startup & Shutdown Behavior

3.8.1 Startup Behavior

Once enabled, the EFP01's DCDC and LDO outputs will immediately begin switching to ramp up to the target output voltage without any soft-start mechanisms (besides the current limit, if enabled, for [DCDC A](#) or [DCDC B](#)).

3.8.2 Shutdown Behavior

The outputs of all disabled DCDCs and LDOs are held in a high-impedance state. Note that if an output was first enabled, and then disabled, the original output voltage may be retained by the output capacitor(s) for a long period of time depending on output load current.

When the DCDC A converter is disabled on devices configured for the Wired Boost, Single-Cell Boost, or Boost Bootstrap configurations, the body diode in the boost powertrain becomes forward-biased once the VOA output voltage drops below the battery voltage. In these configurations, the VOA output (less a diode drop) tracks the battery voltage when DCDC A is disabled.

4.1.2 Wired Buck with LDO C Configuration (EFP0103 & EFP0104)

The wired buck with LDO configuration is targeted at batteries with a nominal voltage above 2.5V where the input voltage may approach the buck converter output voltage. In this mode, DCDC A bucks the supply voltage to a lower voltage until the supply voltage approaches the VOA output voltage. At that point, the converter dynamically switches to use the LDO instead to power the VOA output. Note that in this mode, LDO C is wired in parallel with the VOA output, and thus not available as an independent LDO.

The wired buck with LDO configuration is suitable for a wide range of batteries and input supplies. For example:

- Single lithium (Li/MnO₂) CR2032 coin-cells (1.8 to 3.2V)
- Single lithium thionyl chloride (Li/SOCl₂) primary cell (3.0 to 3.65V)
- Single li-ion/li-polymer (typically LiCoO₂) rechargeable batteries (2.7 to 4.35V)
- Single lithium iron phosphate (LiFePO₄) rechargeable battery (2.5 to 3.65V)
- Line power / USB ($\leq 5.5V$)

The supported operating mode settings for each converter in this configuration are shown below:

Table 4.2. Supported Operating Mode Settings

| Converter / LDO | Operating Mode Bitfield | Supported Modes |
|-----------------|-------------------------|---|
| DCDC A | BB_CTRL3.BB_MODE | WiredBuckLDO |
| DCDC B | BK_CTRL1.BK_MODE | Disabled, BuckOnly, BuckLDO, or LDOOnly |
| LDO C | LDOC_CTRL.LDOC_ENA_SA | Disabled |

Typical power supply connections for a wired buck with LDO configuration are show in the following figure.

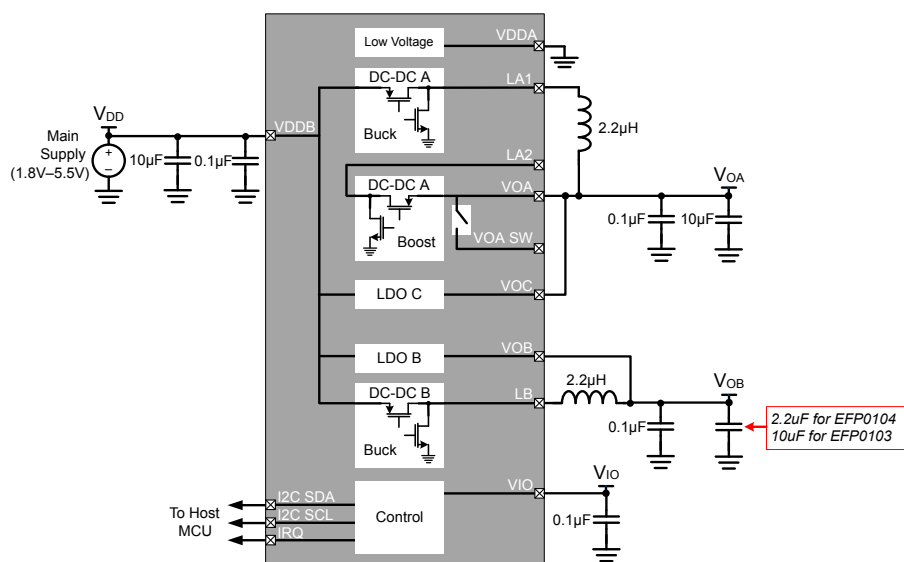


Figure 4.2. Wired Buck with LDO C Configuration

4.1.3 Buck/Boost Configuration (EFP0106 & EFP0107)

The buck/boost configuration is suitable for applications where the battery voltage may be above or below the required VOA output voltage. Although very flexible, this configuration has worse efficiency than wired boost or wired buck configurations due to the losses in the additional power FETs required to support both modes of operation. Typical power supply connections for a buck/boost configuration are shown in the following figure.

The supported operating mode settings for each converter in this configuration are shown below:

Table 4.3. Supported Operating Mode Settings

| Converter / LDO | Operating Mode Bitfield | Supported Modes |
|-----------------|-------------------------|---|
| DCDC A | BB_CTRL3.BB_MODE | Autonomous (ForceBuck, ForceBoost, ForceNTM can be used in special circumstances) |
| DCDC B | BK_CTRL1.BK_MODE | Disabled, BuckOnly, BuckLDO, or LDOOnly |
| LDO C | LDOC_CTRL.LDOC_ENA_SA | Enabled or Disabled |

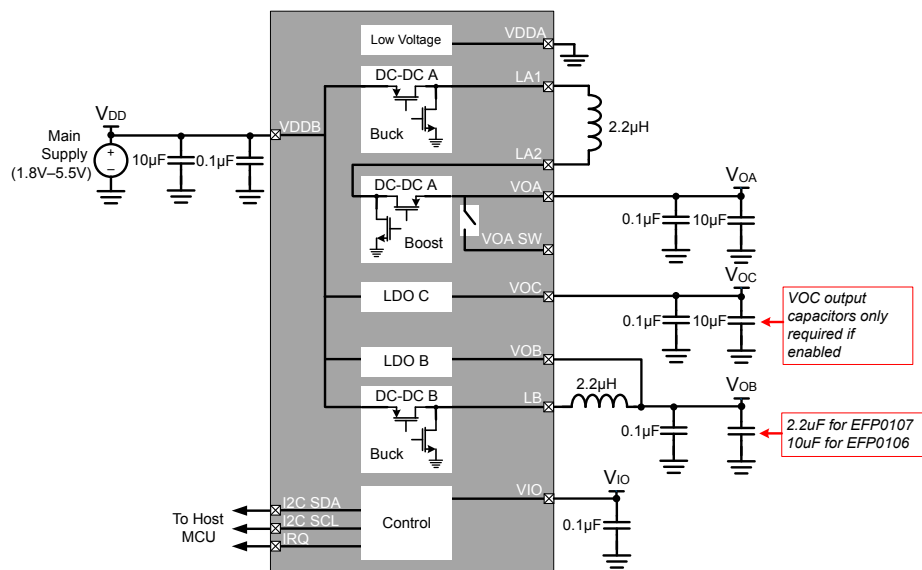


Figure 4.3. Buck/Boost Configuration

4.1.4 Single-Cell Boost Configuration (EFP0108)

The single-cell boost configuration is a variant of the wired boost configuration intended primarily for use cases where the battery nominal voltage may be below the VDDB pin minimum voltage (1.8V) at startup. In this configuration, the EFP01 uses low-voltage supply circuitry powered from the VDDA pin at startup to generate a voltage output on the VOA supply sufficient to meet the VDDB minimum supply input requirement. After startup and once the VDDB voltage is above this minimum, standard boost operation resumes. Note that this configuration requires connecting VDDB to VOA on the printed circuit board.

Single-cell boost configuration is suitable for the following:

- Single alkaline (Zn/MnO₂), zinc-carbon or lithium iron-disulfide (Li/FeS₂) primary cells, or NiMH/NiCd rechargeable cells (0.8 to 1.8 V)

The supported operating mode settings for each converter in this configuration are shown below:

Table 4.4. Supported Operating Mode Settings

| Converter / LDO | Operating Mode Bitfield | Supported Modes |
|-----------------|-------------------------|---|
| DCDC A | BB_CTRL3.BB_MODE | WiredBoost |
| DCDC B | BK_CTRL1.BK_MODE | Disabled, BuckOnly, BuckLDO, or LDOOnly |
| LDO C | LDOC_CTRL.LDOC_ENA_SA | Enabled or Disabled |

In the single-cell boost configuration, up to 3 outputs are available. Typical power supply connections for a single-cell boost configuration are shown below.

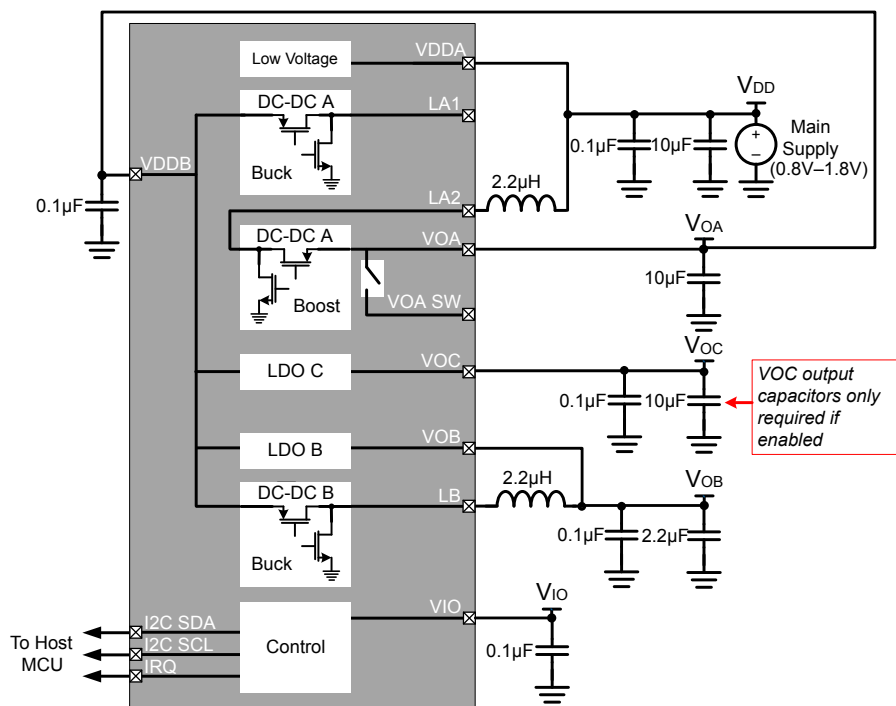


Figure 4.4. Single-Cell Boost Configuration

4.1.5 Wired Boost Configuration (EFP0109 & EFP0110)

Wired boost configuration is suitable for a wide range of batteries. For example:

- Dual alkaline, zinc-carbon or lithium iron-disulfide (Li/FeS₂) primary cells, or NiMH/NiCd rechargeable cells (1.6 to 3.6V)
- Single lithium primary Li/MnO₂ cells (1.8 to 3.2V)
- Single lithium iron phosphate (LiFePO₄) rechargeable battery (2.5 to 3.65V)

The supported operating mode settings for each converter in this configuration are shown below:

Table 4.5. Supported Operating Mode Settings

| Converter / LDO | Operating Mode Bitfield | Supported Modes |
|-----------------|-------------------------|---|
| DCDC A | BB_CTRL3.BB_MODE | WiredBoost |
| DCDC B | BK_CTRL1.BK_MODE | Disabled, BuckOnly, BuckLDO, or LDOOnly |
| LDO C | LDOC_CTRL.LDOC_ENA_SA | Enabled or Disabled |

In the wired boost configuration, up to 3 outputs are available. Typical power supply connections for a wired boost configuration are shown below.

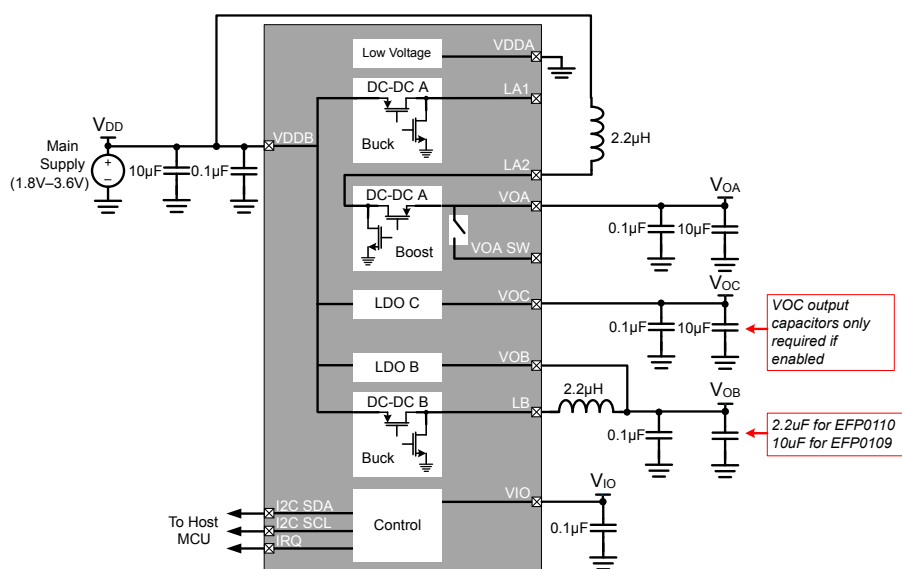


Figure 4.5. Wired Boost Configuration

4.1.6 Boost Bootstrap Configuration (EFP0111)

The boost bootstrap configuration is a variant of the wired boost configuration intended primarily to support high impedance batteries, such as CR2032 lithium coin cells. DCDC A is configured for wired boost with the VOA output voltage set to a high value (e.g., 5.2V), which in turn is used to supply the VDDB input to DCDC B and LDO C.

Inrush current limiting is enabled by default for DCDC A in order to reduce the impact of the battery's internal impedance. However, due to the reduced current, the VOA output is poorly regulated and is expected to droop under heavy load. To compensate, a larger reservoir output capacitor ($\geq 68 \mu\text{F}$) is used to help maintain the VOA output. The actual VOA output capacitor size may need to be adjusted based on the peak output current and duty cycle of the specific application.

The boost bootstrap configuration is suitable for:

- Single lithium (Li/MnO₂) CR2032 coin-cells (1.8 to 3.2V)
- Dual alkaline, zinc-carbon or lithium iron-disulfide (Li/FeS₂) primary cells, or NiMH/NiCd rechargeable cells (1.6 to 3.6V)
- Single lithium iron phosphate (LiFePO₄) rechargeable battery (2.5 to 3.65V)

The supported operating mode settings for each converter in this configuration are shown below:

Table 4.6. Supported Operating Mode Settings

| Converter / LDO | Operating Mode Bitfield | Supported Modes |
|-----------------|-------------------------|---|
| DCDC A | BB_CTRL3.BB_MODE | WiredBoost |
| DCDC B | BK_CTRL1.BK_MODE | Disabled, BuckOnly, BuckLDO, or LDOOnly |
| LDO C | LDOC_CTRL.LDOC_ENA_SA | Enabled or Disabled |

Typical power supply connections for the boost bootstrap configuration are shown below.

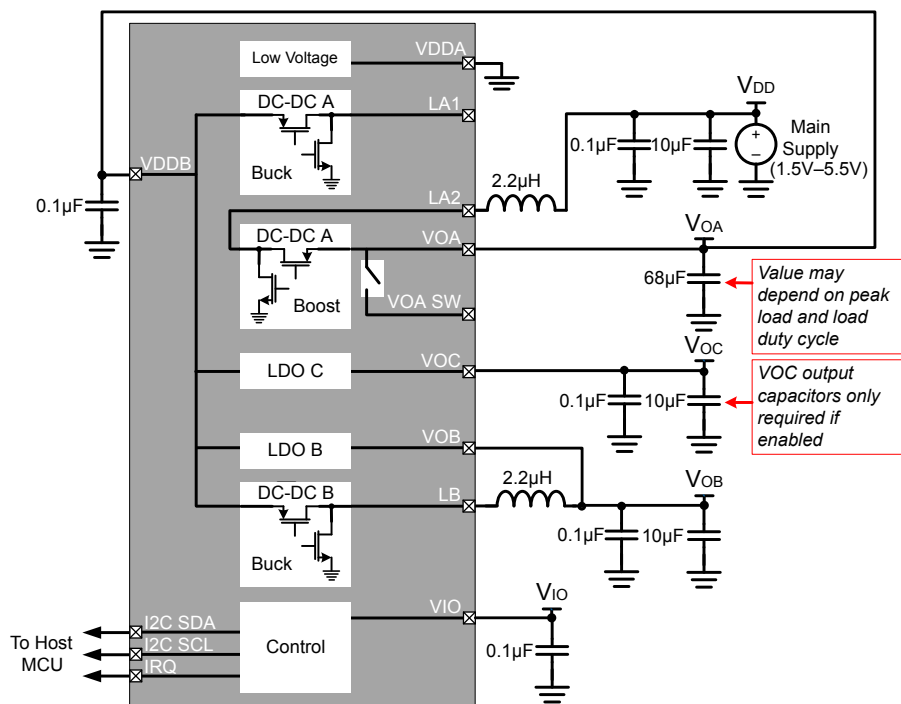


Figure 4.6. Boost Bootstrap Configuration

5. Electrical Specifications

5.1 Electrical Characteristics

Unless stated otherwise, all electrical parameters in all tables are specified under the following conditions:

- Typical values are based on $T_J=25\text{ }^\circ\text{C}$ and $V_{\text{DDB}}=V_{\text{IO}}=3.3\text{V}$ and $V_{\text{OA}}=V_{\text{OB}}=V_{\text{OC}}=1.8\text{V}$, by production test and/or technology characterization.
- Unless stated otherwise, minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature.
- Energy mode (EM0/EM2/EM4) programming is defined in [Table 3.8 Energy Modes Overview on page 22](#)
 - EM0: BIAS_SW.BIAS0=7, EM_CRSREG_CTRL.EM_STSEL=0
 - EM2: BIAS_SW.BIAS2=1, EM_CRSREG_CTRL.EM_STSEL=2
 - EM4: EM_CRSREG_CTRL.EM_STSEL=3
- Test board components:
 - $L_{\text{DCDC}} = 2.2\text{ }\mu\text{H}$ (Samsung CIG22H2R2MAE)
 - $C_{\text{IN}} = C_{\text{OUT}} = 10\text{ }\mu\text{F}$ (Murata GRM31CR71A106KA01)

5.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <https://www.silabs.com/about-us/corporate-responsibility/commitment-to-quality>.

Table 5.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------|--|------|-----|-----------------------|------|
| Storage temperature range | T _{STG} | | -50 | — | 150 | °C |
| DC voltage on input supply pins VDDA ¹ | V _{VDDA} | | -0.3 | — | 2.0 | V |
| DC voltage on input supply pins VDDB ¹ | V _{VDDB_DC} | | -0.3 | — | 5.5 | V |
| Transient voltage on input supply pin VDDB ¹ | V _{VDDB_TRN} | t < 30 μs, duty cycle < 0.01% | — | — | 6.5 | V |
| DC voltage connected through inductor to LA2 pin in boost configurations. ¹ | V _{VBOOST} | | -0.3 | — | 5.5 | V |
| Voltage on output supply pins: VOA, VOB, VOC, VOA_SW | V _{OUT} | | -0.3 | — | 5.5 | V |
| DC voltage on VIO supply pin | V _{VIO} | | -0.3 | — | 5.5 | V |
| DC voltage on any I/O pin | V _{DIGPIN} | | -0.3 | — | V _{VIO} +0.3 | V |
| On-chip power dissipation ² | P _{DIS} | 2-layer PCB, THETA _{JA} = 81.2 °C/W, T _{AMBIENT} = 25 °C | — | — | 923 | mW |
| | | 4-layer PCB, THETA _{JA} = 66.0 °C/W, T _{AMBIENT} = 25 °C | — | — | 1136 | mW |
| Operating Junction temperature | T _J | -G grade devices | -40 | — | 105 | °C |

Note:

- Note that there is no reverse battery insertion protection implemented on-chip. Applications that may be susceptible to a reverse battery insertion should incorporate external protection circuitry.
- Max on-chip power dissipation is given by: $P_{MAX} = (100\text{ °C} - T_{AMBIENT}) / THETA_{JA}$

5.1.2 Thermal Characteristics

Table 5.2. Thermal Characteristic

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|--|-----|------|-----|------|
| Thermal impedance, junction-to-ambient QFN20 (3x3mm) | THETA _{JA} | 2 layer PCB, Natural Convection ¹ | — | 81.2 | — | °C/W |
| | | 4 layer PCB, Natural Convection ¹ | — | 66.0 | — | °C/W |
| Thermal impedance, junction-to-board QFN20 (3x3mm) | THETA _{JB} | 2 layer PCB, Natural Convection ¹ | — | 37.9 | — | °C/W |
| | | 4 layer PCB, Natural Convection ¹ | — | 27 | — | °C/W |
| Thermal impedance, junction-to-case QFN20 (3x3mm) | THETA _{JC} | 2 layer PCB, Natural Convection ¹ | — | 46.5 | — | °C/W |
| | | 4 layer PCB, Natural Convection ¹ | — | 34.6 | — | °C/W |
| Junction-to-top thermal characterization parameter QFN20 (3x3mm) | PSI _{JT} | 2 layer PCB, Natural Convection ¹ | — | 2.6 | — | °C/W |
| | | 4 layer PCB, Natural Convection ¹ | — | 1.9 | — | °C/W |
| Junction-to-bottom thermal characterization parameter QFN20 (3x3mm) | PSI _{JB} | 2 layer PCB, Natural Convection ¹ | — | 39.1 | — | °C/W |
| | | 4 layer PCB, Natural Convection ¹ | — | 26.7 | — | °C/W |

Note:

1. Measured according to JEDEC standard JESD51-2A Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).

5.1.3 General Operating Conditions

5.1.3.1 Power Supply Dependencies

Due to on-chip circuitry (e.g., diodes), some device power supply pins have a dependent relationship with other power supply pins. These internal relationships between the external voltages applied to the various device supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VDDB, VDDA, VBOOST (where VBOOST is the voltage applied to the inductor attached to the LA2 pin in boost configurations): No dependency with each other.
- VIO: If the EFP01 is powered on (i.e., VDDB and/or VDDA powered), VIO should also be powered. When VIO is unpowered, the system may see several hundred microamps of leakage current.

5.1.3.2 General Operating Conditions

Table 5.3. General Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------|---|-----|------|----------------|------|
| Operating junction temperature | T_J | -G grade devices | -40 | — | 100 | °C |
| VIO input voltage range | V_{IOIN} | | 1.7 | — | 5.5 | V |
| Quiescent current into VDDA pin | I_{Q_VDDA} | EM0, VDDA=1.8V | — | 24 | 670 | nA |
| | | EM2, VDDA=1.8V | — | 24 | 670 | nA |
| Quiescent current into VDDB pin ¹ | I_{Q_VDDB} | EM4, all coarse regulators enabled | — | 57 | 2060 | nA |
| | | EM0, 1 output enabled | — | 800 | 13080 | nA |
| | | EM2, 1 output enabled | — | 300 | 12140 | nA |
| | | EM0, 2 outputs enabled | — | 1400 | 16450 | nA |
| | | EM2, 2 outputs enabled | — | 425 | 14820 | nA |
| | | EM0, 3 outputs enabled | — | 2000 | 16940 | nA |
| | | EM2, 3 outputs enabled | — | 525 | 15080 | nA |
| Bootup time from VDDB rising above POR threshold until device ready to receive I2C commands | T_{BOOT} | | — | 1200 | — | μs |
| Time from EM2 to EM0 | T_{EM2_EM0} | Time from EM2 exit until DCDC enters EM0 mode (i.e, EM0 BIAS, IPK, and voltage target settings are applied, but the output voltage target may still be transitioning if there was a voltage target change from EM2 to EM0). | — | 0.2 | — | μs |
| | | Time from EM2 exit until DCDC enters EM0 mode and EM0 output target voltage is reached. Buck Mode, $C_{OUT} = 2.2 \mu F$, $VOB_EM2 = 1.0 V$, $VOB_EM0 = 1.2 V$, $BK_IPK = 16$, $VDDB = 3.0 V$ | — | 4 | — | μs |
| Time from EM4 to EM2 | T_{EM4_EM2} | Time from EM4 exit until until DCDC begins switching in EM2 mode. During this period, no additional load should be applied to the DCDC output | — | 50 | — | μs |
| | | Time from EM4 exit until DCDC begins switching in EM2 mode and output target voltage is reached. Buck Mode, $C_{OUT} = 10 \mu F$, $VDDB = 3.0 V$, $VOA_V = 2.8 V$, $BB_IPK_EM2 = 4$ | — | 125 | — | μs |
| Digital IO internal pull-up resistor | R_{PU} | I2C SDA, I2C SCL, and IRQn | — | 3.7 | — | kΩ |
| Digital output low voltage | V_{OL} | | — | — | $V_{IO} * 0.3$ | V |

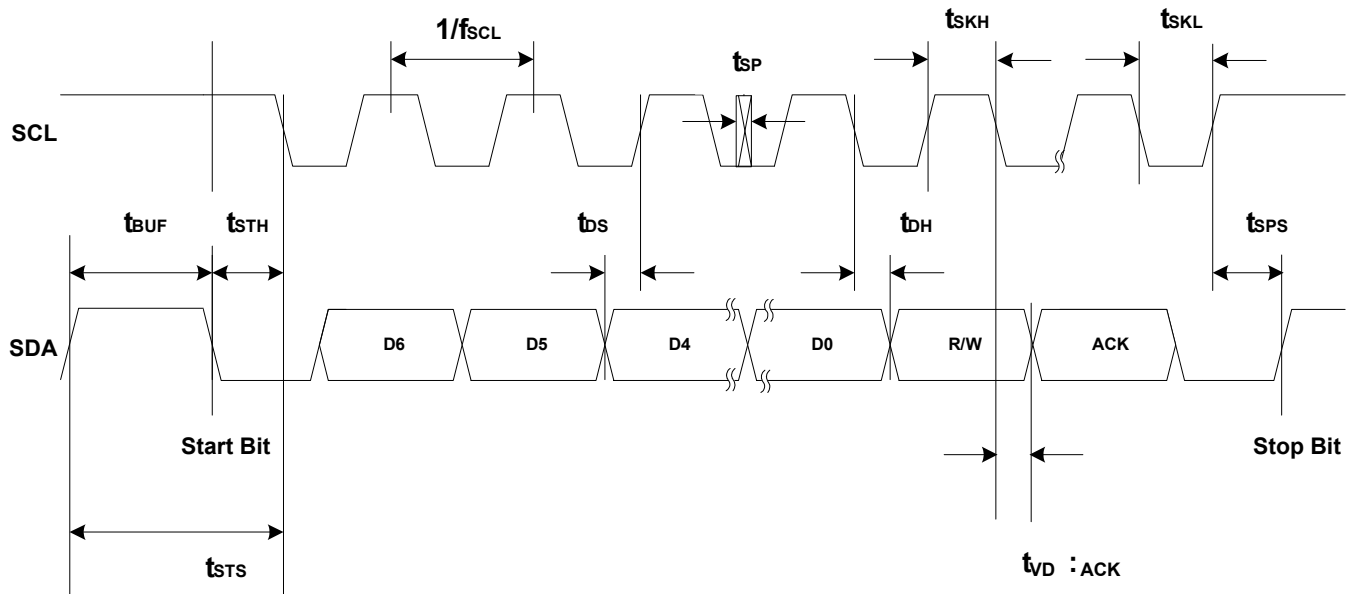
| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------------|---|----------------------|--------|----------------------|------|
| Digital input low voltage | V _{IL} | | — | — | V _{IO} *0.3 | V |
| Digital input high voltage | V _{IH} | | V _{IO} *0.7 | — | — | V |
| Nominal input capacitor ² | C _{IN} | VDDA / VDDDB / VBOOST inputs, 25% tolerance | 4.7 | 10 | — | μF |
| Nominal output capacitor ² | C _{OUT} | VOA / VOB / VOC outputs, 25% tolerance | 2.2 | 10 | — | μF |
| VDDDB internal measurement accuracy | VDDDB _{MEAS_ACC} | | — | -0.112 | — | LSB |
| VDDA internal measurement accuracy | VDDA _{MEAS_ACC} | | — | -0.02 | — | LSB |
| Temperature measurement accuracy | TEMP _{MEAS_ACC} | | — | +/- 10 | — | °C |
| ADC measurement conversion time for one voltage and one temperature sample | T _{MEAS} | | — | 18.6 | — | μs |
| Power-on reset threshold, rising | V _{POR_THR_RIS} | | — | — | 1.702 | V |
| Power-on reset threshold, falling | V _{POR_THR_FAL} | | 1.58 | — | 1.68 | V |
| Under-voltage lockout threshold | V _{UVLO_THR} | | — | 1.2 | — | V |
| VDDDB current when VDDDB < UVLO threshold | I _{UVLO} | VDDDB = 1.0V | — | 24 | — | nA |
| On resistance of DCDC A buck powertrain NMOS FET ³ | R _{DSA_BUCK_NMOS} | VDDDB = 3.3V | — | 0.271 | 1.07 | Ω |
| On resistance of DCDC A buck powertrain PMOS FET ³ | R _{DSA_BUCK_P MOS} | VDDDB = 3.3V | — | 0.150 | 0.676 | Ω |
| On resistance of DCDC A boost powertrain NMOS FET ³ | R _{DSA_BOOST_N MOS} | VDDDB = VOA = 3.3V | — | 0.140 | 0.450 | Ω |
| On resistance of DCDC A boost powertrain PMOS FET ³ | R _{DSA_BOOST_P MOS} | VDDDB = VOA = 3.3V | — | 0.172 | 0.645 | Ω |
| On resistance of DCDC B buck powertrain NMOS FET ³ | R _{DSB_BUCK_NMOS} | VDDDB = 3.3V | — | 0.203 | 0.783 | Ω |
| On resistance of DCDC B buck powertrain PMOS FET ³ | R _{DSB_BUCK_P MOS} | VDDDB = 3.3V | — | 0.294 | 1.26 | Ω |
| On resistance of LDO B in bypass mode ³ | R _{DSB_LDO_BYP} | VDDDB = 3.0V | — | 0.778 | 1.32 | Ω |
| | | VDDDB = 1.8V | — | 1.19 | 1.96 | Ω |
| On resistance of LDO C in bypass mode ³ | R _{SDC_LDO_BYP} | VDDDB = 3.0V | — | 0.76 | 1.32 | Ω |
| | | VDDDB = 1.8V | — | 1.19 | 1.96 | Ω |
| On resistance of VOA switch ³ | R _{DSVSW} | VDDDB = 3.0V | — | 1.38 | 2.91 | Ω |
| | | VDDDB = 1.8V | — | 2.2 | 4.14 | Ω |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| Note: <ol style="list-style-type: none">1. In boost bootstrap and single-cell boost configurations, the VDDDB input is attached to the VOA output. Therefore, the quiescent current at the battery will be the VDDDB quiescent current as seen through the DCDC A conversion.2. The system designer should consult the characteristic specs of the capacitor used to ensure its capacitance value stays within the specified bounds across temperature and DC bias.3. Maximum values guaranteed by characterization. | | | | | | |

Table 5.4. I2C Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------|--|---------------------|-----|------|---------------|
| Hysteresis | V_{HYS} | High-to-low versus low-to-high transition | $V_{IO} \cdot 0.05$ | — | — | V |
| SCL Frequency | f_{SCL} | EFP01 is one of multiple peripherals on I2C bus, $C_{LOAD} \leq 25\text{pF}$ | — | — | 400 | kHz |
| | | EFP01 is sole peripheral on I2C bus, $C_{LOAD} \leq 25\text{pF}$ | — | — | 1000 | kHz |
| SCL High Time | t_{SKH} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 0.6 | — | — | μs |
| SCL Low Time | t_{SKL} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 1.3 | — | — | μs |
| Start Hold Time | t_{STH} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 0.6 | — | — | μs |
| Start Setup Time | t_{STS} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 0.6 | — | — | μs |
| Stop Setup Time | t_{SPS} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 0.6 | — | — | μs |
| Bus Free Time | t_{BUF} | Between Stop and Start, $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 1.3 | — | — | μs |
| SDA Setup Time | t_{DS} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 100 | — | — | ns |
| SDA Hold Time | t_{DH} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 100 | — | — | ns |
| SDA Valid Time | t_{VD_DAT} | From SCL low to data valid, $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | — | — | 0.9 | μs |
| SDA ACK Valid Time | t_{VD_ACK} | From SCL low to data valid, $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | — | — | 0.9 | μs |
| Suppressed Pulse Width (pulses up to and including this duration will be suppressed) | t_{SPW} | $f_{SCL} = 400\text{ kHz}$, $C_{LOAD} = 25\text{ pF}$ | 50 | — | — | ns |

Figure 5.1. I2C Interface Timing



5.1.3.3 EFP0101 / EFP0102

Note: EFP0101 & EFP0102 are nearly identical devices, differing primarily in the VOB configuration at and after startup:

- On EFP0101, the VOB converter output is enabled to 1.858 V at startup and may be programmed after startup in the range 0.8V to 3.3V
- On EFP0102, the VOB converter output is disabled by default, and may be programmed after startup to an output in the range 0.8V to 1.26V

Unless stated otherwise, all parameters in the EFP0101 & EFP0102 electrical specifications tables are specified under the following conditions:

- VDDDB = 3.3 V
- VDDA = GND
- VOA = 1.8 V
- VOB = 1.2 V (EFP0102) / 1.8 V (EFP0101)
- VOC = 1.8 V
- VIO = 1.8 V

Table 5.5. EFP0101/EFP0102 VOA Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|------|------|-----------------|-------|
| Allowed programmable peak current setting | IPK _{ADJ_RANGE} | Buck, EM0, BB_IPK setting | 0 | — | 31 | |
| | | Buck, EM2, BB_IPK_EM2 setting | 0 | — | 7 | |
| VDDB input voltage range | V _{VDDB} | Wired buck, input supply connected to VDDB pin | 1.8 | — | 5.5 | V |
| VDDA input voltage range | V _{VDDA} | Low-voltage circuitry unused | — | GND | — | V |
| Output programmable voltage range | V _{VOA_RANGE} | EFP0101 / EFP0102 | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOA} | EFP0101 / EFP0102 | — | 1.86 | — | V |
| Output load current ¹ | I _{LOAD_MAX} | Wired buck, BB_IPK = 31, EM0, VDDB - VOA > 660 mV, TON_MAX=7 ^{2,3} | 150 | — | — | mA |
| | | Wired buck, BB_IPK_EM2 = 7, EM2, VDDB - VOA > 660 mV, TON_MAX = 7 ^{2,3} | 20 | — | — | mA |
| Output voltage accuracy | V _{VOA_ACC} | Buck, EM0, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA ³ | — | 1.41 | 77.6 | mV |
| | | Buck, EM2, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA ³ | — | 6.8 | 94.7 | mV |
| DC line regulation | LINE _{REG} | Buck mode ³ | — | 1.40 | — | mV/V |
| Load Transient | V _{VOA_LOADPULL} | Buck mode, I _{LOAD} changes between 10 and 80 mA ³ | — | 3.32 | — | mV |
| DC load regulation | LOAD _{REG} | Buck mode ³ | — | 0.07 | — | mV/mA |
| Output voltage range, Coarse Regulator enabled | V _{VOA_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDB) | V |
| Output load current, Coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOA output within V_VOA_COARSE range | — | — | 100 | μA |
| Nominal inductor, 20% tolerance | L _{DCDCA} | Wired buck configuration, VDDB - VOA > 3.0V | — | 3.3 | — | μH |
| | | Wired buck configuration, VDDB - VOA ≤ 3.0V | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ⁴ | T _{START} | Wired buck (VOA), BB_IPK = 18, I _{LOAD} = 10 mA | — | 247 | — | μs |

Note:

- Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
- With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BB_TON_MAX = 7 (2030ns) supports the lowest headroom.
- Specifications assume minimum headroom requirement has been met if (i.e., VDDB - VOA > 660mV, if operating in buck DCDC mode, or VDDB - VOA > 365mV, if operating in LDO mode).
- For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

Table 5.6. EFP0101/EFP0102 VOB Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|----------|------|------|
| VDDB Input voltage range | V _{VDDB} | | 1.8 | — | 5.5 | V |
| Output programmable voltage range | V _{VOB_RANGE} | EFP0101, DCDC Enabled at Startup | 0.8 | — | 3.3 | V |
| | | EFP0102, DCDC Disabled at Startup ¹ | 0.8 | — | 1.26 | V |
| Default output voltage | V _{VOB} | EFP0101 | — | 1.858 | — | V |
| | | EFP0102 | — | Disabled | — | V |
| Output load current ² | I _{LOAD_MAX} | Buck-only, BK_IPK = 31, EM0, VDDB - VOB > 660mV, TON_MAX = 7 ^{3,4,5} | 141 | — | — | mA |
| | | Buck-only, BK_IPK_EM2 = 7, EM2, VDDB - VOB > 660 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | Buck w/LDO, BK_IPK = 31, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 150 | — | — | mA |
| | | Buck w/LDO, BK_IPK_EM2 = 7, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV ^{4,5} | 150 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV ^{4,5} | 20 | — | — | mA |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | LDO mode, VOB = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | LDO mode, VOB = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| | | LDO mode, VOB = 1.2V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| Output voltage accuracy | V _{VOB_ACC} | EM0, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | -0.6 | 14.7 | mV |
| | | EM2, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | 4.1 | 17.9 | mV |
| | | EM0, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 15.9 | 74.9 | mV |
| | | EM2, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 20.9 | 89.2 | mV |
| Load transient | V _{VOB_LOADPULL} | Buck-only, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 0.454 | — | mV |
| | | Buck with LDO in parallel, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 2.339 | — | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|--|------|-------|------------------------------|-------|
| DC line regulation | LINE _{REG} | Buck-only or Buck w/LDO ⁴ | — | 1.76 | — | mV/V |
| | | LDO mode ⁴ | — | 1.32 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck-only or Buck w/LDO ⁴ | — | 0.07 | — | mV/mA |
| | | LDO mode ⁴ | — | 0.116 | — | mV/mA |
| Output voltage range, coarse regulator enabled ¹ | V _{VOB_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, V _{DDB}) | V |
| Output load current, coarse regulator enabled ¹ | I _{LOAD_COARSE} | EM4, VOB output within V _{VOB_COARSE} range | — | — | 100 | μA |
| Nominal inductor (20% Tolerance) | L _{DCDCB} | V _{DDB} - VOB > 3.0V | — | 3.3 | — | μH |
| | | V _{DDB} - VOB ≤ 3.0V | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ^{6,7} | T _{START} | Wired buck / wired buck with LDO (VOB), BK_IPK = 18, I _{LOAD} = 10 mA | — | 193 | — | μs |

Note:

1. For certain OPN variants, VOB is expected to drive an output in the range of 1.1V to 1.2V, and the maximum output voltage of the converter is internally limited to 1.26V. Any programmed VOB_EM0_V or VOB_EM2_V values that would result in a voltage higher than 1.26V will not affect the output voltage. In addition, for these OPNs, the VOB coarse regulator and bypass functionality is disabled in hardware (i.e., setting the enable bit has no effect).
2. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
3. With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BK_TON_MAX = 7 (2030ns) supports the lowest headroom.
4. Specifications assume minimum headroom requirement has been met if (i.e., V_{DDB} - VOB > 660mV, if operating in buck DCDC mode, or V_{DDB} - VOB > 365mV, if operating in LDO mode).
5. In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (V_{DDB}) is powered by the DCDC A output (VOA). Therefore, the maximum output current of DCDC B will also be limited by the maximum output current of the DCDC A converter.
6. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)
7. For the EFP0109/11 OPNs where the VOB converter is enabled by default, the VOB converter won't be enabled until the VOA converter has reached regulation.

Table 5.7. EFP0101/EFP0102 VOC Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|------|-------|-----------------|-------|
| VDDB input voltage range | V _{VDDB} | | 1.8 | — | 5.5 | V |
| Output programmable range | V _{VOC_RANGE} | | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOC} | EFP0101 | — | 1.87 | — | V |
| | | EFP0102 | — | 1.87 | — | V |
| Output load current ¹ | I _{LOAD_MAX} | EM2, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{2,3} | 20 | — | — | mA |
| | | EM0, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{2,3} | 150 | — | — | mA |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | VOC = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | VOC = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| Output voltage accuracy | V _{VOC_ACC} | EM2, VOC ≥ 1.8V, I _{LOAD} = 25 mA ² | — | 6.6 | 69.8 | mV |
| | | EM0, VOC ≥ 1.8V, I _{LOAD} = 25 mA ² | — | -1.8 | 48.7 | mV |
| Load Transient | V _{VOC_LOADPULL} | I _{LOAD} changes between 10 and 80 mA ² | — | 0.774 | — | mV |
| DC line regulation | LINE _{REG} | 2 | — | 2.6 | — | mV/V |
| DC load regulation | LOAD _{REG} | 2 | — | 0.13 | — | mV/mA |
| Output voltage range, coarse Regulator enabled | V _{VOC_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDB) | V |
| Output load current, coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOC output within V _{VOC_COARSE} range | — | — | 100 | μA |
| Startup time from output enabled to output within 1% of final target voltage ⁴ | T _{START} | LDO C (VOC), LDOC_IGAIN = 12, I _{LOAD} = 10 mA | — | 259 | — | μs |

Note:

1. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
2. Specifications assume minimum LDO dropout requirement has been met (i.e., VDDB - VOC > 365mV)
3. In Single-Cell Boost and Boost Bootstrap configurations (e.g., EFP0108 and EFP0111), the LDO C input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output current of LDO C will also be limited by the maximum output current of the DCDC A converter.
4. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

5.1.3.4 EFP0103 / EFP0104

Note: EFP0103 & EFP0104 are nearly identical devices, differing primarily in the VOB configuration at and after startup:

- On EFP0103, the VOB converter output is enabled to 1.858V at startup and may be programmed after startup in the range 0.8V to 3.3V
- On EFP0104, the VOB converter output is disabled by default, and may be programmed after startup to an output in the range 0.8V to 1.26V

Unless stated otherwise, all parameters in the EFP0103 & EFP0104 electrical specifications tables are specified under the following conditions:

- VDDDB = 3.3 V
- VDDA = GND
- VOA = VOC = 1.8 V
- VOB = 1.2 V (EFP0104) / 1.8 V (EFP0103)
- VIO = 1.8 V

Table 5.8. EFP0103/EFP0104 VOA/VOC Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------------|--|-----|-------|------|------|
| Allowed programmable peak current setting | IPK _{ADJ_RANGE} | Buck, EM0, BB_IPK setting | 0 | — | 31 | |
| | | Buck, EM2, BB_IPK_EM2 setting | 0 | — | 7 | |
| VDDB input voltage range | V _{VDDB} | Wired buck with LDO, input supply connected to VDDB pin | 1.8 | — | 5.5 | V |
| VDDA input voltage range | V _{VDDA} | Low-voltage circuitry unused | — | GND | — | V |
| Output programmable voltage range | V _{VOA_RANGE} | EFP0103 / EFP0104 | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOA} | EFP0103 / EFP0104 | — | 1.86 | — | V |
| Output load current ¹ | I _{LOAD_MAX} | Wired buck, BB_IPK = 31, EM0, VDDB - VOA > 660 mV, TON_MAX=7 ^{2,3} | 150 | — | — | mA |
| | | Wired buck, BB_IPK_EM2 = 7, EM2, VDDB - VOA > 660 mV, TON_MAX = 7 ^{2,3} | 20 | — | — | mA |
| | | Wired buck w/LDO, VOC in parallel with VOA, EM0, LDOC_IGAIN = 15, BB_IPK = 31, VDDB - VOA > 365 mV, TON_MAX=7 ^{2,3} | 150 | — | — | mA |
| | | Wired buck w/LDO, VOC in parallel with VOA, EM2, LDOC_IGAIN = 15, BB_IPK = 7, VDDB - VOA > 365 mV, TON_MAX=7 ^{2,3} | 20 | — | — | mA |
| LDO Dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | VOC in parallel with VOA, LDO mode, VOA = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | VOC in parallel with VOA, LDO mode, VOA = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| Output voltage accuracy | V _{VOA_ACC} | Buck, EM0, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA ³ | — | 1.41 | 77.6 | mV |
| | | Buck, EM2, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA ³ | — | 6.8 | 94.7 | mV |
| | | VOC in parallel with VOA, LDO mode, EM0, VOC ≥ 1.8V, I _{LOAD} = 25 mA ³ | — | -1.8 | 48.7 | mV |
| | | VOC in parallel with VOA, LDO mode, EM2, VOC ≥ 1.8V, I _{LOAD} = 25 mA ³ | — | 6.6 | 69.8 | mV |
| Load Transient | V _{VOA_LOADPULL} | Buck mode, I _{LOAD} changes between 10 and 80 mA ³ | — | 3.32 | — | mV |
| | | VOC in parallel with VOA, LDO mode, I _{LOAD} changes between 10 and 80 mA ³ | — | 0.774 | — | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|---|------|------|-------------------------------|---------|
| DC line regulation | LINE _{REG} | Buck mode ³ | — | 1.40 | — | mV/V |
| | | VOC in parallel with VOA, LDO mode, ³ | — | 2.6 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck mode ³ | — | 0.07 | — | mV/mA |
| | | VOC in parallel with VOA, LDO mode, ³ | — | 0.13 | — | mV/mA |
| Output voltage range, Coarse Regulator enabled | V _{VOA_COARSE} | EM4, 0 μ A < I _{LOAD} < 100 μ A | 1.69 | — | MIN(3.40, V _{DDDB}) | V |
| Output load current, Coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOA output within V _{VOA_COARSE} range | — | — | 100 | μ A |
| Nominal inductor, 20% tolerance | L _{DCDCA} | Wired buck configuration, V _{DDDB} - VOA > 3.0V | — | 3.3 | — | μ H |
| | | Wired buck configuration, V _{DDDB} - VOA \leq 3.0V | — | 2.2 | — | μ H |
| Startup time from output enabled to output within 1% of final target voltage ⁴ | T _{START} | Wired buck with LDO (VOA), BB_IPK = 18, I _{LOAD} = 10 mA | — | 247 | — | μ s |

Note:

1. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
2. With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BB_TON_MAX = 7 (2030ns) supports the lowest headroom.
3. Specifications assume minimum headroom requirement has been met if (i.e., V_{DDDB} - VOA > 660mV, if operating in buck DCDC mode, or V_{DDDB} - VOA > 365mV, if operating in LDO mode).
4. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

Table 5.9. EFP0103/EFP0104 VOB Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|----------|------|------|
| VDDB Input voltage range | V _{VDDB} | | 1.8 | — | 5.5 | V |
| Output programmable voltage range | V _{VOB_RANGE} | EFP0103, DCDC Enabled at Startup | 0.8 | — | 3.3 | V |
| | | EFP0104, DCDC Disabled at Startup ¹ | 0.8 | — | 1.26 | V |
| Default output voltage | V _{VOB} | EFP0103 | — | 1.858 | — | V |
| | | EFP0104 | — | Disabled | — | V |
| Output load current ² | I _{LOAD_MAX} | Buck-only, BK_IPK = 31, EM0, VDDB - VOB > 660mV, TON_MAX = 7 ^{3,4,5} | 141 | — | — | mA |
| | | Buck-only, BK_IPK_EM2 = 7, EM2, VDDB - VOB > 660 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | Buck w/LDO, BK_IPK = 31, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 150 | — | — | mA |
| | | Buck w/LDO, BK_IPK_EM2 = 7, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV ^{4,5} | 150 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV ^{4,5} | 20 | — | — | mA |
| Output voltage accuracy | V _{VOB_ACC} | EM2, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | 4.1 | 17.9 | mV |
| | | EM0, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 15.9 | 74.9 | mV |
| | | EM0, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | -0.6 | 14.7 | mV |
| | | EM2, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 20.9 | 89.2 | mV |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | LDO mode, VOB = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | LDO mode, VOB = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| | | LDO mode, VOB = 1.2V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| Load transient | V _{VOB_LOADPULL} | Buck-only, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 0.454 | — | mV |
| | | Buck with LDO in parallel, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 2.339 | — | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|--|------|-------|--------------------------------|-------|
| DC line regulation | LINE _{REG} | Buck-only or Buck w/LDO ⁴ | — | 1.76 | — | mV/V |
| | | LDO mode ⁴ | — | 1.32 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck-only or Buck w/LDO ⁴ | — | 0.07 | — | mV/mA |
| | | LDO mode ⁴ | — | 0.116 | — | mV/mA |
| Output voltage range, coarse regulator enabled ¹ | V _{VOB_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, V _{VDDDB}) | V |
| Output load current, coarse regulator enabled ¹ | I _{LOAD_COARSE} | EM4, VOB output within V_VOB_COARSE range | — | — | 100 | μA |
| Nominal inductor (20% Tolerance) | L _{DCDCB} | V _{VDDDB} - V _{VOB} > 3.0V | — | 3.3 | — | μH |
| | | V _{VDDDB} - V _{VOB} ≤ 3.0V | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ^{6,7} | T _{START} | Wired buck / wired buck with LDO (VOB), BK_IPK = 18, I _{LOAD} = 10 mA | — | 193 | — | μs |

Note:

- For certain OPN variants, VOB is expected to drive an output in the range of 1.1V to 1.2V, and the maximum output voltage of the converter is internally limited to 1.26V. Any programmed VOB_EM0_V or VOB_EM2_V values that would result in a voltage higher than 1.26V will not affect the output voltage. In addition, for these OPNs, the VOB coarse regulator and bypass functionality is disabled in hardware (i.e., setting the enable bit has no effect).
- Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
- With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BK_TON_MAX = 7 (2030ns) supports the lowest headroom.
- Specifications assume minimum headroom requirement has been met if (i.e., V_{VDDDB} - V_{VOB} > 660mV, if operating in buck DCDC mode, or V_{VDDDB} - V_{VOB} > 365mV, if operating in LDO mode).
- In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (V_{VDDDB}) is powered by the DCDC A output (VOA). Therefore, the maximum output current of DCDC B will also be limited by the maximum output current of the DCDC A converter.
- For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)
- For the EFP0109/11 OPNs where the VOB converter is enabled by default, the VOB converter won't be enabled until the VOA converter has reached regulation.

5.1.3.5 EFP0106 / EFP0107

Note: EFP0106 & EFP0107 are nearly identical devices, differing primarily in the VOB configuration at and after startup:

- On EFP0106, the VOB converter output is enabled to 1.858V at startup and may be programmed after startup in the range 0.8V to 3.3V
- On EFP0107, the VOB converter output is disabled by default, and may be programmed after startup to an output in the range 0.8V to 1.26V

Unless stated otherwise, all parameters in the EFP0106 & EFP0107 electrical specifications tables are specified under the following conditions:

- V_{VDDDB} = 3.0 V
- V_{VDDA} = GND
- V_{VOA} = 3.3 V
- V_{VOB} = 1.2 V (EFP0107) / 1.8 V (EFP0106)
- V_{VOC} = 1.8 V
- V_{VIO} = 1.8 V
- BB_IPK = 10, BB_IPK_NOADJ = 0, BB_IRI_CON = 0, BB_IPK_BOOST = 0

Table 5.10. EFP0106/EFP0107 VOA Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|--|-------|-------|------------------|-------|
| Allowed programmable peak current setting | IPK _{ADJ_RANGE} | Buck/Boost, EM0, VOA ≤ 3.3V, BB_IPK setting | 0 | — | 31 | |
| | | Buck/Boost, EM2, VOA ≤ 3.3V, BB_IPK_EM2 setting | 0 | — | 7 | |
| VDDA input voltage range | V _{VDDA} | Low-voltage circuitry unused | — | GND | — | V |
| Output programmable voltage range | V _{VOA_RANGE} | EFP0106 / EFP0107 | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOA} | EFP0106 / EFP0107 | — | 1.86 | — | V |
| VDDDB input voltage range | V _{VDDDB} | Buck-boost, input supply connected to VDDDB pin ¹ | 1.8 | — | 5.5 | V |
| Output load current ² | I _{LOAD_MAX} | Buck-boost, BB_IPK = 31, EM0, 2.5V ≤ VDDDB ≤ 5.5V, VOA=3.3V | 115.9 | — | — | mA |
| | | Buck-boost, BB_IPK_EM2 = 7, EM2, 2.5V ≤ VDDDB ≤ 5.5V, VOA=3.3V | 20 | — | — | mA |
| | | Buck-boost, BB_IPK = 31, EM0, 1.8V ≤ VDDDB ≤ 5.5V, VOA=3.3V | 41.4 | — | — | mA |
| | | Buck-boost, BB_IPK_EM2 = 7, EM2, 1.8V ≤ VDDDB ≤ 5.5V, VOA=3.3V | 20 | — | — | mA |
| Output voltage accuracy | V _{VOA_ACC} | Buck/Boost, EM0, 1.8V ≤ VOA ≤ 3.3V | — | 1.41 | 77.6 | mV |
| | | Buck/Boost, EM2, 1.8V ≤ VOA ≤ 3.3V | — | 6.8 | 94.7 | mV |
| DC line regulation | LINE _{REG} | Buck/Boost mode | — | 1.44 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck/Boost mode | — | 0.181 | — | mV/mA |
| Output voltage range, Coarse Regulator enabled | V _{VOA_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDDB) | V |
| Output load current, Coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOA output within V _{VOA_COARSE} range | — | — | 100 | μA |
| Nominal inductor, 20% tolerance | L _{DCCDA} | Buck/Boost configurations | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ³ | T _{START} | Buck-boost (VOA), BB_IPK = 13, VOA = 3.3V, VDDDB = 1.8V, I _{LOAD} = 10 mA | — | 332 | — | μs |

Note:

1. It is permissible for the input voltage to exceed the output voltage by ~0.3V in boost configurations, using the T_{OFF} max limiting feature. Refer to the boost mode T_{OFF} maximum limiting section of the datasheet.
2. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
3. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

Table 5.11. EFP0106/EFP0107 VOB Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|----------|------|------|
| VDDB Input voltage range | V _{VDDB} | | 1.8 | — | 5.5 | V |
| Output programmable voltage range | V _{VOB_RANGE} | EFP0106, DCDC Enabled at Startup | 0.8 | — | 3.3 | V |
| | | EFP0107, DCDC Disabled at Startup ¹ | 0.8 | — | 1.26 | V |
| Default output voltage | V _{VOB} | EFP0106 | — | 1.858 | — | V |
| | | EFP0107 | — | Disabled | — | V |
| Output load current ² | I _{LOAD_MAX} | Buck-only, BK_IPK = 31, EM0, VDDB - VOB > 660mV, TON_MAX = 7 ^{3,4,5} | 141 | — | — | mA |
| | | Buck-only, BK_IPK_EM2 = 7, EM2, VDDB - VOB > 660 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | Buck w/LDO, BK_IPK = 31, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 150 | — | — | mA |
| | | Buck w/LDO, BK_IPK_EM2 = 7, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV ^{4,5} | 150 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV ^{4,5} | 20 | — | — | mA |
| Output voltage accuracy | V _{VOB_ACC} | EM2, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 20.9 | 89.2 | mV |
| | | EM0, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | -0.6 | 14.7 | mV |
| | | EM2, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | 4.1 | 17.9 | mV |
| | | EM0, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 15.9 | 74.9 | mV |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | LDO mode, VOB = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | LDO mode, VOB = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| | | LDO mode, VOB = 1.2V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| Load transient | V _{VOB_LOADPULL} | Buck-only, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 0.454 | — | mV |
| | | Buck with LDO in parallel, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 2.339 | — | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|--|------|-------|------------------------------|-------|
| DC line regulation | LINE _{REG} | Buck-only or Buck w/LDO ⁴ | — | 1.76 | — | mV/V |
| | | LDO mode ⁴ | — | 1.32 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck-only or Buck w/LDO ⁴ | — | 0.07 | — | mV/mA |
| | | LDO mode ⁴ | — | 0.116 | — | mV/mA |
| Output voltage range, coarse regulator enabled ¹ | V _{VOB_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, V _{DDB}) | V |
| Output load current, coarse regulator enabled ¹ | I _{LOAD_COARSE} | EM4, VOB output within V _{VOB_COARSE} range | — | — | 100 | μA |
| Nominal inductor (20% Tolerance) | L _{DCDCB} | V _{DDB} - VOB > 3.0V | — | 3.3 | — | μH |
| | | V _{DDB} - VOB ≤ 3.0V | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ^{6,7} | T _{START} | Wired buck / wired buck with LDO (VOB), BK_IPK = 18, I _{LOAD} = 10 mA | — | 193 | — | μs |

Note:

- For certain OPN variants, VOB is expected to drive an output in the range of 1.1V to 1.2V, and the maximum output voltage of the converter is internally limited to 1.26V. Any programmed VOB_EM0_V or VOB_EM2_V values that would result in a voltage higher than 1.26V will not affect the output voltage. In addition, for these OPNs, the VOB coarse regulator and bypass functionality is disabled in hardware (i.e., setting the enable bit has no effect).
- Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
- With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BK_TON_MAX = 7 (2030ns) supports the lowest headroom.
- Specifications assume minimum headroom requirement has been met if (i.e., V_{DDB} - VOB > 660mV, if operating in buck DCDC mode, or V_{DDB} - VOB > 365mV, if operating in LDO mode).
- In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (V_{DDB}) is powered by the DCDC A output (VOA). Therefore, the maximum output current of DCDC B will also be limited by the maximum output current of the DCDC A converter.
- For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)
- For the EFP0109/11 OPNs where the VOB converter is enabled by default, the VOB converter won't be enabled until the VOA converter has reached regulation.

Table 5.12. EFP0106/EFP0107 VOC Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|------|-------|-----------------|-------|
| VDDB input voltage range | V _{VDDB} | | 1.8 | — | 5.5 | V |
| Output programmable range | V _{VOC_RANGE} | | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOC} | EFP0106 | — | 1.87 | — | V |
| | | EFP0107 | — | 1.87 | — | V |
| Output load current ¹ | I _{LOAD_MAX} | EM2, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{2,3} | 20 | — | — | mA |
| | | EM0, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{2,3} | 150 | — | — | mA |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | VOC = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | VOC = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| Output voltage accuracy | V _{VOC_ACC} | EM2, VOC ≥ 1.8V, I _{LOAD} = 25 mA ² | — | 6.6 | 69.8 | mV |
| | | EM0, VOC ≥ 1.8V, I _{LOAD} = 25 mA ² | — | -1.8 | 48.7 | mV |
| Load Transient | V _{VOC_LOADPULL} | I _{LOAD} changes between 10 and 80 mA ² | — | 0.774 | — | mV |
| DC line regulation | LINE _{REG} | 2 | — | 2.6 | — | mV/V |
| DC load regulation | LOAD _{REG} | 2 | — | 0.13 | — | mV/mA |
| Output voltage range, coarse Regulator enabled | V _{VOC_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDB) | V |
| Output load current, coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOC output within V _{VOC_COARSE} range | — | — | 100 | μA |
| Startup time from output enabled to output within 1% of final target voltage ⁴ | T _{START} | LDO C (VOC), LDOC_IGAIN = 12, I _{LOAD} = 10 mA | — | 259 | — | μs |

Note:

1. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
2. Specifications assume minimum LDO dropout requirement has been met (i.e., VDDB - VOC > 365mV)
3. In Single-Cell Boost and Boost Bootstrap configurations (e.g., EFP0108 and EFP0111), the LDO C input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output current of LDO C will also be limited by the maximum output current of the DCDC A converter.
4. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

5.1.3.6 EFP0108

Unless stated otherwise, all parameters in the EFP0108 electrical specifications tables are specified under the following conditions:

- VBOOST = VDDA = 1.5 V
- VOA = VDDB = 3.0 V
- VOB = 1.2 V
- VOC = 1.8 V
- VIO = 3.0 V
- BB_IPK = 10, BB_IPK_NOADJ = 0, BB_IRI_CON = 0, BB_IPK_BOOST = 0

Note: VBOOST is the voltage applied to the inductor attached to the LA2 pin in Boost modes

Table 5.13. EFP0108 VOA Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|---|------|-------|------|-------|
| Allowed programmable peak current setting | IPK _{ADJ_RANGE} | Wired boost, EM0, VOA ≤ 3.3V, BB_IPK setting | 0 | — | 31 | |
| | | Wired boost, EM2, VOA ≤ 3.3V, BB_IPK_EM2 setting | 0 | — | 7 | |
| VBOOST input voltage range ¹ | V _{VBOOST} | EFP0108 | 0.8 | — | 1.8 | V |
| VDDA input voltage range | V _{VDDA} | Single-cell boost (at startup), input supply connected to VDDA pin | 0.85 | — | 1.8 | V |
| | | Single-cell boost (after startup), Input supply connected to VDDA pin | 0.80 | — | 1.8 | V |
| Output programmable voltage range | V _{VOA_RANGE} | EFP0108 | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOA} | EFP0108 | — | 1.86 | — | V |
| Output load current ² | I _{LOAD_MAX} | Single-cell boost, BB_IPK = 31, EM0, 0.8V ≤ VDDA/VBOOST ≤ 1.8V, VOA=1.8V | 31.7 | — | — | mA |
| | | Single-cell boost, BB_IPK_EM2 = 2, EM2, 0.8V ≤ VDDA/VBOOST ≤ 1.8V, VOA=1.8V | 20 | — | — | mA |
| | | Single-cell boost, BB_IPK = 31, EM0, 1.0V ≤ VDDA/VBOOST ≤ 1.8V, VOA=1.8V | 59.6 | — | — | mA |
| | | Single-cell boost, BB_IPK_EM2 = 2, EM2, 1.0V ≤ VDDA/VBOOST ≤ 1.8V, VOA=1.8V | 20 | — | — | mA |
| | | Single-cell boost, BB_IPK = 31, EM0, 0.8V ≤ VDDA/VBOOST ≤ 1.8V, VOA=3.0V | 26.4 | — | — | mA |
| | | Single-cell boost, BB_IPK_EM2 = 2, EM2, 0.8V ≤ VDDA/VBOOST ≤ 1.8V, VOA=3.0V | 20 | — | — | mA |
| | | Single-cell boost, BB_IPK = 31, EM0, 1.0V ≤ VDDA/VBOOST ≤ 1.8V, VOA=3.0V | 43.7 | — | — | mA |
| | | Single-cell boost, BB_IPK_EM2 = 2, EM2, 1.0V ≤ VDDA/VBOOST ≤ 1.8V, VOA=3.0V | 20 | — | — | mA |
| Output voltage accuracy | V _{VOA_ACC} | Boost mode, EM0, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA | — | 1.41 | 77.6 | mV |
| | | Boost mode, EM2, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA | — | 6.8 | 94.7 | mV |
| DC line regulation | LINE _{REG} | Boost mode | — | 1.44 | — | mV/V |
| DC load regulation | LOAD _{REG} | Boost mode | — | 0.181 | — | mV/mA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------|---|-----|-----|-----|---------------|
| Nominal inductor, 20% tolerance | L_{DCDCA} | Wired boost configurations | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ³ | T_{START} | Single-cell boost (VOA), $BB_IPK = 10$, $I_{LOAD} = 10\text{ mA}$ | — | 184 | — | μs |

Note:

1. VBOOST is the voltage applied to the inductor attached to the LA2 pin in boost modes.
2. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
3. For converters enabled by default, total startup time will be $T_{START} + T_{BOOT}$ (found in the General Operating Conditions table)

Table 5.14. EFP0108 VOB Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|-----|----------|------|-------|
| VDDB Input voltage range | V _{VDDB} | VDDB powered from VOA output ¹ | 1.8 | — | VOA | V |
| Output programmable voltage range | V _{VOB_RANGE} | EFP0108, DCDC Disabled at Startup ^{2,3} | 0.8 | — | 1.26 | V |
| Default output voltage | V _{VOB} | EFP0108 | — | Disabled | — | V |
| Output load current ⁴ | I _{LOAD_MAX} | Buck-only, BK_IPK = 31, EM0, VDDB - VOB > 660mV, TON_MAX = 7 ^{5,6,1} | 141 | — | — | mA |
| | | Buck-only, BK_IPK_EM2 = 7, EM2, VDDB - VOB > 660 mV, TON_MAX = 7 ^{5,6,1} | 20 | — | — | mA |
| | | Buck w/LDO, BK_IPK = 31, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV, TON_MAX = 7 ^{5,6,1} | 150 | — | — | mA |
| | | Buck w/LDO, BK_IPK_EM2 = 7, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV, TON_MAX = 7 ^{5,6,1} | 20 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV ^{6,1} | 150 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV ^{6,1} | 20 | — | — | mA |
| Output voltage accuracy | V _{VOB_ACC} | EM0, VOB = 1.1V, I _{LOAD} = 25 mA ⁶ | — | -0.6 | 14.7 | mV |
| | | EM2, VOB = 1.1V, I _{LOAD} = 25 mA ⁶ | — | 4.1 | 17.9 | mV |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | LDO mode, VOB = 1.2V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| Load transient | V _{VOB_LOADPULL} | Buck-only, I _{LOAD} changes between 10 and 80 mA ⁶ | — | 0.454 | — | mV |
| | | Buck with LDO in parallel, I _{LOAD} changes between 10 and 80 mA ⁶ | — | 2.339 | — | mV |
| DC line regulation | LINE _{REG} | Buck-only or Buck w/LDO ⁶ | — | 1.76 | — | mV/V |
| | | LDO mode ⁶ | — | 1.32 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck-only or Buck w/LDO ⁶ | — | 0.07 | — | mV/mA |
| | | LDO mode ⁶ | — | 0.116 | — | mV/mA |
| Nominal inductor (20% Tolerance) | L _{DCDCB} | VDDB - VOB > 3.0V | — | 3.3 | — | μH |
| | | VDDB - VOB ≤ 3.0V | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ^{7,8} | T _{START} | Wired buck / wired buck with LDO (VOB), BK_IPK = 18, I _{LOAD} = 10 mA | — | 193 | — | μs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| <ol style="list-style-type: none"> 1. In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output current of DCDC B will also be limited by the maximum output current of the DCDC A converter. 2. For certain OPN variants, VOB is expected to drive an output in the range of 1.1V to 1.2V, and the maximum output voltage of the converter is internally limited to 1.26V. Any programmed VOB_EM0_V or VOB_EM2_V values that would result in a voltage higher than 1.26V will not affect the output voltage. In addition, for these OPNs, the VOB coarse regulator and bypass functionality is disabled in hardware (i.e., setting the enable bit has no effect). 3. In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output voltage of the VOB converter will be limited by the VOA output voltage. 4. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage. 5. With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BK_TON_MAX = 7 (2030ns) supports the lowest headroom. 6. Specifications assume minimum headroom requirement has been met if (i.e., $VDDB - VOB > 660mV$, if operating in buck DCDC mode, or $VDDB - VOB > 365mV$, if operating in LDO mode). 7. For converters enabled by default, total startup time will be $T_{START} + T_{BOOT}$ (found in the General Operating Conditions table) 8. For the EFP0109/11 OPNs where the VOB converter is enabled by default, the VOB converter won't be enabled until the VOA converter has reached regulation. | | | | | | |

Table 5.15. EFP0108 VOC Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|------|----------|-----------------|-------|
| VDDB input voltage range | V _{VDDB} | VDDB powered from VOA output ¹ | 1.8 | — | VOA | V |
| Output programmable range | V _{VOC_RANGE} | VDDB powered from VOA output ² | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOC} | EFP0108 | — | Disabled | — | V |
| Output load current ³ | I _{LOAD_MAX} | EM0, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{4,1} | 150 | — | — | mA |
| | | EM2, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{4,1} | 20 | — | — | mA |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | VOC = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | VOC = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| Output voltage accuracy | V _{VOC_ACC} | EM0, VOC ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | -1.8 | 48.7 | mV |
| | | EM2, VOC ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 6.6 | 69.8 | mV |
| Load Transient | V _{VOC_LOADPULL} | I _{LOAD} changes between 10 and 80 mA ⁴ | — | 0.774 | — | mV |
| DC line regulation | LINE _{REG} | 4 | — | 2.6 | — | mV/V |
| DC load regulation | LOAD _{REG} | 4 | — | 0.13 | — | mV/mA |
| Output voltage range, coarse Regulator enabled | V _{VOC_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDB) | V |
| Output load current, coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOC output within V _{VOC_COARSE} range | — | — | 100 | μA |
| Startup time from output enabled to output within 1% of final target voltage ⁵ | T _{START} | LDO C (VOC), LDOC_IGAIN = 12, I _{LOAD} = 10 mA | — | 259 | — | μs |

Note:

1. In Single-Cell Boost and Boost Bootstrap configurations (e.g., EFP0108 and EFP0111), the LDO C input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output current of LDO C will also be limited by the maximum output current of the DCDC A converter.
2. In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the LDO C input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output voltage at VOC will be limited by the VOA output voltage.
3. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
4. Specifications assume minimum LDO dropout requirement has been met (i.e., VDDB - VOC > 365mV)
5. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

5.1.3.7 EFP0109 / EFP0110

Note: EFP0109 & EFP0110 are nearly identical devices, differing primarily in the VOB configuration at and after startup:

- On EFP0109, the VOB converter output is enabled to 1.858V at startup and may be programmed after startup in the range 0.8V to 3.3V
- On EFP0110, the VOB converter output is disabled by default, and may be programmed after startup to an output in the range 0.8V to 1.26V

Unless stated otherwise, all parameters in the EFP0109 & EFP0110 electrical specifications tables are specified under the following conditions:

- VDDDB = VBOOST = 3.0 V
- VDDA = GND
- VOA = 3.3 V
- VOB = 1.2 V (EFP0110) / 1.8 V (EFP0109)
- VOC = 1.8 V
- VIO = 1.8 V
- BB_IPK = 12, BB_IPK_NOADJ = 0, BB_IRI_CON = 0, BB_IPK_BOOST = 27

Note: VBOOST is the voltage applied to the inductor attached to the LA2 pin in Boost modes

Table 5.16. EFP0109/EFP0120 VOA Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|---|------|-------|-------------------|-------|
| Allowed programmable peak current setting | IPK _{ADJ_RANGE} | Wired boost, EM0, VOA ≤ 3.3V, BB_IPK setting | 0 | — | 31 | |
| | | Wired boost, EM2, VOA ≤ 3.3V, BB_IPK_EM2 setting | 0 | — | 7 | |
| VBOOST input voltage range ¹ | V _{VBOOST} | EFP0109 / EFP0110 | 1.8 | — | MIN(3.6, VOA+0.3) | V |
| VDDA input voltage range | V _{VDDA} | Low-voltage circuitry unused | — | GND | — | V |
| VDDDB input voltage range | V _{VDDDB} | Wired boost, input supply connected to VDDDB pin ² | 1.8 | — | 3.6 | V |
| Output programmable voltage range | V _{VOA_RANGE} | EFP0109 / EFP0110 | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOA} | EFP0109 / EFP0110 | — | 3.327 | — | V |
| Output load current ³ | I _{LOAD_MAX} | Wired boost, BB_IPK = 31, EM0, VOA=3.0V | 90 | — | — | mA |
| | | Wired boost, BB_IPK_EM2 = 3, EM2, VOA=3.0V | 20 | — | — | mA |
| Output voltage accuracy | V _{VOA_ACC} | Boost mode, EM0, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA | — | 1.41 | 77.6 | mV |
| | | Boost mode, EM2, 1.8V ≤ VOA ≤ 3.3V, BB_IPK = 10, I _{LOAD} = 25 mA | — | 6.8 | 94.7 | mV |
| DC line regulation | LINE _{REG} | Boost mode | — | 1.44 | — | mV/V |
| DC load regulation | LOAD _{REG} | Boost mode | — | 0.181 | — | mV/mA |
| Output voltage range, Coarse Regulator enabled | V _{VOA_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDDB) | V |
| Output load current, Coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOA output within V _{VOA_COARSE} range | — | — | 100 | μA |
| Nominal inductor, 20% tolerance | L _{DCDCA} | Wired boost configurations | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ⁴ | T _{START} | Boost (VOA), BB_IPK = 10, VDDDB = 1.8V, VOA = 3.3V, I _{LOAD} = 10 mA | — | 97 | — | μs |

Note:

1. VBOOST is the voltage applied to the inductor attached to the LA2 pin in boost modes.
2. It is permissible for the input voltage to exceed the output voltage by ~0.3V in boost configurations, using the T_{OFF} max limiting feature. Refer to the boost mode T_{OFF} maximum limiting section of the datasheet.
3. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
4. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

Table 5.17. EFP0109/EFP0110 VOB Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|----------|------|------|
| VDDB Input voltage range | V _{VDDB} | | 1.8 | — | 5.5 | V |
| Output programmable voltage range | V _{VOB_RANGE} | EFP0109, DCDC Enabled at Startup | 0.8 | — | 3.3 | V |
| | | EFP0110, DCDC Disabled at Startup ¹ | 0.8 | — | 1.26 | V |
| Default output voltage | V _{VOB} | EFP0109 | — | 1.858 | — | V |
| | | EFP0110 | — | Disabled | — | V |
| Output load current ² | I _{LOAD_MAX} | Buck-only, BK_IPK = 31, EM0, VDDB - VOB > 660mV, TON_MAX = 7 ^{3,4,5} | 141 | — | — | mA |
| | | Buck-only, BK_IPK_EM2 = 7, EM2, VDDB - VOB > 660 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | Buck w/LDO, BK_IPK = 31, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 150 | — | — | mA |
| | | Buck w/LDO, BK_IPK_EM2 = 7, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV, TON_MAX = 7 ^{3,4,5} | 20 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV ^{4,5} | 150 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV ^{4,5} | 20 | — | — | mA |
| Output voltage accuracy | V _{VOB_ACC} | EM2, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | 4.1 | 17.9 | mV |
| | | EM0, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 15.9 | 74.9 | mV |
| | | EM0, VOB = 1.1V, I _{LOAD} = 25 mA ⁴ | — | -0.6 | 14.7 | mV |
| | | EM2, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 20.9 | 89.2 | mV |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | LDO mode, VOB = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | LDO mode, VOB = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| | | LDO mode, VOB = 1.2V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| Load transient | V _{VOB_LOADPULL} | Buck-only, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 0.454 | — | mV |
| | | Buck with LDO in parallel, I _{LOAD} changes between 10 and 80 mA ⁴ | — | 2.339 | — | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|--|------|-------|------------------------------|-------|
| DC line regulation | LINE _{REG} | Buck-only or Buck w/LDO ⁴ | — | 1.76 | — | mV/V |
| | | LDO mode ⁴ | — | 1.32 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck-only or Buck w/LDO ⁴ | — | 0.07 | — | mV/mA |
| | | LDO mode ⁴ | — | 0.116 | — | mV/mA |
| Output voltage range, coarse regulator enabled ¹ | V _{VOB_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, V _{DDB}) | V |
| Output load current, coarse regulator enabled ¹ | I _{LOAD_COARSE} | EM4, VOB output within V _{VOB_COARSE} range | — | — | 100 | μA |
| Nominal inductor (20% Tolerance) | L _{DCDCB} | V _{DDB} - VOB > 3.0V | — | 3.3 | — | μH |
| | | V _{DDB} - VOB ≤ 3.0V | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ^{6,7} | T _{START} | Wired buck / wired buck with LDO (VOB), BK_IPK = 18, I _{LOAD} = 10 mA | — | 193 | — | μs |

Note:

- For certain OPN variants, VOB is expected to drive an output in the range of 1.1V to 1.2V, and the maximum output voltage of the converter is internally limited to 1.26V. Any programmed VOB_EM0_V or VOB_EM2_V values that would result in a voltage higher than 1.26V will not affect the output voltage. In addition, for these OPNs, the VOB coarse regulator and bypass functionality is disabled in hardware (i.e., setting the enable bit has no effect).
- Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
- With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BK_TON_MAX = 7 (2030ns) supports the lowest headroom.
- Specifications assume minimum headroom requirement has been met if (i.e., V_{DDB} - VOB > 660mV, if operating in buck DCDC mode, or V_{DDB} - VOB > 365mV, if operating in LDO mode).
- In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (V_{DDB}) is powered by the DCDC A output (VOA). Therefore, the maximum output current of DCDC B will also be limited by the maximum output current of the DCDC A converter.
- For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)
- For the EFP0109/11 OPNs where the VOB converter is enabled by default, the VOB converter won't be enabled until the VOA converter has reached regulation.

Table 5.18. EFP0109/EFP0110 VOC Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|------|-------|-----------------|-------|
| VDDB input voltage range | V _{VDDB} | | 1.8 | — | 5.5 | V |
| Output programmable range | V _{VOC_RANGE} | | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOC} | EFP0109 | — | 1.87 | — | V |
| | | EFP0110 | — | 1.87 | — | V |
| Output load current ¹ | I _{LOAD_MAX} | EM0, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{2,3} | 150 | — | — | mA |
| | | EM2, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{2,3} | 20 | — | — | mA |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | VOC = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | VOC = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| Output voltage accuracy | V _{VOC_ACC} | EM0, VOC ≥ 1.8V, I _{LOAD} = 25 mA ² | — | -1.8 | 48.7 | mV |
| | | EM2, VOC ≥ 1.8V, I _{LOAD} = 25 mA ² | — | 6.6 | 69.8 | mV |
| Load Transient | V _{VOC_LOADPULL} | I _{LOAD} changes between 10 and 80 mA ² | — | 0.774 | — | mV |
| DC line regulation | LINE _{REG} | 2 | — | 2.6 | — | mV/V |
| DC load regulation | LOAD _{REG} | 2 | — | 0.13 | — | mV/mA |
| Output voltage range, coarse Regulator enabled | V _{VOC_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDB) | V |
| Output load current, coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOC output within V _{VOC_COARSE} range | — | — | 100 | μA |
| Startup time from output enabled to output within 1% of final target voltage ⁴ | T _{START} | LDO C (VOC), LDOC_IGAIN = 12, I _{LOAD} = 10 mA | — | 259 | — | μs |

Note:

1. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
2. Specifications assume minimum LDO dropout requirement has been met (i.e., VDDB - VOC > 365mV)
3. In Single-Cell Boost and Boost Bootstrap configurations (e.g., EFP0108 and EFP0111), the LDO C input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output current of LDO C will also be limited by the maximum output current of the DCDC A converter.
4. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

5.1.3.8 EFP0111

Unless stated otherwise, all parameters in the EFP0111 electrical specifications tables are specified under the following conditions:

- VBOOST = 3.0 V
- VDDA = GND
- VOA = VDDB = 5.2 V
- VOB = 3.0 V
- VOC = 1.8 V
- VIO = 1.8 V
- BB_IPK = 10, BB_IPK_NOADJ = 1, BB_IRI_CON = 14, BB_IPK_BOOST = 39

Note: VBOOST is the voltage applied to the inductor attached to the LA2 pin in Boost modes

Table 5.19. EFP0111 VOA Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|---|------|-------|------------------------------|-------|
| Allowed programmable peak current setting | IPK _{ADJ_RANGE} | Wired boost, EM0, VOA ≤ 3.3V, BB_IPK setting | 0 | — | 31 | |
| | | Wired boost, EM2, VOA ≤ 3.3V, BB_IPK_EM2 setting | 0 | — | 7 | |
| | | Wired boost, EM0, VOA > 3.3V, BB_IPK setting | 0 | — | 15 | |
| | | Wired boost, EM2, VOA > 3.3V, BB_IPK_EM2 setting | 0 | — | 3 | |
| VBOOST input voltage range ¹ | V _{VBOOST} | EFP0111, Boost bootstrap (at startup) ² | 2.5 | — | MIN(5.5, VOA+0.3) | V |
| | | EFP0111, Boost bootstrap (after startup) ² | 1.5 | — | MIN(5.5, VOA+0.3) | V |
| VDDA input voltage range | V _{VDDA} | Low-voltage circuitry unused | — | GND | — | V |
| Output programmable voltage range | V _{VOA_RANGE} | EFP0111 | 1.7 | — | 5.22 | V |
| Default output voltage | V _{VOA} | EFP0111 | — | 5.22 | — | V |
| Output load current ³ | I _{LOAD_MAX} | Boost bootstrap, BB_IPK=15, EM0, VOA=5.2V ⁴ | 2.49 | — | — | mA |
| | | Boost bootstrap, BB_IPK_EM2=3, EM2, VOA=5.2V ⁴ | 0.37 | — | — | mA |
| Output voltage accuracy | V _{VOA_ACC} | Boost Bootstrap, EM0, 1.8V ≤ VOA < 5.0V, BB_IPK = 10 | — | 1.41 | 77.6 | mV |
| | | Boost Bootstrap, EM2, 1.8V ≤ VOA < 5.0V, BB_IPK = 10 | — | 6.8 | 94.7 | mV |
| | | Boost Bootstrap, EM0, VOA ≥ 5.0V, BB_IPK = 10 | — | 14.7 | 84.3 | mV |
| | | Boost Bootstrap, EM2, VOA ≥ 5.0V, BB_IPK = 10 | — | 17.6 | 111 | mV |
| DC line regulation | LINE _{REG} | Boost mode | — | 1.44 | — | mV/V |
| DC load regulation | LOAD _{REG} | Boost mode | — | 0.181 | — | mV/mA |
| Output voltage range, Coarse Regulator enabled | V _{VOA_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, V _{DDB}) | V |
| Output load current, Coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOA output within V _{VOA_COARSE} range | — | — | 100 | μA |
| Nominal inductor, 20% tolerance | L _{DCCDA} | Wired boost configurations | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ⁵ | T _{START} | Boost bootstrap (VOA), BB_IPK = 10 | — | 2603 | — | μs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| Note: <ol style="list-style-type: none">VBOOST is the voltage applied to the inductor attached to the LA2 pin in boost modes.It is permissible for the input voltage to exceed the output voltage by ~0.3V in boost configurations, using the T_{OFF} max limiting feature. Refer to the boost mode T_{OFF} maximum limiting section of the datasheet.Maximum output load current is determined by first measuring the output voltage with a 1.25mA load. Maximum output load is the maximum load at which measured output voltage is no lower than 50mV from the original 1.25mA load measured voltage.In boost bootstrap mode, the DCDC current limit is enabled and VOA will not be tightly regulated. Peak load currents are expected to be primarily sourced from the VOA output capacitor, and the VOA output is expected to droop under load and allowed sufficient time to recover before the next peak load is applied. The maximum output current specification can be interpreted here as the maximum allowed DC current before the VOA output may begin to droop, or as the maximum allowed average current.For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table) | | | | | | |

Table 5.20. EFP0111 VOB Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|-------|------|-------|
| VDDB Input voltage range | V _{VDDB} | VDDB powered from VOA output ¹ | 1.8 | — | VOA | V |
| Output programmable voltage range | V _{VOB_RANGE} | EFP0111, DCDC Enabled at Startup ² | 0.8 | — | 3.3 | V |
| Default output voltage | V _{VOB} | EFP0111 | — | 1.858 | — | V |
| Output load current ³ | I _{LOAD_MAX} | Buck-only, BK_IPK = 31, EM0, VDDB - VOB > 660mV, TON_MAX = 7 ^{4,5,1} | 141 | — | — | mA |
| | | Buck-only, BK_IPK_EM2 = 7, EM2, VDDB - VOB > 660 mV, TON_MAX = 7 ^{4,5,1} | 20 | — | — | mA |
| | | Buck w/LDO, BK_IPK = 31, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV, TON_MAX = 7 ^{4,5,1} | 150 | — | — | mA |
| | | Buck w/LDO, BK_IPK_EM2 = 7, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV, TON_MAX = 7 ^{4,5,1} | 20 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM0, VDDB - VOB > 365 mV ^{5,1} | 150 | — | — | mA |
| | | LDO-only, LDOB_IGAIN = 15, EM2, VDDB - VOB > 365 mV ^{5,1} | 20 | — | — | mA |
| Output voltage accuracy | V _{VOB_ACC} | EM0, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁵ | — | 15.9 | 74.9 | mV |
| | | EM2, VOB ≥ 1.8V, I _{LOAD} = 25 mA ⁵ | — | 20.9 | 89.2 | mV |
| | | EM0, VOB = 1.1V, I _{LOAD} = 25 mA ⁵ | — | -0.6 | 14.7 | mV |
| | | EM2, VOB = 1.1V, I _{LOAD} = 25 mA ⁵ | — | 4.1 | 17.9 | mV |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | LDO mode, VOB = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | LDO mode, VOB = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| Load transient | V _{VOB_LOADPULL} | Buck-only, I _{LOAD} changes between 10 and 80 mA ⁵ | — | 0.454 | — | mV |
| | | Buck with LDO in parallel, I _{LOAD} changes between 10 and 80 mA ⁵ | — | 2.339 | — | mV |
| DC line regulation | LINE _{REG} | Buck-only or Buck w/LDO ⁵ | — | 1.76 | — | mV/V |
| | | LDO mode ⁵ | — | 1.32 | — | mV/V |
| DC load regulation | LOAD _{REG} | Buck-only or Buck w/LDO ⁵ | — | 0.07 | — | mV/mA |
| | | LDO mode ⁵ | — | 0.116 | — | mV/mA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|--|------|-----|------------------------------|------|
| Output voltage range, coarse regulator enabled ⁶ | V _{VOB_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, V _{DDB}) | V |
| Output load current, coarse regulator enabled ⁶ | I _{LOAD_COARSE} | EM4, VOB output within V _{VOB_COARSE} range | — | — | 100 | μA |
| Nominal inductor (20% Tolerance) | L _{DCDCB} | V _{DDB} - VOB > 3.0V | — | 3.3 | — | μH |
| | | V _{DDB} - VOB ≤ 3.0V | — | 2.2 | — | μH |
| Startup time from output enabled to output within 1% of final target voltage ^{7,8} | T _{START} | Wired buck / wired buck with LDO (VOB), BK_IPK = 18, I _{LOAD} = 10 mA | — | 193 | — | μs |

Note:

1. In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (V_{DDB}) is powered by the DCDC A output (VOA). Therefore, the maximum output current of DCDC B will also be limited by the maximum output current of the DCDC A converter.
2. In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the DCDC B input (V_{DDB}) is powered by the DCDC A output (VOA). Therefore, the maximum output voltage of the VOB converter will be limited by the VOA output voltage.
3. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
4. With less than 660 mV of headroom in buck mode, T_{ON} will be limited and the desired peak current can never be reached, resulting in a reduction in output load current. BK_TON_MAX = 7 (2030ns) supports the lowest headroom.
5. Specifications assume minimum headroom requirement has been met if (i.e., V_{DDB} - VOB > 660mV, if operating in buck DCDC mode, or V_{DDB} - VOB > 365mV, if operating in LDO mode).
6. For certain OPN variants, VOB is expected to drive an output in the range of 1.1V to 1.2V, and the maximum output voltage of the converter is internally limited to 1.26V. Any programmed VOB_EM0_V or VOB_EM2_V values that would result in a voltage higher than 1.26V will not affect the output voltage. In addition, for these OPNs, the VOB coarse regulator and bypass functionality is disabled in hardware (i.e., setting the enable bit has no effect).
7. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)
8. For the EFP0109/11 OPNs where the VOB converter is enabled by default, the VOB converter won't be enabled until the VOA converter has reached regulation.

Table 5.21. EFP0111 VOC Output

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|------|-------|-----------------|-------|
| VDDB input voltage range | V _{VDDB} | VDDB powered from VOA output ¹ | 1.8 | — | VOA | V |
| Output programmable range | V _{VOC_RANGE} | VDDB powered from VOA output ² | 1.7 | — | 3.3 | V |
| Default output voltage | V _{VOC} | EFP0111 | — | 1.87 | — | V |
| Output load current ³ | I _{LOAD_MAX} | EM0, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{4,1} | 150 | — | — | mA |
| | | EM2, LDOC_IGAIN = 15, VDDB-VOC > 365mV ^{4,1} | 20 | — | — | mA |
| LDO dropout voltage (headroom required to ensure output in regulation) | V _{DROPOUT} | VOC = 1.8V, I _{LOAD} = 10 mA | — | 20 | — | mV |
| | | VOC = 1.8V, I _{LOAD} = 150 mA | — | — | 365 | mV |
| Output voltage accuracy | V _{VOC_ACC} | EM0, VOC ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | -1.8 | 48.7 | mV |
| | | EM2, VOC ≥ 1.8V, I _{LOAD} = 25 mA ⁴ | — | 6.6 | 69.8 | mV |
| Load Transient | V _{VOC_LOADPULL} | I _{LOAD} changes between 10 and 80 mA ⁴ | — | 0.774 | — | mV |
| DC line regulation | LINE _{REG} | 4 | — | 2.6 | — | mV/V |
| DC load regulation | LOAD _{REG} | 4 | — | 0.13 | — | mV/mA |
| Output voltage range, coarse Regulator enabled | V _{VOC_COARSE} | EM4, 0 μA < I _{LOAD} < 100 μA | 1.69 | — | MIN(3.40, VDDB) | V |
| Output load current, coarse Regulator enabled | I _{LOAD_COARSE} | EM4, VOC output within V _{VOC_COARSE} range | — | — | 100 | μA |
| Startup time from output enabled to output within 1% of final target voltage ⁵ | T _{START} | LDO C (VOC), LDOC_IGAIN = 12, I _{LOAD} = 10 mA | — | 259 | — | μs |

Note:

1. In Single-Cell Boost and Boost Bootstrap configurations (e.g., EFP0108 and EFP0111), the LDO C input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output current of LDO C will also be limited by the maximum output current of the DCDC A converter.
2. In Single-Cell Boost (EFP0108) and Boost Bootstrap (EFP0111) configurations, the LDO C input (VDDB) is powered by the DCDC A output (VOA). Therefore, the maximum output voltage at VOC will be limited by the VOA output voltage.
3. Maximum output load current is determined by first measuring the output voltage with a 5mA load. Maximum output load is the the maximum load at which measured output voltage is no lower than 50mV from the original 5mA load measured voltage.
4. Specifications assume minimum LDO dropout requirement has been met (i.e., VDDB - VOC > 365mV)
5. For converters enabled by default, total startup time will be T_{START} + T_{BOOT} (found in the General Operating Conditions table)

5.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

5.2.1 DCDC A Efficiency

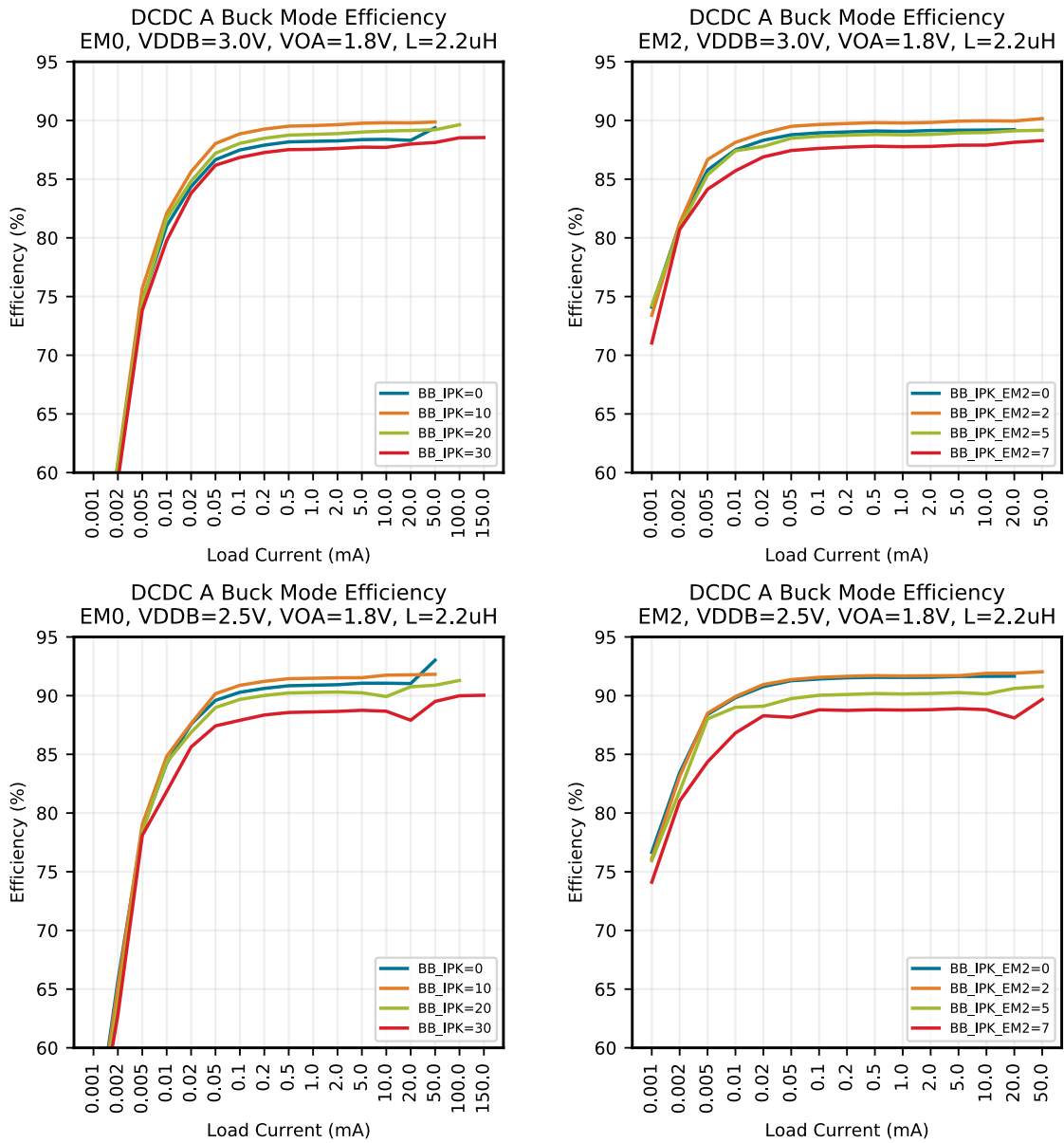


Figure 5.2. Typical DCDC A Buck Efficiency

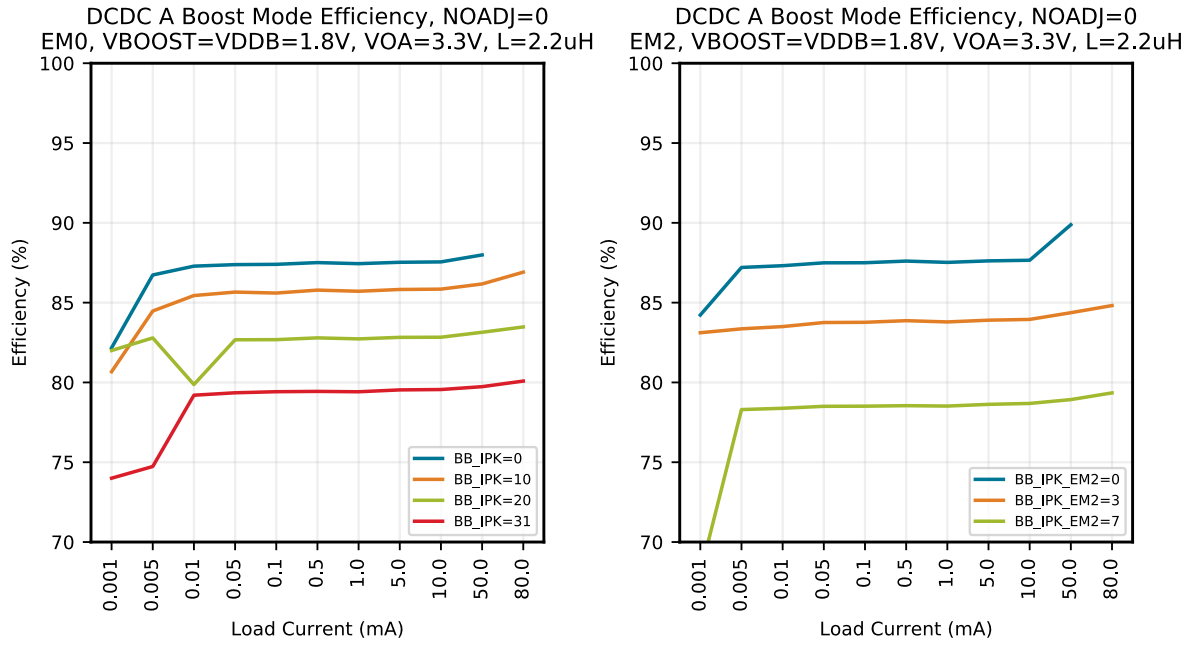
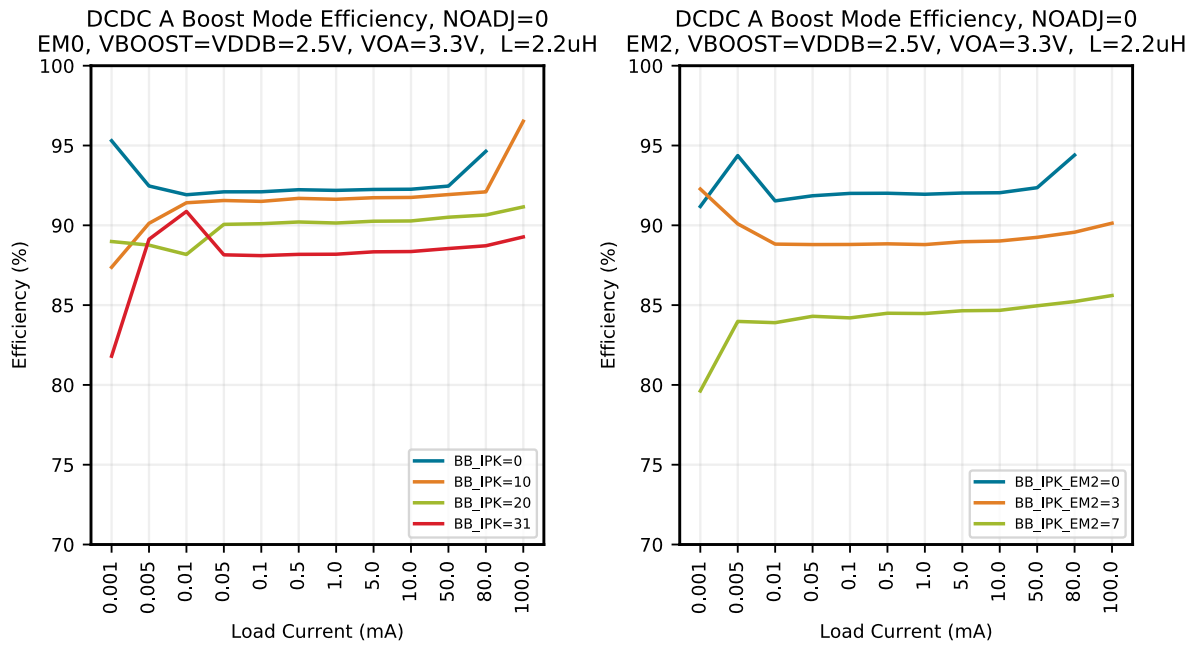


Figure 5.3. Typical DCDC A Boost Efficiency, VOA=3.3V, NOADJ=0



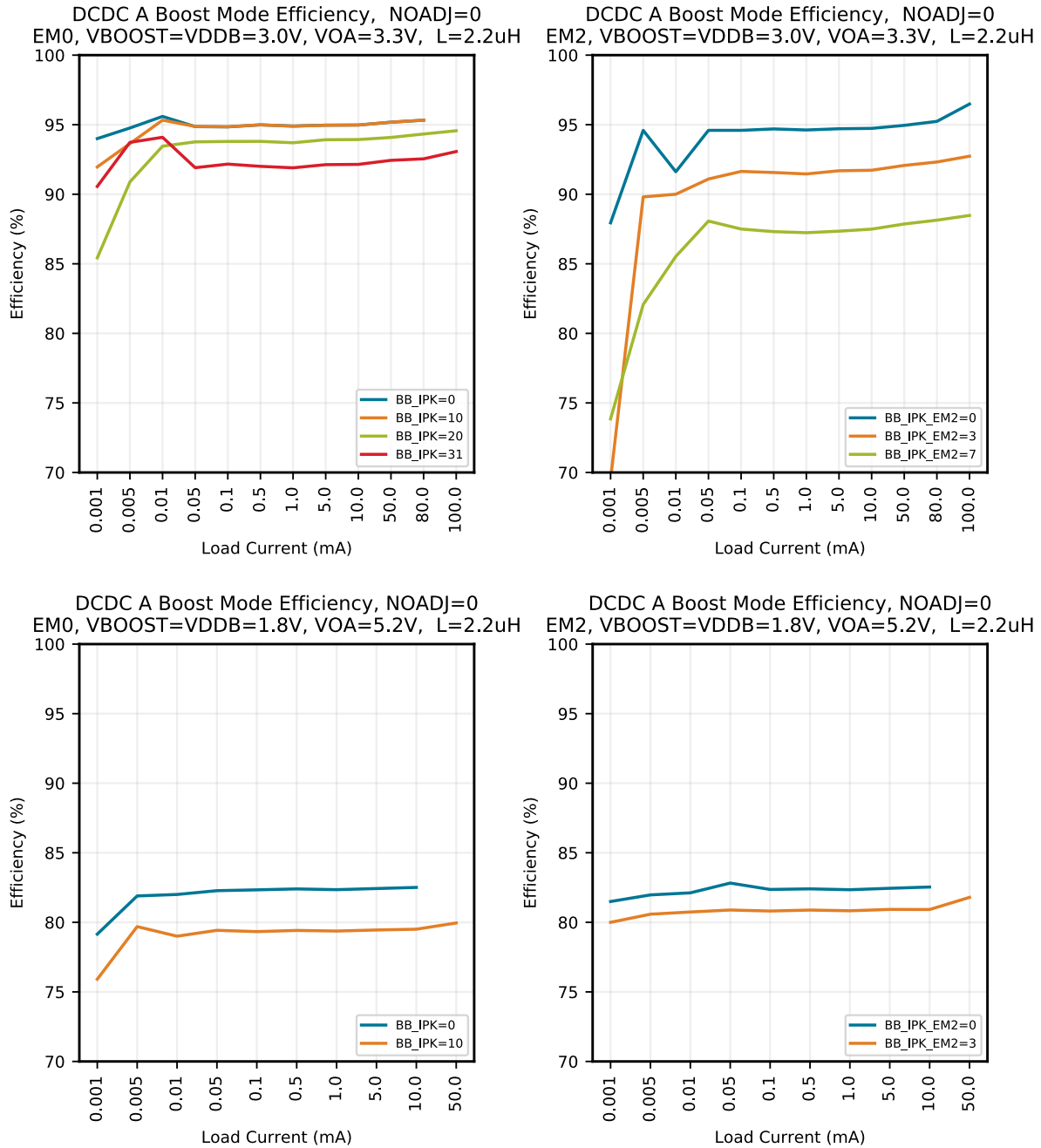
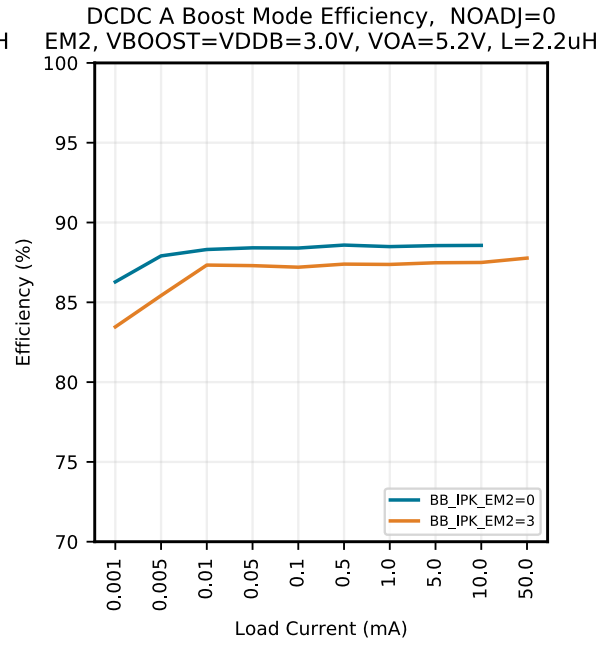
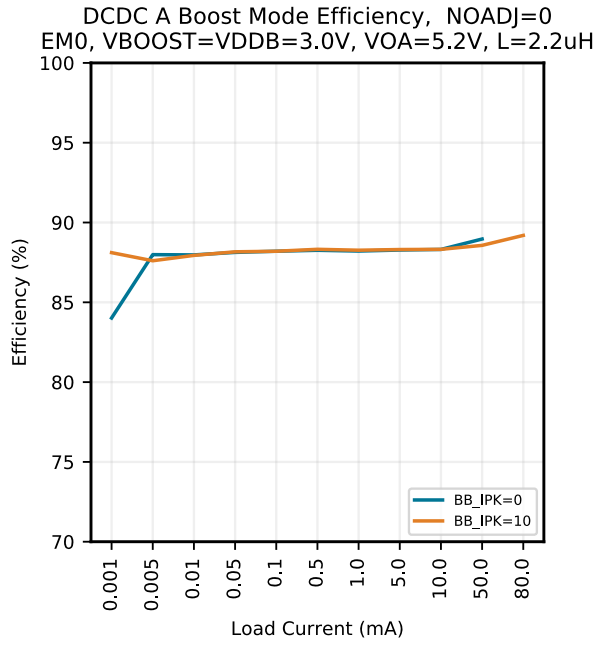
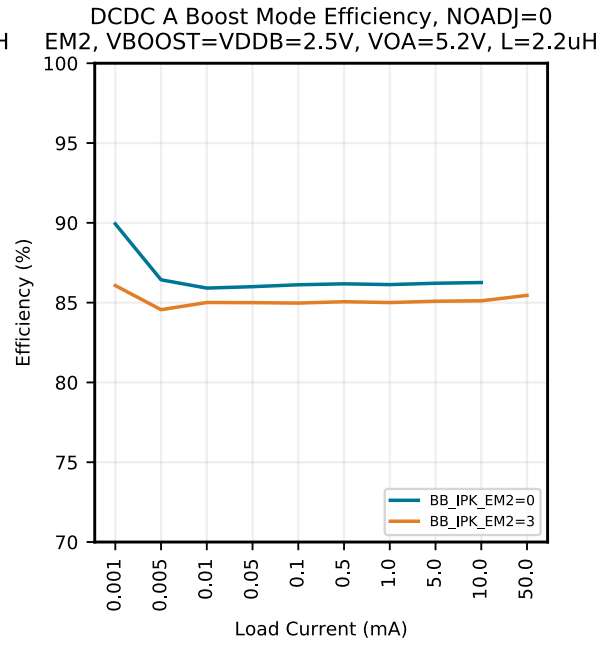
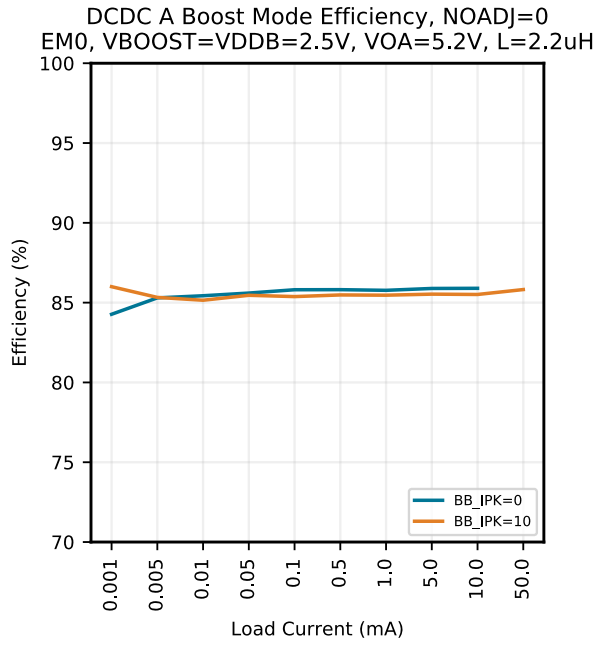


Figure 5.6. Typical DCDC A Boost Efficiency, VOA=5.2V, NOADJ=0



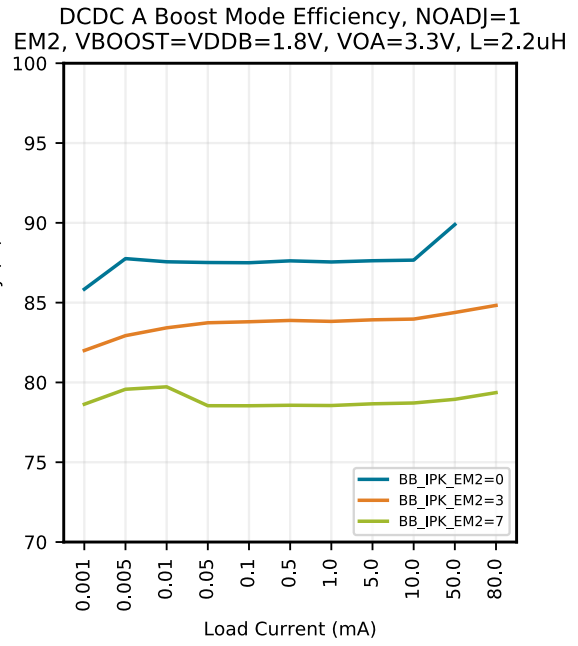
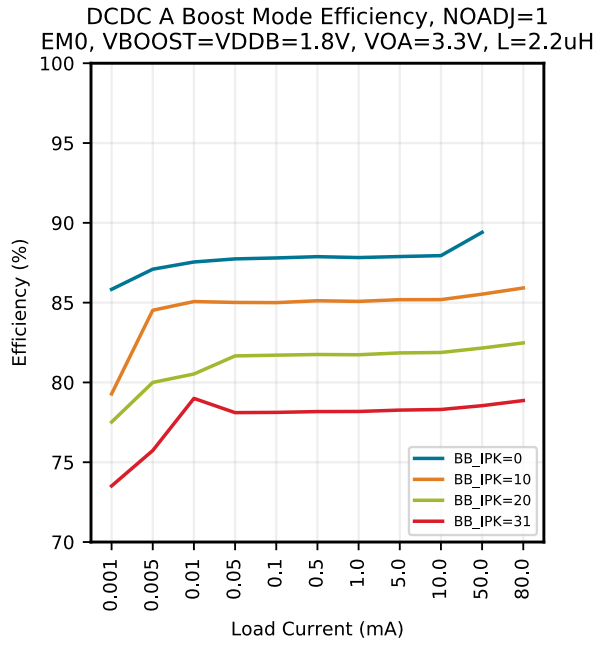
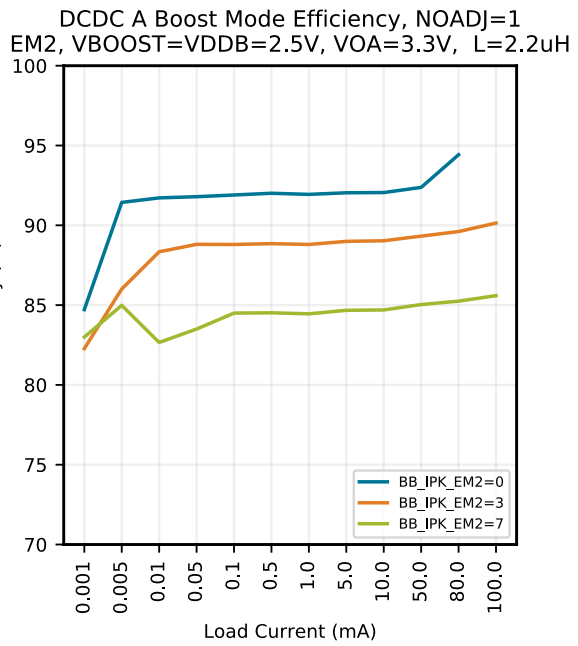
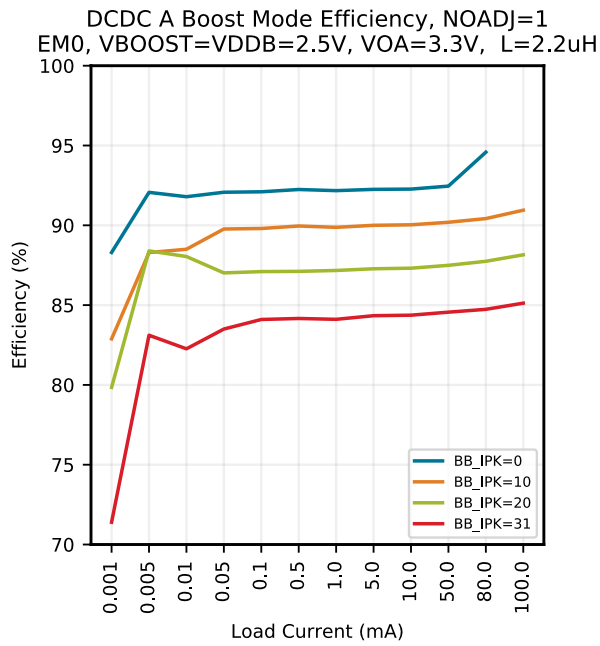


Figure 5.9. Typical DCDC A Boost Efficiency, VOA=3.3V, NOADJ=1



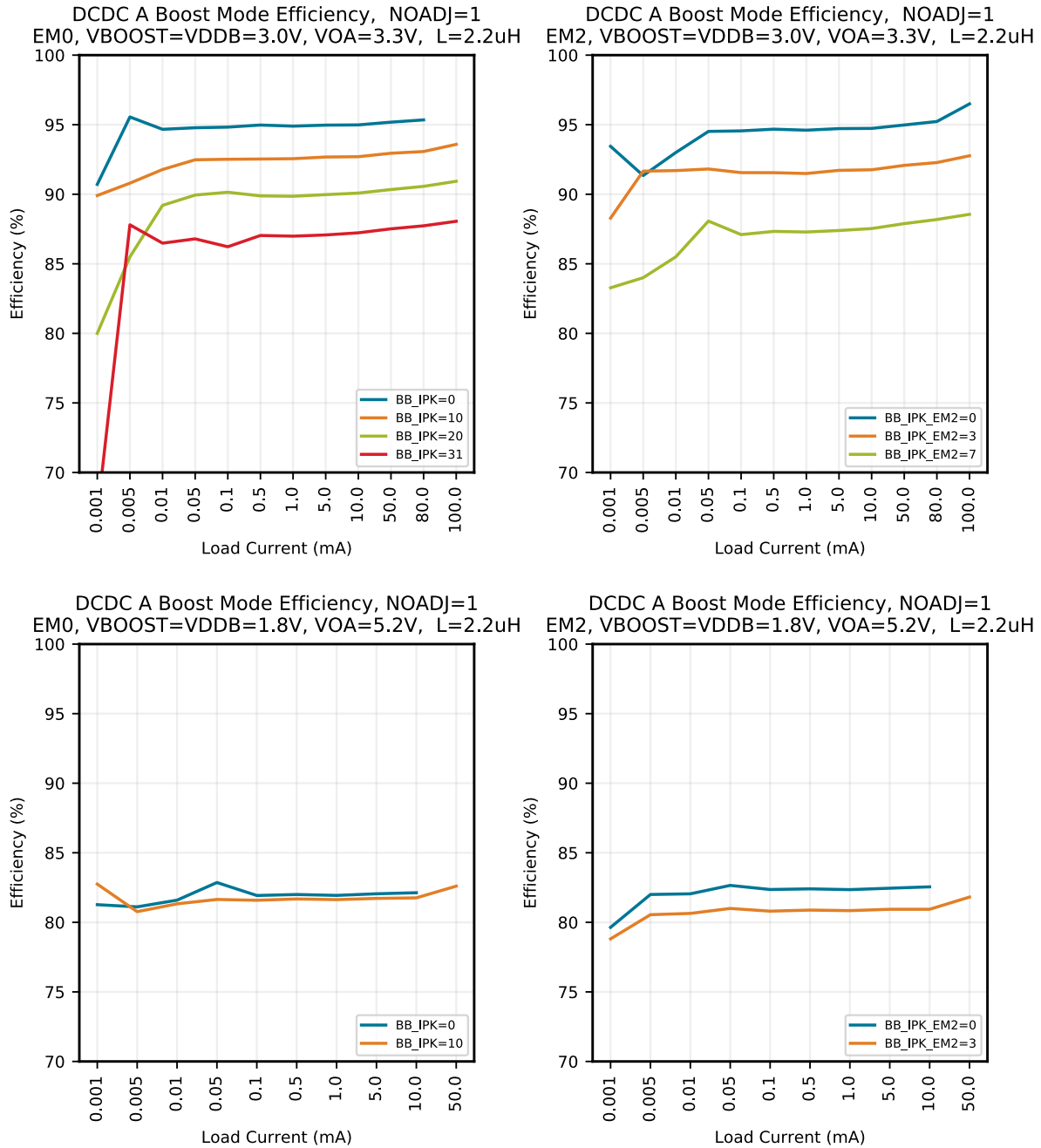


Figure 5.12. Typical DCDC A Boost Efficiency, VOA=5.2V, NOADJ=1

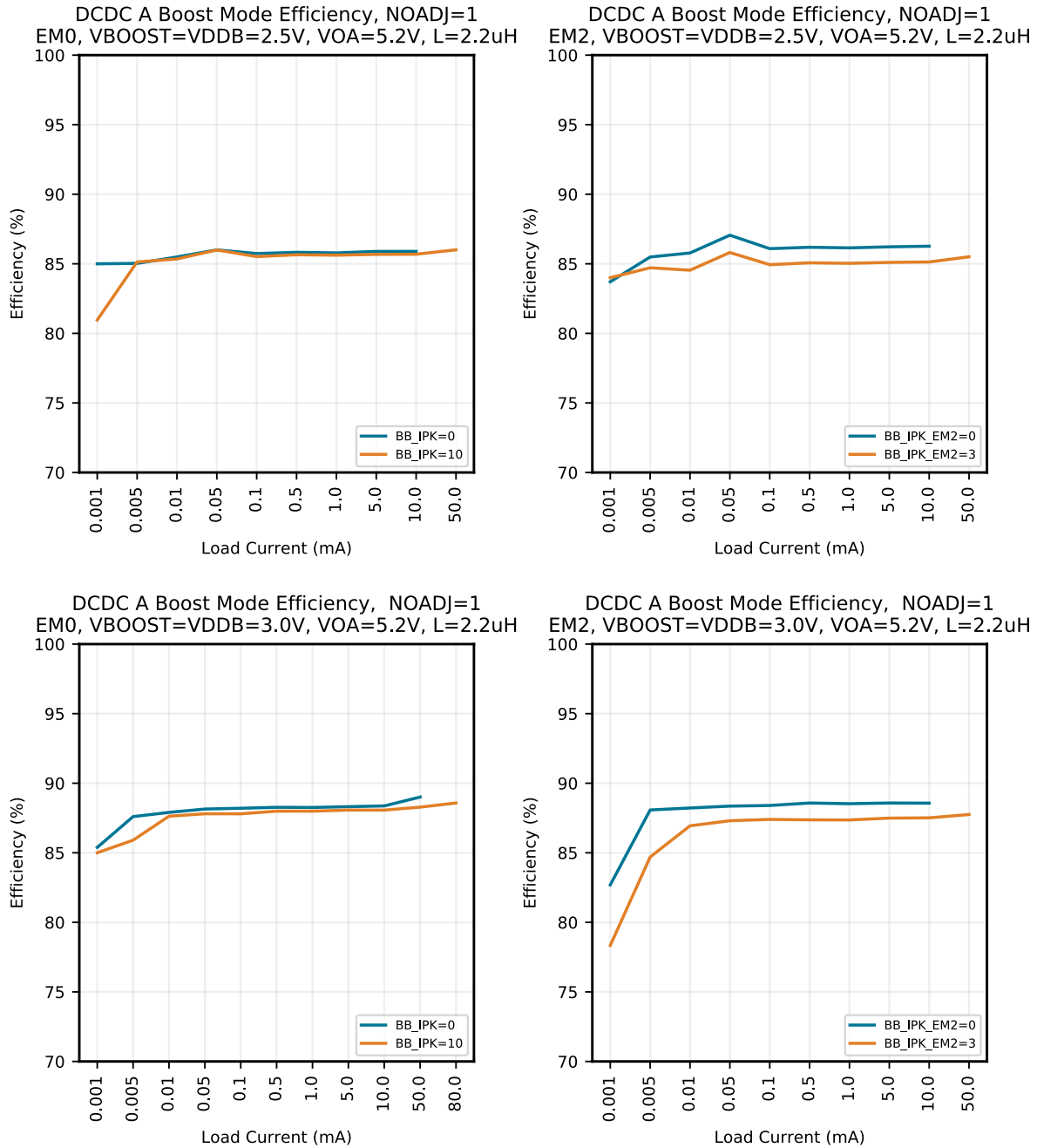
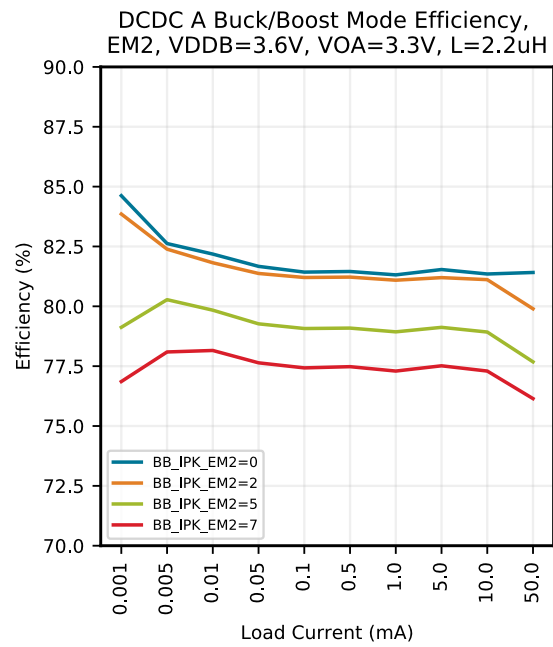
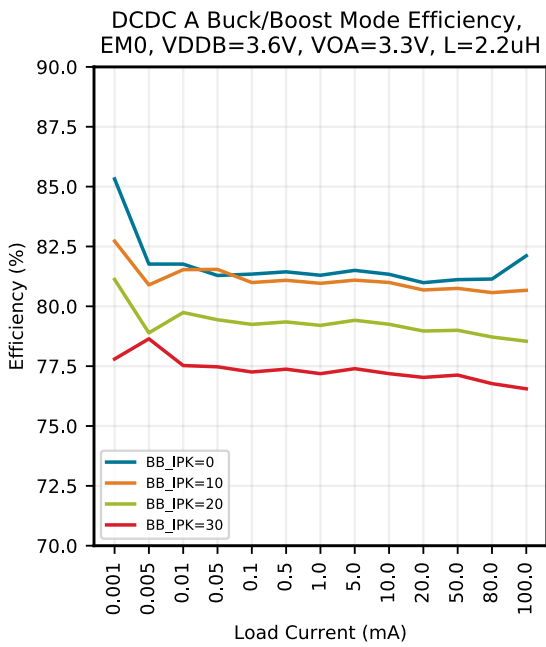
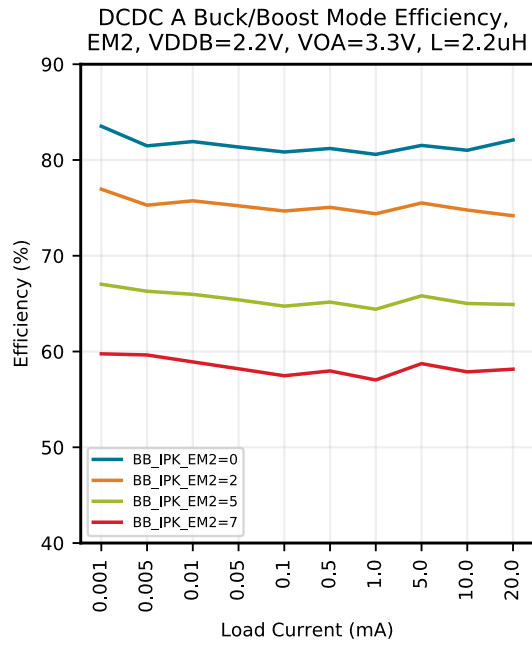
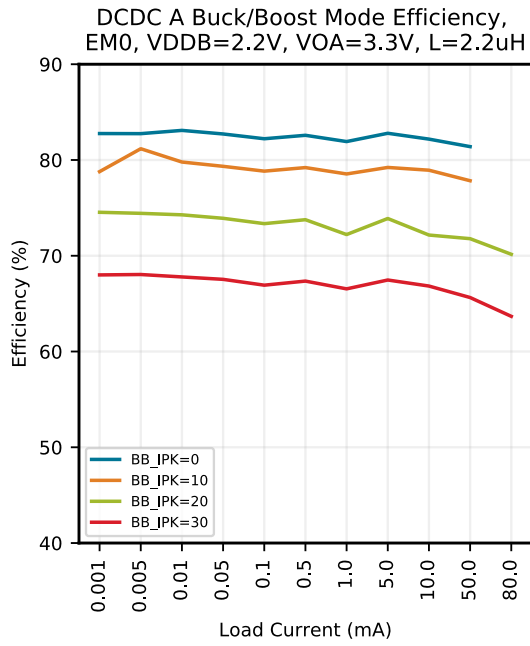


Figure 5.15. Typical DCDC A Buck/Boost Efficiency, VOA=3.3V



5.2.2 DCDC B Efficiency

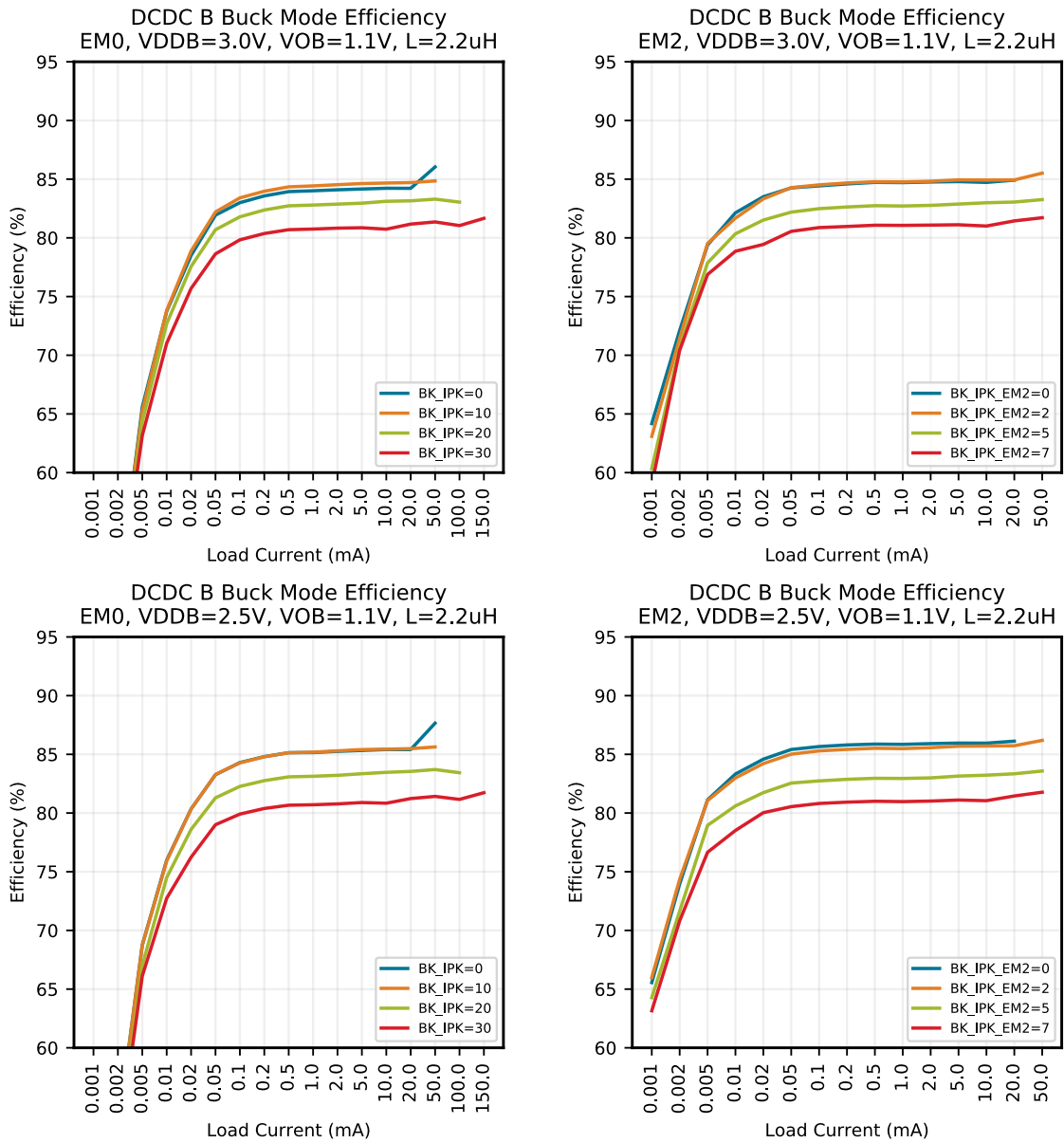
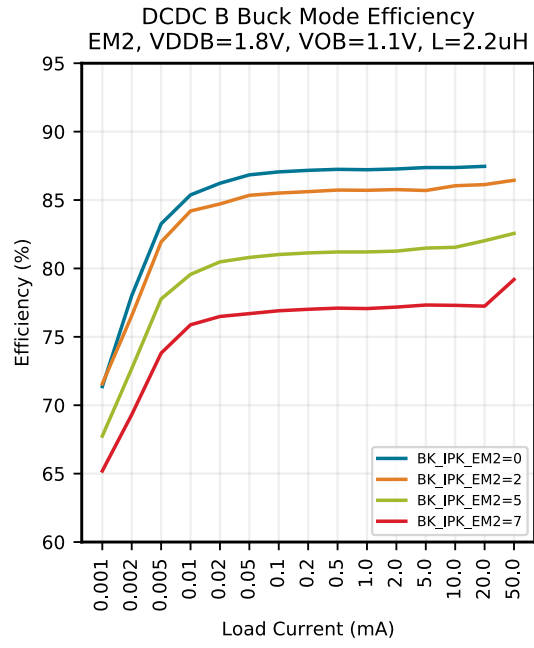
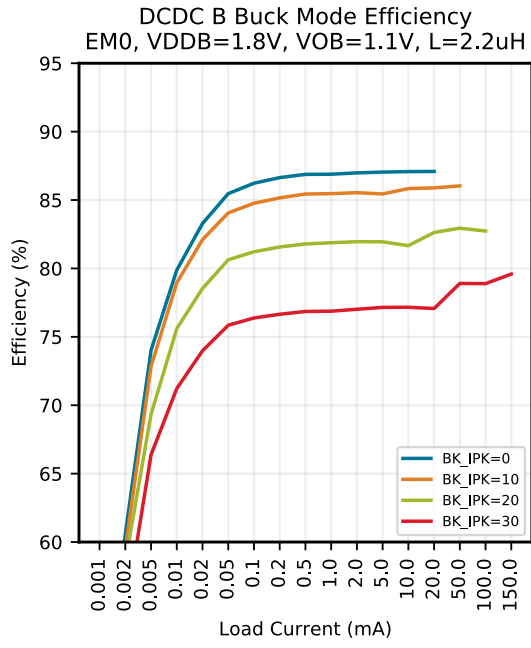


Figure 5.8. Typical DCDC B Buck Efficiency



5.2.3 Quiescent Current

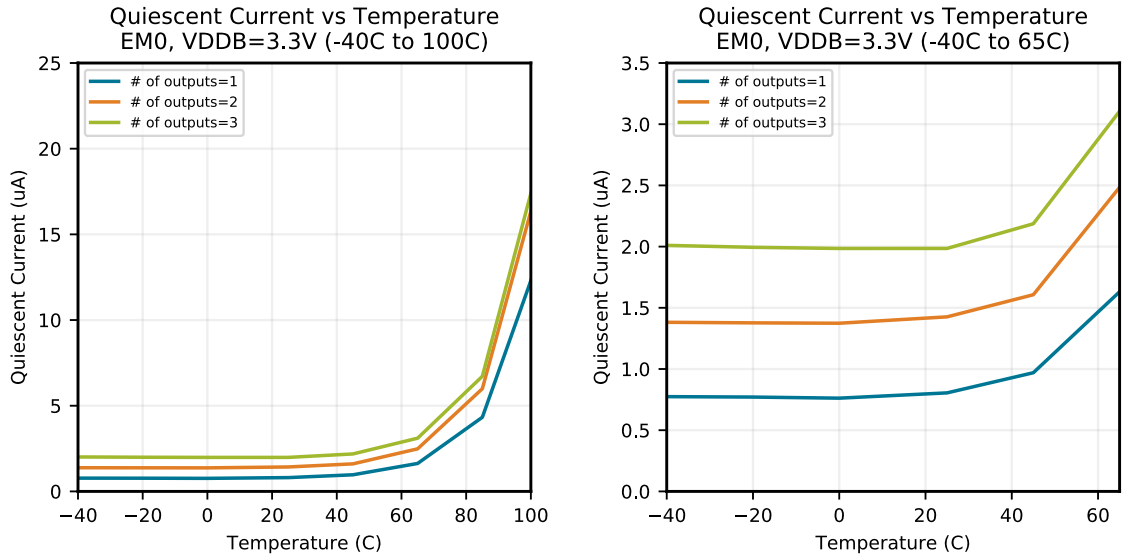


Figure 5.9. Typical EM0 Quiescent Current vs Temperature vs # of Outputs Enabled

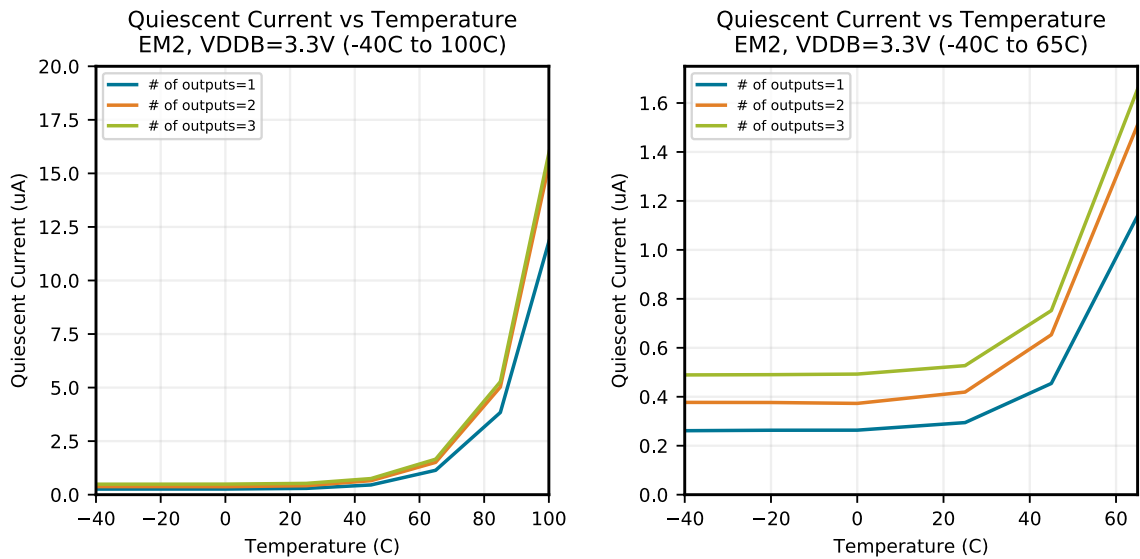


Figure 5.10. Typical EM2 Quiescent Current vs Temperature vs # of Outputs Enabled

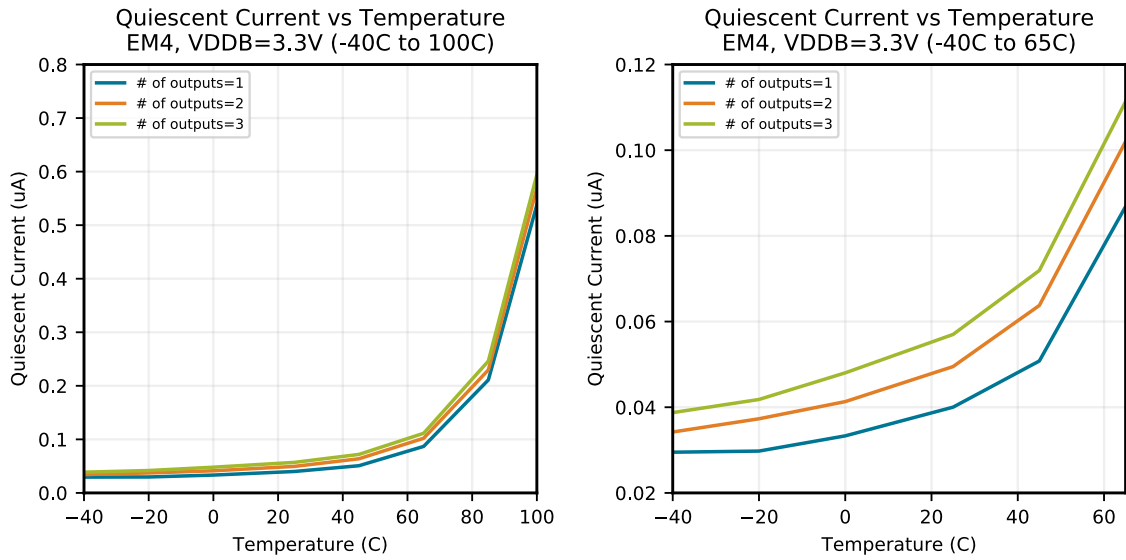


Figure 5.11. Typical EM4 Quiescent Current vs Temperature vs # of Outputs Enabled

5.2.4 RDS ON

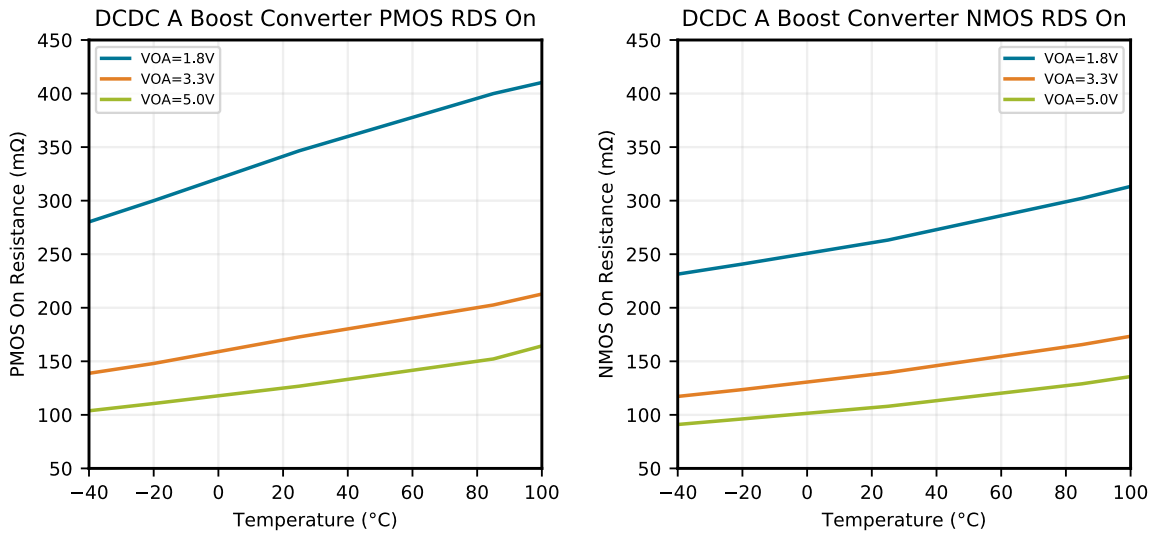


Figure 5.12. Typical DCDC A Boost Powertrain RDS ON vs Temperature

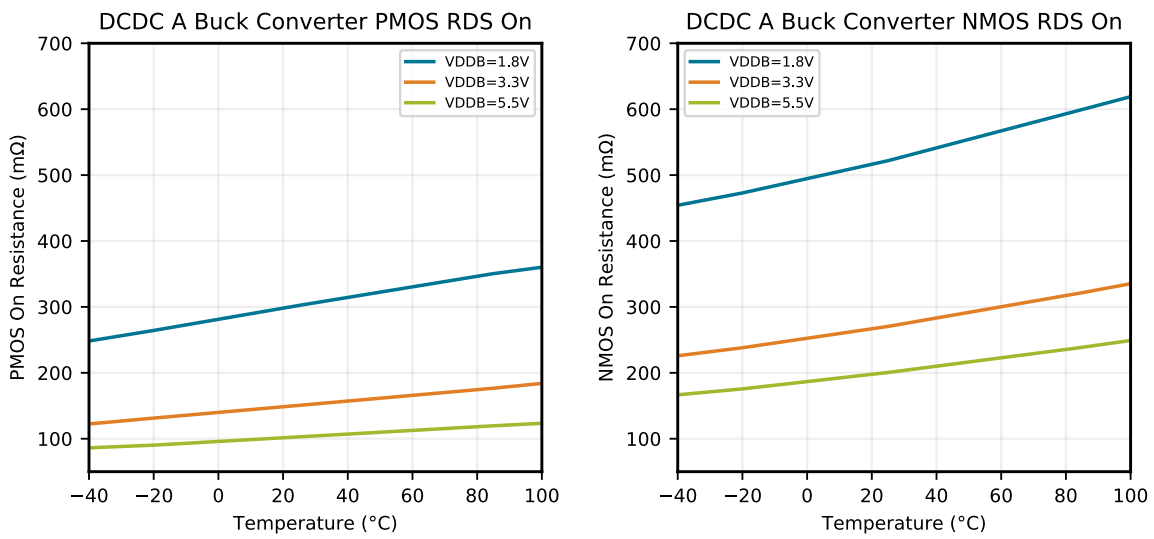


Figure 5.13. Typical DCDC A Buck Powertrain RDS ON vs Temperature

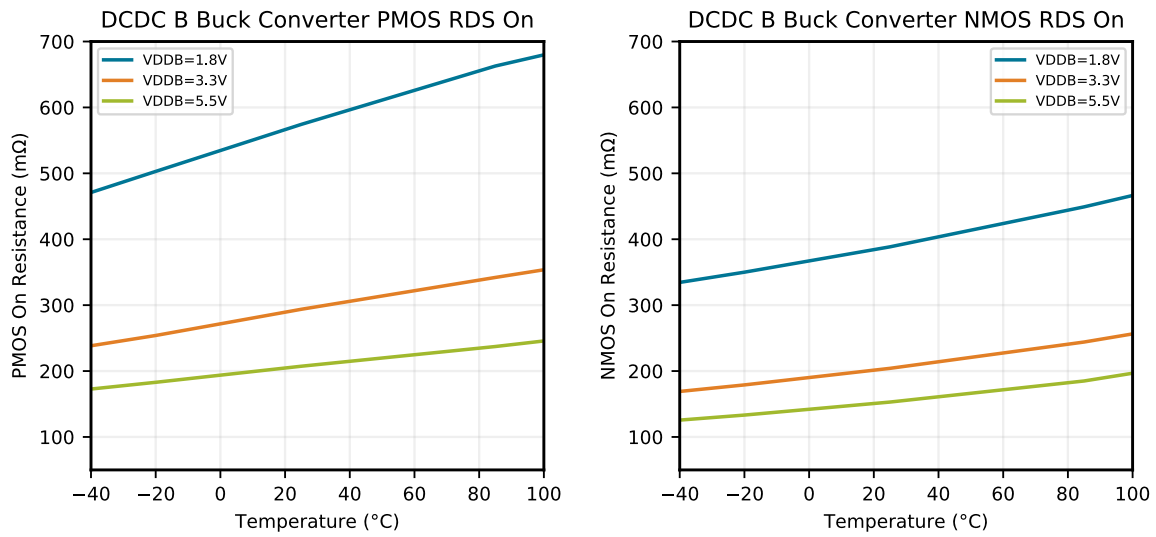


Figure 5.14. Typical DCDC B Buck Powertrain RDS ON vs Temperature

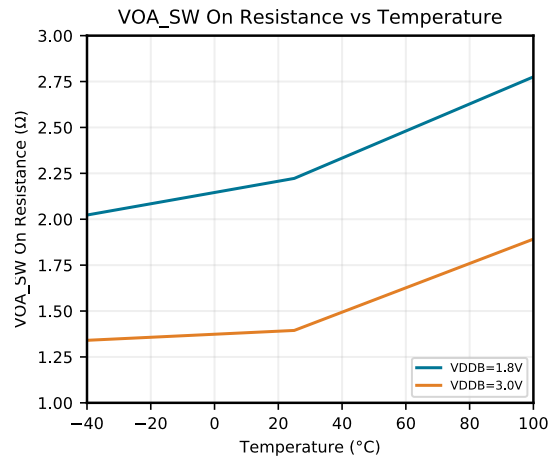


Figure 5.15. Typical VOASW RDS ON vs Temperature

5.2.5 Short Circuit Current

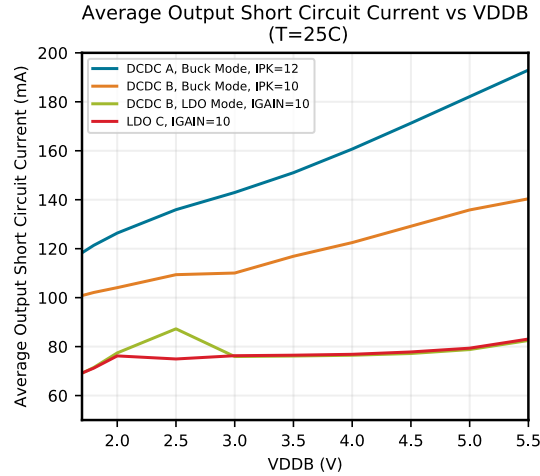


Figure 5.16. Typical Short Circuit Current vs VDDB

5.2.6 ADC

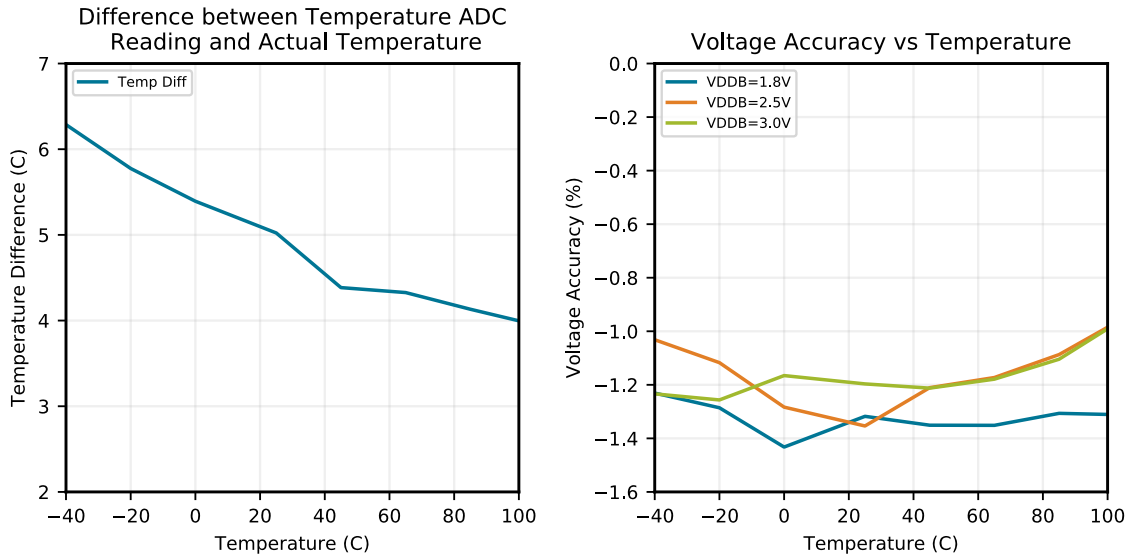


Figure 5.17. Typical ADC Accuracy vs Temperature

6. Register Definitions

6.1 Register Map

Note: Those registers below with a corresponding OTP Address will have their default values automatically overwritten by OTP-programmed values out of reset. Therefore, the actual values of those registers after reset may differ from the default reset values listed below. The [OTP Defaults](#) table shows the expected value of those registers out of reset.

| Address | Name | Access | OTP Address | Description |
|---------|----------------|------------|-------------|--|
| 0x00 | STATUS_G | read-write | - | Status Flags |
| 0x01 | STATUS_V | read-write | - | Status Flags |
| 0x02 | STATUS_GM | read-write | - | Status Flag Unmask |
| 0x03 | STATUS_VM | read-write | - | Status Flag Unmask |
| 0x04 | STATUS_LIVE | read-only | - | Live Status |
| 0x05 | DEVREV_ID | read-only | - | Device Information |
| 0x0A | CC_CAL | read-write | - | Coulomb Counting Configuration |
| 0x0B | OTP_ADDR | read-write | - | OTP Write Address |
| 0x0C | OTP_RDATA | read-only | - | OTP Read Address |
| 0x0E | OTP_STATCTRL | varies | - | OTP Control |
| 0x10 | CMD | write-only | - | Command |
| 0x12 | CC_MODE | read-only | - | Coulomb Counting Configuration |
| 0x13 | CCA_MSBY | read-only | - | VOA Coulomb Counter MS Byte |
| 0x14 | CCA_LSBY | read-only | - | VOA Coulomb Counter LS Byte |
| 0x15 | CCB0_MSBY | read-only | - | VOB EM0 Coulomb Counter MS Byte |
| 0x16 | CCB0_LSBY | read-only | - | VOB EM0 Coulomb Counter LS Byte |
| 0x17 | CCB2_MSBY | read-only | - | VOB EM2 Coulomb Counter MS Byte |
| 0x18 | CCB2_LSBY | read-only | - | VOB EM2 Coulomb Counter LS Byte |
| 0x19 | CCC_MSBY | read-only | - | VOC Coulomb Counter MS Byte |
| 0x1A | CCC_LSBY | read-only | - | VOC Coulomb Counter LS Byte |
| 0x1B | VDD_AVG_MSN | read-only | - | Average Measured VDDA/VDDB Voltage MS Nibble |
| 0x1C | VDD_AVG_LSBY | read-only | - | Average Measured VDDA/VDDB Voltage LS Byte |
| 0x1D | VDD_MIN_MSN | read-only | - | Minimum Measured VDDA/VDDB Voltage MS Nibble |
| 0x1E | VDD_MIN_LSBY | read-only | - | Minimum Measured VDDA/VDDB Voltage LS Byte |
| 0x1F | VDD_MAX_MSN | read-only | - | Maximum Measured VDDA/VDDB Voltage MS Nibble |
| 0x20 | VDD_MAX_LSBY | read-only | - | Maximum Measured VDDA/VDDB Voltage LS Byte |
| 0x21 | TEMP_MSN | read-only | - | Measured Temperature MS Nibble |
| 0x22 | TEMP_LSBY | read-only | - | Measured Temperature LS Byte |
| 0x23 | VOA_SW_STAT | read-only | - | Status |
| 0x40 | I2C_CTRL | read-write | 0x00 | I2C Control |
| 0x41 | CC_CTRL | read-write | 0x01 | Coulomb Counting Control |
| 0x43 | EM_CRSREG_CTRL | read-write | 0x03 | Energy Mode Control |

| Address | Name | Access | OTP Address | Description |
|---------|--------------|------------|-------------|------------------------|
| 0x49 | VOA_V | read-write | 0x09 | VOA Target Voltage |
| 0x4B | VOC_V | read-write | 0x0B | VOC Target Voltage |
| 0x4C | VOB_EM0_V | read-write | 0x0C | VOB EM0 Target Voltage |
| 0x4D | VOB_EM2_V | read-write | 0x0D | VOB EM2 Target Voltage |
| 0x4E | BIAS_SW | read-write | 0x0E | Bias Control |
| 0x4F | BB_IPK | read-write | 0x0F | DCDC A Control |
| 0x50 | BB_CTRL3 | read-write | 0x10 | DCDC A Control |
| 0x51 | BB_CTRL5 | read-write | 0x11 | DCDC A Control |
| 0x52 | BB_CTRL6 | read-write | 0x12 | DCDC A Control |
| 0x53 | LDOB_CTRL | read-write | 0x13 | LDO B Control |
| 0x54 | LDOC_CTRL | read-write | 0x14 | LDO C Control |
| 0x55 | LDOC_BB_CTRL | read-write | 0x15 | LDO C / DCDC A Control |
| 0x56 | BK_CTRL0 | read-write | 0x16 | DCDC B Control |
| 0x57 | BK_CTRL1 | read-write | 0x17 | DCDC B Control |
| 0x58 | BK_IPK | read-write | 0x18 | DCDC B Control |
| 0x59 | BK_CTRL2 | read-write | 0x19 | DCDC B Control |
| 0x5C | ADC_CC_CTRL | read-write | 0x1C | ADC Control |
| 0x5D | ADC_LIMITS | read-write | 0x1D | ADC Limits |

6.2 Register Description

6.2.1 STATUS_G

| Offset | Bit Position | | | | | | | |
|--------|--------------|------------|------------|------------|------------|------------|---------------|------------|
| 0x00 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | read-write | read-write | read-write | read-write | read-write | read-write | read-write | read-write |
| Name | VDD_LOW | CCC_ISDONE | CC_FULL | VOLT_FAULT | TEMP_FAULT | I2C_FAULT | OTP_CRC_FAULT | OTP_READ |

Table 6.1. STATUS_G

| Bit | Name | Reset | Access | Description |
|-----|------------|-------|------------|---|
| 7 | VDD_LOW | 0 | read-write | <p>Status flag indicating VDDDB (or VDDA if CC_MODE.SC_MODE=1) has fallen below threshold programmed in ADC_LIMITS.ADC_V_LIM since last clear. This flag requires ADC_CC_CTRL.ADC_INTERVAL be set to a non-zero value to ensure automatic periodic ADC readings are taken.</p> <p>Note this flag is masked by default - set corresponding bit in the STATUS_GM register to unmask.</p> <p>Can be cleared by writing a "1".</p> |
| 6 | CCC_ISDONE | 0 | read-write | <p>Status flag indicating coloumb counter calibration has completed since last clear.</p> <p>Note this flag is masked by default - set corresponding bit in the STATUS_GM register to unmask.</p> <p>Can be cleared by writing a "1".</p> |
| 5 | CC_FULL | 0 | read-write | <p>Status flag indicating any coloumb counter is over its programmed threshold (set by CC_CTRL>CC_THRSH) since last clear.</p> <p>Note this flag is masked by default - set corresponding bit in the STATUS_GM register to unmask.</p> <p>Can be cleared by writing a "1".</p> |
| 4 | VOLT_FAULT | 0 | read-write | <p>Status flag indicating any unmasked assertion of any flag in the STATUS_V register. To minimize firmware overhead, the VOLT_FAULT flag allows firmware to simply read a single status register (STATUS_G) on an IRQ event. Firmware would only need to read the STATUS_V register after determining the STATUS_G.VOLT_FAULT was set.</p> <p>Note this flag is masked by default - set corresponding bit in the STATUS_GM register to unmask.</p> <p>Can be cleared by writing a "1".</p> |

| Bit | Name | Reset | Access | Description |
|-----|---------------|-------|------------|--|
| 3 | TEMP_FAULT | 0 | read-write | <p>Status flag indicating an over temperature condition has occurred since last clear. Temperature threshold is set by ADC_LIMITS.ADC_T_LIM. This flag requires ADC_CC_CTRL.ADC_INTERVAL be set to a non-zero value to ensure automatic periodic ADC readings are taken.</p> <p>Note this flag is masked by default - set corresponding bit in the STATUS_GM register to unmask.</p> <p>Can be cleared by writing a "1".</p> |
| 2 | I2C_FAULT | 0 | read-write | <p>Status flag indicating an I2C fault has occurred since last clear.</p> <p>Note this flag is masked by default - set corresponding bit in the STATUS_GM register to unmask.</p> <p>Can be cleared by writing a "1".</p> |
| 1 | OTP_CRC_FAULT | 0 | read-write | <p>Status flag indicating an OTP CRC violation has occurred since last clear.</p> <p>Note this flag is masked by default - set corresponding bit in the STATUS_GM register to unmask.</p> <p>Can be cleared by writing a "1".</p> |
| 0 | OTP_READ | 0 | read-write | <p>Status flag indicating that OTP was read since last clear.</p> <p>This flag is expected to be set everytime the EFP01 is powered up, and should be cleared at power-up.</p> <p>It is recommended to keep this flag unmasked always to ensure that any EFP01 reset will result in an IRQ to the host MCU, allowing the host MCU to reinitialize any EFP01 registers.</p> <p>Note this flag is unmasked by default - therefore, every power-up and reset deassertion (which causes an OTP read), results in an unmasked flag and the IRQ pin assertion.</p> <p>Can be cleared by writing a "1".</p> |

6.2.2 STATUS_V

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|------------|------------|------------|------------|------------|------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x01 | | | | | | | | |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | | read-write | read-write | read-write | read-write | read-write | read-write |
| Name | | | VOC_ISLOW | VOB_ISLOW | VOA_ISLOW | VOC_ISGOOD | VOB_ISGOOD | VOA_ISGOOD |

Table 6.2. STATUS_V

| Bit | Name | Reset | Access | Description |
|-----|------------|-------|------------|---|
| 7:6 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 5 | VOC_ISLOW | 0 | read-write | Status flag indicating the VOC output has transitioned from in regulation -> out of regulation since last clear. Can be cleared by writing a "1". |
| 4 | VOB_ISLOW | 0 | read-write | Status flag indicating the VOB output has transitioned from in regulation -> out of regulation since last clear. Note that depending on voltage programming, an energy mode transition from EM2 to EM0 may cause assertion. Can be cleared by writing a "1". |
| 3 | VOA_ISLOW | 0 | read-write | Status flag indicating the VOA output has transitioned from in regulation -> out of regulation since last clear. Can be cleared by writing a "1". |
| 2 | VOC_ISGOOD | 0 | read-write | Status flag indicating the VOC output has transitioned from out of regulation -> into regulation since last clear. Note that if an output voltage target change is very small, the output may never be reported as out of regulation, and this flag will therefore never be set. It is recommended to use the STATUS_LIVE.VOC_IN-REG_LIVE bit instead to determine if the output is in regulation. Can be cleared by writing a "1". |
| 1 | VOB_ISGOOD | 0 | read-write | Status flag indicating the VOB output has transitioned from out of regulation -> into regulation since last clear. Note that when changing the output voltage target, if the change is very small the output will never be reported as out of regulation, and this flag will therefore never be set. It is recommended to use the STATUS_LIVE.VOB_IN-REG_LIVE bit instead to determine if the output is in regulation. Can be cleared by writing a "1". |

| Bit | Name | Reset | Access | Description |
|-----|------------|-------|------------|---|
| 0 | VOA_ISGOOD | 0 | read-write | <p>Status flag indicating the VOA output has transitioned from out of regulation -> into regulation since last clear. Note that when changing the output voltage target, if the change is very small the output will never be reported as out of regulation, and this flag will therefore never be set.</p> <p>It is recommended to use the STATUS_LIVE.VOA_IN-REG_LIVE bit instead to determine if the output is in regulation.</p> <p>Can be cleared by writing a "1".</p> |

6.2.3 STATUS_GM

| Offset | Bit Position | | | | | | | |
|---------------|----------------|-------------------|----------------|-------------------|-------------------|------------------|----------------------|-----------------|
| 0x02 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Access | read-write | read-write | read-write | read-write | read-write | read-write | read-write | read-write |
| Name | VDD_LOW_UNMASK | CCC_ISDONE_UNMASK | CC_FULL_UNMASK | VOLT_FAULT_UNMASK | TEMP_FAULT_UNMASK | I2C_FAULT_UNMASK | OTP_CRC_FAULT_UNMASK | OTP_READ_UNMASK |

Table 6.3. STATUS_GM

| Bit | Name | Reset | Access | Description |
|-----|----------------------|-------|------------|---|
| 7 | VDD_LOW_UNMASK | 0 | read-write | Set to unmask VDD Low status flag in the STATUS_G register. |
| 6 | CCC_ISDONE_UNMASK | 0 | read-write | Set to unmask Coulomb Counting Calibration status flag in the STATUS_G register. |
| 5 | CC_FULL_UNMASK | 0 | read-write | Set to unmask Coulomb Counting over Threshold status flag in the STATUS_G register. |
| 4 | VOLT_FAULT_UNMASK | 0 | read-write | Set to unmask Voltage Fault status flag in the STATUS_G register. |
| 3 | TEMP_FAULT_UNMASK | 0 | read-write | Set to unmask Temperature Fault status flag in the STATUS_G register. |
| 2 | I2C_FAULT_UNMASK | 0 | read-write | Set to unmask I2C Fault status flag in the STATUS_G register. |
| 1 | OTP_CRC_FAULT_UNMASK | 0 | read-write | Set to unmask OTP CRC violation status flag in the STATUS_G register. |
| 0 | OTP_READ_UNMASK | 1 | read-write | Set to unmask OTP Read status flag in the STATUS_G register. This bit is set by default - therefore, every power-up and reset deassertion (which causes an OTP read), results in an unmasked flag and the IRQ pin assertion. It is recommended to keep this flag unmasked always to ensure that any EFP01 reset will result in an IRQ to the host MCU, allowing the host MCU to reinitialize any EFP01 registers. |

6.2.4 STATUS_VM

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|------------------|------------------|------------------|-------------------|-------------------|-------------------|
| 0x03 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | | read-write | read-write | read-write | read-write | read-write | read-write |
| Name | | | VOC_ISLOW_UNMASK | VOB_ISLOW_UNMASK | VOA_ISLOW_UNMASK | VOC_ISGOOD_UNMASK | VOB_ISGOOD_UNMASK | VOA_ISGOOD_UNMASK |

Table 6.4. STATUS_VM

| Bit | Name | Reset | Access | Description |
|-----|-------------------|-------|------------|--|
| 7:6 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 5 | VOC_ISLOW_UNMASK | 0 | read-write | Set to unmask VOC_ISLOW status flag in the STATUS_V register. |
| 4 | VOB_ISLOW_UNMASK | 0 | read-write | Set to unmask VOB_ISLOW status flag in the STATUS_V register. |
| 3 | VOA_ISLOW_UNMASK | 0 | read-write | Set to unmask VOA_ISLOW status flag in the STATUS_V register. |
| 2 | VOC_ISGOOD_UNMASK | 0 | read-write | Set to unmask VOC_ISGOOD status flag in the STATUS_V register. |
| 1 | VOB_ISGOOD_UNMASK | 0 | read-write | Set to unmask VOB_ISGOOD status flag in the STATUS_V register. |
| 0 | VOA_ISGOOD_UNMASK | 0 | read-write | Set to unmask VOA_ISGOOD status flag in the STATUS_V register. |

6.2.5 STATUS_LIVE

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|-----------|--------------|--------------|----------------|----------------|----------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x04 | | | | | | | | |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | | | read-only | read-only | read-only | read-only | read-only | read-only |
| Name | | | CCC_LIVE | TEMP_HI_LIVE | VDD_LOW_LIVE | VOC_INREG_LIVE | VOB_INREG_LIVE | VOA_INREG_LIVE |

Table 6.5. STATUS_LIVE

| Bit | Name | Reset | Access | Description |
|-----|----------------|-------|-----------|---|
| 7:6 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 5 | CCC_LIVE | 0 | read-only | Live view of Coulomb counter calibration operation busy status |
| 4 | TEMP_HI_LIVE | 0 | read-only | Live view of temperature threshold status. This bit requires ADC_CC_CTRL.ADC_INTERVAL be set to a non-zero value to ensure automatic periodic ADC readings are taken. |
| 3 | VDD_LOW_LIVE | 0 | read-only | Live view of VDDB / VDDA threshold status. This bit requires ADC_CC_CTRL.ADC_INTERVAL be set to a non-zero value to ensure automatic periodic ADC readings are taken. |
| 2 | VOC_INREG_LIVE | 0 | read-only | Live view of VOC regulation status. This output is only valid when LDO C is enabled and not used in parallel with DCDC A. |
| 1 | VOB_INREG_LIVE | 0 | read-only | Live view of VOB regulation status. This output is only valid when DCDC B is enabled. |
| 0 | VOA_INREG_LIVE | 0 | read-only | Live view of VOA regulation status. This output is only valid when DCDC A is enabled. |

6.2.6 DEVREV_ID

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|---|-----------|---|---|---|---|
| 0x05 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | 0x1A | | | | |
| Access | read-only | | | read-only | | | | |
| Name | REV_ID | | | DEV_ID | | | | |

Table 6.6. DEVREV_ID

| Bit | Name | Reset | Access | Description |
|-----|--------|-------|-----------|--|
| 7:5 | REV_ID | 0x00 | read-only | EFP01 Revision ID: REV D: 0x01 REV E: 0x00 |
| 4:0 | DEV_ID | 0x1A | read-only | EFP01 Device ID: REV D: 0x19 REV E: 0x1A |

6.2.7 CC_CAL

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|------------|---|------------|---|---|
| 0x0A | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | 0x00 | | 0x00 | | |
| Access | read-write | | | read-write | | read-write | | |
| Name | CC_CAL_NREQ | | | CCL_SEL | | CCL_LVL | | |

Table 6.7. CC_CAL

| Bit | Name | Reset | Access | Description |
|-----|-------------|-------|------------|---|
| 7:5 | CC_CAL_NREQ | 0x00 | read-write | Configures the number of pulses required to be counted during Coulomb counter calibration, where the number of pulses required is $2^{(CC_CAL_NREQ+1)}$. Note that the number of pulses counted during calibration is not affected by the the prescaler (CC_CTRL.CC_PRESCCL). |
| 4:3 | CCL_SEL | 0x00 | read-write | Coulomb counter load select. During calibration, the load current selected by CCL_LVL will be applied to the output selected by CCL_SEL. |
| | Value | Mode | | Description |
| | 0 | NONE | | None |
| | 1 | VOA | | VOA output |
| | 2 | VOB | | VOB output |
| | 3 | VOC | | VOC output |
| 2:0 | CCL_LVL | 0x00 | read-write | Coulomb counter load current source. For $0 \leq CCL_LVL \leq 3$: $CC_Cal_Low = \text{from2sComplement}(\text{OTP_CCCAL_LOW}) * 1.5725\mu\text{A} + 0.87\text{mA}$ For $4 \leq CCL_LVL \leq 7$: $CC_Cal_High = \text{from2sComplement}(\text{OTP_CCCAL_HIGH}) * 23.4375\mu\text{A} + 13.9\text{mA}$ |
| | Value | Mode | | Description |
| | 0 | 440UA | | 0.440 mA nominal, $CC_Cal_Low * 0.5094$ calibrated |
| | 1 | 550UA | | 0.550 mA nominal, $CC_Cal_Low * 0.6352$ calibrated |
| | 2 | 700UA | | 0.700 mA nominal, $CC_Cal_Low * 0.802$ calibrated |
| | 3 | 875UA | | 0.875 mA nominal, $CC_Cal_Low * 1.0$ calibrated |

| Bit | Name | Reset | Access | Description |
|-----|------|---------|--------|--|
| 4 | | 7060UA | | 7.06 mA nominal, CC_Cal_High * 0.5094 calibrated |
| 5 | | 8830UA | | 8.83 mA nominal, CC_Cal_High * 0.6352 calibrated |
| 6 | | 11200UA | | 11.20 mA nominal, CC_Cal_High * 0.802 calibrated |
| 7 | | 14000UA | | 14.00 mA nominal, CC_Cal_High * 1.0 calibrated |

6.2.8 OTP_ADDR

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x0B | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-write | | | | | | | |
| Name | OTP_ADDR | | | | | | | |

Table 6.8. OTP_ADDR

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|------------|-----------------------------------|
| 7 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 6:0 | OTP_ADDR | 0x00 | read-write | OTP address for reads and writes. |

6.2.9 OTP_RDATA

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x0C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | OTP_RDATA | | | | | | | |

Table 6.9. OTP_RDATA

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|-----------|-----------------------|
| 7:0 | OTP_RDATA | 0x00 | read-only | OTP data from reading |

6.2.10 OTP_STATCTRL

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|---|---|-----------|-------------|---|---|
| 0x0E | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | | | 0 | 0 | | |
| Access | | | | | read-only | read-write | | |
| Name | | | | | OTP_BUSY | CMD_READOTP | | |

Table 6.10. OTP_STATCTRL

| Bit | Name | Reset | Access | Description |
|-----|-------------|-------|------------|--|
| 7:4 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 3 | OTP_BUSY | 0 | read-only | OTP state machine busy indicator. Firmware can poll this bit to determine when the OTP read is complete. |
| 2 | CMD_READOTP | 0 | read-write | Read OTP command. |
| 1:0 | RESERVED | 0 | | Reserved. Always write bits to 0. |

6.2.11 CMD

| Offset | Bit Position | | | | | | | |
|--------|--------------|------------|------------|-------------|---|------------|---|------------|
| 0x10 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | | 0 | | 0 |
| Access | write-only | write-only | write-only | write-only | | write-only | | write-only |
| Name | ADC_START | ADC_CLR | CC_CLR | CC_CAL_STRT | | OTP_REREAD | | RESET |

Table 6.11. CMD

| Bit | Name | Reset | Access | Description |
|-----|-------------|-------|------------|---|
| 7 | ADC_START | 0 | write-only | Initiates a single ADC VDD Voltage measurement. Before kicking of the ADC measurement, firmware should set ADC_CC_CTRL.ADC_INTERVAL=0 to disable automated ADC operation and clear the ADC output registers. |
| 6 | ADC_CLR | 0 | write-only | If ADC_CLR is set, the next ADC voltage measurement value (triggered automatically or with ADC_START=1) will be loaded directly into all three 12-bit ADC output result registers. |
| 5 | CC_CLR | 0 | write-only | Clear all Coulomb counters (CCA_MSBY, CCA_LSBY, CCB0_MSBY, CCB0_LSBY, CCB2_MSBY, CCB2_LSBY, CCC_MSBY, CCC_LSBY) |
| 4 | CC_CAL_STRT | 0 | write-only | Initiate calibration of Coulomb counter |
| 3 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 2 | OTP_REREAD | 0 | write-only | Force OTP to be re-read. Will result in the internal control registers being overwritten to their out-of-reset default state. |
| 1 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 0 | RESET | 0 | write-only | Forces a full reset, equivalent to a power supply brownout. All internal registers will be cleared to '0', then the OPN defaults will be reloaded into the registers from OTP. Note use of this bit is not recommended. A reset means that any enabled DCDC outputs are going to be disabled (i.e, when their mode bitfields are cleared to '0') until the OTP default settings are loaded (which can take up to 400usec). The output voltage will be maintained during this period only by the output capacitor, resulting in a power supply-brownout if the load current is large enough to pull the output capacitor voltage below the brownout threshold. Recommend use of the OTP_REREAD bit instead, which will simply repaint the EFP01 registers with the default settings from OTP. Any converters enabled by default will remain enabled when using OTP_REREAD. |

6.2.12 CC_MODE

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|---|---|-----------|-----------|-----------|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x12 | | | | | | | | |
| Reset | | | | | 0 | 0 | 0x00 | |
| Access | | | | | read-only | read-only | read-only | |
| Name | | | | | SC_MODE | CCB_MODE | CCA_MODE | |

Table 6.12. CC_MODE

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|-------------|--|
| 7:4 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 3 | SC_MODE | 0 | read-only | Single Cell Mode indicator. Determined at power-on, based on voltage applied to VDDA pin. If a valid voltage is present at the VDDA pin, SC_MODE = 1; otherwise, SC_MODE = 0. |
| 2 | CCB_MODE | 0 | read-only | Mode of buck converter driving VOB. Calibration of the Coulomb counter (# of Coulombs per pulse, or CPP) depends on the mode of the converter. Calibration involves forcing the current mode (so it's not switching back and forth) for the calibration operation, which yields # of Coulombs per pulse (CPP) in that mode. If reading the CCB_MODE as part of the counter unloading process shows that the mode has changed, firmware should compute the CPP for the new mode. Note that addressing this read-only register causes an inhibition in the updating of the register, to ensure that the capture of the register is not corrupted by changes during the capture process. Users should address these registers only when they are actively reading them. |
| | Value | Mode | Description | |
| | 0 | BUCK | Buck Mode | |
| | 1 | LDOB | LDO Mode | |

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|-----------|---|
| 1:0 | CCA_MODE | 0x00 | read-only | <p>Mode of buck/boost converter driving VOA.</p> <p>Calibration of the Coulomb counter (# of Coulombs per pulse, or CPP) depends on the mode of the converter. Calibration involves forcing the current mode (so it's not switching back and forth) for the calibration operation, which yields # of Coulombs per pulse (CPP) in that mode. If reading the CCA_MODE as part of the counter unloading process shows that the mode has changed, firmware should compute the CPP for the new mode.</p> <p>Note that addressing this read-only register causes an inhibition in the updating of the register, to ensure that the capture of the register is not corrupted by changes during the capture process. Users should address these registers only when they are actively reading them.</p> |
| | Value | Mode | | Description |
| | 0 | BUCK | | Buck Mode |
| | 1 | AUTO | | Autonomous Buck/Boost Mode |
| | 2 | BOOST | | Boost Mode |
| | 3 | LDO | | LDO C Parallel Mode |

6.2.13 CCA_MSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x13 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCA_MSBY | | | | | | | |

Table 6.13. CCA_MSBY

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|-----------|--|
| 7:0 | CCA_MSBY | 0x00 | read-only | <p>Most significant byte of Coulomb counter value for VOA. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESC).</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.14 CCA_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x14 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCA_LSBY | | | | | | | |

Table 6.14. CCA_LSBY

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|-----------|---|
| 7:0 | CCA_LSBY | 0x00 | read-only | <p>Least significant byte of Coulomb counter for VOA. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESCCL).</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.15 CCB0_MSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x15 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCB0_MSBY | | | | | | | |

Table 6.15. CCB0_MSBY

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|-----------|---|
| 7:0 | CCB0_MSBY | 0x00 | read-only | <p>Most significant byte of Coulomb counter for VOB in EM0. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESC).</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.16 CCB0_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x16 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCB0_LSBY | | | | | | | |

Table 6.16. CCB0_LSBY

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|-----------|--|
| 7:0 | CCB0_LSBY | 0x00 | read-only | <p>Least significant byte of Coulomb counter for VOB in EM0. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESC).</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.17 CCB2_MSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x17 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCB2_MSBY | | | | | | | |

Table 6.17. CCB2_MSBY

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|-----------|---|
| 7:0 | CCB2_MSBY | 0x00 | read-only | <p>Most significant byte of Coulomb counter for VOB in EM2. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESC).</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.18 CCB2_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x18 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCB2_LSBY | | | | | | | |

Table 6.18. CCB2_LSBY

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|-----------|--|
| 7:0 | CCB2_LSBY | 0x00 | read-only | <p>Least significant byte of Coulomb counter for VOB in EM2. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESC).</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.19 CCC_MSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x19 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCC_MSBY | | | | | | | |

Table 6.19. CCC_MSBY

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|-----------|---|
| 7:0 | CCC_MSBY | 0x00 | read-only | <p>Most significant byte of Coulomb counter for VOC in LDOC stand-alone mode. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESC).</p> <p>Note that during the calibration of all 3 Coulomb Counters, the CCC counter is used for counting the 10MHz clock cycles that occur during the calibration event. Until the next subsequent CC_CLR event, reading the CCC_MSBY and CCC_LSBY registers returns the 16-bit result from the 10MHz counting operation. To preserve any existing count in the CCC counter, firmware should read and store the CCC registers before initiating a Coulomb Counter calibration event.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.20 CCC_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x1A | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | CCC_LSBY | | | | | | | |

Table 6.20. CCC_LSBY

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|-----------|--|
| 7:0 | CCC_LSBY | 0x00 | read-only | <p>Least significant byte of Coulomb counter for VOC in LDOC stand-alone mode. Each count represents a number of PFM pulses, determined by the prescaler setting (CC_CTRL.CC_PRESC).</p> <p>Note that during the calibration of all 3 Coulomb Counters, the CCC counter is used for counting the 10MHz clock cycles that occur during the calibration event. Until the next subsequent CC_CLR event, reading the CCC_MSBY and CCC_LSBY registers returns the 16-bit result from the 10MHz counting operation. To preserve any existing count in the CCC counter, firmware should read and store the CCC registers before initiating a Coulomb Counter calibration event.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register. Because this can result in some small amount of missed Coulomb counter counts, users should address these registers only when they are actively reading them.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored in a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> |

6.2.21 VDD_AVG_MSN

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|-------------|---|---|---|
| 0x1B | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | | | 0x00 | | | |
| Access | | | | | read-only | | | |
| Name | | | | | VDD_AVG_MSN | | | |

Table 6.21. VDD_AVG_MSN

| Bit | Name | Reset | Access | Description |
|-----|-------------|-------|-----------|--|
| 7:4 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 3:0 | VDD_AVG_MSN | 0x00 | read-only | <p>Most significant nibble of measured VDDA or VDDDB pin IIR low-pass filtered average voltage since last clear. The time constant of the IIR filter is set by ADC_CC_CTRL.ADC_IIR_TAU. The VDDA pin will be measured only if a supply is present on that pin (i.e., CC_MODE.SC_MODE=1), otherwise the VDDDB pin is measured.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> $\text{VDDDB (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.49$ $\text{VDDA (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.01$ |

6.2.22 VDD_AVG_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x1C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | VDD_AVG_LSBY | | | | | | | |

Table 6.22. VDD_AVG_LSBY

| Bit | Name | Reset | Access | Description |
|-----|--------------|-------|-----------|--|
| 7:0 | VDD_AVG_LSBY | 0x00 | read-only | <p>Least significant byte of measured VDDA or VDDB pin IIR low-pass filtered average voltage since last clear. The time constant of the IIR filter is set by ADC_CC_CTRL.ADC_IIR_TAU. The VDDA pin will be measured only if a supply is present on that pin (i.e., CC_MODE.SC_MODE=1), otherwise the VDDB pin is measured.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> $\text{VDDB (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.49$ $\text{VDDA (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.01$ |

6.2.23 VDD_MIN_MSN

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|-------------|---|---|---|
| 0x1D | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | | | 0x00 | | | |
| Access | | | | | read-only | | | |
| Name | | | | | VDD_MIN_MSN | | | |

Table 6.23. VDD_MIN_MSN

| Bit | Name | Reset | Access | Description |
|-----|-------------|-------|-----------|---|
| 7:4 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 3:0 | VDD_MIN_MSN | 0x00 | read-only | <p>Most significant nibble of measured VDDA or VDDDB voltage min since last clear. The VDDA pin will be measured only if a supply is present on that pin (i.e., CC_MODE.SC_MODE=1), otherwise the VDDDB pin is measured.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> <p>$VDDDB (mV) = ((VDD_xxx_MSN \ll 8) + VDD_xxx_LSBY) \times 1.49$</p> <p>$VDDA (mV) = ((VDD_xxx_MSN \ll 8) + VDD_xxx_LSBY) \times 1.01$</p> |

6.2.24 VDD_MIN_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x1E | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | VDD_MIN_LSBY | | | | | | | |

Table 6.24. VDD_MIN_LSBY

| Bit | Name | Reset | Access | Description |
|-----|--------------|-------|-----------|---|
| 7:0 | VDD_MIN_LSBY | 0x00 | read-only | <p>Least significant byte of measured VDDA or VDDB voltage min since last clear. The VDDA pin will be measured only if a supply is present on that pin (i.e., CC_MODE.SC_MODE=1), otherwise the VDDB pin is measured.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> $\text{VDDB (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.49$ $\text{VDDA (mV)} = ((\text{VDD_xxx_MSN} \ll 8) + \text{VDD_xxx_LSBY}) \times 1.01$ |

6.2.25 VDD_MAX_MSN

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|-------------|---|---|---|
| 0x1F | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | | | 0x00 | | | |
| Access | | | | | read-only | | | |
| Name | | | | | VDD_MAX_MSN | | | |

Table 6.25. VDD_MAX_MSN

| Bit | Name | Reset | Access | Description |
|-----|-------------|-------|-----------|---|
| 7:4 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 3:0 | VDD_MAX_MSN | 0x00 | read-only | <p>Most significant nibble of measured VDDA or VDDDB voltage max since last clear. The VDDA pin will be measured only if a supply is present on that pin (i.e., CC_MODE.SC_MODE=1), otherwise the VDDDB pin is measured.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> $VDDDB \text{ (mV)} = ((VDD_xxx_MSN \ll 8) + VDD_xxx_LSBY) \times 1.49$ $VDDA \text{ (mV)} = ((VDD_xxx_MSN \ll 8) + VDD_xxx_LSBY) \times 1.01$ |

6.2.26 VDD_MAX_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x20 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | VDD_MAX_LSBY | | | | | | | |

Table 6.26. VDD_MAX_LSBY

| Bit | Name | Reset | Access | Description |
|-----|--------------|-------|-----------|---|
| 7:0 | VDD_MAX_LSBY | 0x00 | read-only | <p>Least significant byte of measured VDDA or VDDB voltage max since last clear. The VDDA pin will be measured only if a supply is present on that pin (i.e., CC_MODE.SC_MODE=1), otherwise the VDDB pin is measured.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> <p>$VDD_B (mV) = ((VDD_xxx_MSN \ll 8) + VDD_xxx_LSBY) \times 1.49$</p> <p>$VDD_A (mV) = ((VDD_xxx_MSN \ll 8) + VDD_xxx_LSBY) \times 1.01$</p> |

6.2.27 TEMP_MSN

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|---|---|-----------|---|---|---|
| 0x21 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | | | 0x00 | | | |
| Access | | | | | read-only | | | |
| Name | | | | | TEMP_MSN | | | |

Table 6.27. TEMP_MSN

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|-----------|--|
| 7:4 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 3:0 | TEMP_MSN | 0x00 | read-only | Most significant nibble of most recently measured temperature. |

Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.

To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.

Temperature (C) = $40 + (\text{convert_from_2s_complement}((\text{TEMP_MSN} \ll 8) + \text{TEMP_LSBY}) + 2) / 6.04236$

6.2.28 TEMP_LSBY

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x22 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-only | | | | | | | |
| Name | TEMP_LSBY | | | | | | | |

Table 6.28. TEMP_LSBY

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|-----------|--|
| 7:0 | TEMP_LSBY | 0x00 | read-only | <p>Least significant byte of most recently measured temperature.</p> <p>Note that this value is spread over 2 registers and may be continuously updated. To ensure that the capture of the register is not corrupted by changes during the capture process, addressing this read-only register causes an inhibition in the updating of the register.</p> <p>To ensure coherence when reading the most significant and least significant bytes, a MSBY register read causes the corresponding LSBY register value to be stored into a shadow register. Reading the LSBY register will then return the value stored in the LSBY shadow register.</p> <p>Temperature (C) = $40 + (\text{convert_from_2s_complement}((\text{TEMP_MSN} \ll 8) + \text{TEMP_LSBY}) + 2) / 6.04236$</p> |

6.2.29 VOA_SW_STAT

| Offset | Bit Position | | | | | | | | |
|---------------|--------------|---|---|---|---|---|---|---|--------------|
| 0x23 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reset | | | | | | | | | 0 |
| Access | | | | | | | | | read-only |
| Name | | | | | | | | | VOA_SW_ISLOW |

Table 6.29. VOA_SW_STAT

| Bit | Name | Reset | Access | Description |
|-----|--------------|-------|-----------|--|
| 7:1 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 0 | VOA_SW_ISLOW | 0 | read-only | Asserted when the VOA_SW is enabled (see VOA_SW_CON), but the VOA_SW pin voltage is still well below the VOA pin voltage. Polling this after enabling the switch is the recommended method of determining whether the VOA switch turn-on has completed. |

6.2.30 I2C_CTRL

| Offset | Bit Position | | | | | | | | |
|---------------|--------------|---|---|---|---|---|---|---|------------|
| 0x40 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reset | | | | | | | | | 0 |
| Access | | | | | | | | | read-write |
| Name | | | | | | | | | I2C_PU |

Table 6.30. I2C_CTRL

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|------------|---|
| 7:1 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 0 | I2C_PU | 0 | read-write | Enable internal I2C pull-ups on SDA and SCL |

6.2.31 CC_CTRL

| Offset | Bit Position | | | | | | | |
|---------------|--------------|------------|---|------------|------------|---|---|---|
| 0x41 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | 0x00 | | 0 | 0x00 | | | |
| Access | | read-write | | read-write | read-write | | | |
| Name | | CC_THRSH | | CC_EN | CC_PRESCCL | | | |

Table 6.31. CC_CTRL

| Bit | Name | Reset | Access | Description |
|-----|------------|-------|------------|---|
| 7 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 6:5 | CC_THRSH | 0x00 | read-write | Determines threshold for declaring Coulomb counter full and setting the the STATUS_G.CC_FULL flag. Note that the STATUS_G.CC_FULL flag will be set when *any* of the Coulomb counters reaches the threshold. |
| | Value | Mode | | Description |
| | 0 | 50PCT | | 50% of maximum count |
| | 1 | 62PCT | | 62.5% of maximum count |
| | 2 | 75PCT | | 75% of maximum count |
| | 3 | 87PCT | | 87.5% of maximum count |
| 4 | CC_EN | 0 | read-write | Enable all Coulomb counters |
| 3:2 | CC_PRESCCL | 0x00 | read-write | Coulomb counter prescaler. Affects all Coulomb counters, but does not affect calibration. Each count in the Coulomb counter results registers represents $2^{(16-2*CC_PRESCCL)}$ PFM pulses. |
| 1:0 | RESERVED | 0 | | Reserved. Always write bits to 0. |

6.2.32 EM_CRSREG_CTRL

| Offset | Bit Position | | | | | | | |
|--------|--------------|-------------|-------------|------------|------------|------------|---|----------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x43 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0x00 | | 0 |
| Access | read-write | read-write | read-write | read-write | read-write | read-write | | read-write |
| Name | CRSREG_EN_C | CRSREG_EN_B | CRSREG_EN_A | CRSREG_BYP | FORCE_EM0 | EM_SEL | | DIRECT_MODE_EN |

Table 6.32. EM_CRSREG_CTRL

| Bit | Name | Reset | Access | Description |
|-----|-------------|----------|---------------|---|
| 7 | CRSREG_EN_C | 0 | read-write | If set, VOC coarse regulator will be enabled in EM4 mode |
| 6 | CRSREG_EN_B | 0 | read-write | If set, VOB coarse regulator will be enabled in EM4 mode |
| 5 | CRSREG_EN_A | 0 | read-write | If set, VOA coarse regulator will be enabled in EM4 mode |
| 4 | CRSREG_BYP | 0 | read-write | If set, any enabled coarse regulator outputs are shorted to VDDB through an internal switch. |
| 3 | FORCE_EM0 | 0 | read-write | Force EM0 state on any I2C start condition. Recommend to always set FORCE_EM0=1 when using Direct Mode. Refer to usage notes in the EM_SEL bit description. |
| 2:1 | EM_SEL | 0x00 | read-write | <p>Selects energy mode when not using direct mode. Note that this rbit may not accurately reflect the current energy mode state when FORCE_EM0 is set. For example, if FORCE_EM0 =1 and EM_SEL is set to 2, the EFP01 enters EM2 mode. If an I2C read/write occurs at that point, the EFP01 automatically enters EM0, but the EM_SEL bit-field is not updated and will still read 2.</p> <p>Firmware can reliably determine the current EFP01 energy mode as shown below:</p> <p>EFP01 Energy Mode = EM_CRSREG_CTRL.FORCE_EM0 ? 'EM0' : EM_CRSREG_CTRL.EM_STSEL</p> |
| | Value | Mode | Description | |
| | 0 | EM0 | Energy Mode 0 | |
| | 1 | RESERVED | Reserved | |
| | 2 | EM2 | Energy Mode 2 | |
| | 3 | EM4 | Energy Mode 4 | |

| Bit | Name | Reset | Access | Description |
|-----|----------------|-------|------------|--|
| 0 | DIRECT_MODE_EN | 0 | read-write | Set to enable Direct Mode. After DIRECT_MODE_EN is set, on the next I2C stop condition the EFP01 will disable the internal pullups on the I2C lines. At that point, the EFP01's I2C pins are expecting to be driven by push-pull outputs from the host processor to control the energy mode state. If FORCE_EM0==1, an I2C start condition (SCL=1, SDA=0) will cause EFP01 to exit Direct Mode and re-enable the internal I2C pullups. |

6.2.33 VOA_V

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|---|
| 0x49 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | | | | |
| Access | read-write | | | | | | | |
| Name | VOA_V | | | | | | | |

Table 6.33. VOA_V

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|------------|--|
| 7 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 6:0 | VOA_V | 0x00 | read-write | <p>Controls DCDC A output voltage target in EM0/EM2</p> <p>$VOA\ target = 1.7374\ V + (VOA_V * 0.0306\ V)$</p> <p>Note in Boost modes, it is possible to program the VOA target to a higher voltage than supported in the datasheet. The system designer should ensure that the VOA_V output voltage programming does not exceed the datasheet Output Programmable Voltage Range value.</p> <p>The VOA Output Accuracy specifications should be taken into consideration to ensure the output voltage range meets the load's input voltage requirements.</p> |

6.2.34 VOC_V

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|------------|---|---|---|---|---|
| 0x4B | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | 0x00 | | | | | |
| Access | | | read-write | | | | | |
| Name | | | VOC_V | | | | | |

Table 6.34. VOC_V

| Bit | Name | Reset | Access | Description |
|-----|----------|-------|------------|--|
| 7:6 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 5:0 | VOC_V | 0x00 | read-write | Controls LDO C output voltage target in EM0/EM2 $VOC\ target = 1.7178\ V + (VOC_V * 0.0305\ V)$ The VOC Output Accuracy specifications should be taken into consideration to ensure the output voltage range meets the load's input voltage requirements. |

6.2.35 VOB_EM0_V

| Offset | Bit Position | | | | | | | | |
|--------|--------------|---|---|---|---|---|---|------------|--|
| 0x4C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reset | 0 | | | | | | | 0x00 | |
| Access | read-write | | | | | | | read-write | |
| Name | OOR_DIS | | | | | | | VOB_EM0_V | |

Table 6.35. VOB_EM0_V

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|------------|---|
| 7 | OOR_DIS | 0 | read-write | Set to disable the "Out of Range" detector feature in all converters. This will disable all the STATUS_V flags. |
| 6:0 | VOB_EM0_V | 0x00 | read-write | Controls DCDC B output voltage target in EM0 $VOB\ target\ in\ EM0 = 0.8095\ V + (VOB_EM0_V * 0.0223\ V)$ The VOB Output Accuracy specifications should be taken into consideration to ensure the output voltage range meets the load's input voltage requirements. |

6.2.36 VOB_EM2_V

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|---|---|---|------------|
| 0x4D | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | | | | | | 0x00 |
| Access | | | | | | | | read-write |
| Name | | | | | | | | VOB_EM2_V |

Table 6.36. VOB_EM2_V

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|------------|--|
| 7 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 6:0 | VOB_EM2_V | 0x00 | read-write | <p>Controls DCDC B output voltage target in EM2</p> <p>$\text{VOB target in EM2} = 0.8095 \text{ V} + (\text{VOB_EM2_V} * 0.0223 \text{ V})$</p> <p>The VOB Output Accuracy specifications should be taken into consideration to ensure the output voltage range meets the load's input voltage requirements.</p> |

6.2.37 BIAS_SW

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|------------|---|---|------------|---|---|
| 0x4E | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | 0x00 | | | 0x00 | | |
| Access | read-write | | read-write | | | read-write | | |
| Name | VOA_SW_CON | | BIAS2 | | | BIAS0 | | |

Table 6.37. BIAS_SW

| Bit | Name | Reset | Access | Description |
|-----|------------|----------|------------|--|
| 7:6 | VOA_SW_CON | 0x00 | read-write | Enables switch between VOA output and VOA_SW pin Note that if VOA is low, enabling the VOA_SW is disallowed, and can cause extra quiescent current. |
| | Value | Mode | | Description |
| | 0 | OFF | | Disabled unconditionally |
| | 1 | ON | | Enabled in EM0, EM2, and EM4 |
| | 2 | ONINEM0 | | Enabled in EM0 only |
| | 3 | ONINEM02 | | Enabled in EM0 and EM2 only |
| 5:3 | BIAS2 | 0x00 | read-write | Controls bias of all DCDCs and LDOs in EM2 |
| | Value | Mode | | Description |
| | 0 | 87NA | | |
| | 1 | 100NA | | |
| | 2 | 114NA | | |
| | 3 | 147NA | | |
| | 4 | 325NA | | |
| | 5 | 386NA | | |
| | 6 | 453NA | | |
| | 7 | 600NA | | |
| 2:0 | BIAS0 | 0x00 | read-write | Controls bias of all DCDCs and LDOs in EM0 |
| | Value | Mode | | Description |
| | 0 | 87NA | | |
| | 1 | 100NA | | |
| | 2 | 114NA | | |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| | 3 | 147NA | | |
| | 4 | 325NA | | |
| | 5 | 386NA | | |
| | 6 | 453NA | | |
| | 7 | 600NA | | |

6.2.38 BB_IPK

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|------------|---|---|---|---|
| 0x4F | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | 0x00 | | | | |
| Access | read-write | | | read-write | | | | |
| Name | BB_IPK_EM2 | | | BB_IPK | | | | |

Table 6.38. BB_IPK

| Bit | Name | Reset | Access | Description |
|-----|------------|-------|------------|---|
| 7:5 | BB_IPK_EM2 | 0x00 | read-write | Peak Current setting for DCDC A in EM2. |

Note that unlike DCDC B, there is only a single Coulomb counter for DCDC A that is used in both EM0 and EM2 modes. Therefore, if Coulomb counting is used with DCDC A, BB_IPK_EM2 must be set such that the peak current in EM2 is the same as the peak current in EM0 to ensure the charge per pulse is the same in both energy modes. Roughly equivalent peak currents in EM2 and EM0 can be achieved by setting $BB_IPK_EM2 = (BB_IPK - 2) / 4$.

The BB_IPK_EM2 setting is used differently depending on the operating mode of the DCDC A converter, but the resulting peak currents for all modes are derived from the following base peak current equation:

$$IPK_BASE = 0.090A + (0.009A * ((4 * BB_IPK_EM2) + 2))$$

Although the IPK_BASE equation differs between EM2 and EM0, the equations that govern the resulting peak current for each operating mode are the same as documented in the BB_IPK description.

| Bit | Name | Reset | Access | Description |
|-----|--------|-------|------------|--|
| 4:0 | BB_IPK | 0x00 | read-write | <p>Peak Current setting for DCDC A in EM0. The BB_IPK setting is used differently depending on the operating mode of the DCDC A converter, but the resulting peak currents for all modes are derived from the following base peak current equation:</p> $IPK_BASE = 0.090A + (0.009A * BB_IPK)$ <p>When DCDC A is operating in Buck mode:</p> <p>Buck Mode Peak current in EM0 (Amps) = $IPK_BASE + (25ns * (VDDDB - VOA)) / L$</p> <p>In Boost and NTM modes, the peak current depends on the battery voltage (VBAT), which varies depending on the hardware configuration: VBAT is the VDDA pin voltage in Single-Cell Boost Configuration, VBAT is the VDDDB pin voltage in Wired Boost Configuration, and VBAT is the voltage at the battery in Boost Bootstrap Configuration.</p> <p>When DCDC A is operating in NTM mode:</p> <p>NTM Mode Peak current in EM0 (Amps) = $1.15 * IPK_BASE + (25ns * VBAT) / L$</p> <p>When DCDC A is operating in Boost mode with no peak current adjustment:</p> <p>Boost Mode (NOADJ=1) Peak current in EM0 (Amps) = $2.35 * IPK_BASE + (25ns * VBAT) / L$</p> <p>To disable the peak current adjustment in Boost mode, set BB_CTRL6.BB_IPK_NOADJ=1.</p> <p>When DCDC A is operating in Boost mode with peak current adjustment enabled:</p> <p>Boost Mode (NOADJ=0) Peak current in EM0 (Amps) = $2.35 * \text{MIN}(IPK_BASE * VOA / (2 * VBAT), 385mA) + (25ns * VBAT) / L$</p> <p>When operating in Boost mode with peak current adjustment, the peak current will be adjusted to maintain a near constant output load current over the battery voltage range, where the expected output load current is approximately $IPK_BASE / 2$. The Peak Current Adjustment feature requires that BB_CTRL6.BB_IPK_NOADJ=0, that BB_CTRL5.BB_IPK_BOOST_ADJ is programmed as recommended in its register description, and that ADC_CC_CTRL.ADC_INTERVAL > 0 to enable ADC operations.</p> |

6.2.39 BB_CTRL3

| Offset | Bit Position | | | | | | | |
|---------------|---------------|---|---|------------|---|---|------------|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x50 | | | | | | | | |
| Reset | 0x00 | | | 0x00 | | | 0x00 | |
| Access | read-write | | | read-write | | | read-write | |
| Name | NTM_LDO_THRSH | | | NTM_DUR | | | BB_MODE | |

Table 6.39. BB_CTRL3

| Bit | Name | Reset | Access | Description | | | | | | | | | | | | | | | |
|-------|---------------|-------------|------------|--|-------|------|-------------|---|-------|-----|---|-------|-----|---|--------|------|---|--------|------|
| 7:5 | NTM_LDO_THRSH | 0x00 | read-write | <p>Sets the threshold for DCDC A in Buck/Boost mode to enter either NTM or LDO operating modes (depending on BB_MODE setting).</p> <p>For Buck/Boost or Buck with LDO, the buck-to-NTM or buck-to-LDO boundary, respectively, is:</p> <p>Falling => $V_{DDB-VOA} = 105\text{mV} + (87.5\text{mV} * \text{NTM_LDO_THRSH})$</p> <p>Rising => $V_{DDB-VOA} = 130\text{mV} + (87.5\text{mV} * \text{NTM_LDO_THRSH})$</p> <p>For Buck/Boost, the NTM-to-boost boundary is:</p> <p>Falling => $VOA-V_{DDB} = 60\text{mV} + (50\text{mV} * \text{NTM_LDO_THRSH})$</p> <p>Rising => $VOA-V_{DDB} = 85\text{mV} + (50\text{mV} * \text{NTM_LDO_THRSH})$</p> | | | | | | | | | | | | | | | |
| 4:3 | NTM_DUR | 0x00 | read-write | <p>NTM duration in Buck/Boost mode.</p> <p>Normalized to the time required for charging the inductor to I_{peak}.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>60PCT</td> <td>60%</td> </tr> <tr> <td>1</td> <td>83PCT</td> <td>83%</td> </tr> <tr> <td>2</td> <td>107PCT</td> <td>107%</td> </tr> <tr> <td>3</td> <td>130PCT</td> <td>130%</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | 60PCT | 60% | 1 | 83PCT | 83% | 2 | 107PCT | 107% | 3 | 130PCT | 130% |
| Value | Mode | Description | | | | | | | | | | | | | | | | | |
| 0 | 60PCT | 60% | | | | | | | | | | | | | | | | | |
| 1 | 83PCT | 83% | | | | | | | | | | | | | | | | | |
| 2 | 107PCT | 107% | | | | | | | | | | | | | | | | | |
| 3 | 130PCT | 130% | | | | | | | | | | | | | | | | | |
| 2:0 | BB_MODE | 0x00 | read-write | <p>Buck/Boost converter's mode control. In EM4, Buck/Boost converter is disabled regardless of this setting.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> </tr> </tbody> </table> | Value | Mode | Description | | | | | | | | | | | | |
| Value | Mode | Description | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |

| Bit | Name | Reset | Access | Description |
|-----|------|--------------|--------|--|
| 0 | | DISABLED | | Disabled |
| 1 | | AUTONOMOUS | | Autonomous Buck/Boost/NTM mode switching Used in Buck/Boost configuration. |
| 2 | | FORCEBUCK | | Forced Buck mode only. Used in Buck/Boost configuration. |
| 3 | | FORCENTM | | Forced NTM mode only. Used in Buck/Boost configuration. |
| 4 | | FORCEBOOST | | Forced Boost mode only. Used in Buck/Boost configuration. |
| 5 | | WIREDBUCKLDO | | Wired Buck mode only with auto switch to LDO mode when input voltage is too low. Used in Wired Buck w/LDO Configuration. |
| 6 | | WIREDBUCK | | Wired Buck mode only. Used in Wired Buck configuration. |
| 7 | | WIREDBOOST | | Wired Boost mode only. Used in Wired Boost configuration. |

6.2.40 BB_CTRL5

| Offset | Bit Position | | | | | | | |
|---------------|---------------|---|------------------|---|---|---|---|---|
| 0x51 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | 0x00 | | | | | |
| Access | read-write | | read-write | | | | | |
| Name | BB_DRVR_SPEED | | BB_IPK_BOOST_ADJ | | | | | |

Table 6.40. BB_CTRL5

| Bit | Name | Reset | Access | Description |
|-----|------------------|-------|------------|--|
| 7:6 | BB_DRVR_SPEED | 0x00 | read-write | DCDC A pre-driver speed control. Recommend to set to 2 for the highest efficiency, but will also generate the most EMI. Lower settings can be used to reduce EMI at the expense of efficiency. |
| 5:0 | BB_IPK_BOOST_ADJ | 0x00 | read-write | <p>When BB_IPK_NOADJ==0, the value of BB_IPK_BOOST_ADJ controls the adjustments made to the boost mode peak current as the battery voltage drops. When BB_IPK_NOADJ==1, this field has no effect.</p> <p>For Single Cell Mode, BB_IPK_BOOST_ADJ should be programmed:</p> $BB_IPK_BOOST_ADJ = \text{ROUND}(2 * (\text{LN}(0.294 * 4096 * \text{VOA} / 1.22 * (\text{BB_IPK} + 12) / 43) * 23.6 - 163.8), 0)$ <p>For non-Single Cell Modes, BB_IPK_BOOST_ADJ should be programmed:</p> $BB_IPK_BOOST_ADJ = \text{ROUND}(2 * (\text{LN}(0.2 * 4096 * \text{VOA} / 1.22 * (\text{BB_IPK} + 12) / 43) * 23.6 - 157.2), 0)$ |

6.2.41 BB_CTRL6

| Offset | Bit Position | | | | | | | |
|--------|--------------|------------|------------|---|---|---|-------------|---|
| 0x52 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0x00 | | | | 0x00 | |
| Access | read-write | read-write | read-write | | | | read-write | |
| Name | BB_IPK_NOADJ | SW_FAST | BB_IRI_CON | | | | BB_TOFF_MAX | |

Table 6.41. BB_CTRL6

| Bit | Name | Reset | Access | Description |
|-----|--------------|-------|------------|---|
| 7 | BB_IPK_NOADJ | 0 | read-write | <p>If 0, the boost mode peak current in EM0 is increased as the battery voltage drops to allow a near constant maximum output current to be delivered to the load.</p> <p>If 1, the voltage-dependent adjustment of peak current in EM0 is disabled.</p> <p>Peak current adjustment is always disabled in EM2 regardless of this setting.</p> |
| 6 | SW_FAST | 0 | read-write | <p>VOA switch driver uses high speed mode when asserted. Recommend to set SW_FAST=0, unless the load on VOA_SW is > 55mA during the switching process. Firmware should wait until VOA_SW_STAT.VOA_SW_ISLOW has transitioned to 0 before enabling a larger load than 55mA on VOA_SW.</p> |
| 5:2 | BB_IRI_CON | 0x00 | read-write | <p>Controls inrush current for DCDC A by forcing a minimum time between pulse events (i.e. Tsw, the switching period). Inrush current limiting may be needed for operation with batteries that have a large internal impedance and/or limited output current.</p> <p>If BB_IRI_CON>0, the minimum switching period (Tsw) is determined by the following equation:</p> $T_{sw} \text{ (ns)} = 300\text{ns} * (2 * BB_IRI_CON + 1)$ <p>If BB_IRI_CON==0, there is no bound on the switching period.</p> <p>The resulting battery current can be calculated as: $(L * I_{pk}^2) / (2 * (V_{DDB} - V_{OA}) * T_{sw})$. To maintain a constant current limit over the battery voltage range, firmware should occasionally read the battery voltage and recalculate the BB_IRI_CON value.</p> |

| Bit | Name | Reset | Access | Description |
|-----|-------------|---------|------------|---|
| 1:0 | BB_TOFF_MAX | 0x00 | read-write | Allows setting a limit for Toff max in Boost modes to ensure there is no hang-up when inductor fails to discharge naturally. Allows operation in boost or wired boost modes with VOA slightly lower than battery voltage. No limit if BB_TOFF_MAX==0. |
| | Value | Mode | | Description |
| | 0 | NOLIMIT | | No Limit |
| | 1 | 0P9US | | 0.9us |
| | 2 | 1P5US | | 1.5us |
| | 3 | 2P1US | | 2.1us |

6.2.42 LDOB_CTRL

| Offset | Bit Position | | | | | | | |
|---------------|-----------------|------------|------------|---|------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x53 | | | | | | | | |
| Reset | 0 | 0 | 0x00 | | 0x00 | | | |
| Access | read-write | read-write | read-write | | read-write | | | |
| Name | LDO_NO_AUTO_BYP | LDOB_BYP | LDOB_VMIN | | LDOB_IGAIN | | | |

Table 6.42. LDOB_CTRL

| Bit | Name | Reset | Access | Description |
|-----|-----------------|-------|------------|--|
| 7 | LDO_NO_AUTO_BYP | 0 | read-write | If set, neither LDO B or LDO C goes into bypass automatically. |
| 6 | LDOB_BYP | 0 | read-write | If set, when LDO B is enabled it acts only as a bypass switch |
| 5:4 | LDOB_VMIN | 0x00 | read-write | <p>Defines voltage at which output current becomes voltage independent for LDO B. Recommended to set LDOB_VMIN based on the target VOB voltage as given below:</p> <p>LDOB_VMIN=3 for VOB targets >=2.7V</p> <p>LDOB_VMIN=2 for VOB targets between 2.4V and 2.7V</p> <p>LDOB_VMIN=1 for VOB targets between 2.0V and 2.4V</p> <p>LDOB_VMIN=0 for VOB targets < 2.0V</p> |
| 3:0 | LDOB_IGAIN | 0x00 | read-write | <p>Determines the maximum output current supported by LDO B. Recommend to set to the maximum expected load current plus some margin.</p> $i_{max} = VOB / (2.76 * (17 - LDOB_IGAIN))$ |

6.2.43 LDOC_CTRL

| Offset | Bit Position | | | | | | | |
|--------|--------------|------------|------------|---|------------|---|---|---|
| 0x54 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0x00 | | 0x00 | | | |
| Access | read-write | read-write | read-write | | read-write | | | |
| Name | LDOC_ENA_SA | LDOC_BYP | LDOC_VMIN | | LDOC_IGAIN | | | |

Table 6.43. LDOC_CTRL

| Bit | Name | Reset | Access | Description |
|-----|-------------|-------|------------|--|
| 7 | LDOC_ENA_SA | 0 | read-write | <p>If set, LDO C is enabled in StandAlone mode, independent of the DCDC A Buck/Boost converter.</p> <p>In EM4, this bit is treated as zero, which means LDO C will be disabled.</p> <p>Standalone Mode should not be enabled if the DCDC A is configured for wiredBuckLDO (BB_MODE==5) and the VOA and VOC outputs are shorted together in hardware. If LDOC_ENA_SA is set in that configuration, both LDOC C and DCDC A will attempt to drive the same output, with the higher voltage winning. This may trip the overvoltage protection, resulting in unintended current draw.</p> |
| 6 | LDOC_BYP | 0 | read-write | <p>If set, LDO C acts only as a bypass switch (i.e., the input is shorted to the output).</p> |
| 5:4 | LDOC_VMIN | 0x00 | read-write | <p>Defines voltage at which output current becomes voltage independent for LDO C. Recommended to set LDOC_VMIN based on the target VOC voltage as given below:</p> <p>LDOC_VMIN=3 for VOC targets >=2.7V</p> <p>LDOC_VMIN=2 for VOC targets between 2.4V and 2.7V</p> <p>LDOC_VMIN=1 for VOC targets between 2.0V and 2.4V</p> <p>LDOC_VMIN=0 for VOC targets < 2.0V</p> |
| 3:0 | LDOC_IGAIN | 0x00 | read-write | <p>Determines the maximum output current supported by LDO C. Recommend to set to the maximum expected load current plus some margin.</p> $i_{max} = VOC / (2.76 * (17 - LDOC_IGAIN))$ |

6.2.44 LDOC_BB_CTRL

| Offset | Bit Position | | | | | | | |
|--------|--------------|------------|---|---|-------------|---|---|---|
| 0x55 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0x00 | | | 0x00 | | | |
| Access | read-write | read-write | | | read-write | | | |
| Name | SEQ_BB_FIRST | BB_TON_MAX | | | VOC_IRI_CON | | | |

Table 6.44. LDOC_BB_CTRL

| Bit | Name | Reset | Access | Description |
|-----|--------------|---------|------------|--|
| 7 | SEQ_BB_FIRST | 0 | read-write | For Bootstrap modes (i.e., modes where the VDDB is supplied from VOA output), setting this bit delays the enabling of the DCDC B Buck converter and/or LDO C (in stand alone) until after VOA has reached regulation. |
| 6:4 | BB_TON_MAX | 0x00 | read-write | Max Ton is bounded to $70\text{ns} \cdot (4 \cdot \text{BB_TON_MAX} + 1)$ No bound if $\text{BB_TON_MAX} == 0$ |
| | Value | Mode | | Description |
| | 0 | NOLIMIT | | |
| | 1 | 350NS | | |
| | 2 | 630NS | | |
| | 3 | 910NS | | |
| | 4 | 1190NS | | |
| | 5 | 1470NS | | |
| | 6 | 1750NS | | |
| | 7 | 2030NS | | |
| 3:0 | VOC_IRI_CON | 0x00 | read-write | Controls inrush current for LDO C by forcing a minimum time between pulse events (i.e. Tsw, the switching period). Inrush current limiting may be needed for operation with batteries that have a large internal impedance and/or limited output current. If $\text{VOC_IRI_CON} > 0$, the minimum switching period (Tsw) is determined by the following equation: $\text{Tsw (ns)} = 300\text{ns} \cdot (2 \cdot \text{VOC_IRI_CON} + 1)$ If $\text{VOC_IRI_CON} == 0$, there is no bound on the switching period. |

6.2.45 BK_CTRL0

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|---|---|---|---|----------------|------------|
| 0x56 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | | | | | | 0 | 0 |
| Access | | | | | | | read-write | read-write |
| Name | | | | | | | BK_DIS_OV_PROT | CLAMPB |

Table 6.45. BK_CTRL0

| Bit | Name | Reset | Access | Description |
|-----|----------------|-------|------------|---|
| 7:2 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 1 | BK_DIS_OV_PROT | 0 | read-write | <p>If set, disables overvoltage protection on Buck output.</p> <p>Intended use is when not using EM4, but switching back and forth between EM0 and EM2 with substantially different voltages programmed.</p> <p>If cleared, each transition to lower voltage (i.e., EM0->EM2) would cause VOB to be unnecessarily pulled down.</p> |
| 0 | CLAMPB | 0 | read-write | <p>If asserted and in EM4 mode, a diode-connected NMOS and 10KOhm pull-down on VOB is enabled. Intended for use when VOB target is in the range 1V-1.2V and actual load on VOB is < 3uA at high temperature.</p> |

6.2.46 BK_CTRL1

| Offset | Bit Position | | | | | | | |
|---------------|--------------|---|---|------------|---|---------------|---|---|
| 0x57 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | 0x00 | | 0x00 | | |
| Access | read-write | | | read-write | | read-write | | |
| Name | BK_TON_MAX | | | BK_MODE | | BK_DRVR_SPEED | | |

Table 6.46. BK_CTRL1

| Bit | Name | Reset | Access | Description |
|-----|---------------|----------|------------|--|
| 7:5 | BK_TON_MAX | 0x00 | read-write | Max Ton is bounded to $70\text{ns} * (4 * \text{BK_TON_MAX} + 1)$ Ton is not bounded if BK_TON_MAX==0 |
| | Value | Mode | | Description |
| | 0 | NOLIMIT | | |
| | 1 | 350NS | | |
| | 2 | 630NS | | |
| | 3 | 910NS | | |
| | 4 | 1190NS | | |
| | 5 | 1470NS | | |
| | 6 | 1750NS | | |
| | 7 | 2030NS | | |
| 4:3 | BK_MODE | 0x00 | read-write | Sets the mode of the DCDC B converter. Regardless of this setting, in EM4 the DCDC B converter will be disabled. |
| | Value | Mode | | Description |
| | 0 | DISABLED | | Off |
| | 1 | BUCKONLY | | Buck Mode Only |
| | 2 | LDOONLY | | LDOB enabled, Buck Disabled |
| | 3 | BUCKLDO | | Buck or LDOB, depending on DV=VDDDB-VOB |
| 2:1 | BK_DRVR_SPEED | 0x00 | read-write | DCDC B pre-driver speed control. Recommend to set to 2 for the highest efficiency, but will also generate the most EMI. Lower settings can be used to reduce EMI at the expense of efficiency. |
| 0 | RESERVED | 0 | | Reserved. Always write bits to 0. |

6.2.47 BK_IPK

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|------------|---|---|---|---|
| 0x58 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | 0x00 | | | | |
| Access | read-write | | | read-write | | | | |
| Name | BK_IPK_EM2 | | | BK_IPK | | | | |

Table 6.47. BK_IPK

| Bit | Name | Reset | Access | Description |
|-----|------------|-------|------------|--|
| 7:5 | BK_IPK_EM2 | 0x00 | read-write | Peak Current setting for DCDC B in EM2. $\text{Buck converter peak current in EM2 (Amps)} = 0.090\text{A} + 0.009\text{A} * ((\text{BK_IPK_EM2} * 4) + 2) + (25\text{ns} * (\text{VDDDB} - \text{VOB})) / \text{L}$ |
| 4:0 | BK_IPK | 0x00 | read-write | Peak Current setting for DCDC B in EM0. $\text{Buck converter peak current in EM0 (Amps)} = 0.090\text{A} + (0.009\text{A} * \text{BK_IPK}) + (25\text{ns} * (\text{VDDDB} - \text{VOB})) / \text{L}$ |

6.2.48 BK_CTRL2

| Offset | Bit Position | | | | | | | |
|--------|--------------|---------------|---|---|------------|---|---|---|
| 0x59 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | | 0x00 | | | 0x00 | | | |
| Access | | read-write | | | read-write | | | |
| Name | | BK_LDO_THRESH | | | BK_IRI_CON | | | |

Table 6.48. BK_CTRL2

| Bit | Name | Reset | Access | Description |
|-----|---------------|-------|------------|--|
| 7 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 6:4 | BK_LDO_THRESH | 0x00 | read-write | <p>Sets threshold for switching DCDC B to LDO B, $DV=VDDDB-VOB$ for buck/LDO boundary is:</p> $(DV_{rising} ? 25mV : 0) + 105mV + 87.5mV * BK_LDO_THRESH$ |
| 3:0 | BK_IRI_CON | 0x00 | read-write | <p>Controls inrush current for DCDC B by forcing a minimum time between pulse events (i.e. Tsw, the switching period). Inrush current limiting may be needed for operation with batteries that have a large internal impedance and/or limited output current.</p> <p>If $BK_IRI_CON > 0$, the minimum switching period (Tsw) is determined by the following equation:</p> $Tsw (ns) = 300ns * (2 * BK_IRI_CON + 1)$ <p>If $BK_IRI_CON == 0$, there is no bound on the switching period.</p> <p>The resulting battery current can be calculated as: $(L * Ipk^2) / (2 * (VDDDB - VOB) * Tsw)$. To maintain a constant current limit over the battery voltage range, firmware should occasionally read the battery voltage and recalculate the BK_IRI_CON value.</p> |

6.2.49 ADC_CC_CTRL

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|-------------|---|---|--------------|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x5C | | | | | | | | |
| Reset | | | | 0x00 | | | 0x00 | |
| Access | | | | read-write | | | read-write | |
| Name | | | | ADC_IIR_TAU | | | ADC_INTERVAL | |

Table 6.49. ADC_CC_CTRL

| Bit | Name | Reset | Access | Description |
|-----|--------------|-------|------------|---|
| 7:6 | RESERVED | 0 | | Reserved. Always write bits to 0. |
| 5:3 | ADC_IIR_TAU | 0x00 | read-write | Determines the time constant used in the ADC's averaging low-pass IIR filter voltage reading. Time constant = $2^{(ADC_IIR_TAU)}$ |
| 2:0 | ADC_INTERVAL | 0x00 | read-write | <p>If ADC_INTERVAL > 0, automated ADC measurements are enabled in EM0 and EM2. The automated measurements will be triggered when the count of all pulse events in all of the enabled converters is equal to $2^{(ADC_INTERVAL+3)}$. To ensure that measurements occur even when pulse events are very infrequent, an ADC measurement will be triggered approximately every ~400msec at a minimum when ADC_INTERVAL > 0, regardless of the pulse event count.</p> <p>If ADC_INTERVAL > 0 and BB_CTRL2.BB_IPK_NOADJ = 0, automatic inductor peak current adjustments in boost mode will be enabled.</p> <p>If ADC_INTERVAL = 0, there will be no automatic ADC measurements enabled, which means NO temperature-dependent bias refresh and/or boost-mode automated inductor peak current adjustments. In addition, any flags or bits requiring the ADC (e.g., STATUS_G.VDD_LOW and STATUS_G.TEMP_FAULT) will not be updated.</p> |

6.2.50 ADC_LIMITS

| Offset | Bit Position | | | | | | | |
|--------|--------------|---|---|---|------------|---|---|---|
| 0x5D | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0x00 | | | | 0x00 | | | |
| Access | read-write | | | | read-write | | | |
| Name | ADC_V_LIM | | | | ADC_T_LIM | | | |

Table 6.50. ADC_LIMITS

| Bit | Name | Reset | Access | Description |
|-----|-----------|-------|------------|---|
| 7:3 | ADC_V_LIM | 0x00 | read-write | <p>Sets voltage threshold for the STATUS_G.VDD_LOW flag.</p> <p>If measuring VDDA (i.e., SC_MODE==1): VDD_LOW threshold = 800mV + (ADC_V_LIM * 32.42mV)</p> <p>If measuring VDDB (i.e., SC_MODE==0): VDD_LOW threshold = 1699mV + (ADC_V_LIM * 47.66mV)</p> |
| 2:0 | ADC_T_LIM | 0x00 | read-write | <p>Defines temperature limit for over temperature fault, STATUS_G.TEMP_FAULT.</p> <p>Over temperature limit (°C) = 115°C + (5.55°C*ADC_T_LIM)</p> |

7. OTP Definitions

7.1 OTP Definition

Note: Some registers will have their default values automatically overwritten by OTP-programmed values out of reset. Therefore, the actual values of those registers after reset may differ from the default reset values listed in the [Register Description](#) table. The table below shows the expected value of those registers out of reset.

| OTP Register Name | OTP Address | Description |
|--------------------|-------------|---|
| OTP_I2C_CTRL | 0x00 | Contains value loaded into the I2C_CTRL register out of reset |
| OTP_CC_CTRL | 0x01 | Contains value loaded into the CC_CTRL register out of reset |
| OTP_EM_CRSREG_CTRL | 0x03 | Contains value loaded into the EM_CRSREG_CTRL register out of reset |
| OTP_VOA_V | 0x09 | Contains value loaded into the VOA_V register out of reset |
| OTP_VOC_V | 0x0B | Contains value loaded into the VOC_V register out of reset |
| OTP_VOB_EM0_V | 0x0C | Contains value loaded into the VOB_EM0_V register out of reset |
| OTP_VOB_EM2_V | 0x0D | Contains value loaded into the VOB_EM2_V register out of reset |
| OTP_BIAS_SW | 0x0E | Contains value loaded into the BIAS_SW register out of reset |
| OTP_BB_IPK | 0x0F | Contains value loaded into the BB_IPK register out of reset |
| OTP_BB_CTRL3 | 0x10 | Contains value loaded into the BB_CTRL3 register out of reset |
| OTP_BB_CTRL5 | 0x11 | Contains value loaded into the BB_CTRL5 register out of reset |
| OTP_BB_CTRL6 | 0x12 | Contains value loaded into the BB_CTRL6 register out of reset |
| OTP_LDOB_CTRL | 0x13 | Contains value loaded into the LDOB_CTRL register out of reset |
| OTP_LDOC_CTRL | 0x14 | Contains value loaded into the LDOC_CTRL register out of reset |
| OTP_LDOC_BB_CTRL | 0x15 | Contains value loaded into the LDOC_BB_CTRL register out of reset |
| OTP_BK_CTRL0 | 0x16 | Contains value loaded into the BK_CTRL0 register out of reset |
| OTP_BK_CTRL1 | 0x17 | Contains value loaded into the BK_CTRL1 register out of reset |
| OTP_BK_IPK | 0x18 | Contains value loaded into the BK_IPK register out of reset |
| OTP_BK_CTRL2 | 0x19 | Contains value loaded into the BK_CTRL2 register out of reset |
| OTP_ADC_CC_CTRL | 0x1C | Contains value loaded into the ADC_CC_CTRL register out of reset |
| OTP_ADC_LIMITS | 0x1D | Contains value loaded into the ADC_LIMITS register out of reset |
| OTP_UID_LOW | 0x20 | Lower byte of Device Unique ID |
| OTP_UID_HIGH | 0x21 | Upper byte of Device Unique ID |
| OTP_TEMP_CODE | 0x2F | Temperature Grade: 0=Undefined, 1=G (-40 °C to +105 °C), 2=I (-40 °C to +125 °C) |
| OTP_OPN_NUM | 0x30 | OPN (4=EFP0104, 8=EFP0108, 11=EFP0111) |
| OTP_OPN_REV | 0x31 | OPN definition revision |
| OTP_CCCAL_LOW | 0x33 | Coulomb Counter Calibration for CC_LVL=3 load current |
| OTP_CCCAL_HIGH | 0x34 | Coulomb Counter Calibration for CC_LVL=7 load current |
| OTP_OSC10MHZ_CAL | 0x35 | 10MHz Oscillator Calibration Constant |

7.2 OTP Defaults

Note: Certain registers will have their default values automatically overwritten by OTP-programmed values out of reset, so the actual values of those registers after reset may differ from the default reset values listed in the [Register Description](#) table. The table below indicates the expected value of each affected register out of reset.

| Register Name | EFP0101 | EFP0102 | EFP0103 | EFP0104 | EFP0106 | EFP0107 | EFP0108 | EFP0109 | EFP0110 | EFP0111 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| OTP_OPN_REV | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 | 0x03 | 0x03 | 0x03 |
| I2C_CTRL | 0x09 | 0x09 | 0x09 | 0x09 | 0x09 | 0x09 | 0x09 | 0x09 | 0x09 | 0x09 |
| CC_CTRL | 0x68 | 0x68 | 0x68 | 0x68 | 0x68 | 0x68 | 0x68 | 0x68 | 0x68 | 0x68 |
| EM_CRISREG_CTRL | 0xE8 | 0xA8 | 0x68 | 0x28 | 0xE8 | 0xA8 | 0xA8 | 0xE8 | 0xA8 | 0xE8 |
| VOA_V | 0x04 | 0x04 | 0x04 | 0x04 | 0x04 | 0x04 | 0x04 | 0x34 | 0x34 | 0x72 |
| VOC_V | 0x05 | 0x05 | 0x00 | 0x00 | 0x05 | 0x05 | 0x00 | 0x05 | 0x05 | 0x05 |
| VOB_EM0_V | 0xAF | 0x80 | 0xAF | 0x80 | 0xAF | 0x80 | 0x80 | 0xAF | 0x80 | 0xAF |
| VOB_EM2_V | 0x2F | 0x00 | 0x2F | 0x00 | 0x2F | 0x00 | 0x00 | 0x2F | 0x00 | 0x2F |
| BIAS_SW | 0x0F | 0x0F | 0x0F | 0x0F | 0x0F | 0x0F | 0x0F | 0x0F | 0x0F | 0x0F |
| BB_IPK | 0x92 | 0x92 | 0x92 | 0x92 | 0x6D | 0x6D | 0x4A | 0x6C | 0x6C | 0x4A |
| BB_CTRL3 | 0x16 | 0x16 | 0xB5 | 0xB5 | 0xB1 | 0xB1 | 0x17 | 0x17 | 0x17 | 0x17 |
| BB_CTRL5 | 0x80 | 0x80 | 0x80 | 0x80 | 0x80 | 0x80 | 0x80 | 0x9B | 0x9B | 0xA7 |
| BB_CTRL6 | 0x03 | 0x03 | 0x03 | 0x03 | 0x03 | 0x03 | 0x02 | 0x02 | 0x02 | 0xBA |
| LDOB_CTRL | 0x0C | 0x00 | 0x0C | 0x00 | 0x0C | 0x00 | 0x00 | 0x0C | 0x00 | 0x0C |
| LDOC_CTRL | 0x8C | 0x8C | 0x0C | 0x0C | 0x8C | 0x8C | 0x0C | 0x8C | 0x8C | 0x8C |
| LDOC_BB_CTRL | 0x40 | 0x40 | 0x50 | 0x50 | 0x50 | 0x50 | 0xF0 | 0xF0 | 0xF0 | 0xC0 |
| BK_CTRL0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| BK_CTRL1 | 0xFC | 0xE4 | 0xFC | 0xE4 | 0xFC | 0xE4 | 0xE4 | 0xFC | 0xE4 | 0xBC |
| BK_IPK | 0x90 | 0x00 | 0x90 | 0x00 | 0x90 | 0x00 | 0x00 | 0x6C | 0x00 | 0x91 |
| BK_CTRL2 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 | 0x50 | 0x40 |
| ADC_CC_CTRL | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | 0x07 |
| ADC_LIMITS | 0x18 | 0x18 | 0x18 | 0x18 | 0x18 | 0x18 | 0x18 | 0x18 | 0x18 | 0x78 |

8. Pin Definitions

8.1 EFP01 Device Pinout

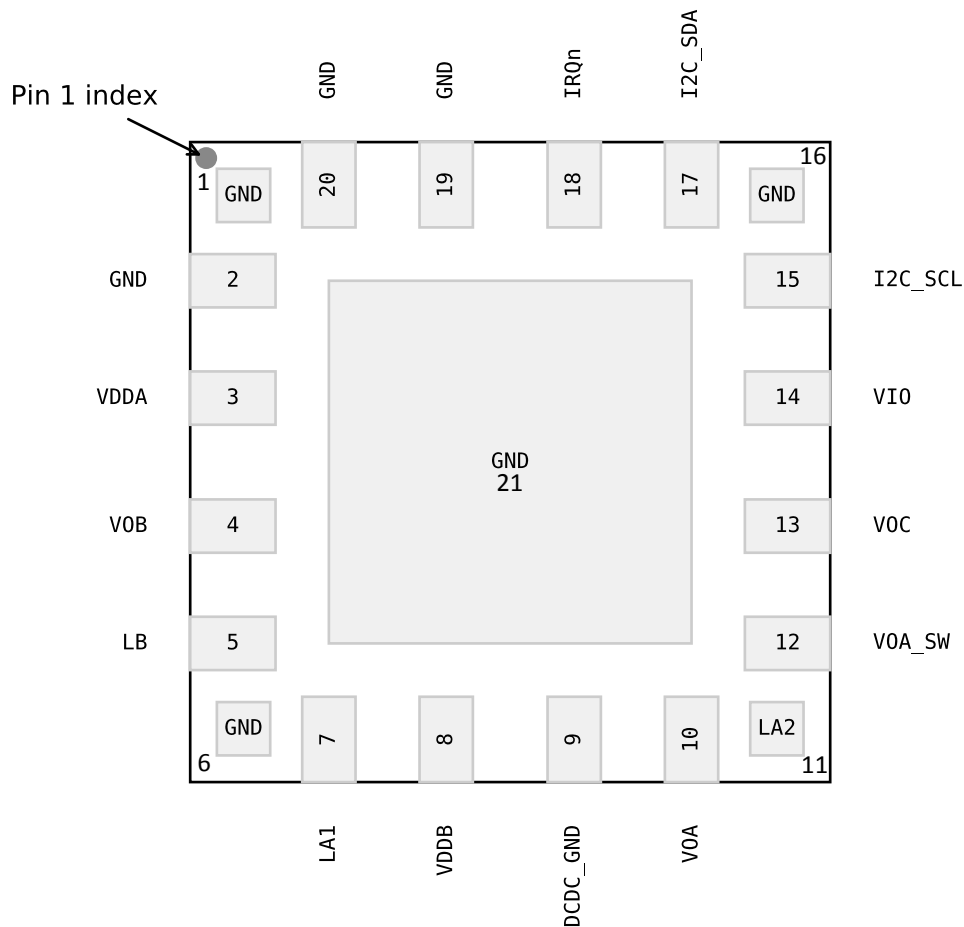


Figure 8.1. EFP01 Device Pinout (Top View)

The following table provides package pin connections and general descriptions of pin functionality.

Table 8.1. EFP01 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|---|----------|--------|---------------------------|
| GND | 1 | Thermal Ground Connection | GND | 2 | Thermal Ground Connection |
| VDDA | 3 | Low-Voltage Circuitry Supply Input for Single-cell Boost (EFP0108) devices. For all other devices, this pin should be grounded. | VOB | 4 | DCDC B Output |
| LB | 5 | DCDC B Switching Node | GND | 6 | Thermal Ground Connection |
| LA1 | 7 | DCDC A Switching Node 1 | VDDB | 8 | DCDC A and B Input |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|--|----------|--------|-----------------------------|
| DCDC_GND | 9 | DCDC Ground. Return path for power-train switch current. | VOA | 10 | DCDC A Output |
| LA2 | 11 | DCDC A Switching Node 2 | VOA_SW | 12 | DCDC A Switched Output |
| VOC | 13 | LDO C Output | VIO | 14 | IO Supply |
| I2C_SCL | 15 | I2C Clock | GND | 16 | Thermal Ground Connection |
| I2C_SDA | 17 | I2C Data | IRQn | 18 | Active Low Interrupt Output |
| GND | 19 | Thermal Ground Connection | GND | 20 | Thermal Ground Connection |
| GND | 21 | Paddle. Thermal Ground Connection | | | |

9. QFN20 Package Specifications

9.1 QFN20 Package Dimensions

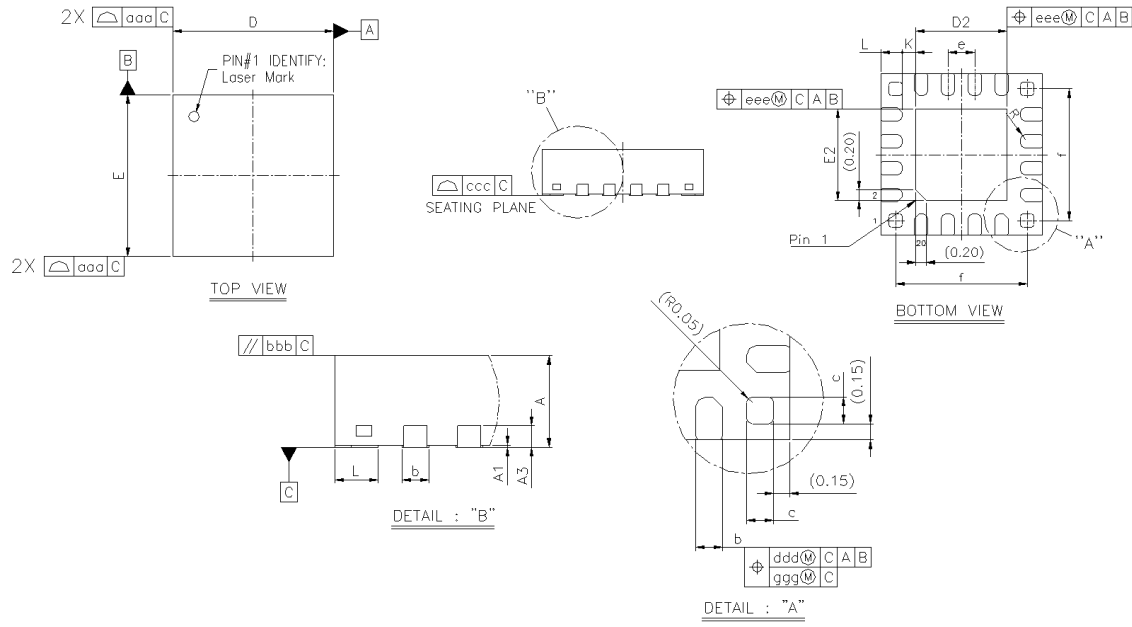


Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.20 | 0.25 | 0.30 |
| D | 3.00 BSC | | |
| D2 | 1.60 | 1.70 | 1.80 |
| e | 0.50 BSC | | |
| E | 3.00 BSC | | |
| E2 | 1.60 | 1.70 | 1.80 |
| f | 2.45 BSC | | |
| K | 0.20 | — | — |
| L | 0.30 | 0.40 | 0.50 |
| R | 0.09 | — | 0.15 |
| aaa | — | — | 0.15 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.10 |
| ggg | — | — | 0.05 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

Table 9.2. QFN20 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| C1 | 3.00 |
| C2 | 3.00 |
| Y2 | 1.80 |
| X2 | 1.80 |
| e | 0.50 |
| f | 2.45 |
| W | 0.30 |
| X1 | 0.30 |
| Y1 | 0.80 |
| R1 | 0.15 |
| R2 | 0.05 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
9. The above notes and stencil design are shared as recommendations only. The customer may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling
10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 QFN20 Package Marking

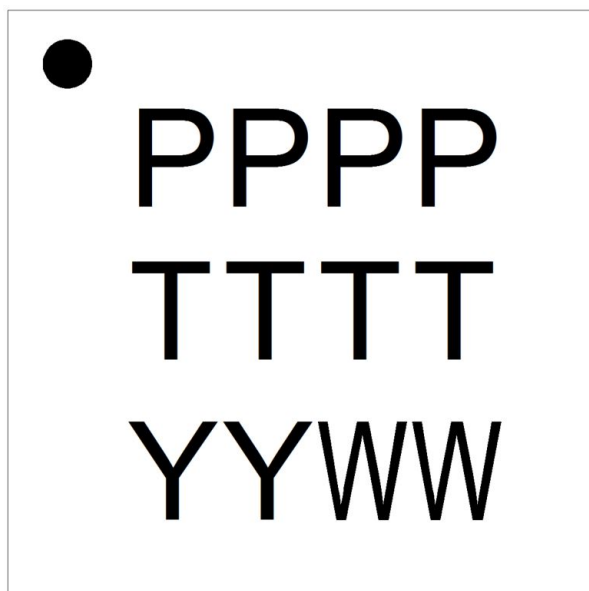


Figure 9.3. QFN20 Package Marking

The package marking consists of the following:

- PPPP – The part number designation.
 1. Family Code (1 character)
 2. Feature Set Code (2 characters)
 3. Temperature Grade (G = -40 to 85 °C)
- TTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

10. Revision History

Revision 1.3

July, 2021

- Updated all OPNs to Rev E in [Table 2.1 Ordering Information on page 3](#)
- Added EFP0101, EFP0102, EFP0103, EFP0106 OPNs to the following sections:
 - [1. Feature List](#)
 - [Table 2.1 Ordering Information on page 3](#)
 - [5.1.3.3 EFP0101 / EFP0102](#)
 - [5.1.3.4 EFP0103 / EFP0104](#)
 - [5.1.3.5 EFP0106 / EFP0107](#)
 - [Table 3.2 DCDC A Configuration and Modes Summary on page 9](#)
 - [3.2.4 Coarse Regulators](#)
 - [7.2 OTP Defaults](#)
- Updated [6.2.6 DEVREV_ID](#) register definitions for Rev E
- Added footnote clarifying that on EFP0109/11 OPNs, the VOB converter won't begin to start until the VOA converter has reached regulation
- Corrected maximum input voltage from 5.5V to 3.6V for the [Figure 4.5 Wired Boost Configuration on page 34](#) diagram

Revision 1.2

March, 2021

- Corrected Top Mark Line 1 of EFP0110GM20-D and EFP0111GM20-D in [Table 2.1 Ordering Information on page 3](#)
- Added EFP0107 OPN to the following sections:
 - [1. Feature List](#)
 - [Table 2.1 Ordering Information on page 3](#)
 - [5.1.3.5 EFP0106 / EFP0107](#)
 - [Table 3.2 DCDC A Configuration and Modes Summary on page 9](#)
 - [7.2 OTP Defaults](#)
- Combined EFP0109 and EFP0110 Electrical Specification tables into single table [5.1.3.7 EFP0109 / EFP0110](#).
- Corrected out-of-reset default voltages in [Table 3.1 OPN-Specific Features on page 8](#) and [Table 2.1 Ordering Information on page 3](#).
- Corrected EM2 Maximum Output Current value in [Table 3.8 Energy Modes Overview on page 22](#).
- VOB output programmable voltage maximum changed from 1.255V to 1.26V.
- EFP0111 VOA [output programmable voltage maximum](#) changed from 5.2V to 5.22V.
- Added absolute maximum voltage for EFP01 outputs pins to [5.1.1 Absolute Maximum Ratings](#).
- Added I2C timing in [I2C Timing Specification](#).
- Added default voltage at startup and LDO dropout voltage to VOA, VOB, and VOC specification tables.
- Added note about the expected VOA shutdown behavior on devices configured for Boost Mode to [3.8.2 Shutdown Behavior](#).
- Added footnote to VOA, VOB, and VOC specification tables clarifying that for converters enabled by default, the total startup time is the sum of the T_{START} and T_{BOOT} times.
- Added footnote to VOB and VOC specification tables for EFP0108 and EFP0111 clarifying that VOB and VOC maximum output voltage is limited by the VOA voltage in these configurations.
- Added [3.2.1.7 NTM Buck/Boost Transitional Mode](#) section for Buck/Boost operation.
- Added [3.2.1.10 Low Voltage Charge Pump](#) section.
- Added [Wired Buck](#) to Typical Connection Diagrams.
- Added Buck/Boost typical efficiency plots.

Revision 1.1

October, 2020

- Added EFP0110 OPN to the following sections:
 - [1. Feature List](#)
 - [Table 3.1 OPN-Specific Features on page 8](#)
 - [Table 2.1 Ordering Information on page 3](#)
 - [5.1.3.7 EFP0109 / EFP0110](#)
 - [Table 3.2 DCDC A Configuration and Modes Summary on page 9](#)
 - [3.2.4 Coarse Regulators](#)
 - [7.2 OTP Defaults](#)
- In [Table 5.8 EFP0104 VOA/VOC Electrical Specs on page 50](#):
 - Corrected Output programmable voltage range maximum value from 5.2V to 3.3V.
 - Corrected Output voltage accuracy conditions from $1.8V \leq VOA \leq 5.0V$ to $1.8V \leq VOA \leq 3.3V$.
- Removed Wired Buck Configuration from [4.1 Device Configurations](#) and [Table 3.2 DCDC A Configuration and Modes Summary on page 9](#).
- Corrected all OPNs in [Table 3.2 DCDC A Configuration and Modes Summary on page 9](#) and [2. Ordering Information](#).
- Corrected valid OTP_TEMP_CODE and OTP_OPN_NUM enumerations in [7.1 OTP Definition](#).
- Corrected EFP0109 Input Voltage Range in [Table 2.1 Ordering Information on page 3](#).
- In [Figure 4.6 Boost Bootstrap Configuration on page 35](#), corrected VOB output capacitor from 2.2 μ F to 10 μ F, added note about VOA capacitor value, added notes on VOC Output capacitors.
- In [4.1.5 Wired Boost Configuration \(EFP0109 & EFP0110\)](#), added clarification of VOB output capacitor size and added notes on VOC Output capacitors.
- In [4.1.4 Single-Cell Boost Configuration \(EFP0108\)](#) and [4.1.3 Buck/Boost Configuration \(EFP0106 & EFP0107\)](#), added notes on VOC Output capacitors.
- Added VOB = 1.8V Output Voltage Accuracy Specs for the EFP0109 VOB output.
- In all VOB and VOC Electrical Specification tables, clarified footnote indicating that when VDDB was powered by VOA (EFP0108 and EFP0111), the DCDC B and LDO C output current is also limited by the VOA output current.
- Added disclaimer clarifying that Maximum Output Current formulas are not a guarantee of performance to the [DCDC A Peak Current Configuration](#), [DCDC B Peak Current Configuration](#), and [LDO Maximum Output Current](#) sections.
- In [5.1.3.8 EFP0111 Electrical Specifications](#), corrected Maximum output current footnote test current (1.25mA instead of 5mA) and added details on how to interpret this specification for Boost Bootstrap.
- Added note to [3.3.4 EM4](#) section that dedicated EM4 hardware support was available for EFP01 starting on EFR32xG22 devices.
- Clarified recommended reset mechanisms and hazards in [3.5.1 OTP](#) section and [6.2.11 CMD](#) register description.

Revision 1.0

June, 2020

- Corrected typical single-output enabled quiescent current on front page.
- Corrected EFP0109GM20 max input voltage range in [Table 3.1 OPN-Specific Features on page 8](#).
- Corrected DCDC A Max Output Current Equations in [3.2.1.2 Peak Current Configuration](#).
- Corrected LDO Max Output Current Equation [3.2.3.3 Maximum Output Current](#).
- Added section explaining Ton_max limiting use in boost mode • [Boost Mode T_{ON_MAX} on page 15](#).
- Added notes clarifying that Direct Mode is intended for use-cases where EFP01 is the only device on the I2C bus to the [I2C 3.6.1 Inter-Integrated Circuit Interface \(I²C\)](#) and Direct Mode [3.3.1.2 Direct Mode Control](#) sections.
- Added note pointing to the AN1188: EFP01 Coulomb Counter app note in [3.4.1 Coulomb Counter](#).
- Updated link to Silicon Labs Quality webpage [5.1.1 Absolute Maximum Ratings](#).
- Updated values in Electrical Specifications:
 - Added Max On-Resistance values
 - Added typical ADC voltage and temperature accuracy specifications
 - Added Max Output Load Current minimum values to the VOA, VOB, VOC Electrical Spec tables, along with updated conditions
 - Updated Typ Line/Load Regulation values
 - Updated VOC output startup time value
- Documented issues with use of the CMD.RESET bit in the [6.1 Register Map](#)

Revision 0.5

March, 2020

- Updated QFN20 Land Pattern Diagram [9.2 QFN20 PCB Land Pattern](#).
- Updated all OPNs in Ordering Information Table.
- Updated Ordering Information Table to add new OPN: EFP0109.
- Updates to Electrical Specifications Table:
 - Added Typical Performance Curves
- Updates to System Overview [3.1 Introduction](#):
 - Added voltage configuration sections
 - Added Startup and Shutdown behavior sections
- Updates to Register Definitions [6.1 Register Map](#).

Revision 0.3

September, 2019

- Updates to Ordering Information Table [Table 2.1 Ordering Information on page 3](#).
- Updates to Electrical Specifications Table.
- Updates System Overview [3.1 Introduction](#).
- Updates to Register Definitions [6.1 Register Map](#).
- Updates to OTP Register Definitions [7.1 OTP Definition](#).
- Updates to Pin Definitions .

Revision 0.2

October, 2018

- Updated package marking decoder.

Revision 0.1

May, 2017

- Initial release.