EFR32FG22 Wireless Gecko SoC Family Data Sheet

The EFR32FG22 Wireless Gecko proprietary protocol family of SoCs is part of the Wireless Gecko portfolio. EFR32FG22 Wireless Gecko SoCs are ideal for enabling energy-friendly proprietary protocol networking for IoT devices.

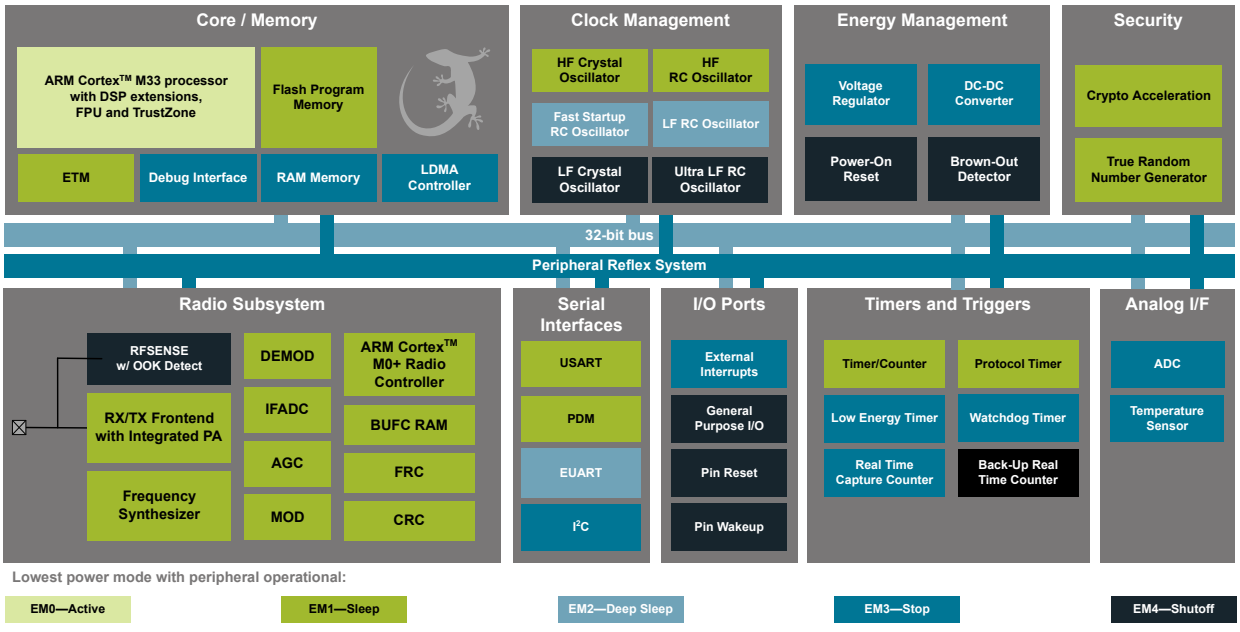
The single-die solution combines a 38.4 MHz Cortex-M33 with a high performance 2.4 GHz radio to provide an industry-leading, energy efficient, wireless SoC for IoT connected applications.

Wireless Gecko applications include:

- Electronic Shelf Labels
- Home and Building Automation and Security
- Industrial Automation
- Commercial and Retail Lighting and Sensing

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 38.4 MHz maximum operating frequency
- Up to 512 kB of flash and 32 kB of RAM
- Energy-efficient radio core with low active and sleep currents
- Integrated PA with up to 6 dBm (2.4 GHz) TX power
- Secure Boot with Root of Trust and Secure Loader (RTSL)
- RFSENSE with selective OOK mode



1. Feature List

The EFR32FG22 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 38.4 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 512 kB flash program memory
  - Up to 32 kB RAM data memory
  - 2.4 GHz radio operation
- **Radio Performance**
  - -102.3 dBm sensitivity @ 250 kbps O-QPSK DSSS
  - -98.9 dBm sensitivity @ 1 Mbit/s GFSK
  - -96.2 dBm sensitivity @ 2 Mbit/s GFSK
  - TX power up to 6 dBm
  - 2.5 mA radio receive current
  - 3.4 mA radio transmit current @ 0 dBm output power
  - 7.5 mA radio transmit current @ 6 dBm output power
- **Low System Energy Consumption**
  - 3.6 mA RX current (1 Mbps GFSK)
  - 3.9 mA RX current (250 kbps O-QPSK DSSS)
  - 4.1 mA TX current @ 0 dBm output power
  - 8.2 mA TX current @ 6 dBm output power
  - 26 µA/MHz in Active Mode (EM0) at 38.4 MHz
  - 1.20 µA EM2 DeepSleep current (8 kB RAM retention and RTC running from LFRCO)
  - 0.17 µA EM4 current
- **Supported Modulation Format**
  - 2 (G)FSK with fully configurable shaping
  - OQPSK DSSS
  - (G)MSK
- **Protocol Support**
  - Proprietary
- **Wide selection of MCU peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 1 × Enhanced Universal Asynchronous Receiver/Transmitter (EUART)
  - 2 × I^2C interface with SMBus support
  - Digital microphone interface (PDM)
  - RFSENSE with selective OOK mode
  - Die temperature sensor with +/-1.5 degree C accuracy after single-point calibration
- **Wide Operating Range**
  - 1.71 V to 3.8 V single power supply
  - -40 °C to 85 °C
- **Security Features**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
- **Packages**
  - **QFN40** 5 mm × 5 mm × 0.85 mm
  - **QFN32** 4 mm × 4 mm × 0.85 mm

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	Max CPU Speed	LFRCO	Flash (kB)	RAM (kB)	GPIO	Package	Temp Range
EFR32FG22C121F512GM32-C	Proprietary	6 dBm	38.4 MHz	Normal	512	32	18	QFN32	-40 to 85 °C
EFR32FG22C121F512GM40-C	Proprietary	6 dBm	38.4 MHz	Normal	512	32	26	QFN40	-40 to 85 °C

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high performance radio transceiver. The devices are well suited for secure connected IoT multi-protocol devices requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG22 Reference Manual.

A block diagram of the EFR32FG22 family is shown in Figure 3.1 Detailed EFR32FG22 Block Diagram on page 7. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

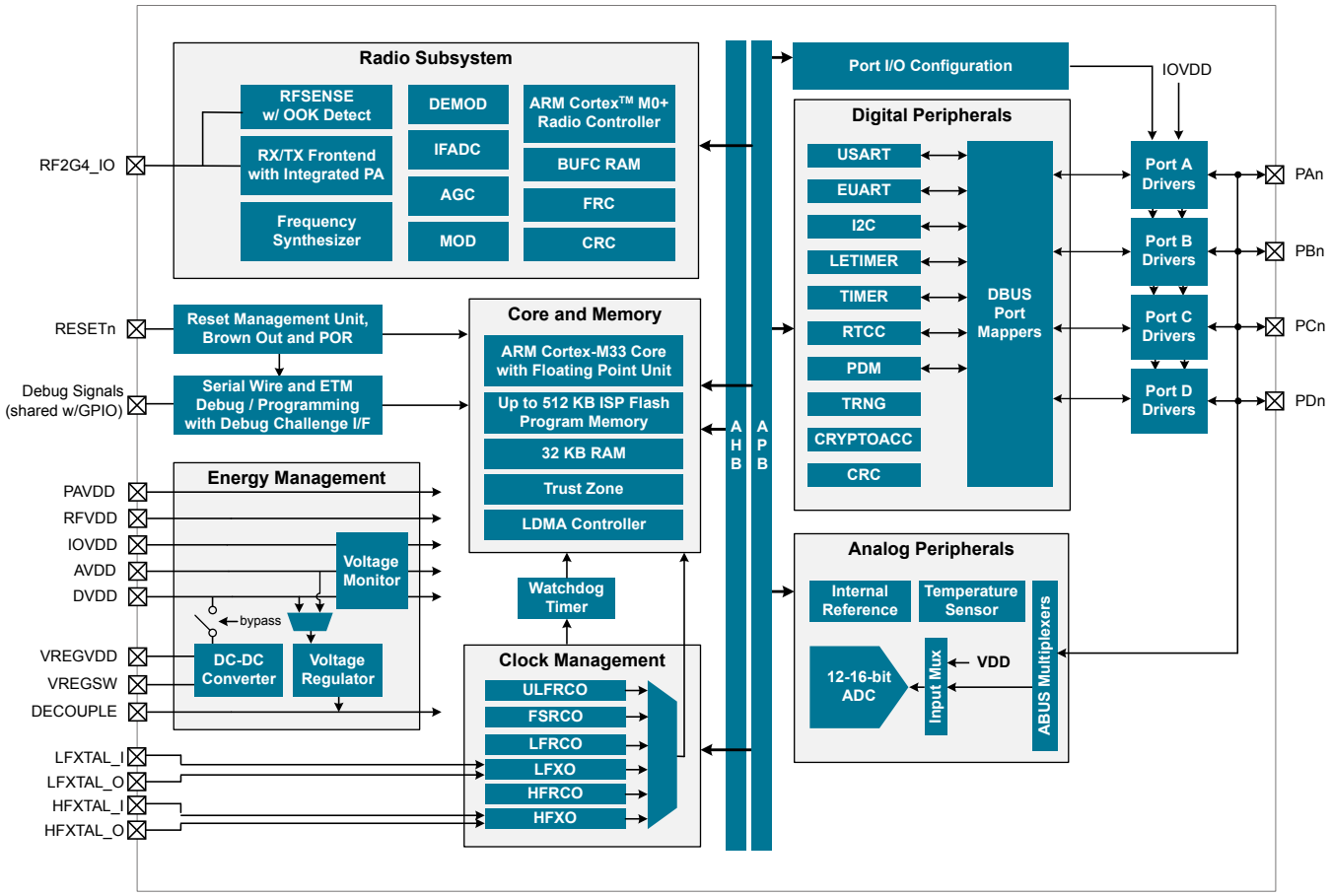

Figure 3.1. Detailed EFR32FG22 Block Diagram

3.2 Radio

The Wireless Gecko family features a radio transceiver supporting proprietary wireless protocols.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of a single-ended pin (RF2G4_IO). The external components for the antenna interface in typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32FG22 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.2.3 Receiver Architecture

The EFR32FG22 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

3.2.4 Transmitter Architecture

The EFR32FG22 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32FG22. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Packet and State Trace

The EFR32FG22 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.6 Data Buffering

The EFR32FG22 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.7 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32FG22. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.8 RFSENSE Interface

The RFSENSE block allows the device to remain in EM2, EM3 or EM4 and wake when RF energy above a specified threshold is detected. When operated in selective mode, the RFSENSE block performs OOK preamble and sync word detection, preventing false wake-up events.

3.3 General Purpose Input/Output (GPIO)

EFR32FG22 has up to 26 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in the Alternate Function Table.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32FG22. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFR32FG22 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO provides excellent RF clocking performance using a 38.4 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 38.4 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition some timers offer dead-time insertion.

See 3.13 Configuration Summary for information on the feature set of each timer.

3.5.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.5.3 Real Time Clock with Capture (RTCC)

The Real Time Clock with Capture (RTCC) is a 32-bit counter providing timekeeping down to EM3. The RTCC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.5.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Enhanced Universal Asynchronous Receiver/Transmitter (EUART)

The Enhanced Universal Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485 and IrDA support. In EM0 and EM1 the EUART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUART may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud.

3.6.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Note that not all instances of I^2C are available in all energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.6.5 Pulse Density Modulation (PDM) Interface

The PDM module provides a serial interface and decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-delta ADCs, digital sensors and other PDM or sigma delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports stereo or mono input data and DMA transfer.

3.7 Security Features

The following security features are available on the EFR32FG22:

- Secure Boot with Root of Trust and Secure Loader (RTSL)
- Cryptographic Accelerator
- True Random Number Generator (TRNG)
- Secure Debug with Lock/Unlock

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed and protects Over The Air updates.

More information on this feature can be found in the Application Note *AN1218: Series 2 Secure Boot with RTSL*.

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator which supports AES encryption and decryption with 128/192/256-bit keys, Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)
- CCM (Counter with CBC-MAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192 and P-256 for ECDH(Elliptic Curve Diffie-Hellman) key derivation and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations.

Supported hashes include SHA-1, SHA2/224, and SHA-2/256.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.7.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, the EFR32FG22 also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

More information on this feature can be found in the Application Note *AN1190: EFR32xG2x Secure Debug*.

3.8 Analog

3.8.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9 Power

The EFR32FG22 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32FG22 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

3.9.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.9.2 Voltage Scaling

The EFR32FG22 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.9.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, provides high efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 60 mA for device and radio operation. RF noise mitigation allows operation of the DC-DC converter without significantly degrading sensitivity of radio components. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

3.9.4 Power Domains

The EFR32FG22 has two peripheral power domains for operation in EM2 and EM3, as well as the ability to selectively retain configurations for EM0/EM1 peripherals. A small set of peripherals always remain powered on in EM2 and EM3, including all peripherals which are available in EM4. If all of the peripherals in PD0B are configured as unused, that power domain will be powered off in EM2 or EM3, reducing the overall current consumption of the device. Likewise, if the application can tolerate the setup time to re-configure used EM0/EM1 peripherals on wake, register retention for these peripherals can be disabled to further reduce the EM2 or EM3 current.

Table 3.1. Peripheral Power Subdomains

Always available in EM2/EM3	Power Domain PD0B
RTCC	LETIMER0
LFRCO (Non-precision mode)[1]	IADC0
LFXO[1]	I2C0
BURTC[1]	WDOG0
RFSENSE[1]	EUART0
ULFRCO[1]	PRS
FSRCO	DEBUG

Note:
1. Peripheral also available in EM4.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32FG22. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 512 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. In addition to the main flash array where Program code is normally written the MSC also provides an Information block where additional information such as special user information or flash-lock bits are stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32FG22 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

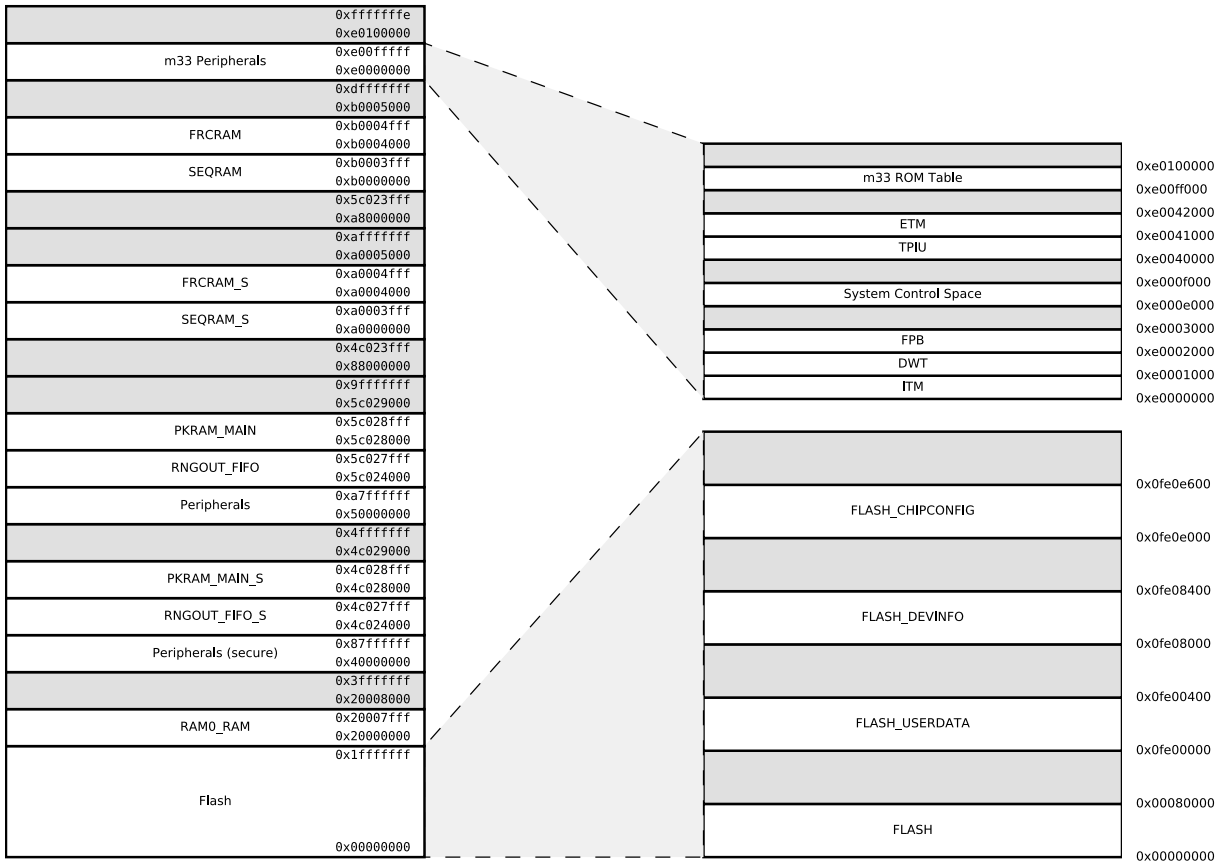

Figure 3.2. EFR32FG22 Memory Map — Core Peripherals and Code Space

3.13 Configuration Summary

The features of the EFR32FG22 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM3[1]	
I2C1	EM1	
IADC0	EM3	
LETIMER0	EM2[1]	
PDM	EM1	2-channel
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	16-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
EUART0	EM1 - Full high-speed operation EM3[1] - Low-energy operation, 9600 Baud	
USART0	EM1	+IrDA, +I2S, +SmartCard
USART1	EM1	+IrDA, +I2S, +SmartCard

Note:

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry (e.g., diodes), some EFR32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD & DVDD
  - In systems using the DCDC converter, DVDD (the buck converter output) should be connected to the recommended L_{DCDC} and C_{DCDC}, and should not be driven by an off-chip regulator.
  - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB (VREGVDD=DVDD)
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pin

4.2 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	+150	°C
Voltage on any supply pin[1]	V_{DDMAX}		-0.3	—	3.8	V
Junction temperature	T_{JMAX}	-G grade	—	—	+105	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
DC voltage on RESETn pin[2]	V_{RESETn}		-0.3	—	3.8	V
Input RF level on RF pins RF2G4_IO	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pin RF2G4_IO	V_{MAX2G4}		-0.3	—	V_{PAVDD} + 0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifications for more details.
2. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade [1]	-40	—	+85	°C
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4[2]	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.0	3.8	V
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.71	3.0	3.8	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.0	3.8	V
VREGVDD operating supply voltage	$V_{VREGVDD}$	DC-DC in regulation[3]	2.2	3.0	3.8	V
		DC-DC in bypass 60 mA load	1.8	3.0	3.8	V
		DC-DC not in use. DVDD externally shorted to VREGVDD	1.71	3.0	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.0	V_{PAVDD}	V
DECOUPLE output capacitor[4]	$C_{DECOUPLE}$	1.0 µF ± 10% X8L capacitor used for performance characterization.	1.0	—	2.75	µF
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE1, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE1	—	—	40	MHz
Radio HCLK frequency[5]	f_{RHCLK}	VSCALE2 or VSCALE1	—	38.4	—	MHz

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
3. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifications for more details.
4. Murata GCM21BL81C105KA58L used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 0.6 µF.
5. The recommended radio crystal frequency is 38.4 MHz. Any crystal frequency other than 38.4 MHz is expressly not supported. See HFXO specifications for more detail on crystal tolerance.

4.4 DC-DC Converter

Test conditions: L_{DCDC} = 2.2 µH (Samsung CIG22H2R2MNE), C_{DCDC} = 4.7 µF (Samsung CL10B475KQ8NQNC), $V_{VREGVDD}$ = 3.0 V, V_{OUT} = 1.8 V, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VREGVDD pin[1]	$V_{VREGVDD}$	DCDC in regulation, I_{LOAD} = 60 mA, EM0/EM1 mode	2.2	3.0	3.8*	V
		DCDC in regulation, I_{LOAD} = 5 mA, EM0/EM1 or EM2/EM3 mode	1.8	3.0	3.8*	V
		Bypass mode	1.8	3.0	3.8	V
Regulated output voltage	V_{OUT}		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	$V_{VREGVDD}$ ≥ 2.2 V, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2.5	—	3.3	%
Regulation total accuracy	ACC_{TOT}	With mode transitions between EM0/EM1 and EM2/EM3 modes	-5	—	7	%
Steady-state output ripple	V_R	I_{LOAD} = 20 mA in EM0/EM1 mode	—	14.3	—	mVpp
DC line regulation	V_{REG}	I_{LOAD} = 60 mA in EM0/EM1 mode, $V_{VREGVDD}$ ≥ 2.2 V	—	5.5	—	mV/V
DC load regulation	I_{REG}	Load current between 100 µA and 60 mA in EM0/EM1 mode	—	0.27	—	mV/mA
Efficiency	EFF	Load current between 100 µA and 60 mA in EM0/EM1 mode, or between 10 µA and 5 mA in EM2/EM3 mode	—	91	—	%
Output load current	I_{LOAD}	EM0/EM1 mode, DCDC in regulation	—	—	60	mA
		EM2/EM3 mode, DCDC in regulation	—	—	5	mA
		Bypass mode	—	—	60	mA
Nominal output capacitor	C_{DCDC}	4.7 µF ± 10% X7R capacitor used for performance characterization[2]	4.7	—	10	µF
Nominal inductor	L_{DCDC}	± 20% tolerance	—	2.2	—	µH
Nominal input capacitor	C_{IN}		C_{DCDC}	—	—	µF
Resistance in bypass mode	R_{BYP}	Bypass switch from VREGVDD to DVDD, $V_{VREGVDD}$ = 1.8 V	—	1.75	3	Ω
		Powertrain PFET switch from VREGVDD to VREGSW, $V_{VREGVDD}$ = 1.8 V	—	0.86	1.5	Ω
Supply monitor threshold programming range	V_{CMP_RNG}	Programmable in 0.1 V steps	2.0	—	2.3	V
Supply monitor threshold accuracy	V_{CMP_ACC}	Supply falling edge trip point	-5	—	5	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply monitor threshold hysteresis	V_{CMP_HYST}	Positive hysteresis on the supply rising edge referred to the falling edge trip point	—	4	—	%
Supply monitor response time	t_{CMP_DELAY}	Supply falling edge at -100 mV / µs	—	0.6	—	µs

Note:

1. The supported maximum $V_{VREGVDD}$ in regulation mode is a function of temperature and 10-year lifetime average load current. See more details in 4.4.1 DC-DC Operating Limits.
2. Samsung CL10B475KQ8NQNC used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 2.4 µF.

4.4.1 DC-DC Operating Limits

The maximum supported voltage on the VREGVDD supply pin is limited under certain conditions. Maximum input voltage is a function of temperature and the average load current over a 10-year lifetime. Figure 4.1 Lifetime average load current limit vs. Maximum input voltage on page 22 shows the safe operating region under specific conditions. Exceeding this safe operating range may impact the reliability and performance of the DC-DC converter.

The average load current for an application can typically be determined by examining the current profile during the time the device is powered. For example, an application that is continuously powered which spends 99% of the time asleep consuming 2 µA and 1% of the time active and consuming 10 mA has an average lifetime load current of about 102 µA.

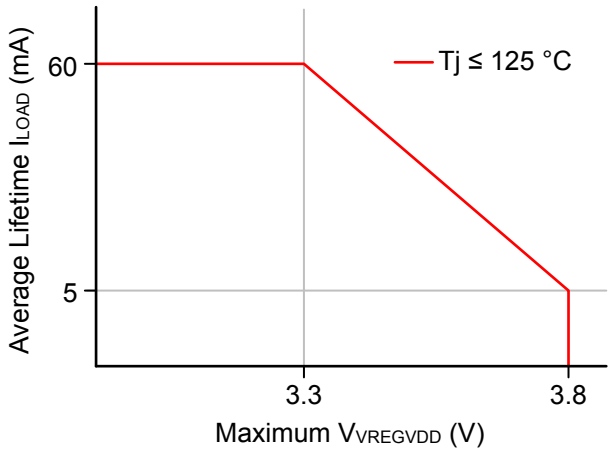

Figure 4.1. Lifetime average load current limit vs. Maximum input voltage

The minimum input voltage for the DC-DC in EM0/EM1 mode is a function of the maximum load current, and the peak current setting. Figure 4.2 Transient maximum load current vs. Minimum input voltage on page 22 shows the max load current vs. input voltage for different DC-DC peak inductor current settings.

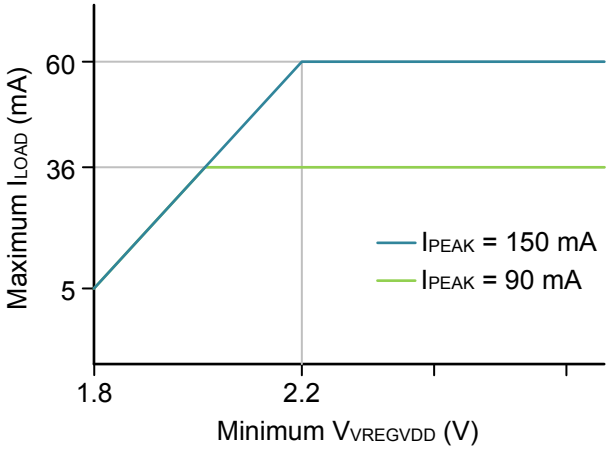

Figure 4.2. Transient maximum load current vs. Minimum input voltage

4.5 Thermal Characteristics

Table 4.4. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient QFN32 (4x4mm) Package	$THE-TA_{JA\_QFN32\_4X4}$	4-Layer PCB, Natural Convection[1]	—	35.4	—	°C/W
Thermal Resistance, Junction to Ambient, QFN40 (5x5mm) Package	$THE-TA_{JA\_QFN40\_5X5}$	4-Layer PCB, Natural Convection[1]	—	32.6	—	°C/W

Note:

1. Measured according to JEDEC standard JESD51-2A. Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).

4.6 Current Consumption

4.6.1 MCU current consumption using DC-DC at 3.0 V input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU current consumption using DC-DC at 3.0 V input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running Prime from flash	—	28	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	26	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	38	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	22	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	24	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	27	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	159	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal	—	17	—	µA/MHz
		38 MHz HFRCO	—	13	—	µA/MHz
		26 MHz HFRCO	—	15	—	µA/MHz
		16 MHz HFRCO	—	18	—	µA/MHz
		1 MHz HFRCO	—	150	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.40	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.32	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.21	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.20	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.03	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.05	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.37	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See for a list of the peripherals in each power domain.

4.6.2 MCU current consumption at 3.0 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 3.0 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. MCU current consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running Prime from flash	—	40	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	39	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	55	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	33	50	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	35	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	40	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	228	830	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal	—	25	—	µA/MHz
		38 MHz HFRCO	—	19	35	µA/MHz
		26 MHz HFRCO	—	21	—	µA/MHz
		16 MHz HFRCO	—	27	—	µA/MHz
		1 MHz HFRCO	—	215	770	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.94	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.95	4.9	µA
		24 kB RAM retention and RTC running from LFXO	—	1.81	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.64	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.65	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.39	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.41	3.7	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.17	0.43	µA
		BURTC with LFXO	—	0.50	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	234	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.56	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See for a list of the peripherals in each power domain.

4.6.3 MCU current consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. MCU current consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running Prime from flash	—	41	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	39	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	55	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	33	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	35	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	40	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	227	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal	—	25	—	µA/MHz
		38 MHz HFRCO	—	19	—	µA/MHz
		26 MHz HFRCO	—	21	—	µA/MHz
		16 MHz HFRCO	—	27	—	µA/MHz
		1 MHz HFRCO	—	213	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.87	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.86	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.73	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.57	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.56	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.32	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.34	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.13	—	µA
		BURTC with LFXO	—	0.44	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	190	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.54	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See for a list of the peripherals in each power domain.

4.6.4 Radio current consumption at 3.0V using DCDC

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = 3.0V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.8. Radio current consumption at 3.0V using DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	3.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	3.9	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	4.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	4.4	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.9	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1	—	4.1	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2	—	4.3	—	mA
System current consumption in receive mode, listening for packet	I_{RX_LISTEN}	1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	3.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	4.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	4.3	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	4.5	—	mA
		802.15.4, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.2	—	mA
		802.15.4, f = 2.4 GHz, VSCALE1	—	4.4	—	mA
		802.15.4, f = 2.4 GHz, VSCALE2	—	4.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	4.1	—	mA
		f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	8.2	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1	—	4.3	—	mA
		f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power, VSCALE1	—	8.4	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2	—	4.4	—	mA
		f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power, VSCALE2	—	8.5	—	mA

4.7 Flash Characteristics

Table 4.9. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V
Program Time	t_{PROG}	one word (32-bits)	42.1	44	45.6	uSec
		average per word over 128 words	10.3	10.9	11.3	uSec
Page Erase Time	t_{PERASE}		11.4	12.9	14.4	ms
Mass Erase Time	t_{MERASE}	Erases all of User Code area	11.7	13	14.3	ms
Program Current	I_{PROG}		—	—	1.45	mA
Page Erase Current	I_{PERASE}	Page Erase	—	—	1.34	mA
Mass Erase Current	I_{MERASE}	Mass Erase	—	—	1.28	mA

4.8 Wake Up, Entry, and Exit times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.10. Wake Up, Entry, and Exit times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
WakeupTime from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	AHB Clocks
		Code execution from RAM	—	1.42	—	µs
WakeupTime from EM2	t_{EM2_WU}	Code execution from flash, No Voltage Scaling	—	13.22	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.15	—	µs
		Voltage scaling up one level[1]	—	37.89	—	µs
		Voltage scaling up two levels[2]	—	50.56	—	µs
WakupTime from EM3	t_{EM3_WU}	Code execution from flash, No Voltage Scaling	—	13.21	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.15	—	µs
		Voltage scaling up one level[1]	—	37.90	—	µs
		Voltage scaling up two levels[2]	—	50.55	—	µs
WakeupTime from EM4	t_{EM4_WU}	Code execution from flash	—	8.81	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.29	—	µs
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	5.23	—	µs
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	5.23	—	µs
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	9.96	—	µs
Voltage scaling in time in EM0[3]	t_{SCALE}	Up from VSCALE1 to VSCALE2	—	32	—	µs
		Down from VSCALE2 to VSCALE1	—	172	—	µs

Note:
1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

4.9 RFSENSE Low-energy Wake-on-RF

Table 4.11. RFSENSE Low-energy Wake-on-RF

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Average current	$I_{RFSENSE}$	RF energy below wake threshold	—	138	—	nA
		Selective mode, RF energy above threshold but no OOK sync detected	—	131	—	nA
RF level above which RFSENSE will detect signal[1]	$THRES_{TRIG}$	Threshold set to -34 dBm	-28	—	—	dBm
		Threshold set to -22 dBm	-19	—	—	dBm
RF level below which RFSENSE will not detect signal[1]	$THRES_{NOTRIG}$	Threshold set to -34 dBm	—	—	-40	dBm
		Threshold set to -22 dBm	—	—	-26	dBm
Sensitivity in selective OOK mode[1]	$SENS_{OOK}$	Sensitivity for > 90% probability of OOK detection[2], threshold set to -34 dBm	-28	—	—	dBm
		Sensitivity for > 90% probability of OOK detection[2], threshold set to -22 dBm	-19	—	—	dBm

Note:

1. Values collected with conducted measurements performed at the end of the matching network.
2. Selective wake signal is 1 kHz OOK Manchester-coded, 8 bits of preamble, 32-bit sync word.

4.10 2.4 GHz RF Transceiver Characteristics

4.10.1 RF Transmitter Characteristics

4.10.1.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.12. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Radio-only current consumption while transmitting[1]	I_{TX_RADIO}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power	—	3.4	—	mA
		f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power	—	7.5	—	mA
Maximum TX power[2]	$POUT_{MAX}$	6 dBm PA[3]	—	6	—	dBm
		0 dBm PA	—	0	—	dBm
Minimum active TX power	$POUT_{MIN}$	6 dBm PA	—	-27	—	dBm
		0 dBm PA	—	-28	—	dBm
Output power variation vs supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	6 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.04	—	dB
		0 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.03	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	0 dBm PA at 0 dBm, (-40 to +85 °C)	—	1.0	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	6 dBm PA, 6 dBm	—	0.20	—	dB
		0 dBm PA, 0 dBm	—	0.19	—	dB
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz.	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-26	—	dBc
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-14G, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-36	—	dBm
Spurious emissions out-of-band, per ETSI 300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 862-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-16	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current to radio, supplied by DC-DC with 3.0 V, measured at VREGVDD.
2. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.
3. The PA is capable of delivering higher than 6 dBm output power (see Figure 4.9 Transmitter Output Power on page 64). However, all transmitter characteristics and recommended application circuits are specified at 6 dBm output. If used with the recommended application circuits above 6 dBm, harmonics may be higher than regulatory limits.

4.10.1.2 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.13. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude per 802.15.4-2011	EVM	Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 6 dBm	—	3.0	—	% rms
		Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 0 dBm	—	3.0	—	% rms
Power spectral density limit	PSD_{LIMIT}	Relative, at carrier ± 3.5 MHz, P_{out} = 6 dBm	—	-50.7	—	dBc/ 100kHz
		Relative, at carrier ± 3.5 MHz, P_{out} = 0 dBm	—	-50.8	—	dBc/ 100kHz
		Absolute, at carrier ± 3.5 MHz, P_{out} = 6 dBm	—	-52.5	—	dBm/ 100kHz
		Absolute, at carrier ± 3.5 MHz, P_{out} = 0 dBm	—	-58.3	—	dBm/ 100kHz
		Per FCC part 15.247, P_{out} = 6 dBm	—	-1.4	—	dBm/ 3kHz
		Per FCC part 15.247, P_{out} = 0 dBm	—	-7.4	—	dBm/ 3kHz
		ETSI 300.328 P_{out} = 6 dBm	—	5.6	—	dBm
		ETSI 300.328 P_{out} = 0 dbm	—	-1.0	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band, P_{out} = 6 dBm	—	2.2	—	MHz
		99% BW at highest and lowest channels in band, P_{out} = 0 dBm	—	2.2	—	MHz

4.10.1.3 RF Transmitter Characteristics for 2GFSK in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.14. RF Transmitter Characteristics for 2GFSK in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 6 dBm	—	630	—	kHz
		P_{out} = 0 dBm	—	640	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 6 dBm, Per FCC part 15.247 at 6 dBm	—	2.9	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-3.2	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	7.1	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 6 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz

4.10.1.4 RF Transmitter Characteristics for 2GFSK in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.15. RF Transmitter Characteristics for 2GFSK in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 6 dBm	—	1250	—	kHz
		P_{out} = 0 dBm	—	1220	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 6 dBm, Per FCC part 15.247 at 6 dBm	—	0.5	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-5.7	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	6.3	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 6 dBm 99% BW at highest and lowest channels in band	—	2.1	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	2.1	—	MHz

4.10.2 RF Receiver Characteristics

4.10.2.1 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.16. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Radio-only current consumption in receive mode[1]	I_{RX_RADIO}		—	2.5	—	mA
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-63	—	dBm
		1 GHz to 12 GHz	—	-53	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, conducted measurement	—	-47	—	dBm
		Above 960 MHz, conducted measurement.	—	-47	—	dBm
2GFSK Sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal, 1% PER	—	-93	—	dBm
		250 kbps 2GFSK signal, 0.1% BER	—	-104	—	dBm

Note:

1. Supply current to radio, supplied by DC-DC with 3.0 V, measured at VREGVDD.

4.10.2.2 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.17. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal[1]. Packet length is 20 octets	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets	—	-102.3	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 3 dB above sensitivity limit	—	-1.7	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{P1}	Interferer is reference signal at +1 channel-spacing	—	34.9	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{M1}	Interferer is reference signal at -1 channel-spacing	—	34.8	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_2	Interferer is reference signal at ± 2 channel-spacing	—	47.1	—	dB
Image rejection , 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	IR	Interferer is CW in image band[3]	—	34.1	—	dB
Blocking rejection of all other channels, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]. Interferer is reference signal	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	53.2	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	53.1	—	dB
RSSI resolution	$RSSI_{RES}$	-100 dBm to +5 dBm	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2003	$RSSI_{LIN}$		—	+/-6	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s.
2. Reference sensitivity level is -85 dBm.
3. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.10.2.3 RF Receiver Characteristics for 2GFSK in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.18. RF Receiver Characteristics for 2GFSK in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 255 byte payload[1]	—	-97.4	—	dBm
		Signal is reference signal, 37 byte payload[2]	—	-98.9	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 4 3 5]	—	-6.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 4 3 5]	—	-6.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-39.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 4 3 5]	—	-45.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 4 3 5]	—	-46.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-23.5	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-40.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-6.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.10.2.4 RF Receiver Characteristics for 2GFSK in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.19. RF Receiver Characteristics for 2GFSK in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-96.2	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-94.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	8.8	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-9.2	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-6.6	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 4 3 5]	—	-43.3	—	dB
		Interferer is reference signal at -4 MHz offset[1 4 3 5]	—	-44.0	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 4 3 5]	—	-48.6	—	dB
		Interferer is reference signal at -6 MHz offset[1 4 3 5]	—	-50.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-23.8	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 5]	—	-43.3	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 5]	—	-9.2	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. Desired signal -64 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.11 Oscillators

4.11.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.20. High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{HFXO}	see note[1]	—	38.4	—	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	38.4 MHz, CL = 10 pF[2] [3]	—	40	60	Ω
Supported range of crystal load capacitance[4]	C_{HFXO_LC}	38.4 MHz, ESR = 40 Ohm[3]	—	10	—	pF
Supply Current	I_{HFXO}		—	415	—	µA
Startup Time	$T_{STARTUP}$	38.4 MHz, ESR = 40 Ohm, CL = 10 pF	—	160	—	µs
On-chip tuning cap step size[5]	SS_{HFXO}		—	0.04	—	pF

Note:

1. The IEEE802.15.4 radio requires a 38.4 MHz crystal with a tolerance of ± 40 ppm over temperature and aging. Please use the recommended crystal.
2. The crystal should have a maximum ESR less than or equal to this maximum rating.
3. RF performance characteristics have been determined using crystals with an ESR of 40 Ω and CL of 10 pF.
4. Total load capacitance as seen by the crystal.
5. The tuning step size is the effective step size when incrementing one of the tuning capacitors by one count. The step size for the each of the indivdual tuning capacitors is twice this value.

4.11.2 Low Frequency Crystal Oscillator

Table 4.21. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kOhm, CL = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	357	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kOhm, CL = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	63	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.11.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.22. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F_{HFRCO_ACC}	For all production calibrated frequencies	-3	—	3	%
Current consumption on all supplies [1]	I_{HFRCO}	F_{HFRCO} = 1 MHz	—	28	—	µA
		F_{HFRCO} = 2 MHz	—	28	—	µA
		F_{HFRCO} = 4 MHz	—	28	—	µA
		F_{HFRCO} = 5 MHz	—	30	—	µA
		F_{HFRCO} = 7 MHz	—	60	—	µA
		F_{HFRCO} = 10 MHz	—	66	—	µA
		F_{HFRCO} = 13 MHz	—	79	—	µA
		F_{HFRCO} = 16 MHz	—	88	—	µA
		F_{HFRCO} = 19 MHz	—	92	—	µA
		F_{HFRCO} = 20 MHz	—	105	—	µA
		F_{HFRCO} = 26 MHz	—	118	—	µA
		F_{HFRCO} = 32 MHz	—	141	—	µA
		F_{HFRCO} = 38 MHz	—	172	—	µA
Clock out current for HFRCODPLL[2]	$I_{CLKOUT\_HFRCODPLL}$	FORECEEN bit of CTRL = 1 and the CLKOUTDIS0 bit of TEST = 1.	—	2.72	—	µA/MHz
		FORECEEN bit of CTRL i= 1 and the CLKOUTDIS1 bit of TEST = 1.	—	0.36	—	µA/MHz
Startup Time[3]	$T_{STARTUP}$	FREQRANGE = 0 to 7	—	1.2	—	µs
		FREQRANGE = 8 to 15	—	0.6	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band Frequency Limits[4]	f_{HFRCO_BAND}	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17.0	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33.0	—	51.0	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
3. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
4. The frequency band limits represent the lowest and highest freqeuncy which each band can achieve over the operating range.

4.11.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.23. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		17.2	20	21.2	MHz

4.11.5 Low Frequency RC Oscillator (LFRCO)

Table 4.24. Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}		-3	—	3	%
Startup time	$t_{STARTUP}$		—	204	—	µs
Current consumption	I_{LFRCO}		—	175	—	nA

4.11.6 Ultra Low Frequency RC Oscillator

Table 4.25. Ultra Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	F_{ULFRCO}		0.944	1.0	1.095	kHz

4.12 GPIO Pins (3V GPIO pins)

Table 4.26. GPIO Pins (3V GPIO pins)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8 V T_A = 85 °C	—	—	150	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3*IOVDD	V
		RESETn	—	—	0.3*DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7*IOVDD	—	—	V
		RESETn	0.7*DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*IOVDD	—	—	V
		RESETn	0.05*DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.13 Analog to Digital Converter (IADC)

Specified at 1 Msps, ADCCLK = 10 MHz, OSR=2, unless otherwise indicated.

Table 4.27. Analog to Digital Converter (IADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	V_{AVDD}	Normal Mode	1.71	—	3.8	V
Maximum Input Range[1]	V_{IN_MAX}	Maximum allowable input voltage	0	—	AVDD	V
Full-Scale Voltage	V_{FS}	Voltage required for Full-Scale measurement	—	V_{REF} / Gain	—	
Input Measurement Range	V_{IN}	Differential Mode - Plus and Minus inputs	$-V_{FS}$	—	$+V_{FS}$	V
		Single Ended Mode - One input tied to ground	0	—	V_{FS}	V
Input Sampling Capacitance	Cs	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	f_{CLK}	Normal Mode	—	—	10	MHz
Throughput rate	f_{SAMPLE}	f_{CLK} = 10 MHz, OSR = 2	—	—	1	Msps
		f_{CLK} = 10 MHz, OSR = 32	—	—	76.9	ksps
Current from all supplies, Continuous operation	I_{ADC_CONT}	Normal Mode, 1 Msps, OSR = 2, f_{CLK} = 10 MHz	—	290	385	µA
Current in Standby mode. ADC is not functional but can wake up in 1us.	I_{STBY}	Normal Mode	—	16	—	µA
ADC Startup Time	$t_{startup}$	From power down state	—	5	—	µs
		From Standby state	—	1	—	µs
ADC Resolution[2]	Resolution		—	12	—	bits
			—	16	—	bits
Differential Nonlinearity	DNL	Differential Input, OSR = 2, (No missing codes) .	-1	+/- 0.25	1.5	LSB12
Integral Nonlinearity	INL	Normal Mode, Differential Input, OSR = 2.	-2.5	+/- 0.65	2.5	LSB12
Effective number of bits[3]	ENOB	Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V. OSR=2	10.5	11.7	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, Internal VREF = 1.21 V.	—	13.5	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, External VREF = 1.25 V.	—	14.3	—	bits

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to Noise + Distortion Ratio[3]	SNDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	65	72.3	—	dB
		Differential Input. Gain=2x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.3	—	dB
		Differential Input. Gain=4x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	68.8	—	dB
		Differential Input. Gain=0.5x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.5	—	dB
Total Harmonic Distortion	THD	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	-80.8	-70	dB
Spurious-Free Dynamic Range	SFDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	72	86.5	—	dB
Common Mode Rejection Ratio	CMRR	Normal Mode. DC to 100 Hz	—	87.0	—	dB
		Normal Mode. AC high frequency	—	68.6	—	dB
Power Supply Rejection Ratio	PSRR	Normal mode. DC to 100 Hz	—	80.4	—	dB
		Normal mode. AC high frequency, using VREF pad.	—	33.4	—	dB
		Normal mode. AC high frequency, using internal VBGR.	—	65.2	—	dB
Gain Error	GE	GAIN=1 and 0.5, using external VREF, direct mode.	-0.3	0.069	0.3	%
		GAIN=2, using external VREF, direct mode.	-0.4	0.151	0.4	%
		GAIN=3, using external VREF, direct mode.	-0.7	0.186	0.7	%
		GAIN=4, using external VREF, direct mode.	-1.1	0.227	1.1	%
		Internal VREF[4], all GAIN settings	-1.5	0.023	1.5	%
Offset	OFFSET	GAIN=1 and 0.5, Differential Input	-3	0.27	3	LSB
		GAIN=2, Differential Input	-4	0.27	4	LSB
		GAIN=3, Differential Input	-4	0.25	4	LSB
		GAIN=4, Differential Input	-4	0.29	4	LSB
External reference voltage range[1]	V_{EVREF}		1.0	—	AVDD	V
Internal Reference voltage	V_{IVREF}		—	1.21	—	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR=2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: ENOB = (SNDR - 1.76) / 6.02.
4. Includes error from internal VREF drift.

4.14 Temperature Sense

Table 4.28. Temperature Sense

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range[1]	T_{RANGE}		-40	—	125	°C
Temperature sensor resolution	$T_{RESOLUTION}$		—	0.25	—	°C
Measurement noise (RMS)	T_{NOISE}	Single measurement	—	0.6	—	°C
		16-sample average (TEMPAVGNUM = 0)	—	0.17	—	°C
		64-sample average (TEMPAVGNUM = 1)	—	0.12	—	°C
Temperature offset	T_{OFF}	Mean error of uncorrected output across full temperature range	—	3.14	—	°C
Temperature sensor accuracy[2] [3]	T_{ACC}	Direct output accuracy after mean error (T_{OFF}) removed	-3	—	3	°C
		After linearization in software, no calibration	-2	—	2	°C
		After linearization in software, with single-temperature calibration at 25 °C[4]	-1.5	—	1.5	°C
Measurement interval	t_{MEAS}		—	250	—	ms

Note:

1. The sensor reports absolute die temperature in °K. All specifications are in °C to match the units of the specified product temperaure range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

4.15 Brown Out Detectors

4.15.1 DVDD BOD

BOD Thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.29. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply Rising	—	1.64	1.71	V
		Supply Falling	1.62	1.65	—	V
BOD response time	$t_{DVDD\_BOD\_DELAY}$	Supply dropping at 100mV/µs slew rate[1]	—	0.95	—	µs
BOD hysteresis	$V_{DVDD\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.15.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.30. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD\_LE\_BOD}$	Supply Falling	1.5	—	1.71	V
BOD response time	$t_{DVDD\_LE\_BOD\_DELAY}$	Supply dropping at 2mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	$V_{DVDD\_LE\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.15.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.31. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	—	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	V_{BOD_HYST}		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.16 PDM Timing Specifications

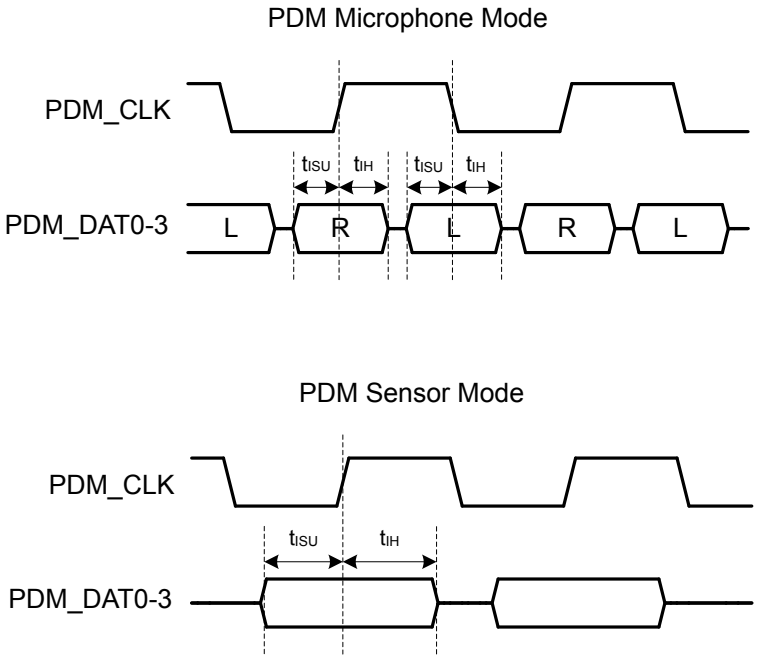

Figure 4.3. PDM Timing Diagrams

4.16.1 Pulse Density Modulator (PDM), Common DBUS

Timing specifications are for all PDM signals routed to the same DBUS (DBUSAB or DBUSCD), though routing to the same GPIO port is the optimal configuration. C_{LOAD} < 20 pF. System voltage scaling = VSCALE1 or VSCALE2. All GPIO set to slew rate = 6. Data delay (PDM_CFG1_DLYMUXSEL) = 0.

Table 4.32. Pulse Density Modulator (PDM), Common DBUS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PDM_CLK frequency during data transfer	F_{PDM_CLK}	Microphone mode	—	—	5	MHz
		Sensor mode	—	—	20	MHz
PDM_CLK duty cycle	DC_{PDM_CLK}		47.5	—	52.5	%
PDM_CLK rise time	t_R		—	—	5.5	ns
PDM_CLK fall time	t_F		—	—	5.5	ns
Input setup time	t_{ISU}	Microphone mode	30	—	—	ns
		Sensor mode	20	—	—	ns
Input hold time	t_{IH}		3	—	—	ns

4.17 USART SPI Main Timing

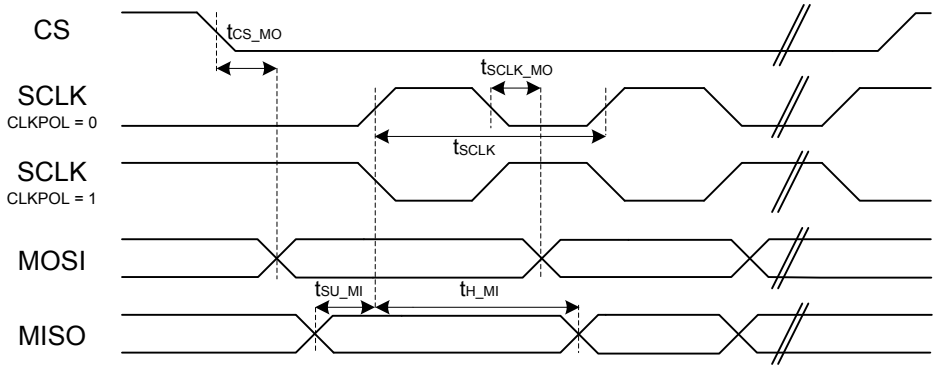

Figure 4.4. SPI Main Timing (SMSDELAY = 0)

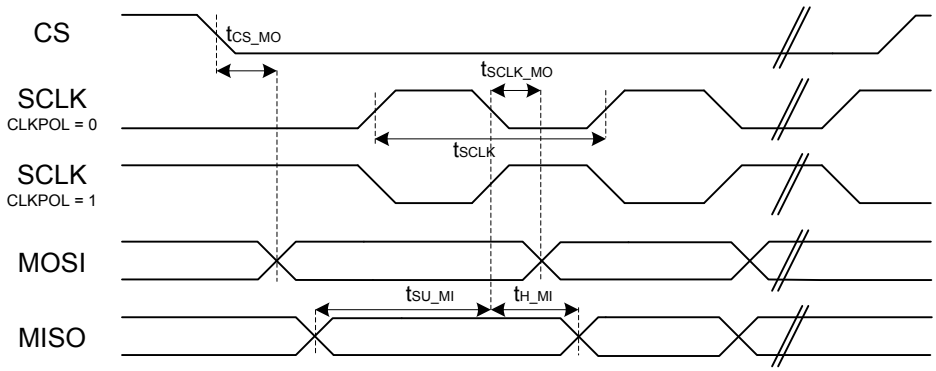

Figure 4.5. SPI Main Timing (SMSDELAY = 1)

4.17.1 SPI Main Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.33. SPI Main Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		$2*t_{PCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		-22	—	22.5	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		-14.5	—	14.5	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.62 V	38.5	—	—	ns
		IOVDD = 3.0 V	28.5	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		-8.5	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. t_{PCLK} is one period of the selected PCLK.

4.17.2 SPI Main Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.34. SPI Main Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		$2*t_{PCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		-33	—	34.5	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		-15	—	26	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.62 V	47	—	—	ns
		IOVDD = 3.0 V	39	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		-9.5	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. t_{PCLK} is one period of the selected PCLK.

4.18 USART SPI Secondary Timing

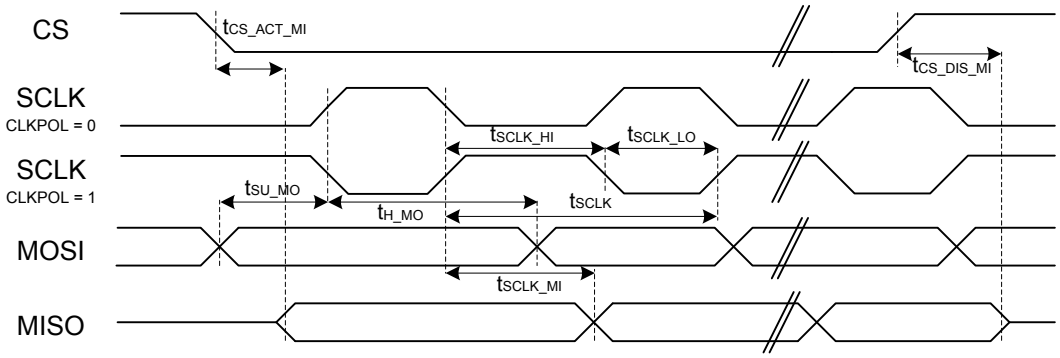

Figure 4.6. SPI Secondary Timing

4.18.1 SPI Secondary Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.35. SPI Secondary Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time [1] [2] [3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time [1] [2] [3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		25	—	47.5	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		19.5	—	38.5	ns
MOSI setup time [1] [2]	t_{SU_MO}		4.5	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		5	—	—	ns
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		22 + 1.5*t_{PCLK}	—	33.5 + 2.5*t_{PCLK}	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. t_{PCLK} is one period of the selected PCLK.

4.18.2 SPI Secondary Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.36. SPI Secondary Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		$6*t_{PCLK}$	—	—	ns
SCLK high time [1] [2] [3]	t_{SCLK_HI}		$2.5*t_{PCLK}$	—	—	ns
SCLK low time [1] [2] [3]	t_{SCLK_LO}		$2.5*t_{PCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		30.5	—	57.5	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		25	—	55	ns
MOSI setup time [1] [2]	t_{SU_MO}		7.5	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		8.5	—	—	ns
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		$24.5 + 1.5*t_{PCLK}$	—	$45.5 + 2.5*t_{PCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. t_{PCLK} is one period of the selected PCLK.

4.19 I2C Electrical Specifications

4.19.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.37. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	µs
STOP condition set-up time	t_{SU_STO}		4.0	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.19.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.38. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.19.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.39. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.20 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.20.1 Supply Current

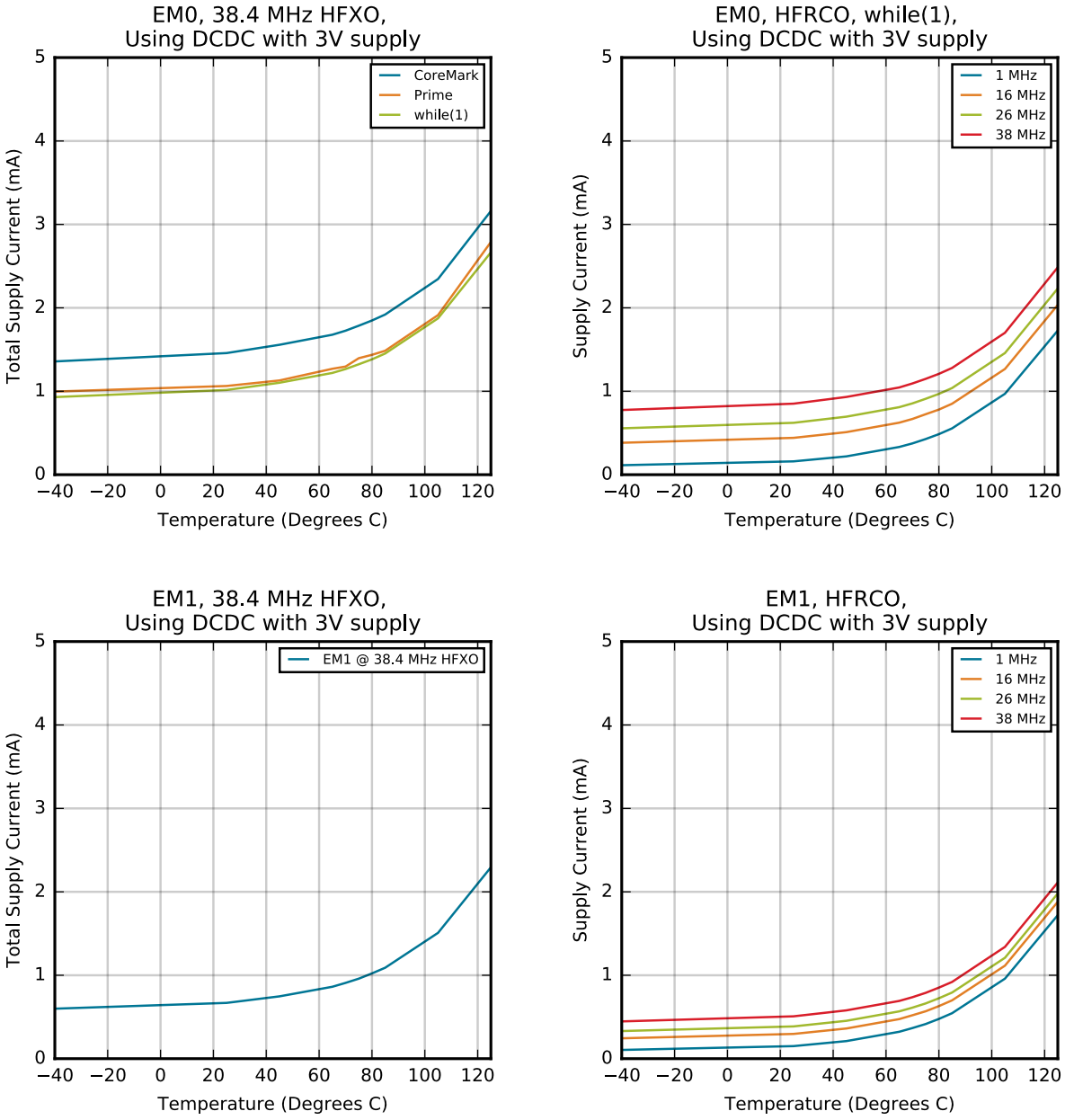

Figure 4.7. EM0 and EM1 Typical Supply Current vs. Temperature

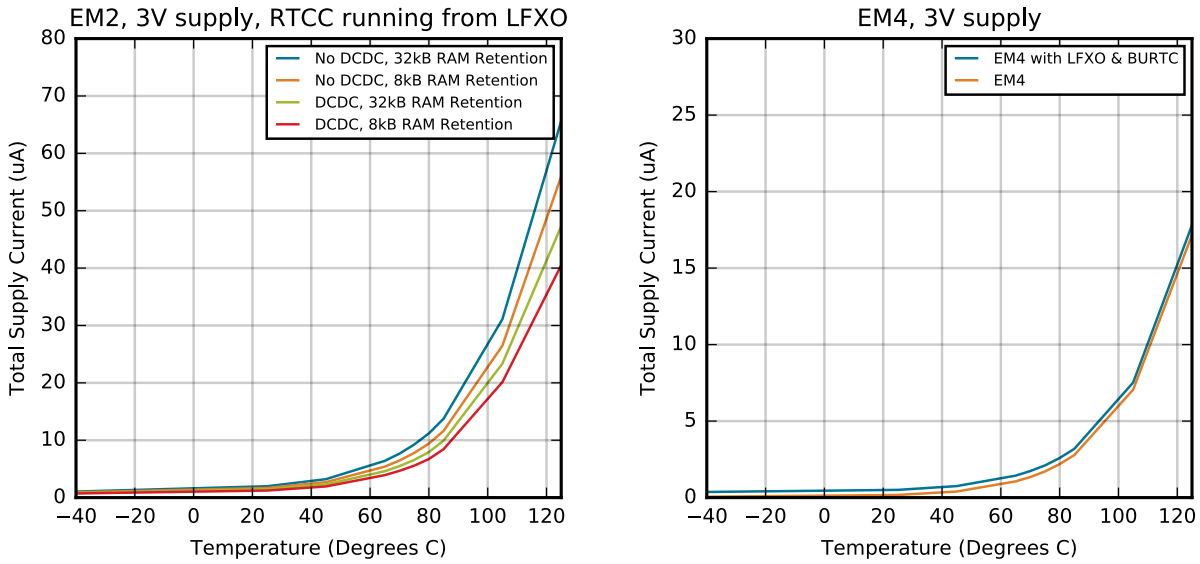

Figure 4.8. EM2 and EM4 Typical Supply Current vs. Temperature

4.20.2 RF Characteristics

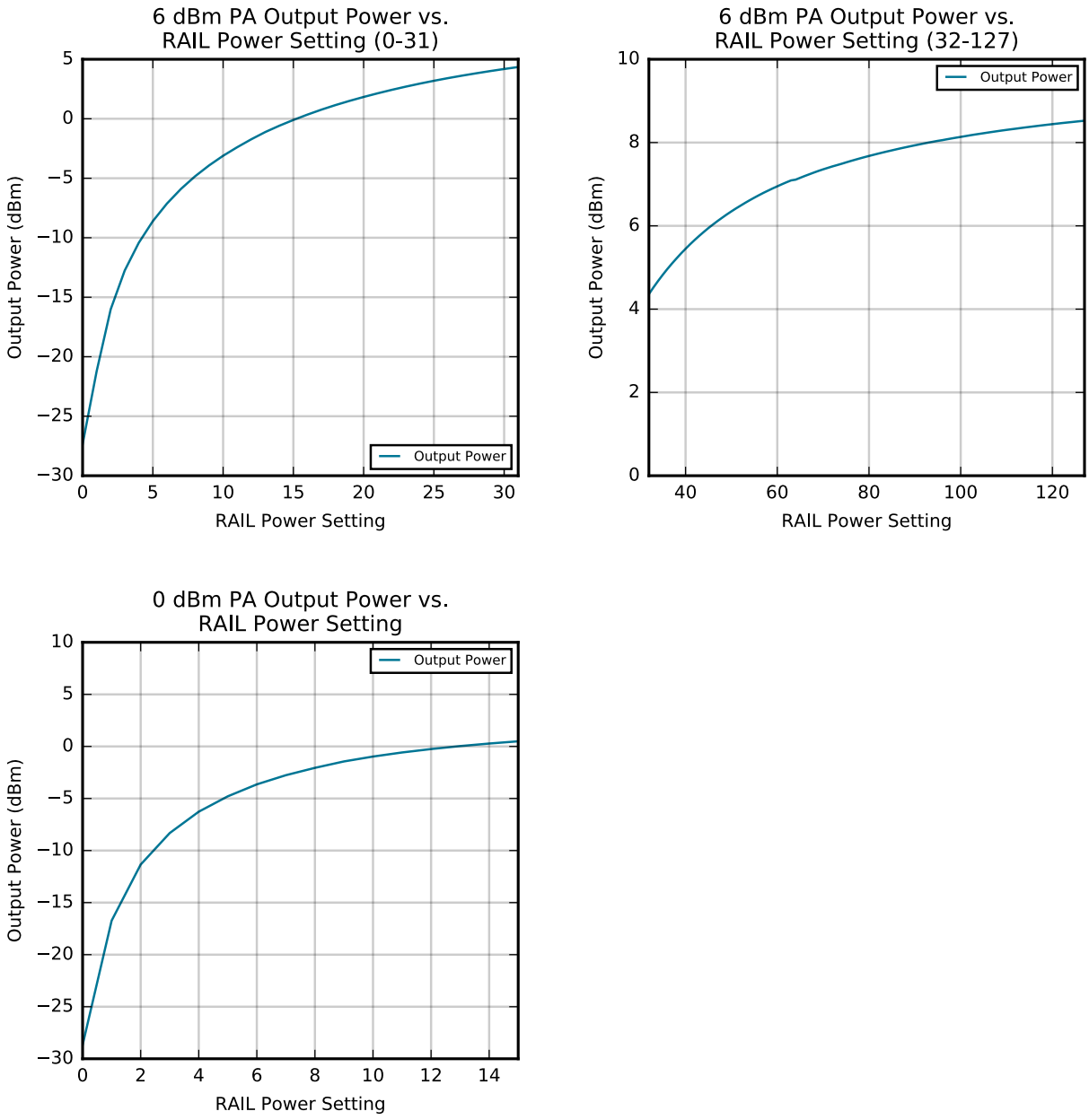

Figure 4.9. Transmitter Output Power

Note: Although the 6 dBm PA is capable of delivering more than 6 dBm output power, all transmitter characteristics and recommended application circuits are specifiat 6 dBm. Above 6 dBm, current consumption will increase and harmonics may be higher than regulatory limits.

4.20.3 DC-DC Converter

Performance characterized with Samsung CIG22H2R2MNE (L_{DCDC} = 2.2 uH) and Samsung CL10B475KQ8NQNC (C_{DCDC} = 4.7 uF)

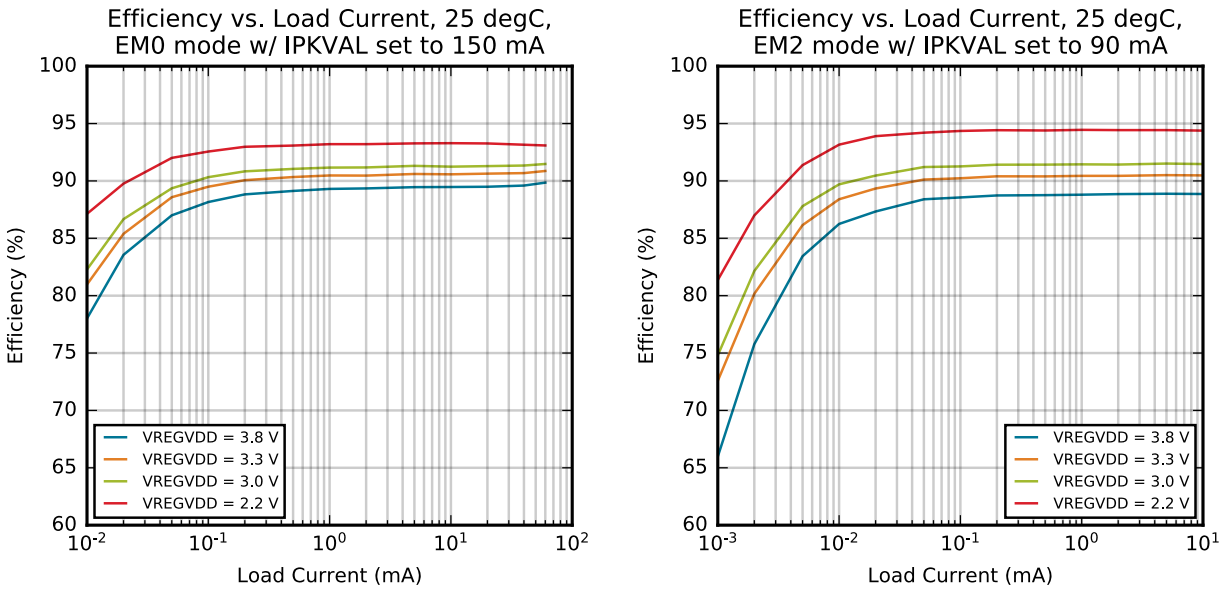

Figure 4.10. DC-DC Efficiency

4.20.4 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

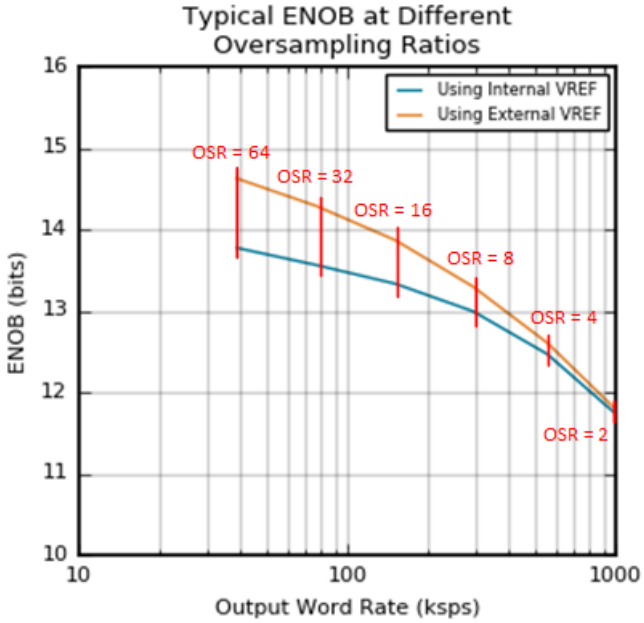

Figure 4.11. Typical ENOB vs. Oversampling Ratio

5. Typical Connections

5.1 Power

Typical power supply connections are shown in the following figures.

Note: PAVDD, RFVDD, AVDD, and IOVDD supply connections are flexible. They may be connected in other configurations or to external supplies as long as the supply limits described in 4.1 Electrical Characteristics are met.

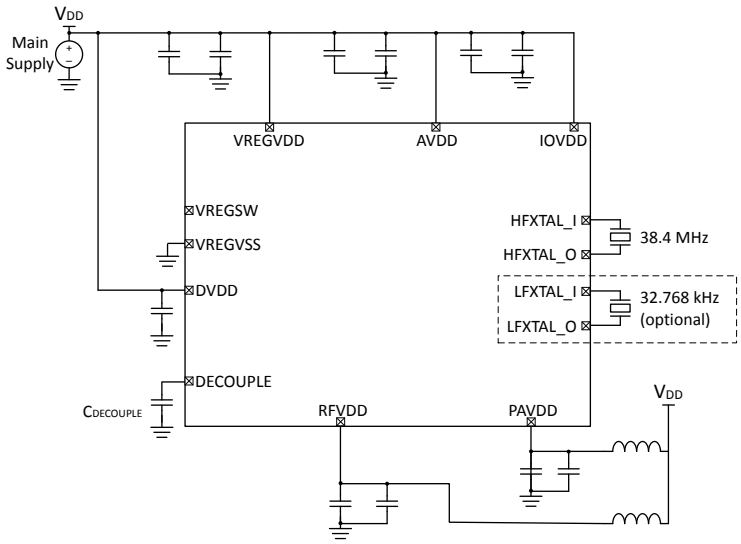

Figure 5.1. EFR32FG22 Typical Application Circuit: Direct Supply Configuration without DCDC

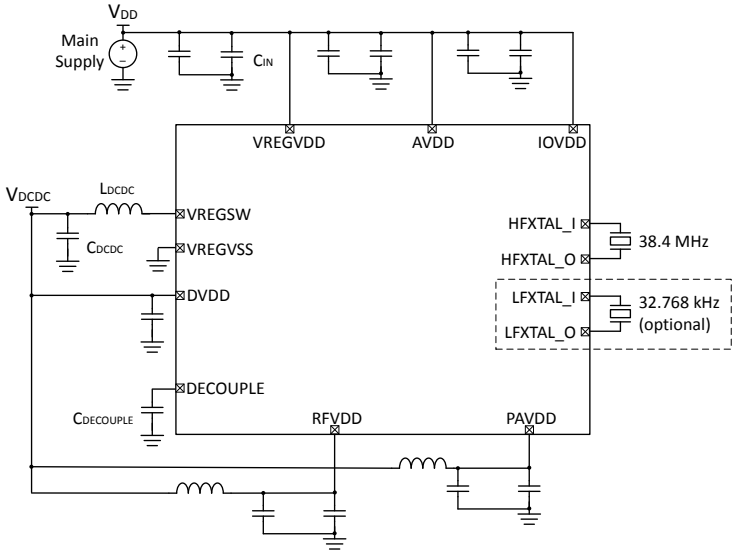

Figure 5.2. EFR32FG22 Typical Application Circuit: DCDC Configuration, PAVDD and RFVDD from DCDC output, AVDD and IOVDD from main supply

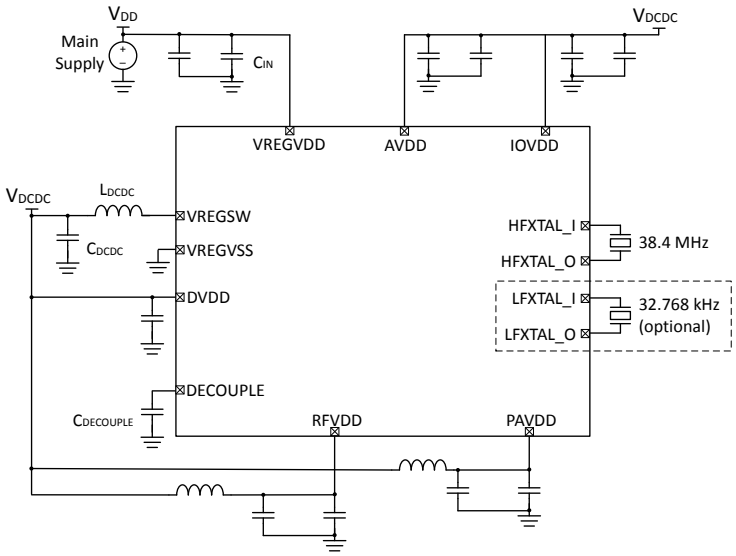

Figure 5.3. EFR32FG22 Typical Application Circuit: DCDC Configuration with PAVDD, RFVDD, AVDD, and IOVDD from DCDC output

5.2 RF Matching Networks

5.2.1 2.4 GHz Matching Network

The recommended RF matching network circuit diagram is shown in Figure 5.4 Typical RF impedance-matching network circuit on page 67. Typical component values are shown in Table 5.1 Component Values on page 67. Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

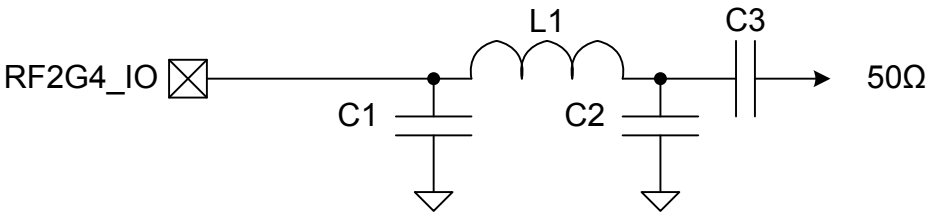

Figure 5.4. Typical RF impedance-matching network circuit

Table 5.1. Component Values

Designator	Value
C1	1.2 pF
C2	1.3 pF
L1	2.6 nH
C3	18 pF

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.2: "EFR32 Wireless Gecko Series 2 Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN32 Device Pinout

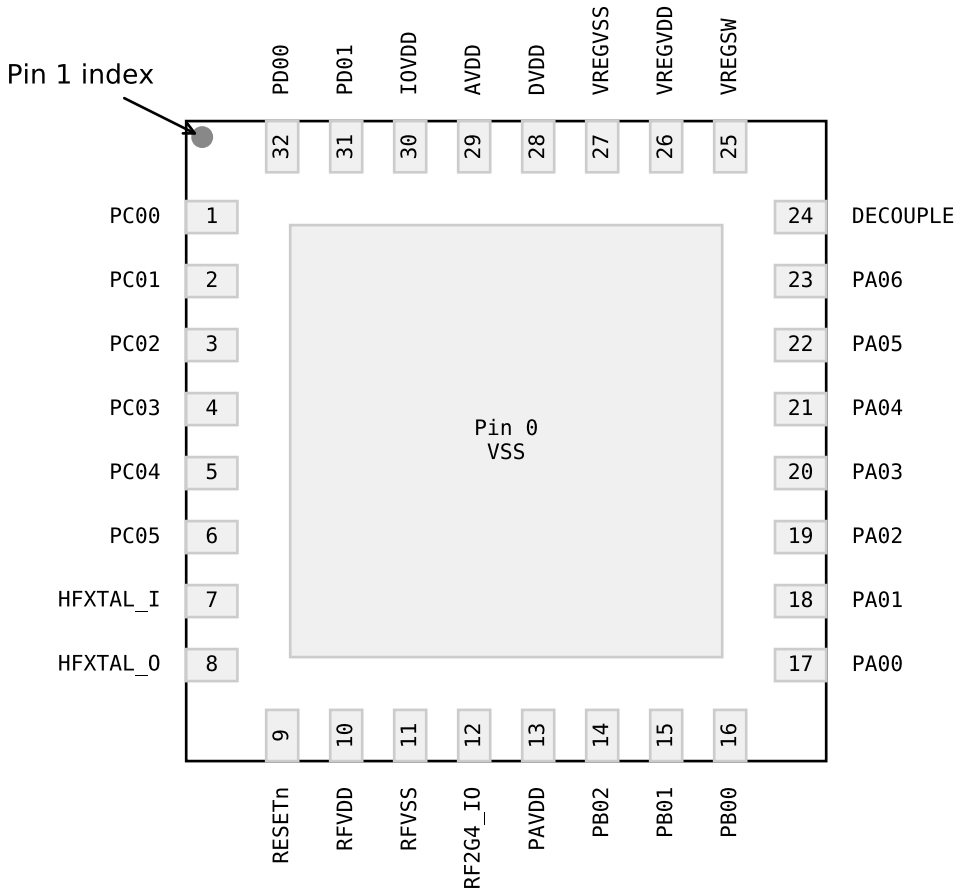

Figure 6.1. QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

Table 6.1. QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	9	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	10	Radio power supply
RFVSS	11	Radio Ground	RF2G4_IO	12	2.4 GHz Single-ended RF input/output
PAVDD	13	Power Amplifier (PA) power supply	PB02	14	GPIO
PB01	15	GPIO	PB00	16	GPIO
PA00	17	GPIO	PA01	18	GPIO
PA02	19	GPIO	PA03	20	GPIO
PA04	21	GPIO	PA05	22	GPIO
PA06	23	GPIO	DECOUPLE	24	Decouple outputput for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	25	DCDC regulator switching node	VREGVDD	26	DCDC regulator input supply
VREGVSS	27	DCDC ground	DVDD	28	Digital power supply
AVDD	29	Analog power supply	IOVDD	30	I/O power supply
PD01	31	GPIO	PD00	32	GPIO

6.2 QFN40 Device Pinout

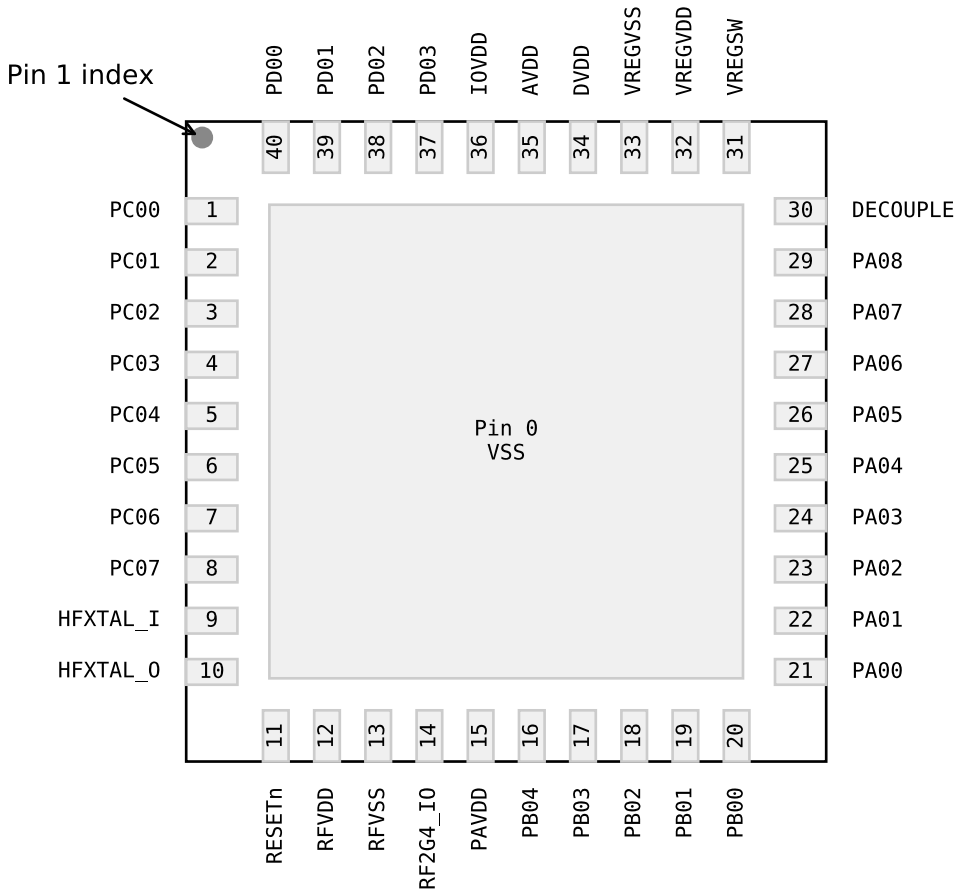

Figure 6.2. QFN40 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

Table 6.2. QFN40 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High Frequency Crystal Input	HFXTAL_O	10	High Frequency Crystal Output
RESETn	11	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RFVSS	13	Radio Ground	RF2G4_IO	14	2.4 GHz Single-ended RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB04	16	GPIO
PB03	17	GPIO	PB02	18	GPIO
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	DECOUPLE	30	Decouple outputput for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	31	DCDC regulator switching node	VREGVDD	32	DCDC regulator input supply
VREGVSS	33	DCDC ground	DVDD	34	Digital power supply
AVDD	35	Analog power supply	IOVDD	36	I/O power supply
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.3 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows what functions are available on each device pin.

Table 6.3. GPIO Alternate Function Table

GPIO	Alternate Function				
PC00	GPIO.EM4WU6	GPIO.THMSW_EN			
PC05	GPIO.EM4WU7				
PC07	GPIO.EM4WU8				
PB03	GPIO.EM4WU4				
PB01	GPIO.EM4WU3				
PB00	IADC0.VREFN				
PA00	IADC0.VREFP				
PA01	GPIO.SWCLK				
PA02	GPIO.SWDIO				
PA03	GPIO.SWV	GPIO.TDO	GPIO.TRACEDATA0		
PA04	GPIO.TDI	GPIO.TRACECLK			
PA05	GPIO.EM4WU0				
PD02	GPIO.EM4WU9				
PD01	LFXO.LFXTAL_I	LFXO.LF_EXTCLK			
PD00	LFXO.LFXTAL_O				

6.4 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is avaliable on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals.

Table 6.4. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.5 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 6.5. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUART0.CTS	Available	Available	Available	Available
EUART0.RTS	Available	Available	Available	Available
EUART0.RX	Available	Available	Available	Available
EUART0.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

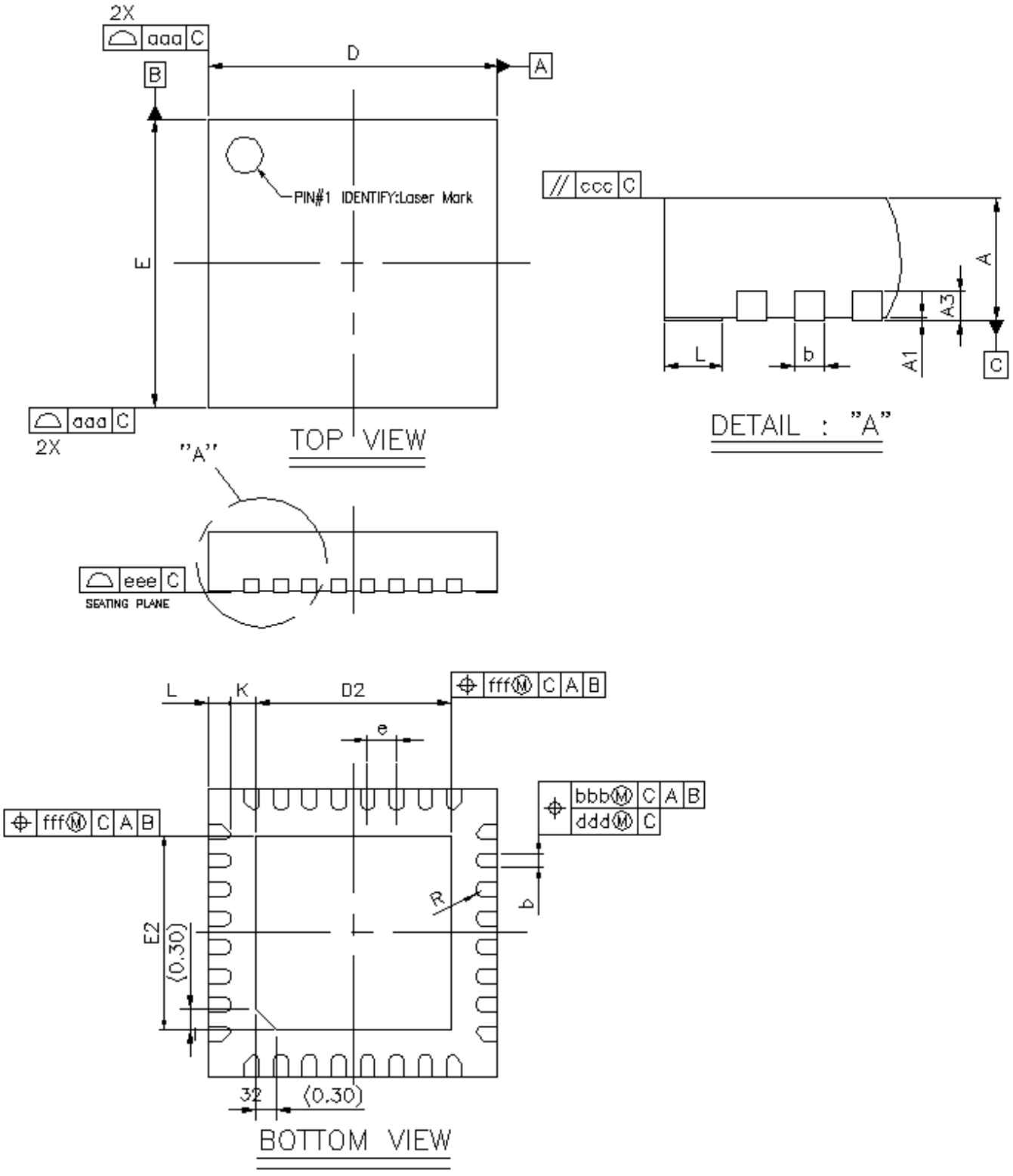

Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.20	0.30	0.40
K	0.20	—	—
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

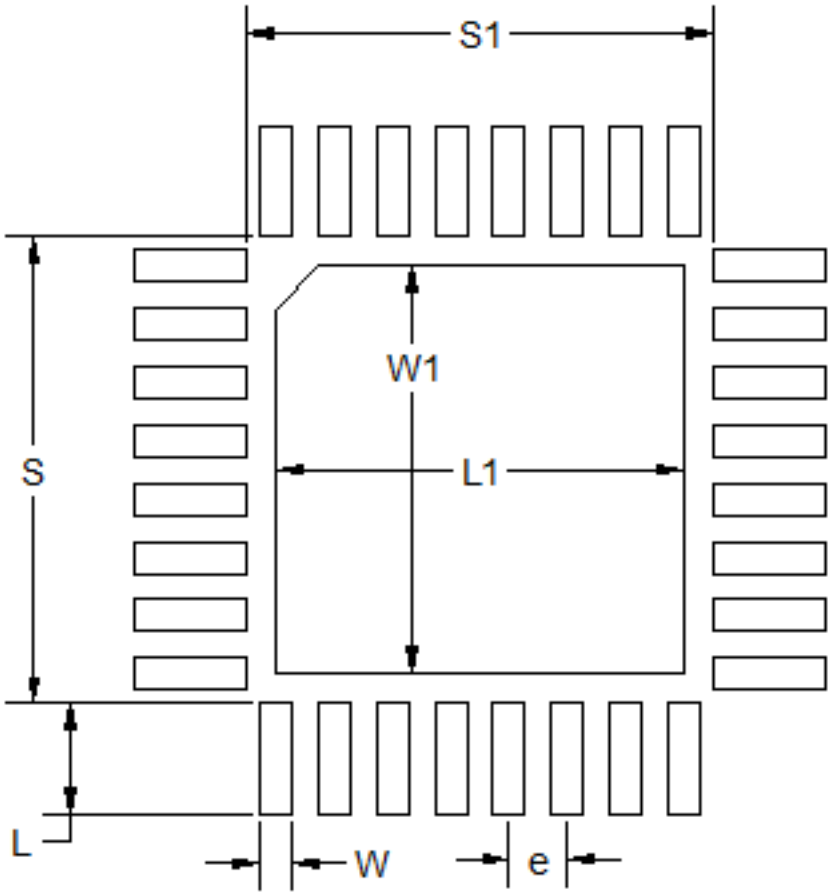

Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
L	0.76
W	0.22
e	0.40
S	3.21
S1	3.21
L1	2.80
W1	2.80

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.101 mm (4 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

7.3 QFN32 Package Marking

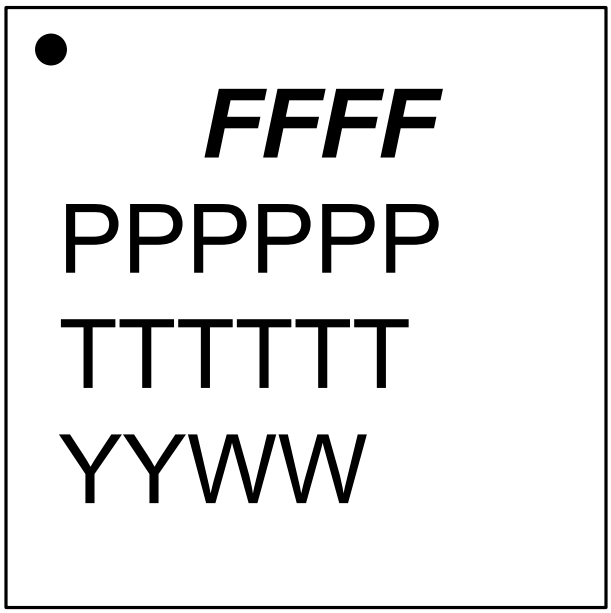

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- FFFF – The product family codes.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Series (2)
  4. Device Configuration (1, 2, 3, ...)
- PPPPPP – The product option codes.
  - 1-2. MCU Feature Codes
  - 3-4. Radio Feature Codes
  - 5. Flash (J = 1024k | I = 768k | H = 512k | W= 352k | G = 256k | F = 128k)
  - 6. Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. QFN40 Package Specifications

8.1 QFN40 Package Dimensions

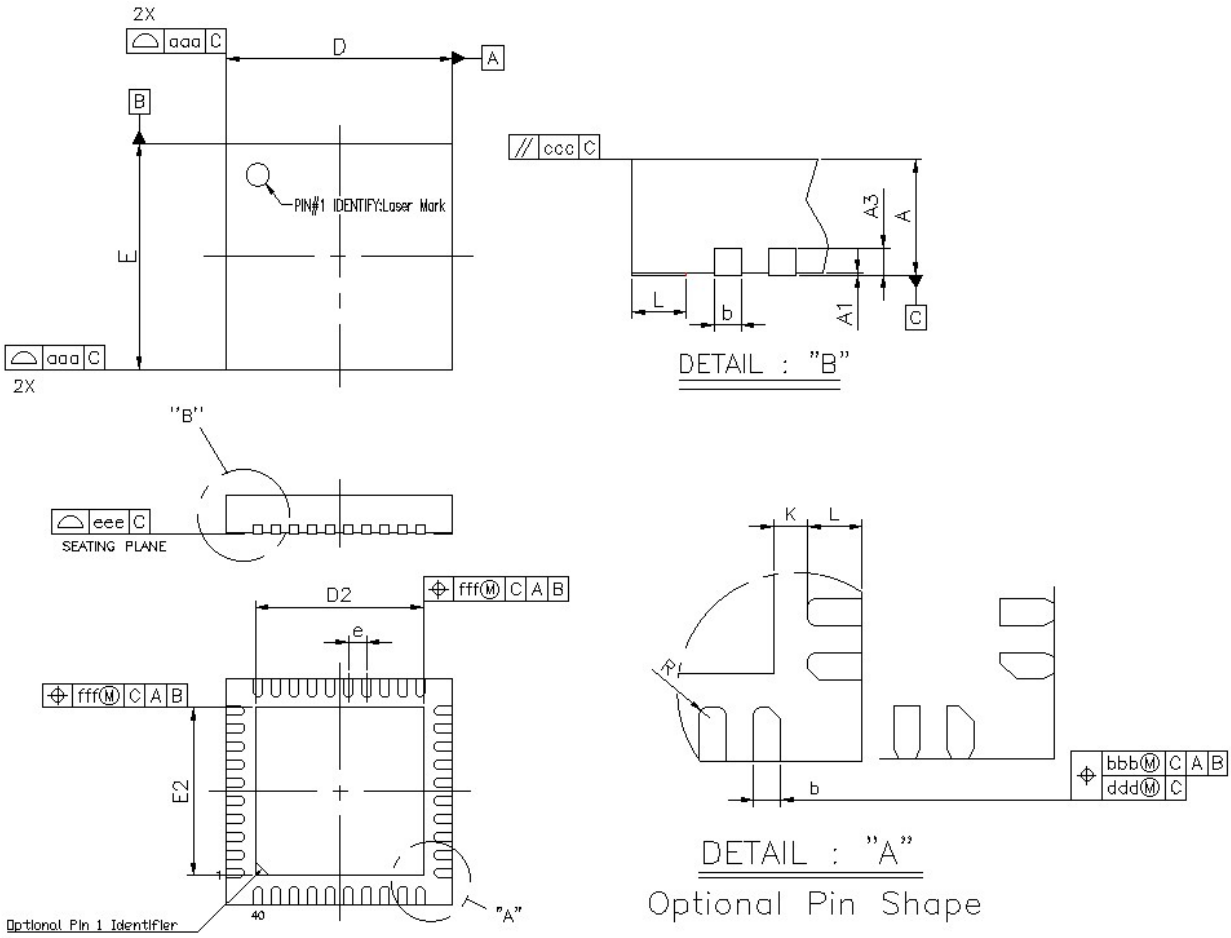

Figure 8.1. QFN40 Package Drawing

Table 8.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

8.2 QFN40 PCB Land Pattern

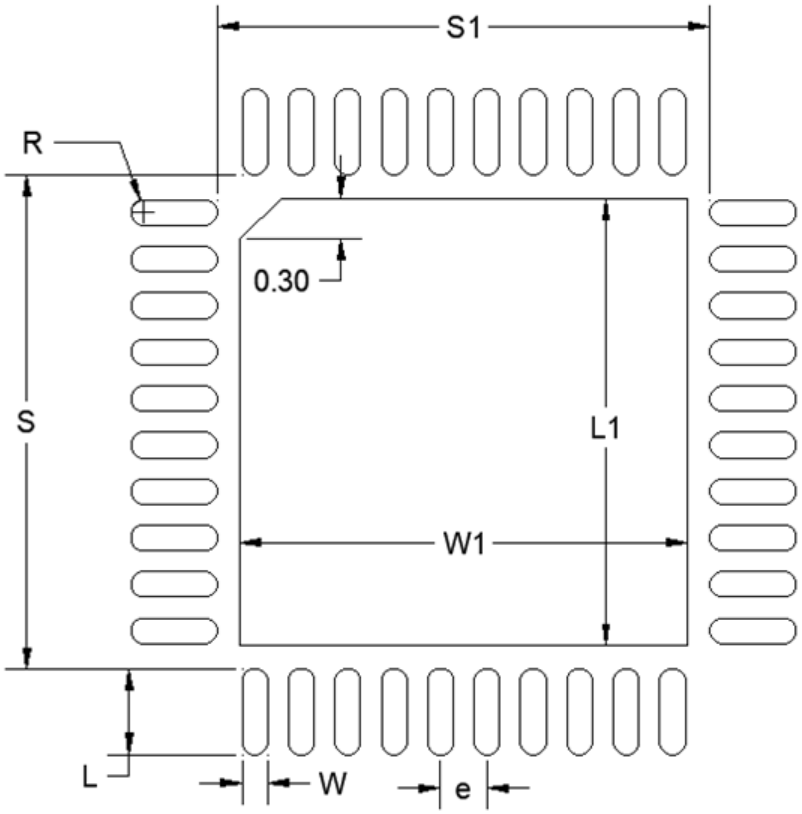

Figure 8.2. QFN40 PCB Land Pattern Drawing

Table 8.2. QFN40 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.25
S	4.25
L1	3.85
W1	3.85
e	0.40
W	0.22
L	0.74
R	0.11

Dimension	Typ

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
9. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

8.3 QFN40 Package Marking

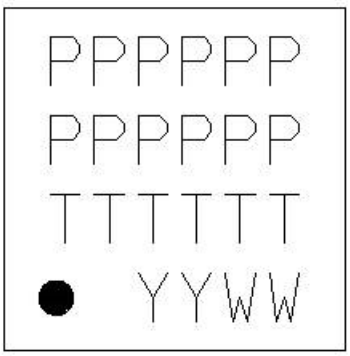

Figure 8.3. QFN40 Package Marking

The package marking consists of:

- Line 1: PPPPPP – The product family codes (TBD)
- Line 2: PPPPPP – The product option codes (TBD)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

9. Revision History

Revision 1.1

June 2021

- Updated lowest energy mode for I2C0, IADC0 and EUART0 to EM3 in 3.13 Configuration Summary.
- Added footnote for crystal load capacitance with Gain=2 test condition in 4.11.2 Low Frequency Crystal Oscillator.
- Added timing specification for RESETn low time in 4.12 GPIO Pins (3V GPIO pins).
- Added IADC 16 bit typical resolution and updated footnote in 4.13 Analog to Digital Converter (IADC).
- Corrected clock reference to PCLK in 4.17 USART SPI Main Timing and 4.18 USART SPI Secondary Timing.
- Added note regarding flexible power supply connections and additional application circuit in 5.1 Power.
- Corrected by removal IADC0.VREFN pinout from 6.3 Alternate Function Table; IADC0.VREFN connected internally to ground.
- Added documentation of chamfered pin 1 and oval land pattern in 8.1 QFN40 Package Dimensions.
- Replaced select terms with inclusive lexicon.
- Minor formatting and styling updates, including TOC locations and boilerplate information throughout document.

Revision 1.0

June, 2020

- 3.7.2 Cryptographic Accelerator: Removed text referencing DPA.
- 3.7.4 Secure Debug with Lock/Unlock: Removed text referencing Secure Element.
- 4.1 Electrical Characteristics:
  - Expanded Power Supply Pin Dependencies section to include more details and restrictions on DECOUPLE.
  - Finalized remaining MIN / MAX specifications according to characterization and qualification results.
  - Corrected 2GFSK Bit Error Rate conditions for sensitivity measurements with 255 byte payload.
  - Added GPIO hysteresis specification.
  - Updated DCDC lifetime condition guideance in 4.4.1 DC-DC Operating Limits.
- Expanded IADC descriptions to include information at higher oversampling ratios and added typical performance curve.

Revision 0.5

February, 2020

- 1. Feature List: Updated list slightly to highlight different features.
- Expanded 3.7 Security Features section and corrected security details.
- Added 3.9.2 Voltage Scaling section.
- 4.1 Electrical Characteristics:
  - Additional characterization results and test limits added where available.
  - Removed thermistor driver specification table until full software support becomes available.
- Removed references to TQFN32 package.
- Updated 5.2 RF Matching Networks section with recommended match values.
- Updated with mark details.

Revision 0.4

December, 2019

- Corrected temperature range in Feature List to -40 to 85 C.
- 4.1 Electrical Characteristics:
  - Added detailed lifetime information to DC-DC specifications section.
  - Additional characterization results and preliminary test limits added where available.
- Added DC-DC efficiency plots and updated supply current plots to 4.20 Typical Performance Curves.

Revision 0.3

October, 2019

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated 3.5.2 Low Energy Timer (LETIMER) lowest energy mode.
- 1. Feature List updated with additional security details.
- 2. Ordering Information:
  - OPN numbering changes for security grade differentiator.
- 4.1 Electrical Characteristics:
  - Additional characterization results and preliminary test limits added where available.
  - Corrected maximum clock speed details in General Operating Conditions Table.
  - Removed specification lines with 3 dBm output power conditions from RF transmit tables.
  - Removed DECOUPLE BOD table.
  - Added timing diagrams and specifications for PDM and USART SPI.
- Added 4.20 Typical Performance Curves.

Revision 0.2

July, 2019

- 2. Ordering Information: Updated to include revsion C part numbers, corrected memory size.
- 4.1 Electrical Characteristics: Added early silicon characterization data to several tables, and refined specification conditions.
- 4.1 Electrical Characteristics: Added flash electrical characteristics table.
- 4.1 Electrical Characteristics: Removed specifications and tables corresponding to 125 kbps and 500 kbps 2GFSK operation.
- Minor wording edits for System Overview sections.
- Added pinout for QFN32 package.

Revision 0.1

April, 2019

Initial release.