VCU128 Evaluation Board

User Guide

UG1302 (v1.1) April 21, 2021

XILINX®

Table of Contents

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
04/21/2021 Version 1.1	
Board Power System	Revised the Renesas smart power stage module part number in the power system block diagram.
12/21/2018 Version 1.0	
Initial release.	N/A

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Chapter 1

Introduction

Overview

The VCU128 board incorporates the VU37P high bandwidth memory (HBM) FPGA, which uses stacked silicon interconnect (SSI) technology to add HBM die next to the FPGA die on the package substrate. The VCU128 evaluation board for the Xilinx® Virtex® UltraScale+™ FPGA provides a hardware environment for developing and evaluating designs targeting the UltraScale+ XCVU37P-2FSVH2892E device. The VCU128 evaluation board is equipped with many of the common board-level features needed for design development as listed here:

- DDR4, RLD-3, and QDR-IV component memory
- Ganged small form-factor pluggable (QSFP28) connectors
- Sixteen-lane PCI Express® interface
- Ethernet PHY
- General purpose I/O
- UART interface

Additional features can be supported using modules compatible with the VITA-57.4 (FMCP HSPC) connector on the VCU128 board.

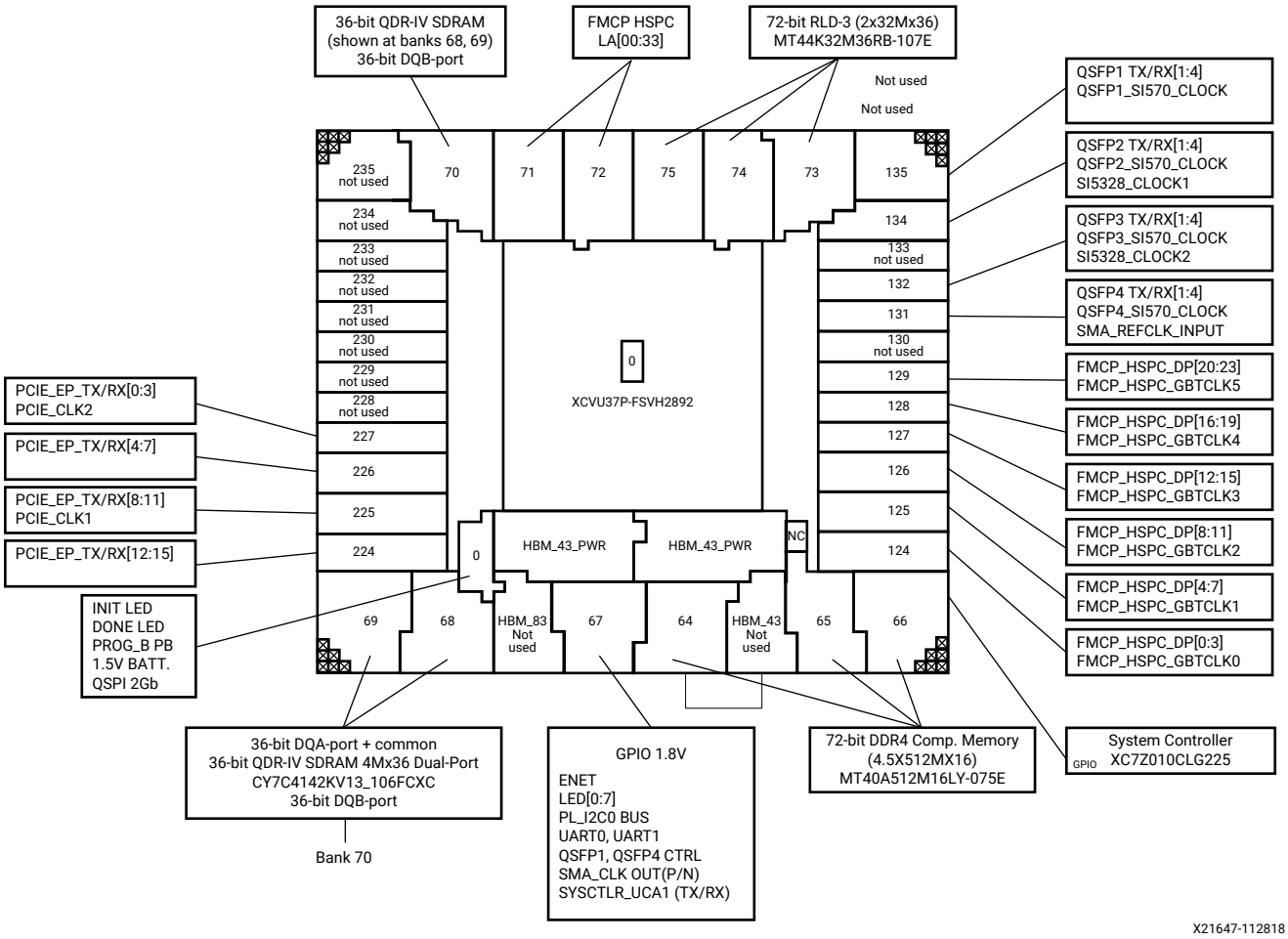
Additional Resources

See Appendix D: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the VCU128 evaluation board.

Block Diagram

A block diagram of the VCU128 evaluation board is shown in the following figure.

Figure 1: **Evaluation Board Block Diagram**



Board Features

The VCU128 evaluation board features are listed here. Detailed information for each feature is provided in Chapter 3: Board Component Descriptions.

- Virtex® UltraScale+™ XCVU37P-2FSVH2892E device
- Zynq®-7000 SoC XC7Z010 based system controller
- 4.5 GB DDR4 72-bit component memory interface (4.5 x [512 Mb x 16])

- 144 Mb 36-bit dual-port QDR-IV component memory interface (1 x [4M x 36])
- 288 MB 72-bit RLD3 component memory interface (2 x [1.125 Gb x 36])
- 2 Gb Quad SPI flash configuration memory
- QSFPF28 - Sixteen (16) GTY transceivers are allocated for a 1x4 QSFP cage
- USB JTAG interface (FTDI FT4232HL with a micro-AB USB connector)
- Clock sources:
  - SMA I/F clocks:
    - FPGA bank 67 SMA clock P/N
  - QSFP clocks:
    - Four Si570 I2C programmable clock oscillators (156.25 MHz default)
    - QSFP clock recovery Si5328 input to GTY132 and GTY134
    - QSFP external SMA diff. clock input to GTY131
  - Memory I/F clocks:
    - Three SiT9120A fixed 100 MHz LVDS clock oscillators
  - PCIe® I/F clock:
    - Fixed 100 MHz HCSL clock from PCI Express® edge input to 1-to-2 clock buffer wired to GTY225 and GTY227
  - System controller clock:
    - SiT8008A 33.33 MHz single-ended clock oscillator
- 96 GTY transceivers (24 Quads)
  - FMCP HSPC connector (twenty-four GTY transceivers)
  - 4x28 Gb/s QSFP+ connectors (eight GTY transceivers)
  - PCIe 16-lane edge connector (sixteen GTY transceivers)
  - Not used (forty-eight GTY transceivers)
- PCI Express® Endpoint connectivity
  - Gen1 (x1, x2, x4, x8, x16)
  - Gen2 (x1, x2, x4, x8, x16)
  - Gen3 (x1, x2, x4, x8, x16)
  - Dual Gen4 (x1, x2, x4, x8)
- Ethernet PHY SGMII interface with RJ-45 connector
- Dual USB-to-UART bridge with micro-B USB connector (shared FTDI FT4232HL)

- I2C bus
- Status LEDs
- User I/O (1 x push-button switch, 8 x LED)
- VITA 57.4 FMC+ HSPC connector (DP[0:23], LA[0:33])
- Power management with I2C voltage monitoring through Intersil power controllers and GUI
- Configuration options:
  - Quad SPI flash memory
  - USB JTAG I/F (FTDI FT4232HL)
  - Platform cable USB II interface 2x7 2 mm keyed connector

Board Specifications

Dimensions

Height: 7.53 inch (19.14 cm)

Length: 9.50 inch (24.13 cm)

Thickness (±5%): 0.061 inch (0.1549 cm)

***Note*:** A 3D model of this board is not available.

IMPORTANT! *The VCU128 board height exceeds the standard 4.376-inch (11.15 cm) height of a PCI Express® card.*

Environmental

Temperature

Operating: 0°C to +45°C, Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 VDC

Chapter 2

Board Setup and Configuration

Standard ESD Measures

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

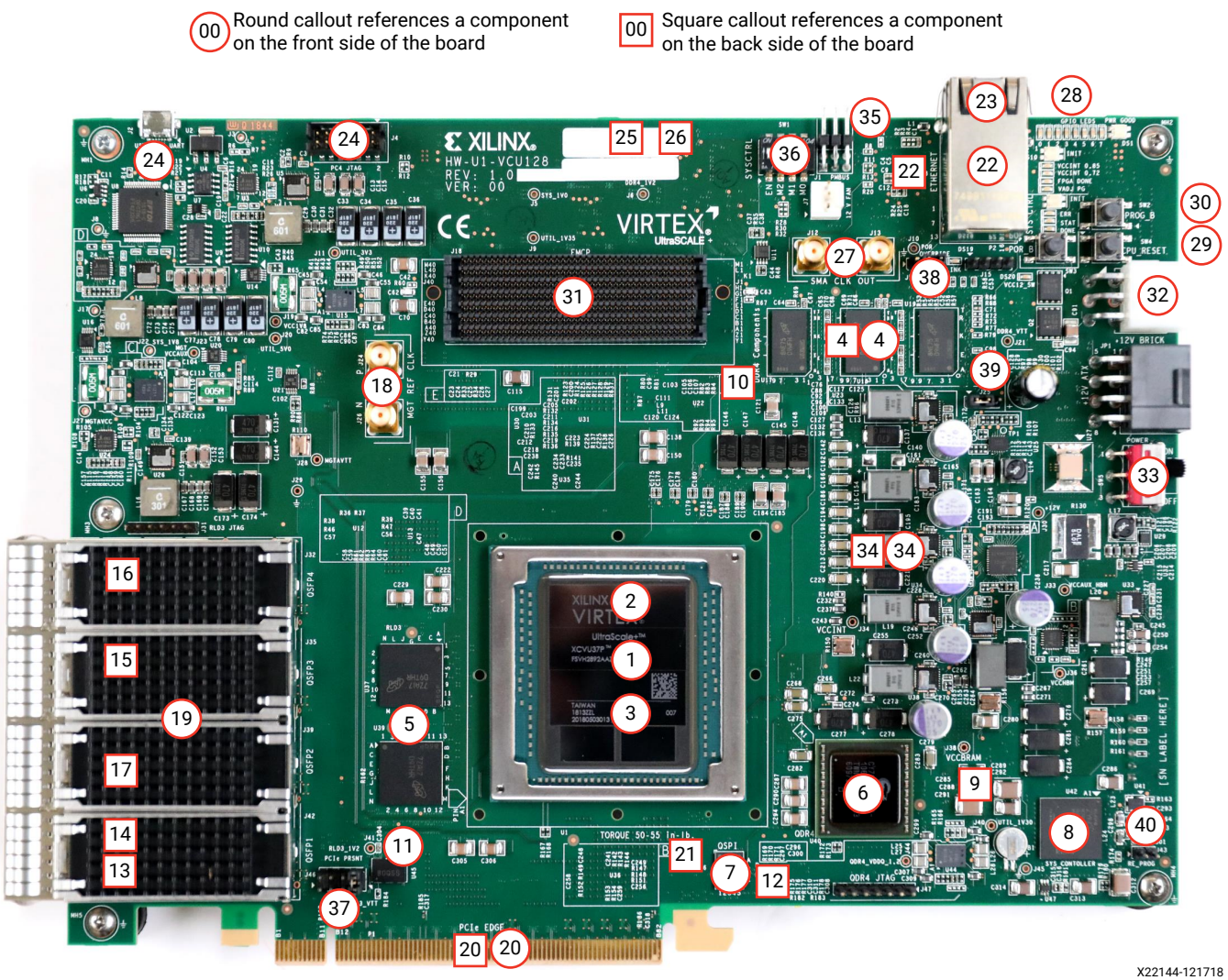
Board Component Location

The following figure shows the VCU128 board component locations. Each numbered component shown in the figure is keyed to the table in Board Component Descriptions.

IMPORTANT! *The board component locations figure is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT! *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific VCU128 version of interest for such details.*

Figure 2: **Evaluation Board Component Locations**



Board Component Descriptions

The following table identifies the components, references the respective schematic page numbers, and links to a detailed functional description of the components and board features in Chapter 3: Board Component Descriptions.

Table 1: **Board Component Descriptions**

Callout	Feature [U#] = Bottom	Notes	Schematic Page Number
1	Virtex UltraScale+ XCVU37P-2FSVH2892E Device (with fan-sink on soldered FPGA)	XCVU37P-2FSVH2892E Cofan 30-4811	
2	GTY transceivers, Right-side Quads (twelve quads)	Embedded within FPGA U1	14-15
3	GTY transceivers, Left-side Quads (twelve quads)	Embedded within FPGA U1	16-17
4	DDR4 Component Memory, 72-bit DDR4 component memory I/F, (U17-U19), [U73, U74]	5 x Micron MT40A256M16GE-075E	24-26
5	RLD3 Component Memory, RLD3 72-bit component memory I/F (U37, U39)	2 x Micron MT44K32M36RB-107E	29-30
6	QDR4 Component Memory (U40)	Cypress CY7C4142KV13-106FCXC	27
7	Quad SPI Flash Memory (U46)	Micron MT25QU02GCBB8E12-0SIT	3
8	System Controller, Zynq®-7000 SoC (U42)	XC7Z010CLG225	48-50
9	System Controller Quad SPI Flash Memory [U89]	Micron MT25QU02GCBB8E12-0SIT	49
10	DDR4 Component Memory I/F clock, fixed 100 MHz LVDS [U76]	SiTime SIT9120AI-2D3-33E100.0000	32
11	RLD3 Component Memory I/F clock, fixed 100 MHz LVDS (U45)	SiTime SIT9120AI-2D3-33E100.0000	32
12	QDR4 Component Memory I/F clock, fixed 100 MHz LVDS [U96]	SiTime SIT9120AI-2D3-33E100.0000	32
13	Programmable QSFP1 Clock I2C, LVDS [U95]	Silicon Labs SI570BAB0000544DG (default 156.250 MHz)	40
14	Programmable QSFP2 Clock I2C, LVDS [U90]	Silicon Labs SI570BAB0000544DG (default 156.250 MHz)	40
15	Programmable QSFP3 Clock I2C, LVDS [U82]	Silicon Labs SI570BAB0000544DG (default 156.250 MHz)	40
16	Programmable QSFP4 Clock I2C, LVDS [U80]	Silicon Labs SI570BAB0000544DG (default 156.250 MHz)	40
17	QSFP Jitter Attenuated Clock, [U87]	Silicon Labs SI5328B-C-GMR	40
18	User QSFP SMA Clock pair J24(P)/J26(N) input to XCVU37P U1 GTY131 MGTREFCLK1P/N	Rosenberger 32K10K-400L5	12
19	Four 28 Gb/s zQSFP+ Module Connectors, QSFP1-4 (J42), (J39), (J35), (J32) + 1x4 ganged cage	4 x TE 1551920-2 connectors with TE 2170745-2 cage with heatsink	38, 39

Table 1: **Board Component Descriptions** *(cont'd)*

Callout	Feature [U#] = Bottom	Notes	Schematic Page Number
20	PCI Express Endpoint Connectivity, PCI Express® 16-lane connector (P1)	16-lane card edge connector	41
21	PCI Express Endpoint Connectivity 100 MHz REFCLK 1-to-2 clock buffer, differential-to-LVDS [U94]	ICS ICS85411AMLF	14
22	10/100/1000 Mb/s Tri-speed Ethernet PHY with RJ45, SGMII mode only, [U62], (P2)	TI DP83867ISRGZ with Wurth 7499111221A RJ45 (with magnetics)	37
23	Ethernet PHY Status LEDs, LEDs are integrated into P2 bezel	Wurth 7499111221A RJ45 integrated status LEDs	37
24	USB JTAG Interface, USB bridge (U8) with mini-B USB connector (J2) and 2x7 2 mm prog. cable connector (J4)	FTDI FT4232HL bridge Hirose ZX62D-AB-5P8 connector Molex 87832-1420	34
25	I2C Bus, Topology, and Switches I2C0 bus topology: I2C bus MUX [U55], 16-bit expansion port [U65]	TI PCA9544ARGYR TI TCA6416APWR	35
26	I2C Bus, Topology, and Switches I2C0 bus topology: 2 x I2C bus MUX [U53, U54]	2 x TI TCA9548APWR	36
28	User GPIO LEDs (DS2-DS9), active-High	Lumex SML-LX0603GW-TR	47
29	User GPIO pushbutton, CPU reset (SW4), active-High	E-Switch TL3301EF100QG	47
30	Switches, program_B pushbutton, (SW2), active-Low	E-Switch TL3301EF100QG	3
31	FMCP Connector J18, (J18)	Samtec ASP_184329_01	42-46
32	Board Power System Power Input Connector, (J16)	2x6 Molex-39-30-1060	52
33	Board Power System power input switch, on/off slide switch (SW5)	C&K 1201M2S3AQE2	52
34	Board Power System, power management system (top and bottom)	Intersil power system	54-65
35	Monitoring Voltage and Current, PMBus 2x3 R.A. male pin header (J1)	Amphenol 68021-406HLF	54
36	Configuration Options, FPGA U1 configuration mode DIP switch, (SW1)	4-pole CTS 218-4LPSTRF	3
37	PCI Express Endpoint Connectivity, lane width select header, (J46)	2x4 0.1-inch male header Sullins PBC36DAAN	41
38	Jumpers, FPGA POR_OVERRIDE select header, (J14)	1x3 0.1-inch male header Sullins PBC36SAAN	3
39	Jumpers, FPGA VCCINT select header, (J25)	1x3 0.1-inch male header Sullins PBC36SAAN	54
40	Jumpers, SYS CTLR RE-PROG header, (J43)	1x2 0.1-inch male header Sullins PBC36SAAN	50

The VCU128 board schematics are available for download from the VCU128 Evaluation Kit website.

Default Switch and Jumper Settings

Switches

Default switch settings are listed in the following table. The switch locations are shown in Figure 2. The following table also references the respective schematic page numbers.

Table 2: **Default Switch Settings**

Switch	Function	Default	Comments	Figure 2 Callout	Schematic Page
SW5	On/Off SPST slide switch	OFF	Board shipped with power switch off	33	52
SW1	4-pole configuration[1] Default = SPI	SW1[1:4] = 0001	Position 1 = System Controller Enable SW1[2:4] = FPGA U1 mode M[2:0] = 001	36	3
SW2	FPGA_PROG_B P.B.	NA	U1 XCVU37P PROG_B (active low)	30	3
SW3	SYSCTLR_POR_B P.B.	NA	U42 XC7Z010 POR_B (active low)	Near 29	50
SW4	CPU_RESET P.B.	NA	U1 XCVU37P USER P.B. (active high)	29	47

Notes:

1. DIP switch sections are active-High (connected net is pulled High when DIP switch is closed = 1).

Jumpers

Default jumper settings are listed in the following table. Jumper header locations are shown in Figure 2. The following table also references the respective schematic page numbers.

Table 3: **Default Jumper Settings**

Jumper	Function	Default	Comments	Figure 2 Callout	Schematic Page
J14	Power on reset (POR) override	2-3	U1 POR_OVERRIDE pin BG15 to GND	38	3
J25	VCCINT select	1-2	1-2: 0.85V; 2-3: 0.72V[1]	39	54
J46	PCIe® lane size select	7-8	16-lane configuration	37	41
J43	SYSCTLR RE-PROG	Off	U42 XCZU7010 MIO5 pin A9	40	50

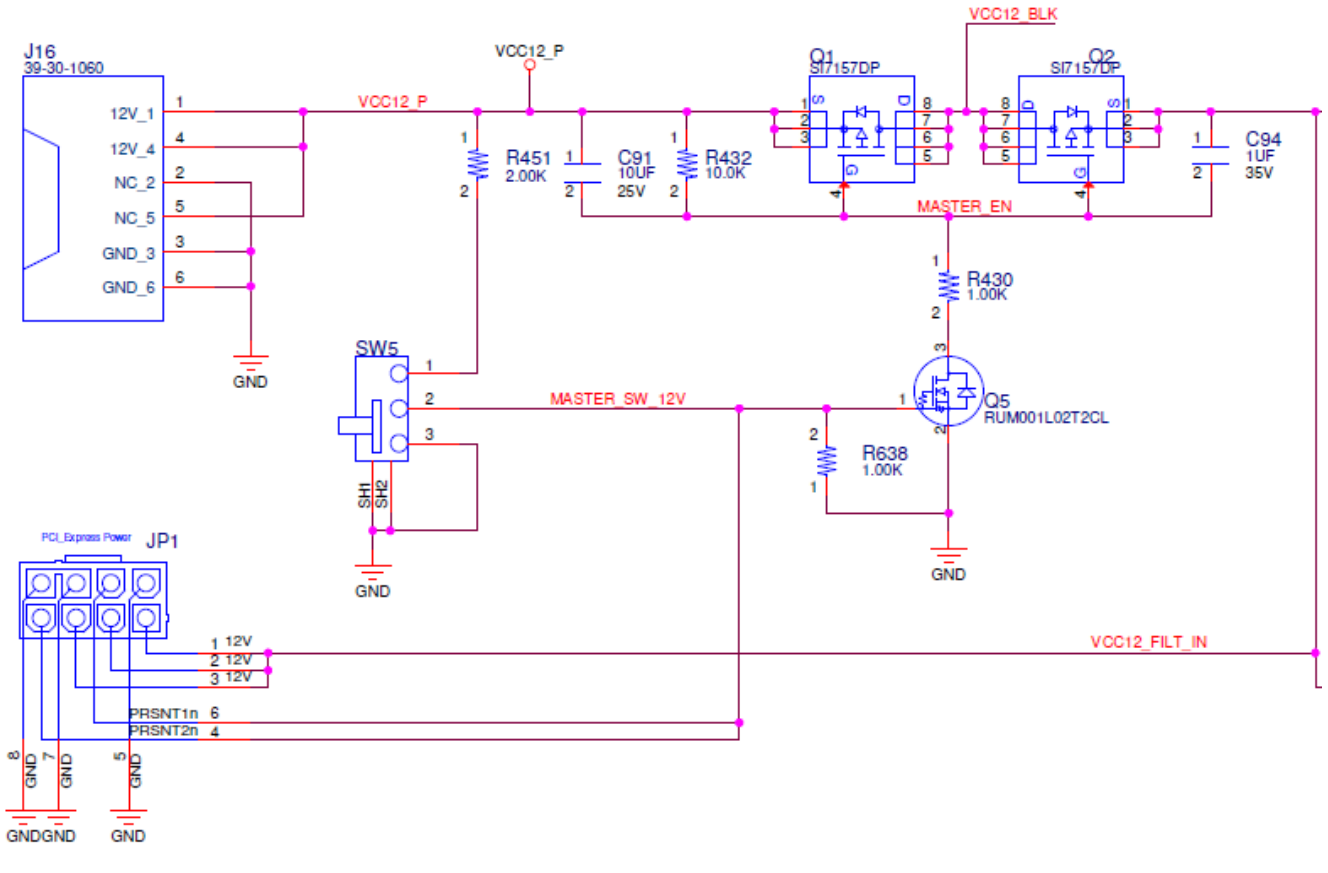
Notes:

1. VCCINT select header J25 should always have a jumper block installed.

Installing the Board in a PC Chassis

The VCU128 board 12V power input circuitry allows 12V to be applied through one of two connectors, J16 (typically used with the stand-alone VCU128 power adapter) or JP1, as shown in the following figure.

Figure 3: **12V Power Entry**



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Installation of the VCU128 board inside a computer chassis is required when developing or testing PCI Express® functionality. When the VCU128 board is used inside a computer chassis (i.e., plugged in to a PCIe slot), power is provided by choosing one of two mutually exclusive ATX power supply cables as described in this section (use one cable or the other).

- The ATX power supply 4-pin (1x4) peripheral connector, which requires using the ATX adapter cable (see the following figure) to connect to J16 on the VCU128 board. The Xilinx part number for this cable is 2600304. See ATX Power Supply Adapter Cable.

Figure 4: **ATX Power Supply Adapter Cable**

- The ATX supply 8-pin (2x4) PCIe power connector, which plugs into JP1 on the VCU128 board.

Steps to Install Board

To install the board in a PC chassis:

1. On the VCU128 board, remove the five screws retaining the five rubber feet and standoffs, and the PCIe bracket. Reinstall the PCIe® bracket using two of the previously removed screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. The VCU128 board has a large cooling fan that requires two adjacent PCIe slots. Ensure the slot adjacent to the front of the board is free of obstructions.
5. Remove the PCIe expansion slot cover (at the back of the chassis) which aligns with the VCU128 PCIe bracket, by removing the screws on the top and bottom of the cover.
6. Plug the VCU128 board into the appropriate open slot.
7. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the VCU128 board in its slot.
8. If using the ATX supply 4-pin (1x4) peripheral connector, connect power to the VCU128 board using the ATX power supply adapter cable as shown in the previous figure.
    a. Plug the 6-pin 2 x 3 Molex connector end of the adapter cable into J16 on the VCU128 board.
    b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter connector end of the cable.

> **CAUTION!** *Do NOT plug a PC ATX power supply 6-pin connector into J16 on the VCU128 evaluation board. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VCU128 evaluation board and voids the board warranty.*

    c. Slide the VCU128 board power switch SW5 to the ON position. The PC can now be powered on.

9. If using the ATX supply 8-pin (2x4) PCIe power connector, plug the connector into VCU128 board JP1. The PC can now be powered on.

FPGA Configuration

The VCU128 board supports two of the five UltraScale+™ FPGA configuration modes:

- Quad SPI flash memory (2 Gb)
- JTAG using:
  - USB JTAG configuration port (U8 FT4232HL + USB J2 micro-AB)
  - Xilinx Platform Cable USB II, 2 mm, keyed flat cable header (J4)

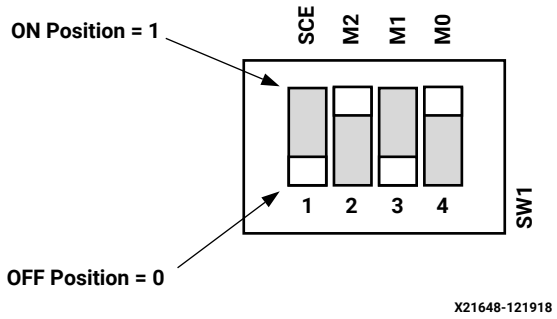
Each configuration interface corresponds to one or more configuration modes and bus widths, as listed in the following table. The mode switches M2, M1, and M0 are on SW1 positions 2, 3, and 4, respectively. The FPGA default mode setting M[2:0] = `001` selects the master SPI configuration mode.

Table 4: **Configuration Modes**

Configuration Mode	SW1 DIP Switch Settings M[2:0]	Bus Width	CCLK Direction
Master SPI	`1`	x1, x2, x4	Output
JTAG	`101`	x1	NA

For complete details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570). The following figure shows the configuration mode DIP switch SW1 JTAG switch positions.

Figure 5: **SW1 JTAG Mode Settings**



JTAG

The Vivado®, Xilinx SDK, or third-party tools can establish a JTAG connection to the XCVU37P FPGA through the FTDI FT4232 USB-to-JTAG/USB UART device (U8) connected to the micro-USB connector (J2). Alternatively, a JTAG cable can be connected to the keyed flat cable header (J4). JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pins M[2:0], wired to SW1 positions [2:4].

Quad SPI

To boot from the dual Quad SPI non-volatile configuration memory, follow these steps.

1. Store a valid XCVU37P FPGA boot image in the 2 Gbit Quad SPI flash device (U46) connected to the FPGA bank 0 Quad SPI interface. See the *VCU128 Restoring Flash Tutorial* (XTP533) for information on programming the QSPI.
2. Set the boot mode pins SW1 M[2:0] as indicated in the configuration modes table in FPGA Configuration for master SPI.
3. Power-cycle the VCU128 board. Mode SW1 is callout 36 in Figure 2.

See the *VCU128 Software Install and Board Setup Tutorial* (XTP535) for more information.

See System Controller for an overview of query and control of select programmable board features such as clocks, FMCP functionality, and power systems. See the *VCU128 System Controller Tutorial* (XTP534) for more information.

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Chapter 3

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 1 identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Figure 2.

Component Descriptions

Virtex UltraScale+ XCVU37P-2FSVH2892E Device

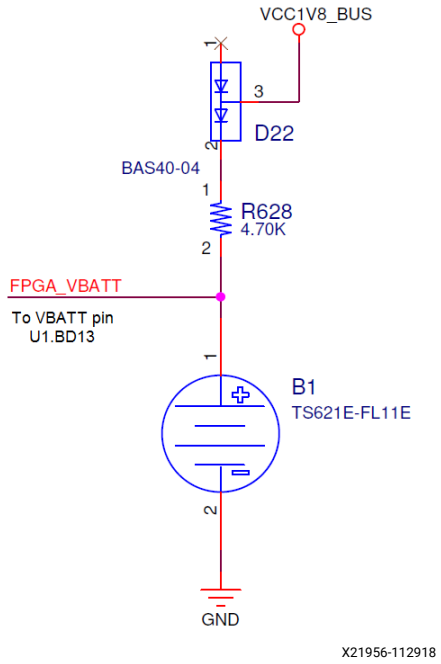
[Figure 2, callout 1]

The VCU128 board incorporates the VU37P high bandwidth memory (HBM) FPGA, which utilizes stacked silicon interconnect (SSI) technology to add HBM die next to the FPGA die on the package substrate. The VCU128 board is populated with the Virtex® UltraScale+™ XCVU37P-2FSVH2892E device. For more information on Virtex UltraScale+ FPGAs, see *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

Encryption Key Battery Backup Circuit

The XCVU37P device U1 implements bitstream encryption key technology. The VCU128 board provides the encryption key backup battery circuit shown in the following figure.

Figure 6: **Encryption Key Backup Circuit**



The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCVU37P device U1 VBATT pin BD13. The battery supply current IBATT specification is 150 nA maximum when the board power is off. B1 is charged from the VCC1V8_BUS 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V.

I/O Voltage Rails

There are 12 I/O banks and 2 high-bandwidth memory (HBM) banks available on the XCVU37P device. The VCU128 board does not use the HBM banks. The voltages applied to the FPGA I/O banks on the VCU128 board are listed in the following table.

Table 5: **I/O Bank Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8	1.8V
HP bank 64	DDR4_VDDQ_1V2	1.2V
HP bank 65	DDR4_VDDQ_1V2	1.2V
HP bank 66	DDR4_VDDQ_1V2	1.2V
HP bank 67	VCC1V8	1.8V
HP bank 68	QDR4_VDDQ_1V2	1.2V
HP bank 69	QDR4_VDDQ_1V2	1.2V
HP bank 70	QDR4_VDDQ_1V2	1.2V
HP bank 71	VADJ	1.8V

Table 5: **I/O Bank Voltage Rails** *(cont'd)*

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
HP bank 72	VADJ	1.8V
HP bank 73	RLD3_VDDQ_1V2	1.2V
HP bank 74	RLD3_VDDQ_1V2	1.2V
HP bank 75	RLD3_VDDQ_1V2	1.2V
HBM_43 (not used)	VCCHBM/VCCAUX_HBM	1.2V/1.8V
HBM_83 (not used)	VCCHBM/VCCAUX_HBM	1.2V/1.8V

DDR4 Component Memory

[Figure 2, callout 4]

The 4.5 GB DDR4 component memory system is comprised of five 512 Mb x 16 DDR4 SDRAM devices implemented in clam-shell fashion located at U17-U19 (top) and U73-U74 (bottom). Half of the U19 16-bits are used (4.5 x 16-bits = 72-bit wide interface).

- Manufacturer: Micron
- Part Number: MT40A512M16LY-075E
- Description:
  - 8 Gb (512 Mb x 16)
  - 1.2V 96-ball TFBGA
  - DDR4-2666

The VCU128 XCVU37P FPGA DDR4 interface performance is documented in the *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

The 72-bit wide DDR4 memory system is connected to XCVU37P U1 HP banks 64, 65 and 66. The DDR4 0.6V VTT termination voltage (net DDR4_VTERM_0V6) is sourced from the TI TPS51200DR linear regulator U71. The DDR4 memory interface bank VREF pins are not connected, which, coupled with an XDC set_property INTERNAL VREF constraint, invoke the INTERNAL VREF mode. The connections between the 72-bit interface DDR4 component memories and XCVU37P banks 64, 65, and 66 are listed in the following table.

Table 6: **DDR4 Memory 72-bit I/F to FPGA U1 Banks 64, 65, and 66**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
BM45	PL_DDR4_DQ0	POD12_DCI	A3	DQ8	U74
BP44	PL_DDR4_DQ1	POD12_DCI	B8	DQ9	U74
BP47	PL_DDR4_DQ2	POD12_DCI	C3	DQ10	U74
BN45	PL_DDR4_DQ3	POD12_DCI	C7	DQ11	U74
BM44	PL_DDR4_DQ4	POD12_DCI	C2	DQ12	U74
BN44	PL_DDR4_DQ5	POD12_DCI	C8	DQ13	U74
BN47	PL_DDR4_DQ6	POD12_DCI	D3	DQ14	U74
BP43	PL_DDR4_DQ7	POD12_DCI	D7	DQ15	U74
BN46	PL_DDR4_DQS0_T	DIFF_POD12_DCI	B7	UDQS_T	U74
BP46	PL_DDR4_DQS0_C	DIFF_POD12_DCI	A7	UDQS_C	U74
BN42	PL_DDR4_DM0_B	POD12_DCI	E2	NF/UDM_B/UDBI_B	U74
BL45	PL_DDR4_DQ8	POD12_DCI	G2	DQ0	U17
BK44	PL_DDR4_DQ9	POD12_DCI	F7	DQ1	U17
BL46	PL_DDR4_DQ10	POD12_DCI	H3	DQ2	U17
BK43	PL_DDR4_DQ11	POD12_DCI	H7	DQ3	U17
BL43	PL_DDR4_DQ12	POD12_DCI	H2	DQ4	U17
BJ44	PL_DDR4_DQ13	POD12_DCI	H8	DQ5	U17
BL42	PL_DDR4_DQ14	POD12_DCI	J3	DQ6	U17
BJ43	PL_DDR4_DQ15	POD12_DCI	J7	DQ7	U17
BK45	PL_DDR4_DQS1_T	DIFF_POD12_DCI	G3	LDQS_T	U17
BK46	PL_DDR4_DQS1_C	DIFF_POD12_DCI	F3	LDQS_C	U17
BL47	PL_DDR4_DM1_B	POD12_DCI	E7	NF/LDM_B/LDBI_B	U17
BK41	PL_DDR4_DQ16	POD12_DCI	G2	DQ0	U74
BG44	PL_DDR4_DQ17	POD12_DCI	F7	DQ1	U74
BG42	PL_DDR4_DQ18	POD12_DCI	H3	DQ2	U74
BH44	PL_DDR4_DQ19	POD12_DCI	H7	DQ3	U74
BH45	PL_DDR4_DQ20	POD12_DCI	H2	DQ4	U74
BG45	PL_DDR4_DQ21	POD12_DCI	H8	DQ5	U74
BG43	PL_DDR4_DQ22	POD12_DCI	J3	DQ6	U74
BJ41	PL_DDR4_DQ23	POD12_DCI	J7	DQ7	U74
BH46	PL_DDR4_DQS2_T	DIFF_POD12_DCI	G3	LDQS_T	U74
BJ46	PL_DDR4_DQS2_C	DIFF_POD12_DCI	F3	LDQS_C	U74
BH42	PL_DDR4_DM2_B	POD12_DCI	E7	NF/LDM_B/LDBI_B	U74
BE43	PL_DDR4_DQ24	POD12_DCI	G2	DQ0	U18
BF42	PL_DDR4_DQ25	POD12_DCI	F7	DQ1	U18
BC42	PL_DDR4_DQ26	POD12_DCI	H3	DQ2	U18
BF43	PL_DDR4_DQ27	POD12_DCI	H7	DQ3	U18
BD42	PL_DDR4_DQ28	POD12_DCI	H2	DQ4	U18

Table 6: **DDR4 Memory 72-bit I/F to FPGA U1 Banks 64, 65, and 66** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
BF45	PL_DDR4_DQ29	POD12_DCI	H8	DQ5	U18
BE44	PL_DDR4_DQ30	POD12_DCI	J3	DQ6	U18
BF46	PL_DDR4_DQ31	POD12_DCI	J7	DQ7	U18
BE45	PL_DDR4_DQS3_T	DIFF_POD12_DCI	G3	LDQS_T	U18
BE46	PL_DDR4_DQS3_C	DIFF_POD12_DCI	F3	LDQS_C	U18
BD41	PL_DDR4_DM3_B	DIFF_POD12_DCI	E7	NF/LDM_B/LDBI_B	U18
BP32	PL_DDR4_DQ32	POD12_DCI	G2	DQ0	U73
BP29	PL_DDR4_DQ33	POD12_DCI	F7	DQ1	U73
BP31	PL_DDR4_DQ34	POD12_DCI	H3	DQ2	U73
BP28	PL_DDR4_DQ35	POD12_DCI	H7	DQ3	U73
BN32	PL_DDR4_DQ36	POD12_DCI	H2	DQ4	U73
BM30	PL_DDR4_DQ37	POD12_DCI	H8	DQ5	U73
BN31	PL_DDR4_DQ38	POD12_DCI	J3	DQ6	U73
BL30	PL_DDR4_DQ39	POD12_DCI	J7	DQ7	U73
BN29	PL_DDR4_DQS4_T	DIFF_POD12_DCI	G3	LDQS_T	U73
BN30	PL_DDR4_DQS4_C	DIFF_POD12_DCI	F3	LDQS_C	U73
BM28	PL_DDR4_DM4_B	POD12_DCI	E7	NF/LDM_B/LDBI_B	U73
BL32	PL_DDR4_DQ40	POD12_DCI	G2	DQ0	U19
BP34	PL_DDR4_DQ41	POD12_DCI	F7	DQ1	U19
BN34	PL_DDR4_DQ42	POD12_DCI	H3	DQ2	U19
BK33	PL_DDR4_DQ43	POD12_DCI	H7	DQ3	U19
BL31	PL_DDR4_DQ44	POD12_DCI	H2	DQ4	U19
BL33	PL_DDR4_DQ45	POD12_DCI	H8	DQ5	U19
BM33	PL_DDR4_DQ46	POD12_DCI	J3	DQ6	U19
BK31	PL_DDR4_DQ47	POD12_DCI	J7	DQ7	U19
BL35	PL_DDR4_DQS5_T	DIFF_POD12_DCI	G3	LDQS_T	U19
BM35	PL_DDR4_DQS5_C	DIFF_POD12_DCI	F3	LDQS_C	U19
BM34	PL_DDR4_DM5_B	POD12_DCI	E7	NF/LDM_B/LDBI_B	U19
BJ34	PL_DDR4_DQ48	POD12_DCI	A3	DQ8	U18
BG35	PL_DDR4_DQ49	POD12_DCI	B8	DQ9	U18
BH34	PL_DDR4_DQ50	POD12_DCI	C3	DQ10	U18
BH35	PL_DDR4_DQ51	POD12_DCI	C7	DQ11	U18
BJ33	PL_DDR4_DQ52	POD12_DCI	C2	DQ12	U18
BF35	PL_DDR4_DQ53	POD12_DCI	C8	DQ13	U18
BG34	PL_DDR4_DQ54	POD12_DCI	D3	DQ14	U18
BF36	PL_DDR4_DQ55	POD12_DCI	D7	DQ15	U18
BK34	PL_DDR4_DQS6_T	DIFF_POD12_DCI	B7	UDQS_T	U18
BK35	PL_DDR4_DQS6_C	DIFF_POD12_DCI	A7	UDQS_C	U18

Table 6: **DDR4 Memory 72-bit I/F to FPGA U1 Banks 64, 65, and 66** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
BH32	PL_DDR4_DM6_B	POD12_DCI	E2	NF/UDM_B/UDBI_B	U18
BF31	PL_DDR4_DQ56	POD12_DCI	A3	DQ8	U73
BH30	PL_DDR4_DQ57	POD12_DCI	B8	DQ9	U73
BJ31	PL_DDR4_DQ58	POD12_DCI	C3	DQ10	U73
BG32	PL_DDR4_DQ59	POD12_DCI	C7	DQ11	U73
BH31	PL_DDR4_DQ60	POD12_DCI	C2	DQ12	U73
BF32	PL_DDR4_DQ61	POD12_DCI	C8	DQ13	U73
BH29	PL_DDR4_DQ62	POD12_DCI	D3	DQ14	U73
BF33	PL_DDR4_DQ63	POD12_DCI	D7	DQ15	U73
BJ29	PL_DDR4_DQS7_T	DIFF_POD12_DCI	B7	UDQS_T	U73
BK30	PL_DDR4_DQS7_C	DIFF_POD12_DCI	A7	UDQS_C	U73
BG29	PL_DDR4_DM7_B	POD12_DCI	E2	NF/UDM_B/UDBI_B	U73
BN51	PL_DDR4_DQ64	POD12_DCI	A3	DQ8	U17
BM52	PL_DDR4_DQ65	POD12_DCI	B8	DQ9	U17
BN50	PL_DDR4_DQ66	POD12_DCI	C3	DQ10	U17
BL52	PL_DDR4_DQ67	POD12_DCI	C7	DQ11	U17
BM48	PL_DDR4_DQ68	POD12_DCI	C2	DQ12	U17
BL53	PL_DDR4_DQ69	POD12_DCI	C8	DQ13	U17
BN49	PL_DDR4_DQ70	POD12_DCI	D3	DQ14	U17
BL51	PL_DDR4_DQ71	POD12_DCI	D7	DQ15	U17
BM49	PL_DDR4_DQS8_T	DIFF_POD12_DCI	B7	UDQS_T	U17
BM50	PL_DDR4_DQS8_C	DIFF_POD12_DCI	A7	UDQS_C	U17
BP48	PL_DDR4_DM8_B	POD12_DCI	E2	NF/UDM_B/UDBI_B	U17
COMMON					
BF50	PL_DDR4_A0	SSTL12_DCI	P3	A0	U17-U19 U73-U74
BD51	PL_DDR4_A1	SSTL12_DCI	P7	A1	U17-U19 U73-U74
BG48	PL_DDR4_A2	SSTL12_DCI	R3	A2	U17-U19 U73-U74
BE50	PL_DDR4_A3	SSTL12_DCI	N7	A3	U17-U19 U73-U74
BE49	PL_DDR4_A4	SSTL12_DCI	N3	A4	U17-U19 U73-U74
BE51	PL_DDR4_A5	SSTL12_DCI	P8	A5	U17-U19 U73-U74
BF53	PL_DDR4_A6	SSTL12_DCI	P2	A6	U17-U19 U73-U74
BG50	PL_DDR4_A7	SSTL12_DCI	R8	A7	U17-U19 U73-U74
BF51	PL_DDR4_A8	SSTL12_DCI	R2	A8	U17-U19 U73-U74
BG47	PL_DDR4_A9	SSTL12_DCI	R7	A9	U17-U19 U73-U74
BF47	PL_DDR4_A10	SSTL12_DCI	M3	A10/AP	U17-U19 U73-U74
BG49	PL_DDR4_A11	SSTL12_DCI	T2	A11	U17-U19 U73-U74
BF48	PL_DDR4_A12	SSTL12_DCI	M7	A12/BC_B	U17-U19 U73-U74
BF52	PL_DDR4_A13	SSTL12_DCI	T8	A13	U17-U19 U73-U74

Table 6: **DDR4 Memory 72-bit I/F to FPGA U1 Banks 64, 65, and 66** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
BE54	PL_DDR4_BA0	SSTL12_DCI	N2	BA0	U17-U19 U73-U74
BE53	PL_DDR4_BA1	SSTL12_DCI	N8	BA1	U17-U19 U73-U74
BG54	PL_DDR4_BG0	SSTL12_DCI	M2	BG0	U17-U19 U73-U74
BG53	PL_DDR4_WE_B	SSTL12_DCI	L2	WE_B/A14	U17-U19 U73-U74
BJ54	PL_DDR4_RAS_B	SSTL12_DCI	L8	RAS_B/A16	U17-U19 U73-U74
BH54	PL_DDR4_CAS_B	SSTL12_DCI	M8	CAS_B_A15	U17-U19 U73-U74
BK53	PL_DDR4_CK_T	DIFF_SSTL12_DCI	K7	CK_T	U17-U19 U73-U74
BK54	PL_DDR4_CK_C	DIFF_SSTL12_DCI	K8	CK_C	U17-U19 U73-U74
BH52	PL_DDR4_CKE	SSTL12_DCI	K2	CKE	U17-U19 U73-U74
BG52	PL_DDR4_ACT_B	SSTL12_DCI	L3	ACT_B	U17-U19 U73-U74
BJ53	PL_DDR4_TEN	SSTL12_DCI	N9	TEN	U17-U19 U73-U74
BJ52	PL_DDR4_ALERT_B	SSTL12_DCI	P9	ALERT_B	U17-U19 U73-U74
BL48	PL_DDR4_PARITY	SSTL12_DCI	T3	PAR	U17-U19 U73-U74
BH50	PL_DDR4_RESET_B	LVCMOS12	P1	RESET_B	U17-U19 U73-U74
BH49	PL_DDR4_ODT	SSTL12_DCI	K3	ODT	U17-U19 U73-U74
BP49	PL_DDR4_CS_B	SSTL12_DCI	L7	CS_B	U17-U19 U73-U74

The VCU128 DDR4 memory component interfaces adhere to the constraints guidelines documented in the “DDR3/DDR4 Design Guidelines” section of the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150). The VCU128 board DDR4 memory component interface is a 40Ω impedance implementation.

For more information on the internal VREF, see the “Supply Voltages for the SelectIO Pins VREF” and the “Internal VREF” sections in the *UltraScale Architecture SelectIO Resources User Guide* (UG571). For more details about the Micron DDR4 component memory, see the Micron MT40A512M16LY data sheet at the Micron Technology website.

RLD3 Component Memory

[Figure 2, callout 5]

The 288 MB RLD3 72-bit wide component memory system is comprised of two 36-bit 1.125 Gb RLDRAM3 devices located at U39 and U37.

- Manufacturer: Micron
- Part Number: MT44K32M36RB-107E
- Description:
  - 1.125 Gb (32 Mb x 36)

- 1.2V 168-ball BGA
- Up to RL3-1866

The VCU128 XCVU37P FPGA RLDRAM3 interface performance is documented in the *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

This memory system is connected to the XCVU37P HP banks 73, 74, and 75. The RLD3 0.6V VTT termination voltage (net RLD3_VTERM_0V6) is sourced from TI TPS51200DR linear regulator U92. The RLD3 memory interface bank VREF pins are not connected, which, coupled with an XDC set_property INTERNAL_VREF constraint, invoke the INTERNAL VREF mode. The connections between the RLD3 component memories and XCVU37P banks 73, 74, and 75 are listed in the following table.

Table 7: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 73, 74, and 75**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
K29	RLD3_72B_DQ0	SSTL12	D11	DQ0	U39
J30	RLD3_72B_DQ1	SSTL12	E10	DQ1	U39
K32	RLD3_72B_DQ2	SSTL12	C8	DQ2	U39
J31	RLD3_72B_DQ3	SSTL12	C10	DQ3	U39
L29	RLD3_72B_DQ4	SSTL12	C12	DQ4	U39
L31	RLD3_72B_DQ5	SSTL12	B9	DQ5	U39
L30	RLD3_72B_DQ6	SSTL12	B11	DQ6	U39
J32	RLD3_72B_DQ7	SSTL12	A8	DQ7	U39
K31	RLD3_72B_DQ8	SSTL12	A10	DQ8	U39
G30	RLD3_72B_DQ9	SSTL12	J10	DQ9	U39
H30	RLD3_72B_DQ10	SSTL12	K11	DQ10	U39
F31	RLD3_72B_DQ11	SSTL12	K13	DQ11	U39
G28	RLD3_72B_DQ12	SSTL12	L8	DQ12	U39
H29	RLD3_72B_DQ13	SSTL12	L10	DQ13	U39
G31	RLD3_72B_DQ14	SSTL12	L12	DQ14	U39
G32	RLD3_72B_DQ15	SSTL12	M9	DQ15	U39
H32	RLD3_72B_DQ16	SSTL12	M11	DQ16	U39
F28	RLD3_72B_DQ17	SSTL12	N8	DQ17	U39
E33	RLD3_72B_DQ18	SSTL12	D3	DQ18	U39
F29	RLD3_72B_DQ19	SSTL12	E4	DQ19	U39
E29	RLD3_72B_DQ20	SSTL12	C6	DQ20	U39
C32	RLD3_72B_DQ21	SSTL12	C4	DQ21	U39
F33	RLD3_72B_DQ22	SSTL12	C2	DQ22	U39
D30	RLD3_72B_DQ23	SSTL12	B5	DQ23	U39
D32	RLD3_72B_DQ24	SSTL12	B3	DQ24	U39
D29	RLD3_72B_DQ25	SSTL12	A6	DQ25	U39

Table 7: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 73, 74, and 75** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
D31	RLD3_72B_DQ26	SSTL12	A4	DQ26	U39
A31	RLD3_72B_DQ27	SSTL12	J4	DQ27	U39
B32	RLD3_72B_DQ28	SSTL12	K3	DQ28	U39
A33	RLD3_72B_DQ29	SSTL12	K1	DQ29	U39
B30	RLD3_72B_DQ30	SSTL12	L6	DQ30	U39
A30	RLD3_72B_DQ31	SSTL12	L4	DQ31	U39
C28	RLD3_72B_DQ32	SSTL12	L2	DQ32	U39
C29	RLD3_72B_DQ33	SSTL12	M5	DQ33	U39
A29	RLD3_72B_DQ34	SSTL12	M3	DQ34	U39
B28	RLD3_72B_DQ35	SSTL12	N6	DQ35	U39
G42	RLD3_72B_DQ36	SSTL12	D11	DQ0	U37
G41	RLD3_72B_DQ37	SSTL12	E10	DQ1	U37
H42	RLD3_72B_DQ38	SSTL12	C8	DQ2	U37
G40	RLD3_72B_DQ39	SSTL12	C10	DQ3	U37
H43	RLD3_72B_DQ40	SSTL12	C12	DQ4	U37
J42	RLD3_72B_DQ41	SSTL12	B9	DQ5	U37
H40	RLD3_72B_DQ42	SSTL12	B11	DQ6	U37
J40	RLD3_72B_DQ43	SSTL12	A8	DQ7	U37
J41	RLD3_72B_DQ44	SSTL12	A10	DQ8	U37
D44	RLD3_72B_DQ45	SSTL12	J10	DQ9	U37
F45	RLD3_72B_DQ46	SSTL12	K11	DQ10	U37
F44	RLD3_72B_DQ47	SSTL12	K13	DQ11	U37
D46	RLD3_72B_DQ48	SSTL12	L8	DQ12	U37
F46	RLD3_72B_DQ49	SSTL12	L10	DQ13	U37
E44	RLD3_72B_DQ50	SSTL12	L12	DQ14	U37
E46	RLD3_72B_DQ51	SSTL12	M9	DQ15	U37
G45	RLD3_72B_DQ52	SSTL12	M11	DQ16	U37
H45	RLD3_72B_DQ53	SSTL12	N8	DQ17	U37
B46	RLD3_72B_DQ54	SSTL12	D3	DQ18	U37
A46	RLD3_72B_DQ55	SSTL12	E4	DQ19	U37
C43	RLD3_72B_DQ56	SSTL12	C6	DQ20	U37
B45	RLD3_72B_DQ57	SSTL12	C4	DQ21	U37
A45	RLD3_72B_DQ58	SSTL12	C2	DQ22	U37
C45	RLD3_72B_DQ59	SSTL12	B5	DQ23	U37
C44	RLD3_72B_DQ60	SSTL12	B3	DQ24	U37
D42	RLD3_72B_DQ61	SSTL12	A6	DQ25	U37
A43	RLD3_72B_DQ62	SSTL12	A4	DQ26	U37
D40	RLD3_72B_DQ63	SSTL12	J4	DQ27	U37

Table 7: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 73, 74, and 75** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
C40	RLD3_72B_DQ64	SSTL12	K3	DQ28	U37
A39	RLD3_72B_DQ65	SSTL12	K1	DQ29	U37
A41	RLD3_72B_DQ66	SSTL12	L6	DQ30	U37
B41	RLD3_72B_DQ67	SSTL12	L4	DQ31	U37
B40	RLD3_72B_DQ68	SSTL12	L2	DQ32	U37
D41	RLD3_72B_DQ69	SSTL12	M5	DQ33	U37
B42	RLD3_72B_DQ70	SSTL12	M3	DQ34	U37
E41	RLD3_72B_DQ71	SSTL12	N6	DQ35	U37
J29	RLD3_72B_DM0	SSTL12	B7	DM0	U39
A28	RLD3_72B_DM1	SSTL12	M7	DM1	U39
G43	RLD3_72B_DM2	SSTL12	B7	DM0	U37
A40	RLD3_72B_DM3	SSTL12	M7	DM1	U37
D39	RLD3_72B_A0	SSTL12	E2	A0	U37, U39
A38	RLD3_72B_A1	SSTL12	F5	A1	U37, U39
B38	RLD3_72B_A2	SSTL12	F4	A2	U37, U39
J34	RLD3_72B_A3	SSTL12	F9	A3	U37, U39
K34	RLD3_72B_A4	SSTL12	F10	A4	U37, U39
K37	RLD3_72B_A5	SSTL12	F12	A5	U37, U39
C38	RLD3_72B_A6	SSTL12	G3	A6	U37, U39
E36	RLD3_72B_A7	SSTL12	F1	A7	U37, U39
B35	RLD3_72B_A8	SSTL12	G11	A8	U37, U39
L35	RLD3_72B_A9	SSTL12	F13	A9	U37, U39
D34	RLD3_72B_A10	SSTL12	H13	A10	U37, U39
E39	RLD3_72B_A11	SSTL12	D1	A11	U37, U39
A35	RLD3_72B_A12	SSTL12	H11	A12	U37, U39
C35	RLD3_72B_A13	SSTL12	D13	A13	U37, U39
E37	RLD3_72B_A14	SSTL12	H3	A14	U37, U39
E38	RLD3_72B_A15	SSTL12	G2	A15	U37, U39
C37	RLD3_72B_A16	SSTL12	H4	A16	U37, U39
B36	RLD3_72B_A17	SSTL12	H10	A17	U37, U39
F34	RLD3_72B_A18	SSTL12	G12	A18	U37, U39
J37	RLD3_72B_A19	SSTL12	H1	A19	U37, U39
C39	RLD3_72B_A20	SSTL12	F2	NF_A20	U37, U39
C34	RLD3_72B_BA0	SSTL12	G9	BA0	U37, U39
B37	RLD3_72B_BA1	SSTL12	G5	BA1	U37, U39
A36	RLD3_72B_BA2	SSTL12	H8	BA2	U37, U39
D36	RLD3_72B_BA3	SSTL12	H6	BA3	U37, U39
D37	RLD3_72B_WE_B	SSTL12	F6	WE_B	U37, U39

Table 7: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 73, 74, and 75** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
E34	RLD3_72B_REF_B	SSTL12	F8	REF_B	U37, U39
G37	RLD3_72B_CK_P	SSTL12	H7	CK	U37, U39
F38	RLD3_72B_CK_N	SSTL12	G7	CK_B	U37, U39
D35	RLD3_72B_RESET_B	SSTL12	A13	RESET_B	U37, U39
A34	RLD3_72B_CS_B	SSTL12	E12	CS_B	U37, U39
H37	RLD3_72B_DK0_P	DIFF_SSTL12	D7	DK0	U39
H38	RLD3_72B_DK0_N	DIFF_SSTL12	C7	DK0_B	U39
H34	RLD3_72B_DK1_P	DIFF_SSTL12	K7	DK1	U39
H35	RLD3_72B_DK1_N	DIFF_SSTL12	L7	DK1_B	U39
G38	RLD3_72B_DK2_P	DIFF_SSTL12	D7	DK0	U37
F39	RLD3_72B_DK2_N	DIFF_SSTL12	C7	DK0_B	U37
G35	RLD3_72B_DK3_P	DIFF_SSTL12	K7	DK1	U37
G36	RLD3_72B_DK3_N	DIFF_SSTL12	L7	DK1_B	U37
L33	RLD3_72B_QK0_P	DIFF_SSTL12	D9	QK0	U39
K33	RLD3_72B_QK0_N	DIFF_SSTL12	E8	QK0_B	U39
H33	RLD3_72B_QK1_P	DIFF_SSTL12	K9	QK1	U39
G33	RLD3_72B_QK1_N	DIFF_SSTL12	J8	QK1_B	U39
E31	RLD3_72B_QK2_P	DIFF_SSTL12	D5	QK2	U39
E32	RLD3_72B_QK2_N	DIFF_SSTL12	E6	QK2_B	U39
C30	RLD3_72B_QK3_P	DIFF_SSTL12	K5	QK3	U39
B31	RLD3_72B_QK3_N	DIFF_SSTL12	J6	QK3_B	U39
K41	RLD3_72B_QK4_P	DIFF_SSTL12	D9	QK0	U37
K42	RLD3_72B_QK4_N	DIFF_SSTL12	E8	QK0_B	U37
J44	RLD3_72B_QK5_P	DIFF_SSTL12	K9	QK1	U37
H44	RLD3_72B_QK5_N	DIFF_SSTL12	J8	QK1_B	U37
E42	RLD3_72B_QK6_P	DIFF_SSTL12	D5	QK2	U37
E43	RLD3_72B_QK6_N	DIFF_SSTL12	E6	QK2_B	U37
F40	RLD3_72B_QK7_P	DIFF_SSTL12	K5	QK3	U37
F41	RLD3_72B_QK7_N	DIFF_SSTL12	J6	QK3_B	U37
F30	RLD3_72B_QVLD0	SSTL12	J12	QVLD0	U39
E28	RLD3_72B_QVLD1	SSTL12	J2	QVLD1	U39
D45	RLD3_72B_QVLD2	SSTL12	J12	QVLD0	U37
A44	RLD3_72B_QVLD3	SSTL12	J2	QVLD1	U37

The VCU128 RLD3 72-bit memory component interface adheres to the constraints guidelines documented in the "RLD3 Design Guidelines" section of the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150). The VCU128 RLD3 memory component interface is a 40Ω impedance implementation.

For more information on the internal VREF, see the "Supply Voltages for the SelectIO Pins", “VREF”, and “Internal VREF” sections in the *UltraScale Architecture SelectIO Resources User Guide* (UG571). For more details about the Micron RLD3 component memory, see the Micron MT44K32M36RB Data Sheet at the Micron Technology website.

QDR4 Component Memory

[Figure 2, callout 6]

The 4.5 GB QDR4 component memory system is comprised of one 144-Mbit density (4M × 36) QDR4 SRAM device located at U40.

- Manufacturer: Cypress
- Part Number: CY7C4142KV13_106FCXC
- Description:
  - 144-Mbit density (4M × 36)
  - Dual independent 36-bit bidirectional double data rate (DDR) data ports
  - Supports concurrent read/write transactions on both ports
  - Single address port used to control both data ports
  - 1.2V 361-ball FCBGA
  - Maximum operating frequency of 1066 MHz

The VCU128 XCVU37P FPGA QDR IV interface performance is documented in the *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

The 72-bit wide QDR4 memory is connected to XCVU37P U1 HP banks 68, 69, and 70. The QDR4 memory interface bank VREF pins are not connected, which, coupled with an XDC set_property INTERNAL VREF constraint, invoke the INTERNAL VREF mode. The connections between the 72-bit interface QDR4 component memories and XCVU37P banks 68, 69, and 70 are listed in the following table.

Table 8: **QDR4 Memory 72-bit I/F to FPGA U1 Banks 68, 69, and 70**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory	
			Pin #	Pin Name
QDR4 A-side Data				
BM14	QDR4_DQA0		C8	DQA0
BM13	QDR4_DQA1		B7	DQA1
BN15	QDR4_DQA2		C6	DQA2
BN12	QDR4_DQA3		D5	DQA3
BM15	QDR4_DQA4		D7	DQA4
BP13	QDR4_DQA5		A4	DQA5
BP14	QDR4_DQA6		F5	DQA6
BM12	QDR4_DQA7		A6	DQA7
BL15	QDR4_DQA8		A8	DQA8
BM9	QDR4_DQA9		H3	DQA9
BK9	QDR4_DQA10		H5	DQA10
BL10	QDR4_DQA11		J2	DQA11
BK10	QDR4_DQA12		J4	DQA12
BL8	QDR4_DQA13		B2	DQA13
BN10	QDR4_DQA14		E2	DQA14
BM10	QDR4_DQA15		G2	DQA15
BN9	QDR4_DQA16		G4	DQA16
BJ9	QDR4_DQA17		B5	DQA17
BL12	QDR4_DQA18		C12	DQA18
BK14	QDR4_DQA19		B13	DQA19
BJ12	QDR4_DQA20		C14	DQA20
BK15	QDR4_DQA21		D15	DQA21
BL13	QDR4_DQA22		D13	DQA22
BH14	QDR4_DQA23		A16	DQA23
BH15	QDR4_DQA24		F15	DQA24
BJ14	QDR4_DQA25		A14	DQA25
BJ13	QDR4_DQA26		A12	DQA26
BE9	QDR4_DQA27		H17	DQA27
BE10	QDR4_DQA28		H15	DQA28
BG13	QDR4_DQA29		J18	DQA29
BE11	QDR4_DQA30		J16	DQA30
BF10	QDR4_DQA31		B18	DQA31
BG12	QDR4_DQA32		E18	DQA32
BG9	QDR4_DQA33		G18	DQA33
BG10	QDR4_DQA34		G16	DQA34
BF12	QDR4_DQA35		B15	DQA35

Table 8: **QDR4 Memory 72-bit I/F to FPGA U1 Banks 68, 69, and 70** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory	
			Pin #	Pin Name
QDR4 A-side Control				
BP12	QDR4_DKA0_P		F4	DKA0_P
BP11	QDR4_DKA0_N		F3	DKA0_N
BH10	QDR4_DKA1_P		F16	DKA1_P
BH9	QDR4_DKA1_N		F17	DKA1_N
BP9	QDR4_QKA0_P		C4	QKA0_P
BP8	QDR4_QKA0_N		D3	QKA0_N
BJ11	QDR4_QKA1_P		C16	QKA1_P
BK11	QDR4_QKA1_N		D17	QKA1_N
BM8	QDR4_QVLDA0		C3	QVLDA0
BK13	QDR4_QVLDA1		C17	QVLDA1
BM3	QDR4_LDA_N		H8	LDA_N
BM4	QDR4_RWA_N		H10	RWA_N
R522(GND)[1]	QDR4_DINVA0		D8	DINVA0
R519(GND)[1]	QDR4_DINVA1		D12	DINVA1
QDR4 B-side Data				
H15	QDR4_DQB0		U8	DQB0
J15	QDR4_DQB1		V7	DQB1
J12	QDR4_DQB2		U6	DQB2
J11	QDR4_DQB3		T5	DQB3
H14	QDR4_DQB4		T7	DQB4
G13	QDR4_DQB5		W4	DQB5
J14	QDR4_DQB6		P5	DQB6
H12	QDR4_DQB7		W6	DQB7
H13	QDR4_DQB8		W8	DQB8
G11	QDR4_DQB9		M3	DQB9
E12	QDR4_DQB10		M5	DQB10
F10	QDR4_DQB11		L2	DQB11
E11	QDR4_DQB12		L4	DQB12
D10	QDR4_DQB13		V2	DQB13
E9	QDR4_DQB14		R2	DQB14
F9	QDR4_DQB15		N2	DQB15
F11	QDR4_DQB16		N4	DQB16
D11	QDR4_DQB17		V5	DQB17
E14	QDR4_DQB18		U12	DQB18
A14	QDR4_DQB19		V13	DQB19
D15	QDR4_DQB20		U14	DQB20
B15	QDR4_DQB21		T15	DQB21

Table 8: **QDR4 Memory 72-bit I/F to FPGA U1 Banks 68, 69, and 70** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory	
			Pin #	Pin Name
F13	QDR4_DQB22		T13	DQB22
C15	QDR4_DQB23		W16	DQB23
F15	QDR4_DQB24		P15	DQB24
A15	QDR4_DQB25		W14	DQB25
F14	QDR4_DQB26		W12	DQB26
C12	QDR4_DQB27		M17	DQB27
A11	QDR4_DQB28		M15	DQB28
B13	QDR4_DQB29		L18	DQB29
B12	QDR4_DQB30		L16	DQB30
A8	QDR4_DQB31		V18	DQB31
A9	QDR4_DQB32		R18	DQB32
B11	QDR4_DQB33		N18	DQB33
B10	QDR4_DQB34		N16	DQB34
A10	QDR4_DQB35		V15	DQB35
QDR4 B-side Control				
K14	QDR4_DKB0_P		P4	DKB0_P
K13	QDR4_DKB0_N		P3	DKB0_N
C10	QDR4_DKB1_P		P16	DKB1_P
C9	QDR4_DKB1_N		P17	DKB1_N
H10	QDR4_QKB0_P		U4	QKB0_P
G10	QDR4_QKB0_N		T3	QKB0_N
E13	QDR4_QKB1_P		U16	QKB1_P
D12	QDR4_QKB1_N		T17	QKB1_N
D9	QDR4_QVLDB0		U3	QVLDB0
D14	QDR4_QVLDB1		U17	QVLDB1
BL2	QDR4_LDB_N		H12	LDB_N
BL3	QDR4_RWB_N		L10	RWB_N
R606(GND)[1]	QDR4_DINVB0		T8	DINVB0
R602(GND)[1]	QDR4_DINVB1		T12	DINVB1
Common				
BF5	QDR4_A0		F10	A0
BF1	QDR4_A1		G10	A1
BE1	QDR4_A2		N10	A2
BE3	QDR4_A3		G7	A3
BE4	QDR4_A4		G13	A4
BE5	QDR4_A5		J7	A5
BE6	QDR4_A6		J13	A6
BF2	QDR4_A7		L7	A7

Table 8: **QDR4 Memory 72-bit I/F to FPGA U1 Banks 68, 69, and 70** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory	
			Pin #	Pin Name
BF3	QDR4_A8		L13	A8
BG2	QDR4_A9		N7	A9
BG3	QDR4_A10		N13	A10
BG4	QDR4_A11		M8	A11
BG5	QDR4_A12		M12	A12
BF7	QDR4_A13		F8	A13
BF8	QDR4_A14		F12	A14
BG7	QDR4_A15		P8	A15
BG8	QDR4_A16		P12	A16
BJ7	QDR4_A17		L9	A17
BH7	QDR4_A18		L11	A18_36M
BK8	QDR4_A19		J9	A19_72M
BJ8	QDR4_A20		J11	A20_144M
BJ6	QDR4_A21		G9	A21_288M
BK5	QDR4_A22		G11	A22_576M
BH6	QDR4_A23		N9	A23_1152M
BK4	QDR4_A24		N11	A24_2304M
BK6	QDR4_AP		P10	AP
BJ1	QDR4_AINV		M10	AINV
BH5	QDR4_CK_P		J10	CK_P
BH4	QDR4_CK_N		K10	CK_N
BJ3	QDR4_LBK0_N		A10	LBK0_N
BH1	QDR4_LBK1_N		B10	LBK1_N
BH2	QDR4_CFG_N		D10	CFG_N
BJ2	QDR4_PE_N		V10	PE_N
BK1	QDR4_RST_N		K18	RST_N
QDR4 U40 ZQ_ZT pin W10 is wired to 220Ω R604 to GND				

Notes:

1. Resistors to GND are 100Ω.

The VCU128 QDR-IV dual independent 36-bit bidirectional data port memory component interfaces adhere to the constraints guidelines documented in the "QDR-IV Design Guidelines" section of the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150). The VCU128 QDR-IV memory component interface is a 40Ω impedance implementation.

For more information on the internal VREF, see the "Supply Voltages for the SelectIO Pins", “VREF”, and “Internal VREF” sections in the *UltraScale Architecture SelectIO Resources User Guide* (UG571). For more details about the Cypress QDR-IV component memory, see the Cypress CY7C4142KV13_106FCXC Data Sheet at the Cypress Semiconductor website.

Quad SPI Flash Memory

[Figure 2, callout 7]

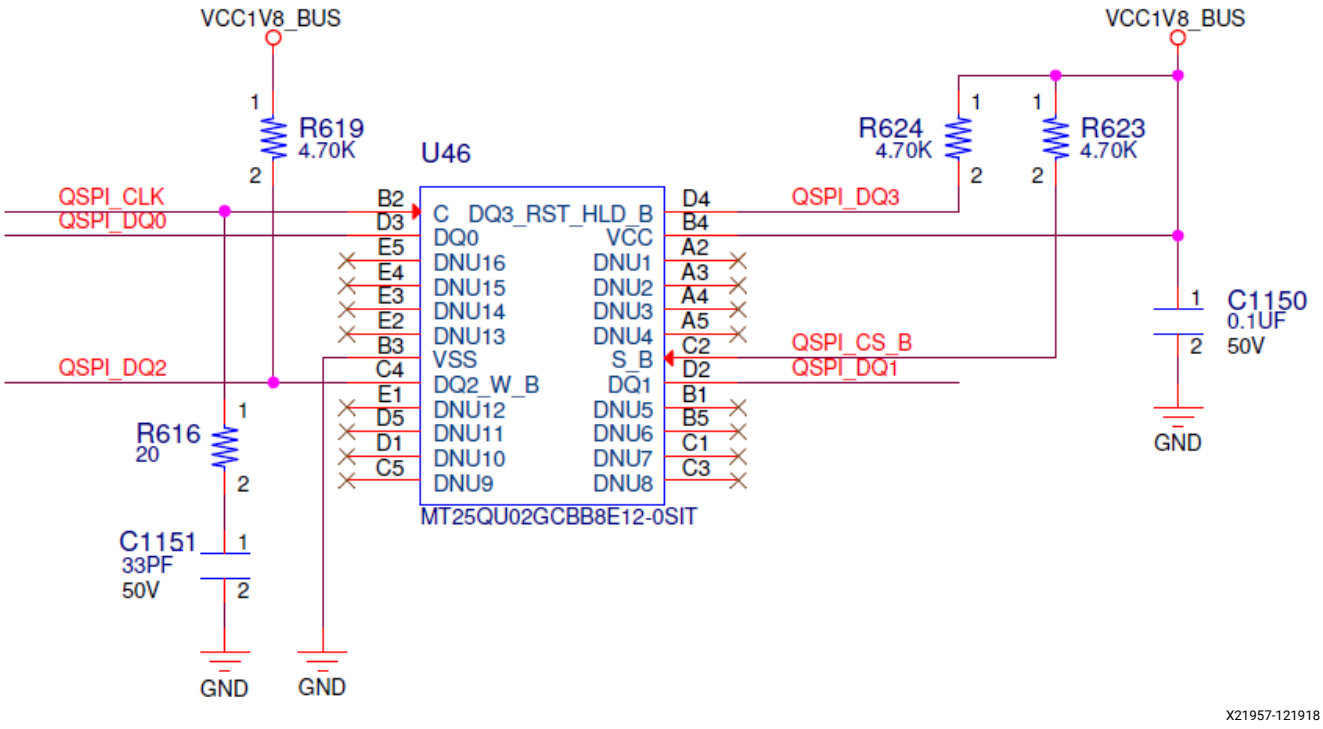
VCU128 boards host a Micron MT25QU02GCBB8E12-0SIT serial NOR flash Quad SPI flash memory capable of holding the boot image for the XCVU37P FPGA. This interface supports the QSPI32 boot mode as defined in the *UltraScale Architecture Configuration User Guide* (UG570).

The Quad SPI flash memory U46 provides 2 Gb of non-volatile storage that can be used for configuration and data storage.

- Part number: MT25QU02GCBB8E12-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: various depending on single/dual/quad mode

The Quad SPI circuitry is shown in the following figure.

Figure 7: **Quad SPI (2 Gbit) Flash Memory**



The connections between the Quad SPI flash memory and the XCVU37P FPGA are listed in the following table.

Table 9: **Quad-SPI Component Connections to FPGA U1**

XCVC37P (U1) Pin	Net Name	U46 Quad SPI	
		Pin #	Pin Name
AW15	QSPI_DQ0	D3	DQ0
AY15	QSPI_DQ1	D2	DQ1
AY14	QSPI_DQ2	C4	DQ2_W_B
AY13	QSPI_DQ3	D4	DQ3_RST_HLD_B
BD14	QSPI _CLK	B2	C
BC15	QSPI_CS_B	C2	S_B

The *UltraScale Architecture Configuration User Guide* (UG570) provides FPGA configuration details. For more Quad SPI component information, see the Micron MT25QU02GCBB8E12-0SIT data sheet at the Micron Technology website.

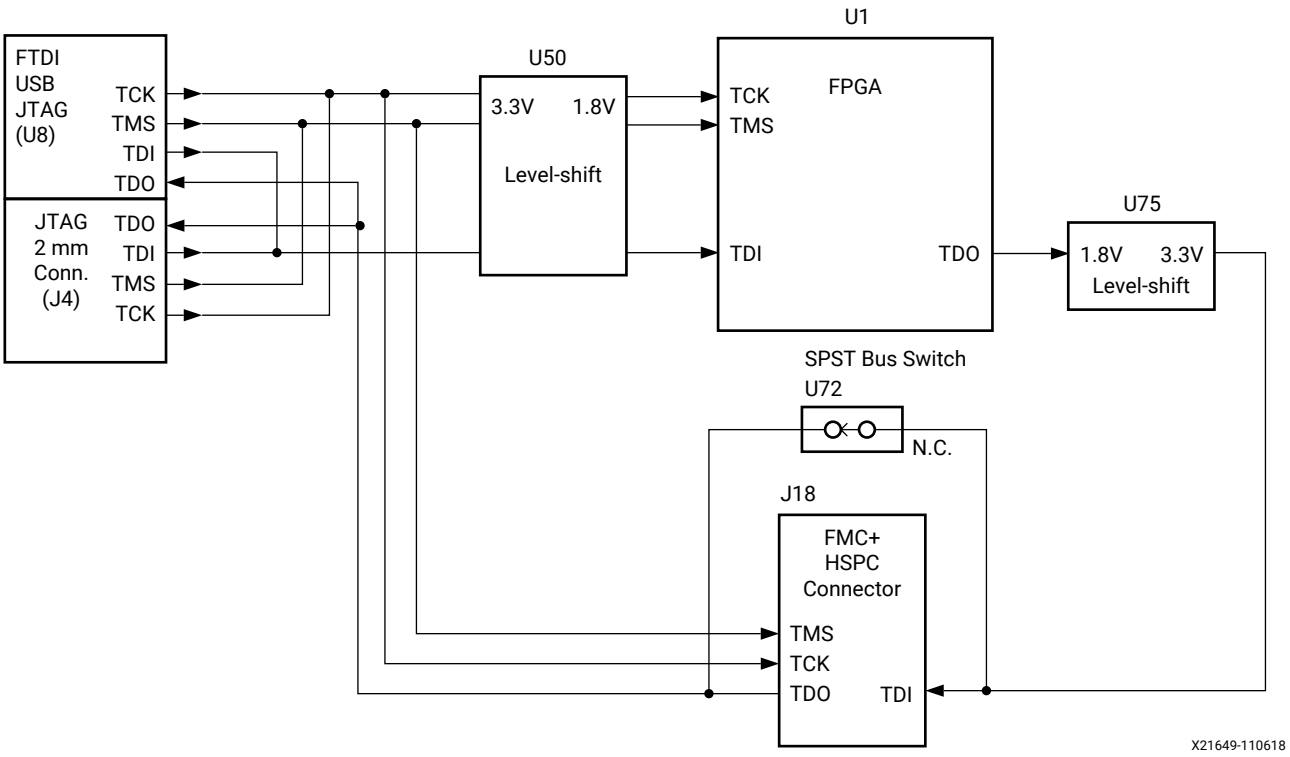
USB JTAG Interface

[Figure 2, callout 24]

JTAG configuration is provided through a dual-function FTDI FT4232HL USB-to-JTAG/UART bridge device (U8) where a host computer accesses the VCU128 board JTAG chain through a type-A (PC host side) to micro-AB (VCU128 board side J2) USB cable.

A 2 mm JTAG header (J4) is also provided in parallel for access by Xilinx® download cables, such as the Platform Cable USB II. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pins M[2:0], wired to SW1 positions [2:4]. The JTAG chain of the VCU128 board is shown in the following figure.

Figure 8: **JTAG Chain Block Diagram**



FMCP Connector JTAG Bypass

When an FMC is attached to the VCU128 board FMC+ HSPC connector J18, it is automatically added to the JTAG chain through the electronically controlled single-pole single-throw (SPST) switch U72. The SPST switch is in a normally closed state and transitions to an open state when the FMC is attached. Switch U72 adds an attached FMC to the FPGA JTAG chain as determined by the `FMCP_HSPC_PRSNT_M2C_B` signal.

IMPORTANT! *The attached FMC must implement a TDI-to-TDO connection through a device or bypass jumper to ensure that the JTAG chain connects to the FPGA U1.*

The JTAG connectivity on the VCU128 board allows a host computer to download bitstreams to the FPGA using the Xilinx tools. In addition, the JTAG connector allows debug tools such as the Vivado® serial I/O analyzer or a software debugger to access the FPGA. The Xilinx tools can also program the Quad SPI flash memory.

USB UART Interface

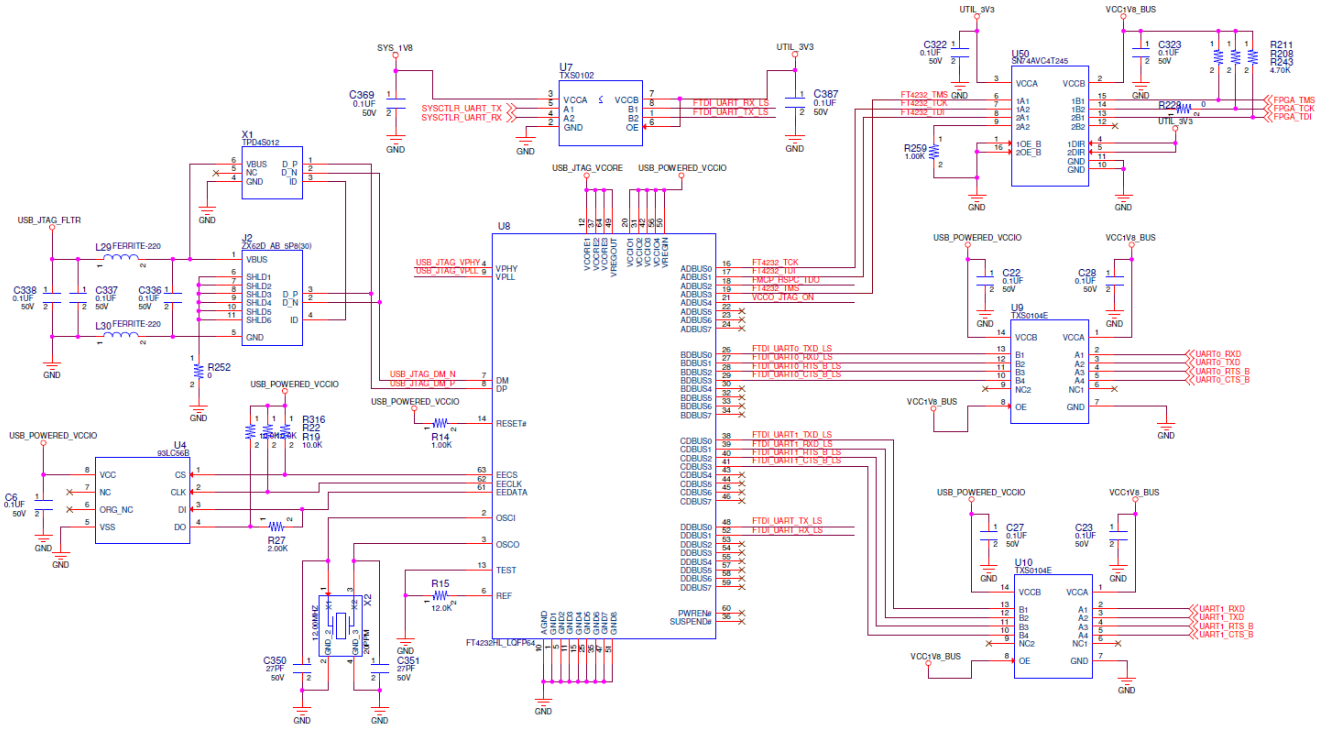
[Figure 2, callout 24]

The FT4232HL U8 multi-function USB-UART on the VCU128 board provides three level-shifted UART connections through the single micro-AB USB connector J2.

- Channel A is configured in JTAG mode to support the JTAG chain
- Channel B implements 4-wire UART0 (level-shifted) FPGA U1 bank 67 connections
- Channel C implements 4-wire UART1 (level-shifted) FPGA U1 bank 67 connections
- Channel D implements 2-wire (level-shifted) SYSCTLR U42 bank 501 connections

The USB UART interface circuit is shown in the following figure. The FTDI FT4232HL data sheet is available on the Future Technology Devices International Ltd. website.

Figure 9: **FTDI USB JTAG/UART Circuit**



Clock Generation

[Figure 2, callout 10-18]

The VCU128 evaluation board clock sources to the FPGA are listed in the following table.

Table 10: **Board Clock Sources**

Clock Name	Clock Ref. Des.	Description
Memory Interface Clocks		
DDR4 clock 100 MHz	U76	SiTime SiT9120AI 3.3V fixed frequency 100.000 MHz (DDR4_CLK_100MHZ_P/N)
QDR4 clock 100 MHz	U96	SiTime SiT9120AI 3.3V fixed frequency 100.000 MHz (QDR4_CLK_100MHZ_P/N)
RLD3 clock 100 MHz	U45	SiTime SiT9120AI 3.3V fixed frequency 100.000 MHz (RLD3_CLK_100MHZ_P/N)
QSFP Interface Clocks		
QSFP1 clock 156.250 MHz	U95	Silicon Labs Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default. (QSFP1_SI570_CLOCK_P/N)
QSFP2 clock 156.250 MHz	U90	Silicon Labs Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default. (QSFP2_SI570_CLOCK_P/N)
QSFP3 clock 156.250 MHz	U82	Silicon Labs Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default. (QSFP3_SI570_CLOCK_P/N)
QSFP4 clock 156.250 MHz	U80	Silicon Labs Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default. (QSFP4_SI570_CLOCK_P/N)
SMA GTY REFCLK and User Clock		
QSFP GTY131 REFCLK1 SMA clock	SMA J24 (P)/SMA J26 (N)	Bank 131 series capacitor coupled SMA clock (SMA_REFCLK_INPUT_P/N)
FPGA U1 bank 67 GPIO user SMA clock	SMA J12 (P)/SMA J13 (N)	Bank 67 QBC direct connect GPIO SMA (SMA_CLK_OUTPUT_P/N)
QSFP1/2 recovery clocks		
QSFP1/2 jitter attenuated clock	U87	Silicon Labs Si5328B LVDS precision clock, multiplier/jitter attenuator. See Jitter Attenuated Clock (SI5328_CLOCK1/2_P/N)

The following table lists the VCU128 clock sources-to-FPGA U1 connections.

Table 11: **Clock Sources to XCVU37P FPGA U1 Connections**

Clock Source Device/ U#.Pin#	Schematic Net Name	I/O Standard	FPGA (U1) Pin
Memory Interface Clocks			
SIT9120AI/U76.4	DDR4_CLK_100MHZ_P	LVDS	BH51
SIT9120AI/U76.5	DDR4_CLK_100MHZ_N	LVDS	BJ51
SIT9120AI/U96.4	QDR4_CLK_100MHZ_P	LVDS	BJ4

Table 11: **Clock Sources to XCVU37P FPGA U1 Connections** *(cont'd)*

Clock Source Device/ U#.Pin#	Schematic Net Name	I/O Standard	FPGA (U1) Pin
SIT9120AI/U96.5	QDR4_CLK_100MHZ_N	LVDS	BK3
SIT9120AI/U45.4	RLD3_CLK_100MHZ_P	LVDS	F35
SIT9120AI/U45.5	RLD3_CLK_100MHZ_N	LVDS	F36
QSFP Interface Clocks			
SI570/U95.4	QSFP1_SI570_CLOCK_P	[1]	P42
SI570/U95.5	QSFP1_SI570_CLOCK_N	[1]	P43
SI570/U90.4	QSFP2_SI570_CLOCK_P	[1]	T42
SI570/U90.5	QSFP2_SI570_CLOCK_N	[1]	T43
SI570/U82.4	QSFP3_SI570_CLOCK_P	[1]	Y42
SI570/U82.5	QSFP3_SI570_CLOCK_N	[1]	Y43
SI570/U80.4	QSFP4_SI570_CLOCK_P	[1]	AB42
SI570/U80.5	QSFP4_SI570_CLOCK_N	[1]	AB43
SMA GTY REFCLK and User Clock			
SMA J24.1	SMA_REFCLK_INPUT_P	[1]	AA40
SMA J26.1	SMA_REFCLK_INPUT_N	[1]	AA41
SMA J12.1	SMA_CLK_OUTPUT_P	[2]	BK26
SMA J13.1	SMA_CLK_OUTPUT_N	[2]	BL25
QSFP1/2 Recovery Clocks			
SI5328B/U87.29	SI5328_CLOCK1_P	[1]	R40
SI5328B/U87.28	SI5328_CLOCK1_P	[1]	R41
SI5328B/U87.35	SI5328_CLOCK2_P	[1]	W40
SI5328B/U87.34	SI5328_CLOCK2_P	[1]	W41

Notes:

1. Series capacitor coupled, MGT connections I/O standard is not applicable.
2. Signal amplitude not to exceed FPGA U1 bank 67 VCCO = VCC1V8 rail = 1.8V.

DDR4 Interface Clock

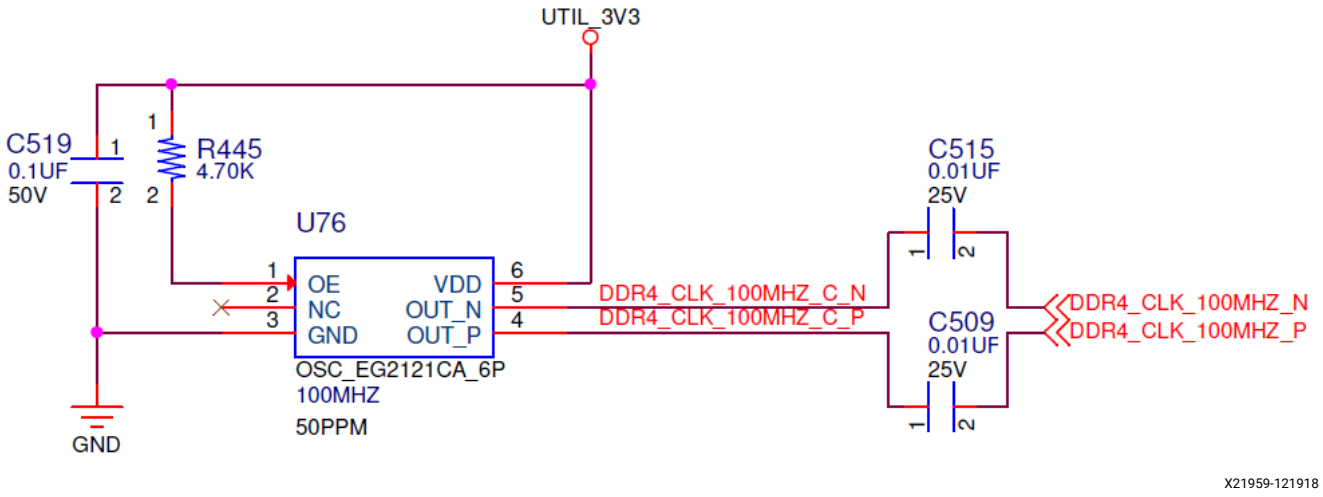
[Figure 2, callout 10]

The VCU128 evaluation board has a SiTime 100 MHz fixed frequency low-jitter 3.3V LVDS differential oscillator (U76) connected to FPGA U1 HP bank 66 DDR4 interface GC pins BH51 (P) and BJ51 (N) and is series capacitor coupled.

- Fixed frequency oscillator: SiTime SIT9120AI-2D3-33E100.0000 (100 MHz)
- 0.6 ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- 3.3V LVDS differential output

The DDR4 interface fixed frequency clock circuit is shown in the following figure.

Figure 10: **DDR4 Interface Clock**



QDR4 Interface Clock

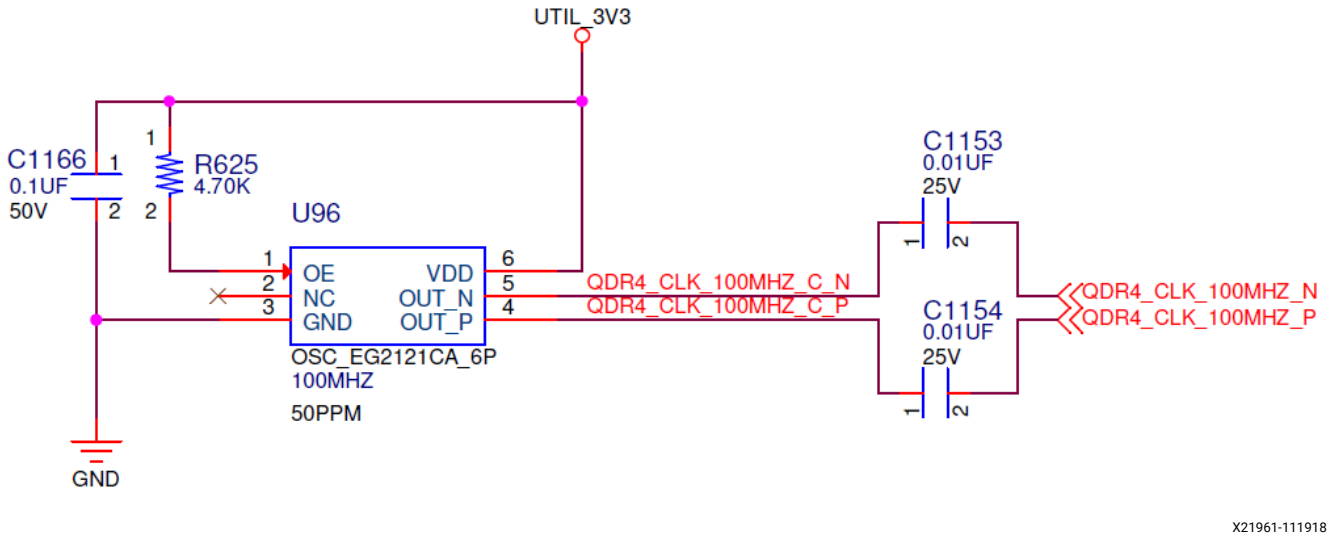
[Figure 2, callout 12]

The VCU128 evaluation board has a SiTime 100 MHz fixed frequency low-jitter 3.3V LVDS differential oscillator (U96) connected to FPGA U1 HP bank 69 QDR4 interface GC pins BJ4 (P) and BK3 (N) and is series capacitor coupled.

- Fixed frequency oscillator: SiTime SIT9120AI-2D3-33E100.0000 (100 MHz)
- 0.6 ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- 3.3V LVDS differential output

The QDR4 interface fixed frequency clock circuit is shown in the following figure.

Figure 11: **QDR4 Interface Clock**



RLD3 Interface Clock

[Figure 2, callout 11]

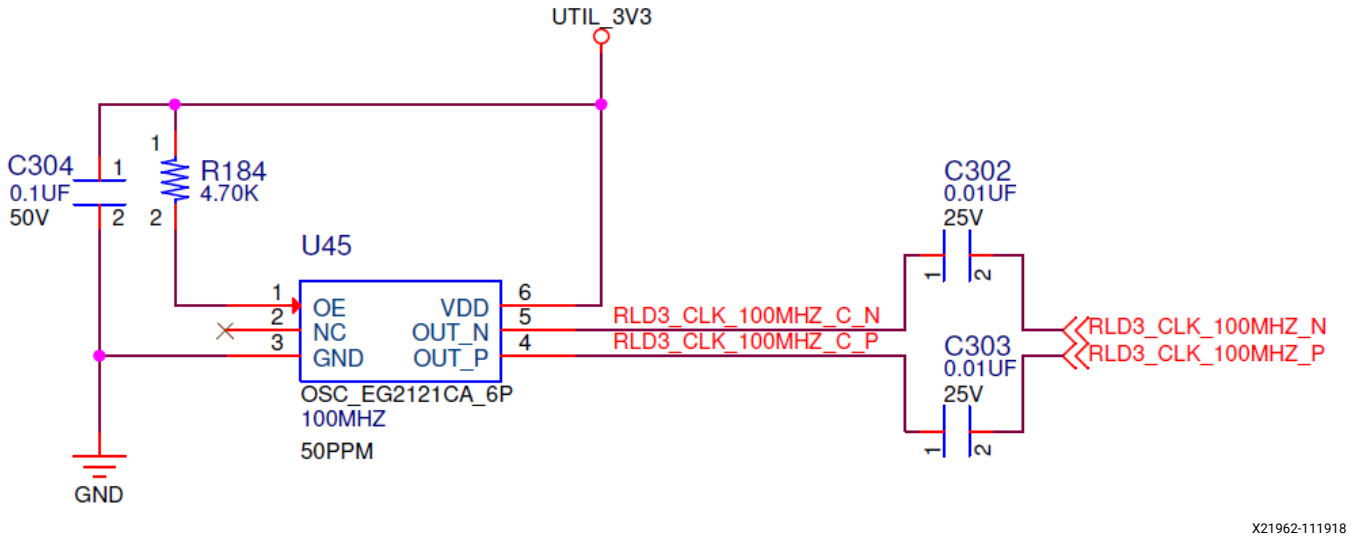
The VCU128 evaluation board has a SiTime 100 MHz fixed frequency low-jitter 3.3V LVDS differential oscillator (U45) connected to FPGA U1 HP bank 74 RLD3 interface GC pins F35 (P) and F36 (N) and is series capacitor coupled.

- Fixed frequency oscillator: SiTime SIT9120AI-2D3-33E100.0000 (100 MHz)
- 0.6 ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- 3.3V LVDS differential output

The RLD3 interface fixed frequency clock circuit is shown in the following figure.

The SiTime SiT9120AI data sheet is available on the SiTime Corp. website.

Figure 12: **RLD3 Interface Clock**



Programmable QSFP1 Clock

[Figure 2, callout 13]

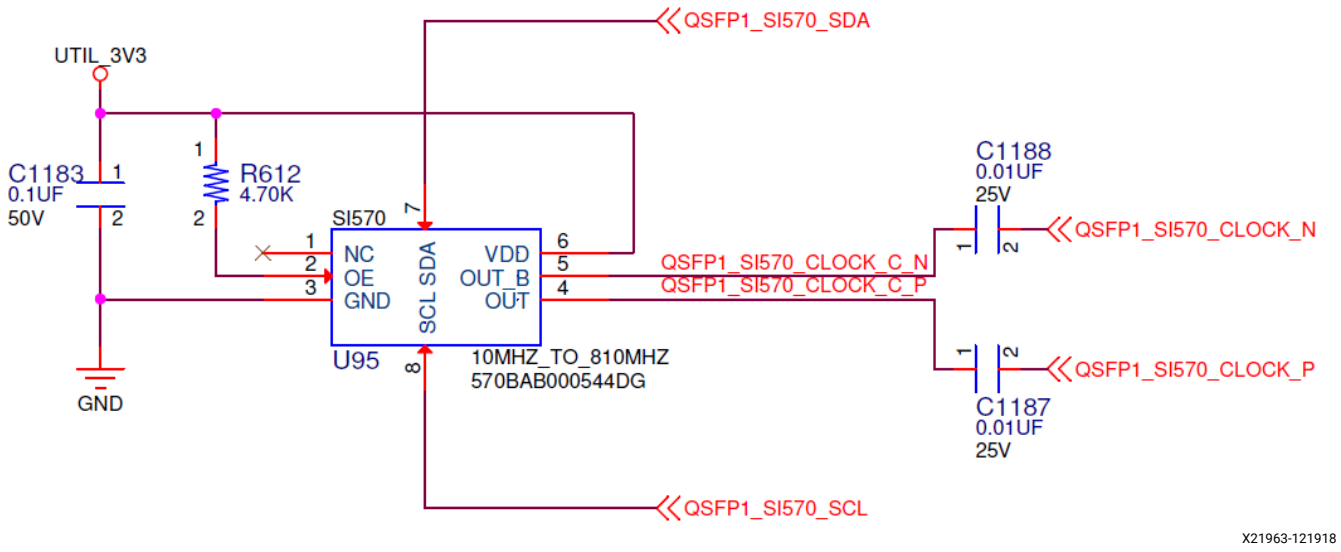
The VCU128 evaluation board has a SI570 I2C programmable low-jitter 3.3V LVDS differential oscillator (U95) connected to FPGA U1 GTY bank 135 MGTREFCLK0 P/N pins P42 and P43 (series capacitor coupled), respectively.

On power-up, the U95 SI570 user clock defaults to an output frequency of 156.250 MHz. The Zynq-7000 SoC system controller or FPGA implemented user IP can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the VCU128 evaluation board resets the QSFP1 clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

The programmable QSFP1 clock circuit is shown in the following figure.

Figure 13: **QSFP1 Clock**



Programmable QSFP2 Clock

[Figure 2, callout 14]

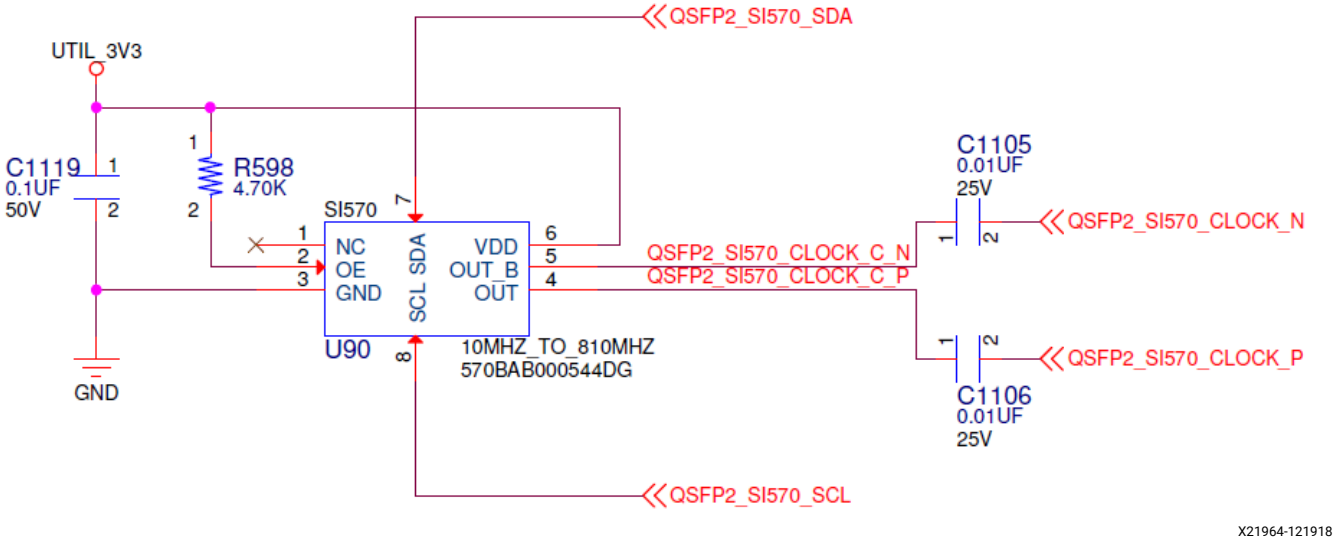
The VCU128 evaluation board has a SI570 I2C programmable low-jitter 3.3V LVDS differential oscillator (U90) connected to FPGA U1 GTY bank 134 MGTREFCLK0 P/N pins T42 and T43 (series capacitor coupled), respectively.

On power-up, the U90 SI570 user clock defaults to an output frequency of 156.250 MHz. The Zynq-7000 SoC system controller or FPGA implemented user IP can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the VCU128 evaluation board resets the QSFP2 clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

The programmable QSFP2 clock circuit is shown in the following figure.

Figure 14: **QSFP2 Clock**



Programmable QSFP3 Clock

[Figure 2, callout 15]

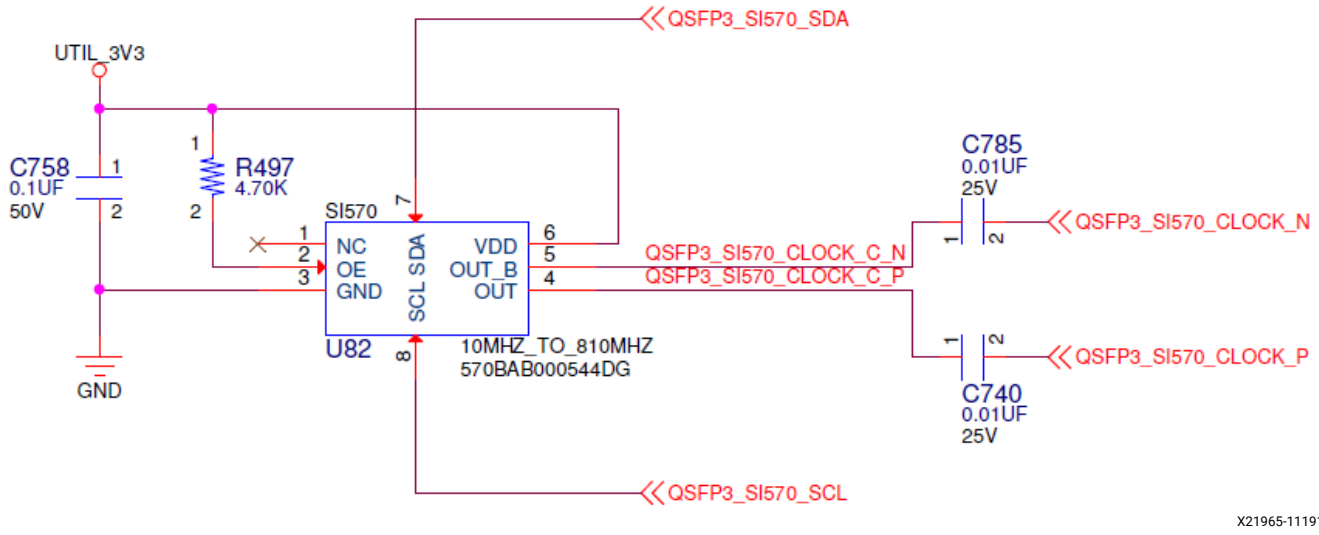
The VCU128 evaluation board has a SI570 I2C programmable low-jitter 3.3V LVDS differential oscillator (U82) connected to FPGA U1 GTY bank 132 MGTREFCLK0 P/N pins Y42 and Y43 (series capacitor coupled), respectively.

On power-up, the U82 SI570 user clock defaults to an output frequency of 156.250 MHz. The Zynq-7000 SoC system controller or FPGA implemented user IP can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the VCU128 evaluation board resets the QSFP3 clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

The programmable QSFP3 clock circuit is shown in the following figure.

Figure 15: **QSFP3 Clock**



Programmable QSFP4 Clock

[Figure 2, callout 16]

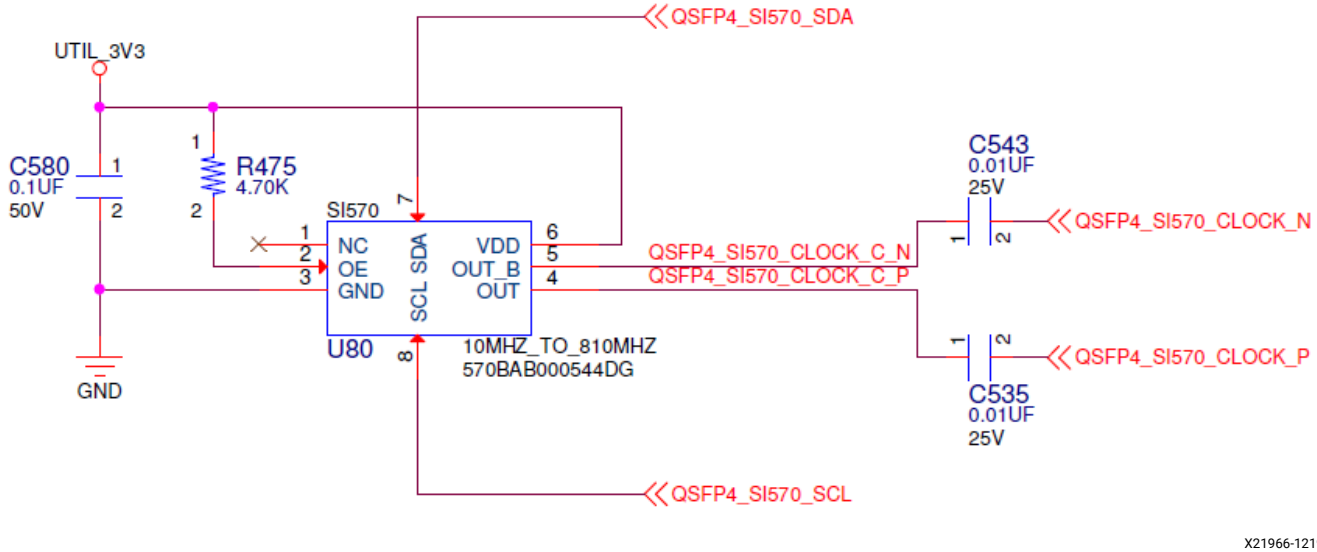
The VCU128 evaluation board has a SI570 I2C programmable low-jitter 3.3V LVDS differential oscillator (U80) connected to FPGA U1 GTY bank 131 MGTREFCLK0 P/N pins AB42 and AB43 (series capacitor coupled), respectively.

On power-up, the U80 SI570 user clock defaults to an output frequency of 156.250 MHz. The Zynq-7000 SoC system controller or FPGA implemented user IP can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the VCU128 evaluation board resets the QSFP4 clock to the default frequency of 156.250 MHz

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

The programmable QSFP4 clock circuit is shown in the following figure.

Figure 16: **QSFP4 Clock**

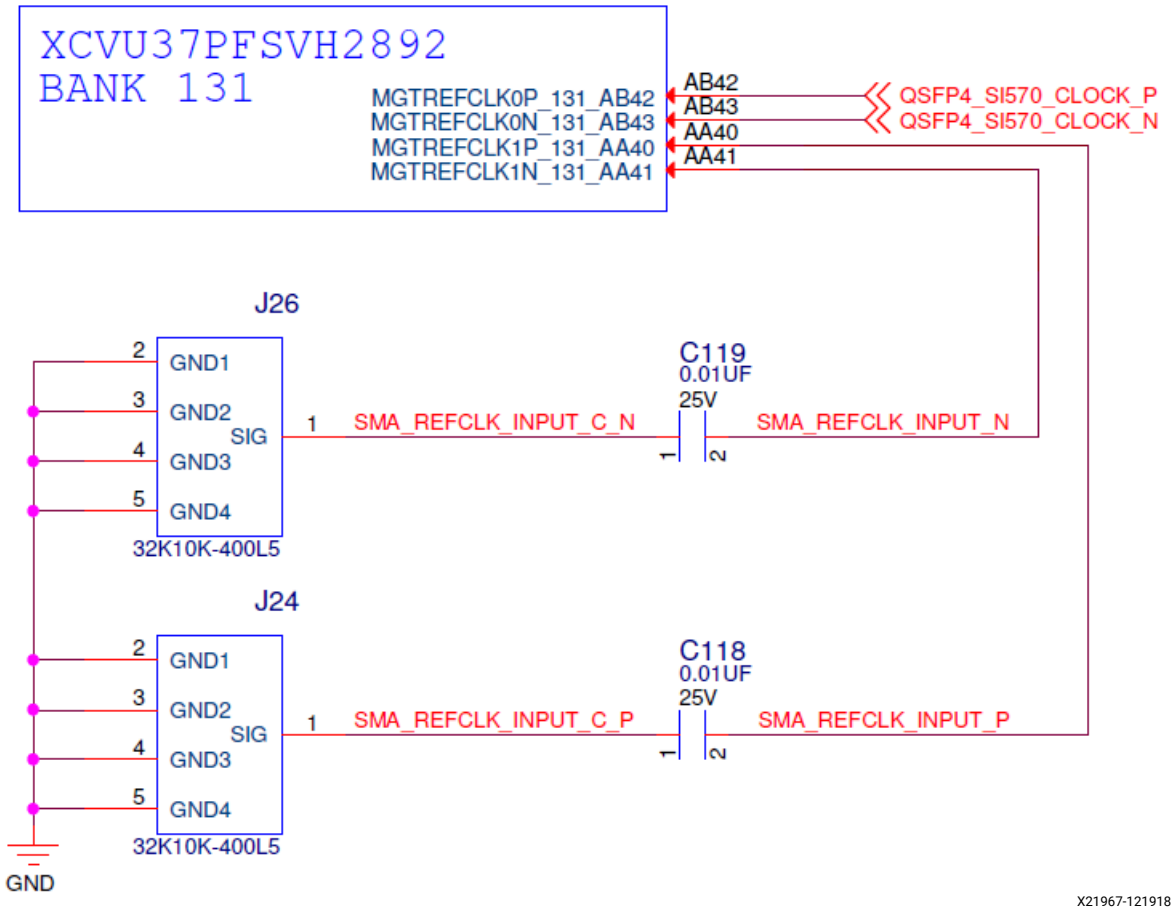


QSFP SMA Clock

[Figure 2, callout 18]

The VCU128 board provides a pair of SMAs for differential user clock input into FPGA U1 GTY bank 131. The P-side SMA J24 signal SMA_REFCLK_INPUT_P is connected to FPGA U1 GTY bank 131 MGTREFCLK1P pin AA40, with the N-side SMA J26 signal SMA_REFCLK_INPUT_N connected to U1 GTY bank 131 MGTREFCLK1N pin AA41. The transceiver reference clock pin absolute input voltage range is –0.5V min. to 1.3V max. The user SMA MGT clock circuit is shown in the following figure.

Figure 17: **QSFP SMA Clock**

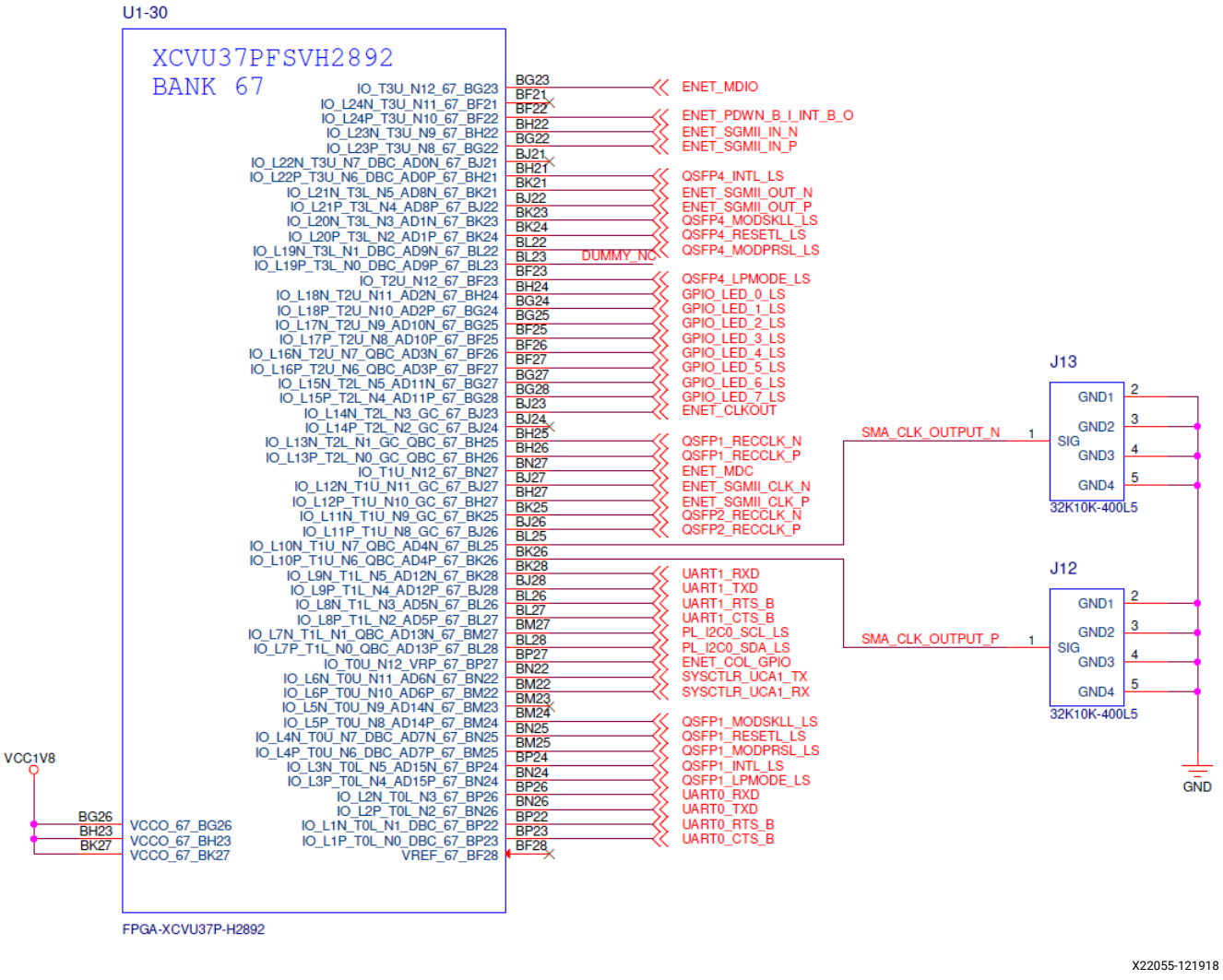


User SMA Clock

[Figure 2, callout 27]

The VCU128 board provides a pair of SMAs for differential user clock I/O on FPGA U1 HP bank 67. The P-side SMA J12 net SMA_CLK_OUTPUT_P is connected to FPGA U1 HP bank 67 QBC pin BK26. The N-side SMA J13 net SMA_CLK_OUTPUT_N is connected to FPGA U1 HP bank 67 QBC pin BL25. Bank 67 VCC1V8 VCCO is nominally 1.8V. Any signal connected to the SMA_CLK_OUTPUT SMA connectors in input mode must be equal to or less than the VCCO for bank 67. This value must be confirmed prior to applying signals to the SMA_CLK_OUTPUT connectors.

Figure 18: **User SMA Clock**



Jitter Attenuated Clock

[Figure 2, callout 17]

The VCU128 board includes a Silicon Labs Si5328B jitter attenuator U87 on the back side of the board. FPGA U1 bank 67 implements two QSFP RX differential clocks (QSFP1_RECCLK_P, pin BH26 and QSFP1_RECCLK_N, pin BH25, and QSFP2_RECCLK_P, pin BJ26 and QSFP2_RECCLK_N, pin BK25) for jitter attenuation.

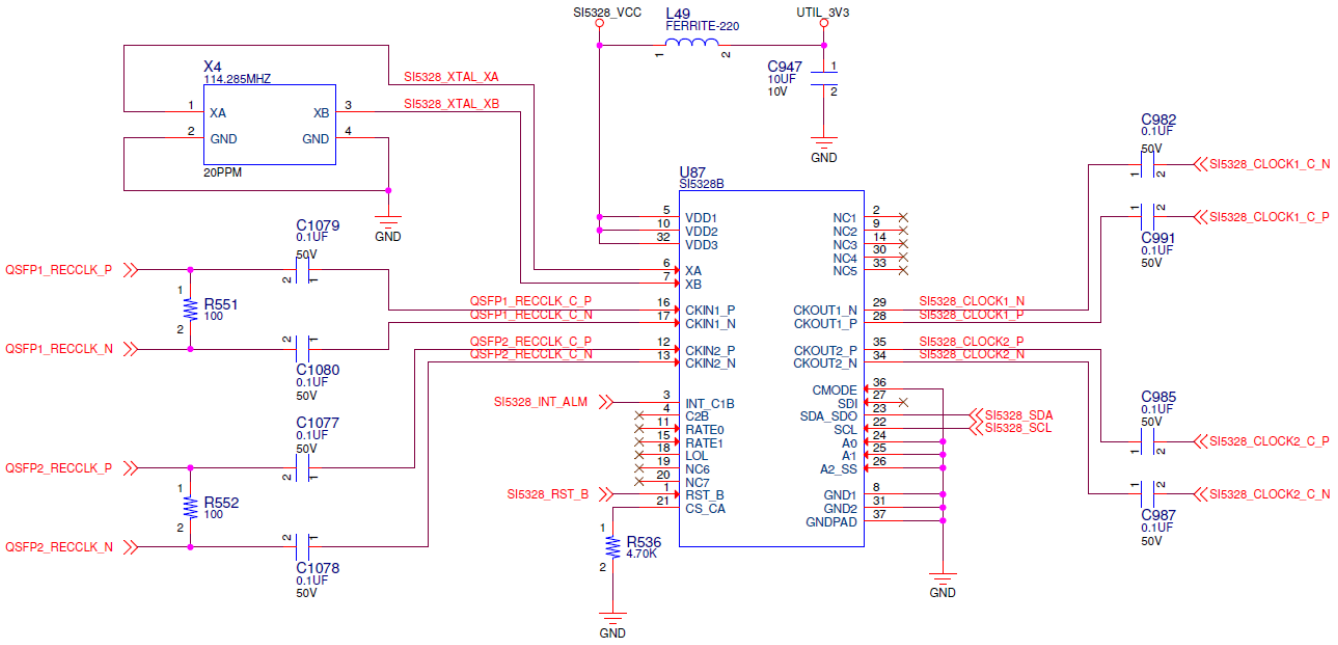
The jitter attenuated clock pair (SI5328_CLOCK1_C_P (U87 output pin 28), SI5328_CLOCK1_C_N (U87 output pin 29) is routed as a reference clock to FPGA U1 QSFP2 I/F GTY Quad 134 inputs MGTREFCLK1P (U1 pin R40) and MGTREFCLK1N (U1 pin R41).

The jitter attenuated clock pair (SI5328_CLOCK2_C_P (U87 output pin 35), SI5328_CLOCK2_C_N (U87 output pin 34) is routed as a reference clock to FPGA U1 QSFP3 I/F GTY Quad 132 inputs MGTREFCLK1P (U1 pin W40) and MGTREFCLK1N (U1 pin W41).

The primary purpose of this clock is to support synchronous protocols, such as common packet radio interface (CPRI) or open base station architecture initiative (OBSAI). These synchronous protocols perform clock recovery from user-supplied QSFP/QSFP+ modules, and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTY transceiver.

The jitter attenuated clock circuit is shown in the following figure.

Figure 19: **QSFP Recovery Clock**



X21968-121918

The SI5328B U87 I2C interface is connected to port 1 of the I2C0 bus TCA9548A U53 bus switch and can be configured by either the U42 system controller or U1 FPGA IP.

The system controller configures SI5328B U87 in free-run mode or automatically switches over to one of two recovered clock inputs for synchronous operation. Enabling the jitter attenuation feature requires additional user programming through the I2C bus. The Silicon Labs Si570 and Si5328B data sheets are available on the Silicon Labs website.

GTY Transceivers

The GTY transceivers in the XCVU37P are grouped into four channels or quads. The XCVU37P has twelve GTY quads on the left side of the device and twelve GTY Quads on the right side of the device.

The VCU128 board provides access to 14 of the 24 GTY Quads:

- Four of the GTY Quads are wired to QSFP[1:4] Module Connectors (J42, J39, J35, J32)
- Six of the GTY Quads are wired to FMC+ HSPC connector DP[0:23] (J18)
- Four of the GTY Quads are wired to the PCIe 16-lane edge connector (P1)
- Ten GTY Quads are not used (GTYs 130, 133, 228-235)

The reference clock for a Quad can be sourced from the Quad above or the Quad below the GTY Quad of interest.

Right-side Quads

The ten connected GTY Quads on the right side of the XCVU37P FPGA are described in this section (MGTY133 and MGTY130 are not used).

Quad 135

- MGTREFCLK0 – QSFP1_SI570_CLOCK_P/N
- MGTREFCLK1 – NC
- Four GTY transceivers allocated to QSFP1_TX/RX[1:4]_P/N

Quad 134

- MGTREFCLK0 – QSFP2_SI570_CLOCK_P/N
- MGTREFCLK1 – SI5328_CLOCK1_C_P/N
- Four GTY transceivers allocated to QSFP2_TX/RX[1:4]_P/N

Quad 132

- MGTREFCLK0 – QSFP3_SI570_CLOCK_P/N

- MGTREFCLK1 – SI5328_CLOCK2_C_P/N
- Four GTY transceivers allocated to QSFP3_TX/RX[1:4]_P/N

Quad 131

- MGTREFCLK0 – QSFP4_SI570_CLOCK_P/N
- MGTREFCLK1 – SMA_REFCLK_INPUT_P/N
- Four GTY transceivers allocated to QSFP4_TX/RX[1:4]_P/N

Quad 129

- MGTREFCLK0 - FMCP_HSPC_GBTCLK5_M2C_P/N
- NC
- Four GTY transceivers allocated to FMCP_HSPC_DP[20:23]

Quad 128

- MGTREFCLK0 - FMCP_HSPC_GBTCLK4_M2C_P/N
- NC
- Four GTY transceivers allocated to FMCP_HSPC_DP[16:19]

Quad 127

- MGTREFCLK0 – FMCP_HSPC_GBTCLK3_M2C_P/N
- NC
- Four GTY transceivers allocated to FMCP_HSPC_DP[12:15]

Quad 126

- MGTREFCLK0 – FMCP_HSPC_GBTCLK2_M2C_P/N
- NC
- Four GTY transceivers allocated to FMCP_HSPC_DP[8:11]

Quad 125

- MGTREFCLK0 – FMCP_HSPC_GBTCLK1_M2C_P/N
- NC
- Four GTY transceivers allocated to FMCP_HSPC_DP[4:7]

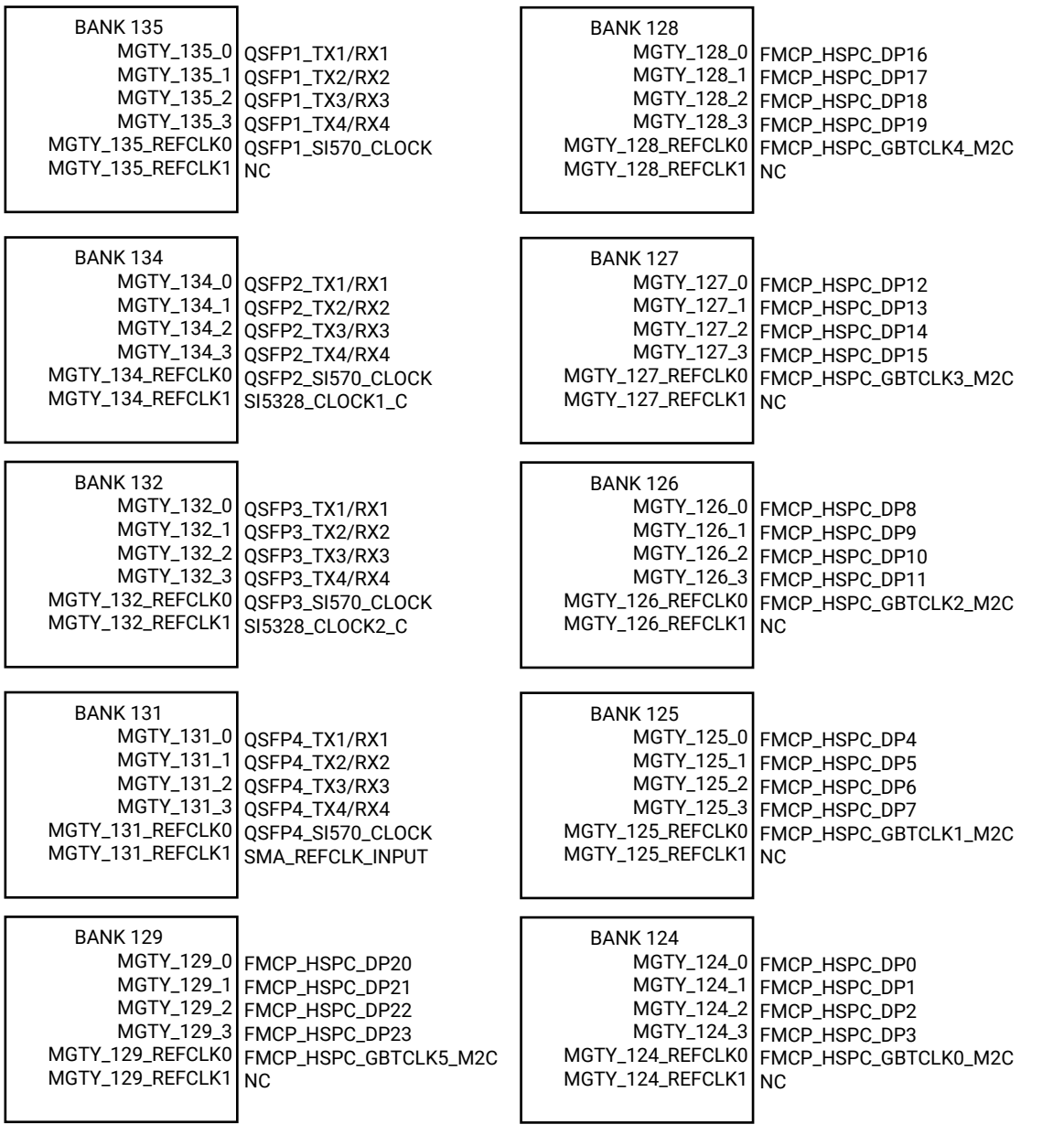
Quad 124

- MGTREFCLK0 – FMCP_HSPC_GBTCLK0_M2C_P/N
- NC

- Four GTY transceivers allocated to FMCP_HSPC_DP[0:3]

The XCVU37P right-side GTY transceiver interface assignments are shown in the following figure.

Figure 20: **XCVU37P Right-side GTY Transceiver Assignments**



Right-side GTY Transceiver Connectivity

The following tables list the connectivity of the ten XCVU37P FPGA U1 right-side GTY transceivers.

Table 12: **XCVU37P U1 GTY Transceiver Bank 135 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 135	G48	MGTYTXP0_135	QSFP1_TX1_P	36	TX1P	QSFP1 J42
	G49	MGTYTXN0_135	QSFP1_TX1_N	37	TX1N	
	G53	MGTYRXP0_135	QSFP1_RX1_P	17	RX1P	
	G54	MGTYRXN0_135	QSFP1_RX1_N	18	RX1N	
	E48	MGTYTXP1_135	QSFP1_TX2_P	3	TX2P	
	E49	MGTYTXN1_135	QSFP1_TX2_N	2	TX2N	
	F51	MGTYRXP1_135	QSFP1_RX2_P	22	RX2P	
	F52	MGTYRXN1_135	QSFP1_RX2_N	21	RX2N	
	C48	MGTYTXP2_135	QSFP1_TX3_P	33	TX3P	
	C49	MGTYTXN2_135	QSFP1_TX3_N	34	TX3N	
	E53	MGTYRXP2_135	QSFP1_RX3_P	14	RX3P	
	E54	MGTYRXN2_135	QSFP1_RX3_N	15	RX3N	
	A49	MGTYTXP3_135	QSFP1_TX4_P	6	TX4P	
	A50	MGTYTXN3_135	QSFP1_TX4_N	5	TX4N	
	D51	MGTYRXP3_135	QSFP1_RX4_P	25	RX4P	
	D52	MGTYRXN3_135	QSFP1_RX4_N	24	RX4N	
	P42	MGTREFCLK0P_135	QSFP_SI570_CLOCK_P[1]	4	OUT	U95 SI570 I2C prog. osc.
	P43	MGTREFCLK0N_135	QSFP_SI570_CLOCK_N[1]	5	OUT_B	
	M42	MGTREFCLK1P_135	NC	NC	NC	NC
	M43	MGTREFCLK1N_135				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 13: **XCVU37P U1 GTY Transceiver Bank 134 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 134	L48	MGTYTXP0_134	QSFP2_TX1_P	36	TX1P	
	L49	MGTYTXN0_134	QSFP2_TX1_N	37	TX1N	
	L53	MGTYRXP0_134	QSFP2_RX1_P	17	RX1P	
	L54	MGTYRXN0_134	QSFP2_RX1_N	18	RX1N	
	L44	MGTYTXP1_134	QSFP2_TX2_P	3	TX2P	
	L45	MGTYTXN1_134	QSFP2_TX2_N	2	TX2N	
	K51	MGTYRXP1_134	QSFP2_RX2_P	22	RX2P	
	K52	MGTYRXN1_134	QSFP2_RX2_N	21	RX2N	
	K46	MGTYTXP2_134	QSFP2_TX3_P	33	TX3P	
	K47	MGTYTXN2_134	QSFP2_TX3_N	34	TX3N	
	J53	MGTYRXP2_134	QSFP2_RX3_P	14	RX3P	
	J54	MGTYRXN2_134	QSFP2_RX3_N	15	RX3N	
	J48	MGTYTXP3_134	QSFP2_TX4_P	6	TX4P	
	J49	MGTYTXN3_134	QSFP2_TX4_N	5	TX4N	
	H51	MGTYRXP3_134	QSFP2_RX4_P	25	RX4P	
	H52	MGTYRXN3_134	QSFP2_RX4_N	24	RX4N	
	T42	MGTREFCLK0P_134	QSFP2_SI570_CLOCK_P[1]	4	OUT	U90 SI570 I2C prog. osc.
	T43	MGTREFCLK0N_134	QSFP2_SI570_CLOCK_N[1]	5	OUT_B	
	R40	MGTREFCLK1P_134	SI5328_CLOCK1_C_P[1]	28	CKOUT1_P	U87 SI5328B jitter atten.
	R41	MGTREFCLK1N_134	SI5328_CLOCK1_C_N[1]	29	CKOUT1_N	

Notes:

1. Series 0.01 µF capacitor coupled.

Table 14: **XCVU37P U1 GTY Transceiver Bank 132 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 132	V46	MGTYTXP0_132	QSFP3_TX1_P	36	TX1P	QSFP2 J35
	V47	MGTYTXN0_132	QSFP3_TX1_N	37	TX1N	
	U53	MGTYRXP0_132	QSFP3_RX1_P	17	RX1P	
	U54	MGTYRXN0_132	QSFP3_RX1_N	18	RX1N	
	U44	MGTYTXP1_132	QSFP3_TX2_P	3	TX2P	
	U45	MGTYTXN1_132	QSFP3_TX2_N	2	TX2N	
	U49	MGTYRXP1_132	QSFP3_RX2_P	22	RX2P	
	U50	MGTYRXN1_132	QSFP3_RX2_N	21	RX2N	
	T46	MGTYTXP2_132	QSFP3_TX3_P	33	TX3P	
	T47	MGTYTXN2_132	QSFP3_TX3_N	34	TX3N	
	T51	MGTYRXP2_132	QSFP3_RX3_P	14	RX3P	
	T52	MGTYRXN2_132	QSFP3_RX3_N	15	RX3N	
	R44	MGTYTXP3_132	QSFP3_TX4_P	6	TX4P	
	R45	MGTYTXN3_132	QSFP3_TX4_N	5	TX4N	
	R53	MGTYRXP3_132	QSFP3_RX4_P	25	RX4P	
	R54	MGTYRXN3_132	QSFP3_RX4_N	24	RX4N	
	Y42	MGTREFCLK0P_132	QSFP3_SI570_CLOCK_P [1]	4	OUT	U82 SI570 I2C prog. osc.
	Y43	MGTREFCLK0N_132	QSFP3_SI570_CLOCK_N[1]	5	OUT_B	
	W40	MGTREFCLK1P_132	SI5328_CLOCK2_C_P[1]	35	CKOUT2_P	U87 SI5328B jitter atten.
	W41	MGTREFCLK1N_132	SI5328_CLOCK2_C_N[1]	34	CKOUT2_N	

Notes:

1. Series 0.01 µF capacitor coupled.

Table 15: **XCVU37P U1 GTY Transceiver Bank 131 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 131	AA44	MGTYTXP0_131	QSFP4_TX1_P	36	TX1P	QSFP2 J32
	AA45	MGTYTXN0_131	QSFP4_TX1_N	37	TX1N	
	AA53	MGTYRXP0_131	QSFP4_RX1_P	17	RX1P	
	AA54	MGTYRXN0_131	QSFP4_RX1_N	18	RX1N	
	Y46	MGTYTXP1_131	QSFP4_TX2_P	3	TX2P	
	Y47	MGTYTXN1_131	QSFP4_TX2_N	2	TX2N	
	Y51	MGTYRXP1_131	QSFP4_RX2_P	22	RX2P	
	Y52	MGTYRXN1_131	QSFP4_RX2_N	21	RX2N	
	W48	MGTYTXP2_131	QSFP4_TX3_P	33	TX3P	
	W49	MGTYTXN2_131	QSFP4_TX3_N	34	TX3N	
	W53	MGTYRXP2_131	QSFP4_RX3_P	14	RX3P	
	W54	MGTYRXN2_131	QSFP4_RX3_N	15	RX3N	
	W44	MGTYTXP3_131	QSFP4_TX4_P	6	TX4P	
	W45	MGTYTXN3_131	QSFP4_TX4_N	5	TX4N	
	V51	MGTYRXP3_131	QSFP4_RX4_P	25	RX4P	
	V52	MGTYRXN3_131	QSFP4_RX4_N	24	RX4N	
	AB42	MGTREFCLK0P_131	QSFP4_SI570_CLOCK_P[1]	4	OUT	U80 SI570 I2C prog. osc.
	AB43	MGTREFCLK0N_131	QSFP4_SI570_CLOCK_N[1]	5	OUT_B	
	AA40	MGTREFCLK1P_131	SMA_REFCLK_INPUT_P[1]	1	SIG	SMA J24 (P) SMA J26 (N)
	AA41	MGTREFCLK1N_131	SMA_REFCLK_INPUT_N[1]	1	SIG	

Notes:

1. Series 0.01 µF capacitor coupled.

Table 16: **XCVU37P U1 GTY Transceiver Bank 129 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 129	AG48	MGTYTXP0_129	FMCP_HSPC_DP20_C2M_P	Z8	DP20_C2M_P	FMCP HSPC J18
	AG49	MGTYTXN0_129	FMCP_HSPC_DP20_C2M_N	Z9	DP20_C2M_N	
	AG53	MGTYRXP0_129	FMCP_HSPC_DP20_M2C_P	M14	DP20_M2C_P	
	AG54	MGTYRXN0_129	FMCP_HSPC_DP20_M2C_N	M15	DP20_M2C_N	
	AG44	MGTYTXP1_129	FMCP_HSPC_DP21_C2M_P	Y6	DP21_C2M_P	
	AG45	MGTYTXN1_129	FMCP_HSPC_DP21_C2M_N	Y7	DP21_C2M_N	
	AF51	MGTYRXP1_129	FMCP_HSPC_DP21_M2C_P	M10	DP21_M2C_P	
	AF52	MGTYRXN1_129	FMCP_HSPC_DP21_M2C_N	M11	DP21_M2C_N	
	AF46	MGTYTXP2_129	FMCP_HSPC_DP22_C2M_P	Z4	DP22_C2M_P	
	AF47	MGTYTXN2_129	FMCP_HSPC_DP22_C2M_N	Z5	DP22_C2M_N	
	AE53	MGTYRXP2_129	FMCP_HSPC_DP22_M2C_P	M6	DP22_M2C_P	
	AE54	MGTYRXN2_129	FMCP_HSPC_DP22_M2C_N	M7	DP22_M2C_N	
	AE44	MGTYTXP3_129	FMCP_HSPC_DP23_C2M_P	Y2	DP23_C2M_P	
	AE45	MGTYTXN3_129	FMCP_HSPC_DP23_C2M_N	Y3	DP23_C2M_N	
	AE49	MGTYRXP3_129	FMCP_HSPC_DP23_M2C_P	M2	DP23_M2C_P	
	AE50	MGTYRXN3_129	FMCP_HSPC_DP23_M2C_N	M3	DP23_M2C_N	
	AG40	MGTREFCLK0P_129	FMCP_HSPC_GBTCLK5_M2C_P[1]	Z20	GBTCLK5_M2C_P	
	AG41	MGTREFCLK0N_129	FMCP_HSPC_GBTCLK5_M2C_N[1]	Z21	GBTCLK5_M2C_N	
	AF42	MGTREFCLK1P_129	NC	NC	NC	NC
	AF43	MGTREFCLK1N_129				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 17: **XCVU37P U1 GTY Transceiver Bank 128 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 128	AK46	MGTYTXP0_128	FMCP_HSPC_DP16_C2M_P	M26	DP16_C2M_P	FMCP HSPC J18
	AK47	MGTYTXN0_128	FMCP_HSPC_DP16_C2M_N	M27	DP16_C2M_N	
	AL49	MGTYRXP0_128	FMCP_HSPC_DP16_M2C_P	Z32	DP16_M2C_P	
	AL50	MGTYRXN0_128	FMCP_HSPC_DP16_M2C_N	Z33	DP16_M2C_N	
	AJ48	MGTYTXP1_128	FMCP_HSPC_DP17_C2M_P	M30	DP17_C2M_P	
	AJ49	MGTYTXN1_128	FMCP_HSPC_DP17_C2M_N	M31	DP17_C2M_N	
	AK51	MGTYRXP1_128	FMCP_HSPC_DP17_M2C_P	Y34	DP17_M2C_P	
	AK52	MGTYRXN1_128	FMCP_HSPC_DP17_M2C_N	Y35	DP17_M2C_N	
	AJ44	MGTYTXP2_128	FMCP_HSPC_DP18_C2M_P	M34	DP18_C2M_P	
	AJ45	MGTYTXN2_128	FMCP_HSPC_DP18_C2M_N	M35	DP18_C2M_N	
	AJ53	MGTYRXP2_128	FMCP_HSPC_DP18_M2C_P	Z36	DP18_M2C_P	
	AJ54	MGTYRXN2_128	FMCP_HSPC_DP18_M2C_N	Z37	DP18_M2C_N	
	AH46	MGTYTXP3_128	FMCP_HSPC_DP19_C2M_P	M38	DP19_C2M_P	
	AH47	MGTYTXN3_128	FMCP_HSPC_DP19_C2M_N	M39	DP19_C2M_N	
	AH51	MGTYRXP3_128	FMCP_HSPC_DP19_M2C_P	Y38	DP19_M2C_P	
	AH52	MGTYRXN3_128	FMCP_HSPC_DP19_M2C_N	Y39	DP19_M2C_N	
	AJ40	MGTREFCLK0P_128	FMCP_HSPC_GBTCLK4_M2C_P[1]	L4	GBTCLK4_M2C_P	
	AJ41	MGTREFCLK0N_128	FMCP_HSPC_GBTCLK4_M2C_N [1]	L5	GBTCLK4_M2C_N	
	AH42	MGTREFCLK1P_128	NC	NC	NC	NC
	AH43	MGTREFCLK1N_128				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 18: **XCVU37P U1 GTY Transceiver Bank 127 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 127	AP46	MGTYTXP0_127	FMCP_HSPC_DP12_C2M_P	Z28	DP12_C2M_P	FMCP HSPC J18
	AP47	MGTYTXN0_127	FMCP_HSPC_DP12_C2M_N	Z29	DP12_C2M_N	
	AN53	MGTYRXP0_127	FMCP_HSPC_DP12_M2C_P	Y14	DP12_M2C_P	
	AN54	MGTYRXN0_127	FMCP_HSPC_DP12_M2C_N	Y15	DP12_M2C_N	
	AN44	MGTYTXP1_127	FMCP_HSPC_DP13_C2M_P	Y30	DP13_C2M_P	
	AN45	MGTYTXN1_127	FMCP_HSPC_DP13_C2M_N	Y31	DP13_C2M_N	
	AN49	MGTYRXP1_127	FMCP_HSPC_DP13_M2C_P	Z16	DP13_M2C_P	
	AN50	MGTYRXN1_127	FMCP_HSPC_DP13_M2C_N	Z17	DP13_M2C_N	
	AM46	MGTYTXP2_127	FMCP_HSPC_DP14_C2M_P	M18	DP14_C2M_P	
	AM47	MGTYTXN2_127	FMCP_HSPC_DP14_C2M_N	M19	DP14_C2M_N	
	AM51	MGTYRXP2_127	FMCP_HSPC_DP14_M2C_P	Y18	DP14_M2C_P	
	AM52	MGTYRXN2_127	FMCP_HSPC_DP14_M2C_N	Y19	DP14_M2C_N	
	AL44	MGTYTXP3_127	FMCP_HSPC_DP15_C2M_P	M22	DP15_C2M_P	
	AL45	MGTYTXN3_127	FMCP_HSPC_DP15_C2M_N	M23	DP15_C2M_N	
	AL53	MGTYRXP3_127	FMCP_HSPC_DP15_M2C_P	Y22	DP15_M2C_P	
	AL54	MGTYRXN3_127	FMCP_HSPC_DP15_M2C_N	Y23	DP15_M2C_N	
	AL40	MGTREFCLK0P_127	FMCP_HSPC_GBTCLK3_M2C_P[1]	L8	GBTCLK3_M2C_P	
	AL41	MGTREFCLK0N_127	FMCP_HSPC_GBTCLK3_M2C_N[1]	L9	GBTCLK3_M2C_N	
	AK42	MGTREFCLK1P_127	NC	NC	NC	NC
	AK43	MGTREFCLK1N_127				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 19: **XCVU37P U1 GTY Transceiver Bank 126 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 126	AU48	MGTYTXP0_126	FMCP_HSPC_DP8_C2M_P	B28	DP8_C2M_P	FMCP HSPC J18
	AU49	MGTYTXN0_126	FMCP_HSPC_DP8_C2M_N	B29	DP8_C2M_N	
	AU53	MGTYRXP0_126	FMCP_HSPC_DP8_M2C_P	B8	DP8_M2C_P	
	AU54	MGTYRXN0_126	FMCP_HSPC_DP8_M2C_N	B9	DP8_M2C_N	
	AT46	MGTYTXP1_126	FMCP_HSPC_DP9_C2M_P	B24	DP9_C2M_P	
	AT47	MGTYTXN1_126	FMCP_HSPC_DP9_C2M_N	B25	DP9_C2M_N	
	AT51	MGTYRXP1_126	FMCP_HSPC_DP9_M2C_P	B4	DP9_M2C_P	
	AT52	MGTYRXN1_126	FMCP_HSPC_DP9_M2C_N	B5	DP9_M2C_N	
	AR48	MGTYTXP2_126	FMCP_HSPC_DP10_C2M_P	Z24	DP10_C2M_P	
	AR49	MGTYTXN2_126	FMCP_HSPC_DP10_C2M_N	Z25	DP10_C2M_N	
	AR53	MGTYRXP2_126	FMCP_HSPC_DP10_M2C_P	Y10	DP10_M2C_P	
	AR54	MGTYRXN2_126	FMCP_HSPC_DP10_M2C_N	Y11	DP10_M2C_N	
	AR44	MGTYTXP3_126	FMCP_HSPC_DP11_C2M_P	Y26	DP11_C2M_P	
	AR45	MGTYTXN3_126	FMCP_HSPC_DP11_C2M_N	Y27	DP11_C2M_N	
	AP51	MGTYRXP3_126	FMCP_HSPC_DP11_M2C_P	Z12	DP11_M2C_P	
	AP52	MGTYRXN3_126	FMCP_HSPC_DP11_M2C_N	Z13	DP11_M2C_N	
	AN40	MGTREFCLK0P_126	FMCP_HSPC_GBTCLK2_M2C_P[1]	L12	GBTCLK2_M2C_P	
	AN41	MGTREFCLK0N_126	FMCP_HSPC_GBTCLK2_M2C_N1	L13	GBTCLK2_M2C_N	
	AM42	MGTREFCLK1P_126	NC	NC	NC	NC
	AM43	MGTREFCLK1N_126				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 20: **XCVU37P U1 GTY Transceiver Bank 125 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY bank 125	AY46	MGTYTXP0_125	FMCP_HSPC_DP4_C2M_P	A34	DP4_C2M_P	FMCP HSPC J18
	AY47	MGTYTXN0_125	FMCP_HSPC_DP4_C2M_N	A35	DP4_C2M_N	
	AY51	MGTYRXP0_125	FMCP_HSPC_DP4_M2C_P	A14	DP4_M2C_P	
	AY52	MGTYRXN0_125	FMCP_HSPC_DP4_M2C_N	A15	DP4_M2C_N	
	AW44	MGTYTXP1_125	FMCP_HSPC_DP5_C2M_P	A38	DP5_C2M_P	
	AW45	MGTYTXN1_125	FMCP_HSPC_DP5_C2M_N	A39	DP5_C2M_N	
	AW53	MGTYRXP1_125	FMCP_HSPC_DP5_M2C_P	A18	DP5_M2C_P	
	AW54	MGTYRXN1_125	FMCP_HSPC_DP5_M2C_N	A19	DP5_M2C_N	
	AV46	MGTYTXP2_125	FMCP_HSPC_DP6_C2M_P	B36	DP6_C2M_P	
	AV47	MGTYTXN2_125	FMCP_HSPC_DP6_C2M_N	B37	DP6_C2M_N	
	AW49	MGTYRXP2_125	FMCP_HSPC_DP6_M2C_P	B16	DP6_M2C_P	
	AW50	MGTYRXN2_125	FMCP_HSPC_DP6_M2C_N	B17	DP6_M2C_N	
	AU44	MGTYTXP3_125	FMCP_HSPC_DP7_C2M_P	B32	DP7_C2M_P	
	AU45	MGTYTXN3_125	FMCP_HSPC_DP7_C2M_N	B33	DP7_C2M_N	
	AV51	MGTYRXP3_125	FMCP_HSPC_DP7_M2C_P	B12	DP7_M2C_P	
	AV52	MGTYRXN3_125	FMCP_HSPC_DP7_M2C_N	B13	DP7_M2C_N	
	AR40	MGTREFCLK0P_125	FMCP_HSPC_GBTCLK1_M2C_P[1]	B20	GBTCLK1_M2C_P	
	AR41	MGTREFCLK0N_125	FMCP_HSPC_GBTCLK1_M2C_N[1]	B21	GBTCLK1_M2C_N	
	AP42	MGTREFCLK1P_125	NC	NC	NC	NC
	AP43	MGTREFCLK1N_125				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 21: **XCVU37P U1 GTY Transceiver Bank 124 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 124	BC48	MGTYTXP0_124	FMCP_HSPC_DP0_C2M_P	C2	DP0_C2M_P	FMCP HSPC J18
	BC49	MGTYTXN0_124	FMCP_HSPC_DP0_C2M_N	C3	DP0_C2M_N	
	BC53	MGTYRXP0_124	FMCP_HSPC_DP0_M2C_P	C6	DP0_M2C_P	
	BC54	MGTYRXN0_124	FMCP_HSPC_DP0_M2C_N	C7	DP0_M2C_N	
	BC44	MGTYTXP1_124	FMCP_HSPC_DP1_C2M_P	A22	DP1_C2M_P	
	BC45	MGTYTXN1_124	FMCP_HSPC_DP1_C2M_N	A23	DP1_C2M_N	
	BB51	MGTYRXP1_124	FMCP_HSPC_DP1_M2C_P	A2	DP1_M2C_P	
	BB52	MGTYRXN1_124	FMCP_HSPC_DP1_M2C_N	A3	DP1_M2C_N	
	BB46	MGTYTXP2_124	FMCP_HSPC_DP2_C2M_P	A26	DP2_C2M_P	
	BB47	MGTYTXN2_124	FMCP_HSPC_DP2_C2M_N	A27	DP2_C2M_N	
	BA53	MGTYRXP2_124	FMCP_HSPC_DP2_M2C_P	A6	DP2_M2C_P	
	BA54	MGTYRXN2_124	FMCP_HSPC_DP2_M2C_N	A7	DP2_M2C_N	
	BA44	MGTYTXP3_124	FMCP_HSPC_DP3_C2M_P	A30	DP3_C2M_P	
	BA45	MGTYTXN3_124	FMCP_HSPC_DP3_C2M_N	A31	DP3_C2M_N	
	BA49	MGTYRXP3_124	FMCP_HSPC_DP3_M2C_P	A10	DP3_M2C_P	
	BA50	MGTYRXN3_124	FMCP_HSPC_DP3_M2C_N	A11	DP3_M2C_N	
	AV42	MGTREFCLK0P_124	FMCP_HSPC_GBTCLK0_M2C_P[1]	D4	GBTCLK0_M2C_P	
	AV43	MGTREFCLK0N_124	FMCP_HSPC_GBTCLK0_M2C_N[1]	D5	GBTCLK0_M2C_N	
	AT42	MGTREFCLK1P_124	NC	NC	NC	NC
	AT43	MGTREFCLK1N_124				

Notes:

1. Series 0.01 µF capacitor coupled.

Left-side Quads

The four connected GTY Quads on the left side of the XCVU37P FPGA are described in this section (MGTY235- MGTY228 are not used).

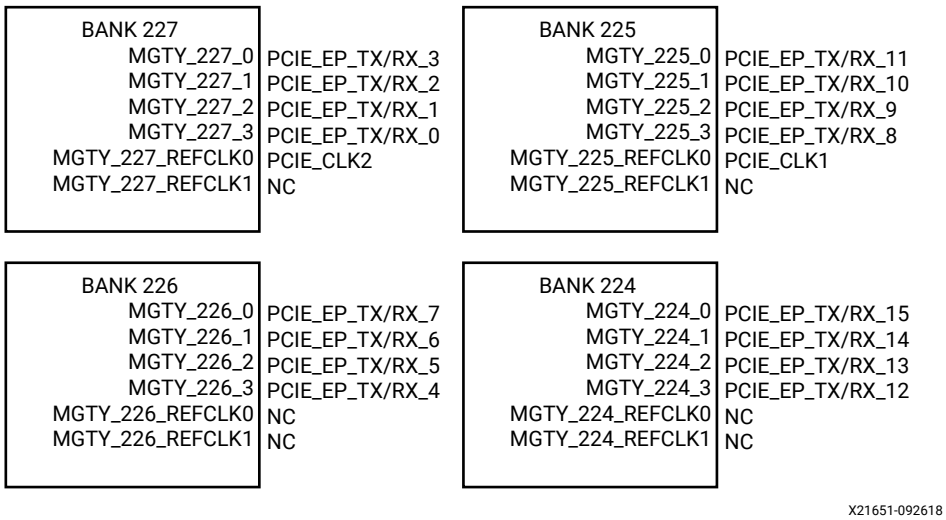
- Quad 227
  - MGTREFCLK0 - PCIE_CLK2_P/N (U94)
  - MGTREFCLK1 - not connected
  - Four GTY transceivers allocated to PCIe lanes 3:0 PCIE_EP_TX/RX[3:0]
- Quad 226
  - MGTREFCLK0 - not connected
  - MGTREFCLK1 - not connected

- Four GTY transceivers allocated to PCIe lanes 7:4 PCIE_EP_TX/RX[7:4]

- Quad 225
  - MGTREFCLK0 - PCIE_CLK1_P/N (U94)
  - MGTREFCLK1 - not connected
  - Four GTY transceivers allocated to PCIe lanes 11:8 PCIE_EP_TX/RX[11:8]
- Quad 224
  - MGTREFCLK0 - not connected
  - MGTREFCLK1 - not connected
  - Four GTY transceivers allocated to PCIe lanes 15:12 PCIE_EP_TX/RX[15:12]

The XCVU37P left-side GTY transceiver interface assignments are shown in the following figure.

Figure 21: **XCVU37P Left-side GTY Transceiver Assignments**



Left-side GTY Transceiver Connectivity

The following tables list the XCVU37P FPGA U1 GTY transceiver banks 227, 226, 225, and 224 connections, respectively.

For additional information on GTY transceivers, see the *UltraScale Architecture GTY Transceivers User Guide* (UG578). Also see the *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182). For additional information about the quad small form factor pluggable (28 Gb/s QSFP28) module, see the SFF-8663 and SFF-8679 specifications for the 28 Gb/s QSFP+ at the SNIA Technology Affiliates website.

Table 22: **XCVU37P U1 GTY Transceiver Bank 227 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name TX[1]	Connected Pin	Connected Pin Name	Connected Device
GTY bank 227	AP9	MGTYTXP0_227	PCIE_EP_TX3_P	A29	PERP3	PCIE 16-lane edge conn. P1
	AP8	MGTYTXN0_227	PCIE_EP_TX3_N	A30	PERN3	
	AN2	MGTYRXP0_227	PCIE_EP_RX3_P	B27	PETP3	
	AN1	MGTYRXN0_227	PCIE_EP_RX3_N	B28	PETN3	
	AN11	MGTYTXP1_227	PCIE_EP_TX2_P	A25	PERP2	
	AN10	MGTYTXN1_227	PCIE_EP_TX2_N	A26	PERN2	
	AN6	MGTYRXP1_227	PCIE_EP_RX2_P	B23	PETP2	
	AN5	MGTYRXN1_227	PCIE_EP_RX2_N	B24	PETN2	
	AM9	MGTYTXP2_227	PCIE_EP_TX1_P	A21	PERP1	
	AM8	MGTYTXN2_227	PCIE_EP_TX1_N	A22	PERN1	
	AM4	MGTYRXP2_227	PCIE_EP_RX1_P	B19	PETP1	
	AM3	MGTYRXN2_227	PCIE_EP_RX1_N	B20	PETN1	
	AL11	MGTYTXP3_227	PCIE_EP_TX0_P	A16	PERP0	
	AL10	MGTYTXN3_227	PCIE_EP_TX0_N	A17	PERN0	
	AL2	MGTYRXP3_227	PCIE_EP_RX0_P	B14	PETP0	
	AL1	MGTYRXN3_227	PCIE_EP_RX0_N	B15	PETN0	
	AL15	MGTREFCLK0P_227	PCIE_CLK2_P[1]	3	Q1	ICS85411A U94 clock buffer
	AL14	MGTREFCLK0N_227	PCIE_CLK2_N[1]	4	NQ1	
	AK13	MGTREFCLK1P_227	NC	NC	NC	NC
	AK12	MGTREFCLK1N_227				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 23: **XCVU37P U1 GTY Transceiver Bank 226 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name TX[1]	Connected Pin	Connected Pin Name	Connected Device
GTY bank 226	AU11	MGTYTXP0_226	PCIE_EP_TX7_P	A47	PERP7	PCIE 16-lane edge conn. P1
	AU10	MGTYTXN0_226	PCIE_EP_TX7_N	A48	PERN7	
	AU2	MGTYRXP0_226	PCIE_EP_RX7_P	B45	PETP7	
	AU1	MGTYRXN0_226	PCIE_EP_RX7_N	B46	PETN7	
	AT9	MGTYTXP1_226	PCIE_EP_TX6_P	A43	PERP6	
	AT8	MGTYTXN1_226	PCIE_EP_TX6_N	A44	PERN6	
	AT4	MGTYRXP1_226	PCIE_EP_RX6_P	B41	PETP6	
	AT3	MGTYRXN1_226	PCIE_EP_RX6_N	B42	PETN6	
	AR7	MGTYTXP2_226	PCIE_EP_TX5_P	A39	PERP5	
	AR6	MGTYTXN2_226	PCIE_EP_TX5_N	A40	PERN5	
	AR2	MGTYRXP2_226	PCIE_EP_RX5_P	B37	PETP5	
	AR1	MGTYRXN2_226	PCIE_EP_RX5_N	B38	PETN5	
	AR11	MGTYTXP3_226	PCIE_EP_TX4_P	A35	PERP4	
	AR10	MGTYTXN3_226	PCIE_EP_TX4_N	A36	PERN4	
	AP4	MGTYRXP3_226	PCIE_EP_RX4_P	B33	PETP4	
	AP3	MGTYRXN3_226	PCIE_EP_RX4_N	B34	PETN4	
	AN15	MGTREFCLK0P_226	NC	NC	NC	NC
	AN14	MGTREFCLK0N_226				
	AM13	MGTREFCLK1P_226	NC	NC	NC	NC
	AM12	MGTREFCLK1N_226				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 24: **XCVU37P U1 GTY Transceiver Bank 225 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name TX	Connected Pin	Connected Pin Name	Connected Device
GTY bank 225	AY9	MGTYTXP0_225	PCIE_EP_TX11_P	A64	PERP11	PCIE 16-lane edge conn. P1
	AY8	MGTYTXN0_225	PCIE_EP_TX11_N	A65	PERN11	
	AY4	MGTYRXP0_225	PCIE_EP_RX11_P	B62	PETP11	
	AY3	MGTYRXN0_225	PCIE_EP_RX11_N	B63	PETN11	
	AW11	MGTYTXP1_225	PCIE_EP_TX10_P	A60	PERP10	
	AW10	MGTYTXN1_225	PCIE_EP_TX10_N	A61	PERN10	
	AW2	MGTYRXP1_225	PCIE_EP_RX10_P	B58	PETP10	
	AW1	MGTYRXN1_225	PCIE_EP_RX10_N	B59	PETN10	
	AV9	MGTYTXP2_225	PCIE_EP_TX9_P	A56	PERP9	
	AV8	MGTYTXN2_225	PCIE_EP_TX9_N	A57	PERN9	
	AW6	MGTYRXP2_225	PCIE_EP_RX9_P	B54	PETP9	
	AW5	MGTYRXN2_225	PCIE_EP_RX9_N	B55	PETN9	
	AU7	MGTYTXP3_225	PCIE_EP_TX8_P	A52	PERP8	
	AU6	MGTYTXN3_225	PCIE_EP_TX8_N	A53	PERN8	
	AV4	MGTYRXP3_225	PCIE_EP_RX8_P	B50	PETP8	
	AV3	MGTYRXN3_225	PCIE_EP_RX8_N	B51	PETN8	
	AR15	MGTREFCLK0P_225	PCIE_CLK1_P[1]	1	Q0	ICS85411A U94 clock buffer
	AR14	MGTREFCLK0N_225	PCIE_CLK1_N[1]	2	NQ0	
	AP13	MGTREFCLK1P_225	NC	NC	NC	NC
	AP12	MGTREFCLK1N_225				

Notes:

1. Series 0.01 µF capacitor coupled.

Table 25: **XCVU37P U1 GTY Transceiver Bank 224 Connections**

MGT bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name TX	Connected Pin	Connected Pin Name	Connected device
GTY bank 224	BC7	MGTYTXP0_224	PCIE_TX15_P	A80	PERP15	PCIE 16-lane edge conn. P1
	BC6	MGTYTXN0_224	PCIE_TX15_N	A81	PERN15	
	BC2	MGTYRXP0_224	PCIE_RX15_P	B78	PETP15	
	BC1	MGTYRXN0_224	PCIE_RX15_N	B79	PETN15	
	BC11	MGTYTXP1_224	PCIE_TX14_P	A76	PERP14	
	BC10	MGTYTXN1_224	PCIE_TX14_N	A77	PERN14	
	BB4	MGTYRXP1_224	PCIE_RX14_P	B74	PETP14	
	BB3	MGTYRXN1_224	PCIE_RX14_N	B75	PETN14	
	BB9	MGTYTXP2_224	PCIE_TX13_P	A72	PERP13	
	BB8	MGTYTXN2_224	PCIE_TX13_N	A73	PERN13	
	BA2	MGTYRXP2_224	PCIE_RX13_P	B70	PETP13	
	BA1	MGTYRXN2_224	PCIE_RX13_N	B71	PETN13	
	BA11	MGTYTXP3_224	PCIE_TX12_P	A68	PERP12	
	BA10	MGTYTXN3_224	PCIE_TX12_N	A69	PERN12	
	BA6	MGTYRXP3_224	PCIE_RX12_P	B66	PETP12	
	BA5	MGTYRXN3_224	PCIE_RX12_N	B67	PETN12	
	AV13	MGTREFCLK0P_224	NC	NC	NC	NC
	AV12	MGTREFCLK0N_224				
	AT13	MGTREFCLK1P_224	NC	NC	NC	NC
	AT12	MGTREFCLK1N_224				

Notes:

1. Series 0.01 µF capacitor coupled.

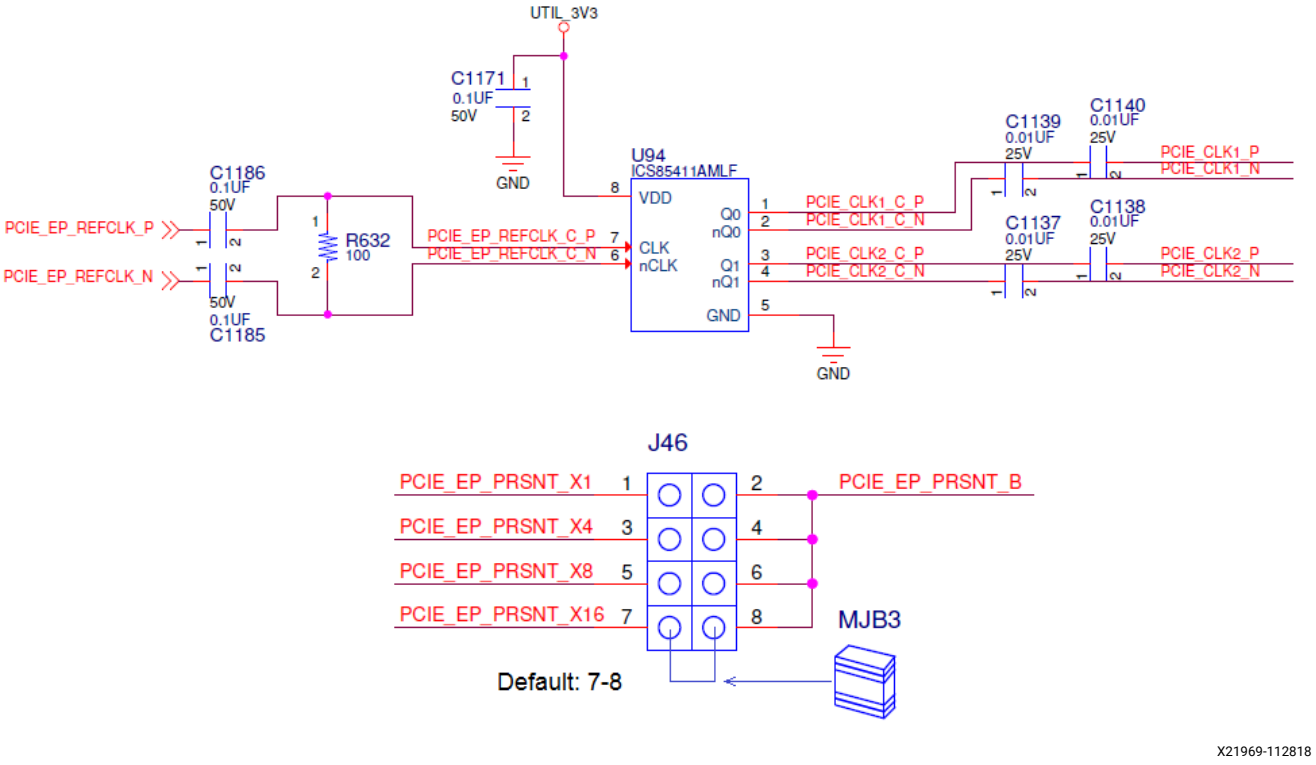
PCI Express Endpoint Connectivity

[Figure 2, callout 20]

The 16-lane PCI Express® edge connector P1 performs data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications, 8.0 GT/s for Gen3 applications and 16.0 GT/s for Gen4 applications. The PCIe® transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair.

The XCVU37P-2FSVH2892E (-2 speed grade) is deployed on the VCU128 to support up to Gen4 x8. User selectable as PCIe Gen3 x16 or dual Gen4 x8. The PCIe reference clock is input from the P1 edge connector. The PCIe clock is routed from P1 pin A16 (P) and pin A17 (N) to a 1-to-2 ICS85411A clock buffer U94. The Q0 output of U94 is wired to the GTY225 MGTHREFCLK0 input (see Table 24). The Q1 output of U94 is wired to the GTY227 MGTHREFCLK0 input (see Table 22). PCIe lane width/size is selected by jumper J46. The default lane size selection is 16-lane (J46 pins 7 and 8 jumpered). The 1-to-2 U94 PCIe clock buffer circuit and J46 lane size jumper are shown in the following figure.

Figure 22: **PCI Express Lane Clock Circuit and Size Select Jumper J46**



The tables in Left-side GTY Transceiver Connectivity list the PCIe P1 edge connector wiring to the XCVU37P FPGA U1 MGTY transceiver banks 227-224. The two PCIe P1 edge connector control signals PCIE_EP_WAKE (P1 pin B11) and PCIE_EP_PERST (P1 pin A11) are level-shifted by SN74AVC2T245 U70 and connected to the XCVU39P U1 bank 65 pin BJ42 and pin BF41, respectively. For additional information about UltraScale™ PCIe functionality, see the *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156). Additional information about the PCI Express standard is available on the PCI Express standard website.

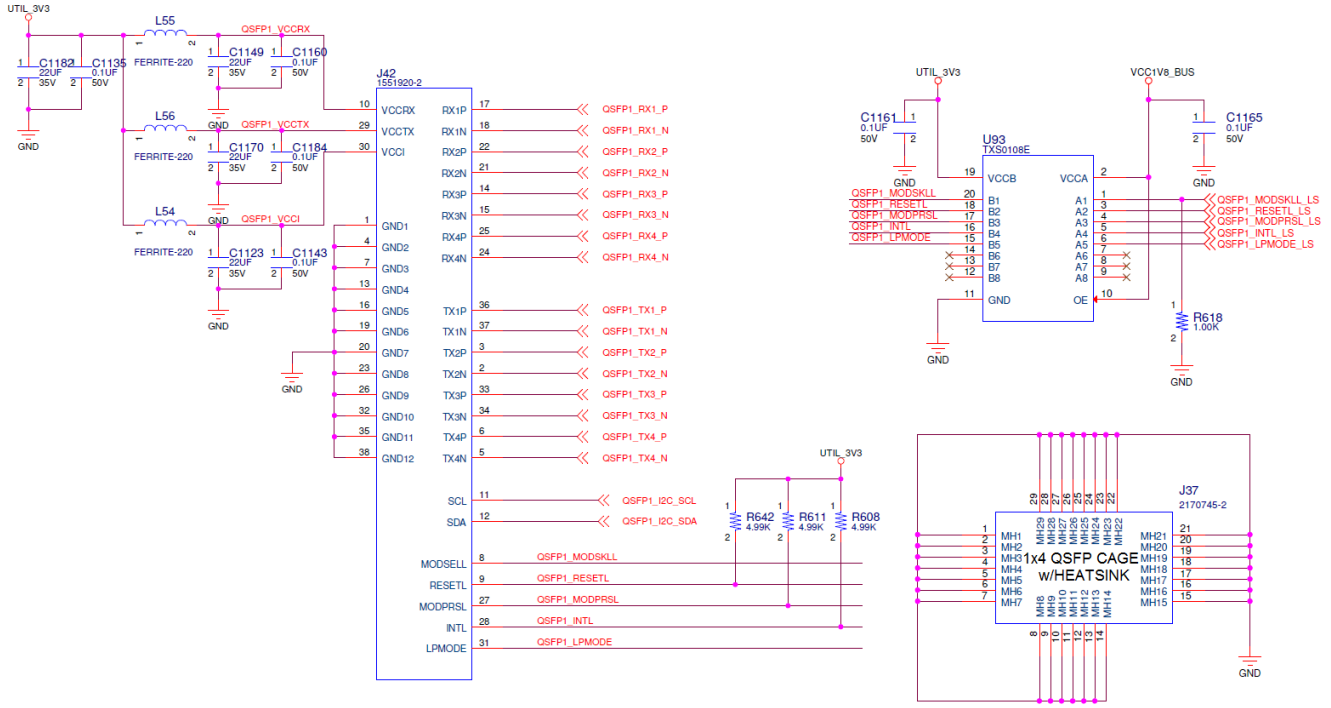
28 Gb/s zQSFP+ Module Connectors

[Figure 2, callout 19]

The VCU128 board hosts four QSFP28 small form-factor pluggable (28 Gb/s QSFP+) connectors: QSFP1 J42, QSFP2 J39, QSFP3 J35, and QSFP4 J32, which accept 28 Gb/s QSFP+ optical modules. The four connectors are housed within a single 1x4 ganged 28 Gb/s QSFP+ cage assembly J37. The following figure shows a typical implementation of the 28 Gb/s QSFP28 module connector circuitry.

Table 12 through Table 15 in Right-side GTY Transceiver Connectivity list the QSFP28 connections to the XCVU37P FPGA U1 MGTY transceiver banks 135 (QSFP1), 134 (QSFP2), 132 (QSFP3), and 131 (QSFP4).

Figure 23: **28 Gb/s QSFP28 Module Connector**



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QSFP28 Connections to Transceiver Banks 67 and 69

The following table lists the QSFP28 module level-shifted control signal connections to XCVU37P FPGA U1 bank 67 (QSFP1, QSFP4) and bank 69 (QSFP2, QSFP3).

Table 26: **XCVU37P U1 to QSFP28 Module Control and I2C Connections**

FPGA (U1) Pin	Schematic Net Name[1,2]	FPGA (U1) Direction	Module Pin Num	Module Pin Name
QSFP1 J42 (U1 bank 67)				
BM24	QSFP1_MODSKLL_LS	Output	8	MODSELL
BN25	QSFP1_RESETL_LS	Output	9	RESETL
BM25	QSFP1_MODPRSL_LS	Output	27	MODPRSL
BP24	QSFP1_INTL_LS	Input	28	INTL
BN24	QSFP1_LPMODE_LS	Output	31	LPMODE
U54.13	QSFP1_I2C_SDA	BiDir	12	SDA
U54.14	QSFP1_I2C_SCL	Output	11	SCL
QSFP2 J39 (U1 bank 69)				
BN5	QSFP2_MODSKLL_LS	Output	8	MODSELL
BN6	QSFP2_RESETL_LS	Output	9	RESETL
BN7	QSFP2_MODPRSL_LS	Output	27	MODPRSL
BP6	QSFP2_INTL_LS	Input	28	INTL
BP7	QSFP2_LPMODE_LS	Output	31	LPMODE
U54.15	QSFP2_I2C_SDA	BiDir	12	SDA
U54.16	QSFP2_I2C_SCL	Output	11	SCL
QSFP3 J35 (U1 bank 69)				
BM5	QSFP3_MODSKLL_LS	Output	8	MODSELL
BL6	QSFP3_RESETL_LS	Output	9	RESETL
BM7	QSFP3_MODPRSL_LS	Output	27	MODPRSL
BL7	QSFP3_INTL_LS	Input	28	INTL
BN4	QSFP3_LPMODE_LS	Output	31	LPMODE
U54.17	QSFP3_I2C_SDA	BiDir	12	SDA
U54.18	QSFP3_I2C_SCL	Output	11	SCL
QSFP4 J32 (U1 bank 67)				
BK23	QSFP4_MODSKLL_LS	Output	8	MODSELL
BK24	QSFP4_RESETL_LS	Output	9	RESETL
BL22	QSFP4_MODPRSL_LS	Output	27	MODPRSL
BH21	QSFP4_INTL_LS	Input	28	INTL
BH21	QSFP4_LPMODE_LS	Output	31	LPMODE
U54.19	QSFP4_I2C_SDA	BiDir	12	SDA

Table 26: **XCVU37P U1 to QSFP28 Module Control and I2C Connections** *(cont'd)*

FPGA (U1) Pin	Schematic Net Name[1,2]	FPGA (U1) Direction	Module Pin Num	Module Pin Name
U54.20	QSFP4_I2C_SCL	Output	11	SCL

Notes:

1. The QSFP28 connector control signals are level-shifted.
2. The four QSFP28 connector I2C SCL/SDA signals are connected via I2C switch U54 to the I2C1_SCL/SDA bus. See I2C Bus, Topology, and Switches section.

For additional information about the quad small form factor pluggable (28 Gb/s QSFP28) module, see the SFF-8663 and SFF-8679 specifications for the 28 Gb/s QSFP+ on the SNIA Technology Affiliates website.

10/100/1000 Mb/s Tri-speed Ethernet PHY

[Figure 2, callout 22]

The VCU128 evaluation board uses the TI PHY device DP83867ISRGZ (U62) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through RJ-45 connector P2, a Wurth 7499111221A with built-in magnetics and status LEDs. On power-up, or on reset, the PHY is configured to operate in SGMII mode with PHY address[4:0] = `00011`. The following table lists the FPGA U1 to U62 DP83867ISRGZ Ethernet PHY connections. This table also shows the net names for the connections from the FPGA to the Ethernet PHY. ENET_SGMII_IN correlates with the SGMII_TX ports in the FPGA design, and ENET_SGMII_OUT correlates with the SGMII_RX ports.

Table 27: **XCVC37P U1 to Ethernet PHY U62 Connections**

FPGA (U1) Pin	Net Name	I/O Standard	DP83867ISRGZ U62	
			Pin	Name
BG23	ENET_MDIO	LVCMOS18	17	MDIO
BN27	ENET_MDC	LVCMOS18	16	MDC
BF22	ENET_PDWN_B_I_INT_B_O	LVCMOS18	44	INT_PWDN
BH22	ENET_SGMII_IN_N	LVCMOS18	28	TX_D1_SGMII_SIP
BG22	ENET_SGMII_IN_P	LVCMOS18	27	TX_D0_SGMII_SIN
BJ21	ENET_SGMII_OUT_N	LVCMOS18	36	RX_D3_SGMII_SON
BH21	ENET_SGMII_OUT_P	LVCMOS18	35	RX_D2_SGMII_SOP
BK22	ENET_SGMII_CLK_N	LVCMOS18	34	RX_D1_SGMII_CON
BK23	ENET_SGMII_CLK_P	LVCMOS18	33	RX_D0_SGMII_COP
U65.10	GEM3_ENET_RESET_B	NA	43	RESET_B
BP27	ENET_COL_GPIO	LVCMOS18	39	GPIO_2
BJ23	ENET_CLKOUT	LVCMOS18	18	CLK_OUT

Ethernet PHY Status LEDs

[Figure 2, callout 23]

Two Ethernet PHY status LEDs are integrated into the metal frame of the P2 RJ-45 connector, installed on the top edge and towards the back of the VCU128 board. The two PHY status LEDs are visible within the frame of the RJ45 Ethernet jack as shown in the following figure. As viewed from the front opening, the left green LED is the link activity indicator and the right green LED is the 1000BASE-T link mode indicator.

Figure 24: **Ethernet PHY Status LEDs**

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A separate discrete LED on top of the board (DS19, near item 38 in Figure 2) indicates link established. Details about the tri-mode Ethernet MAC core are provided in the *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051). The TI DP83867ISRGZ data sheet is on the TI website.

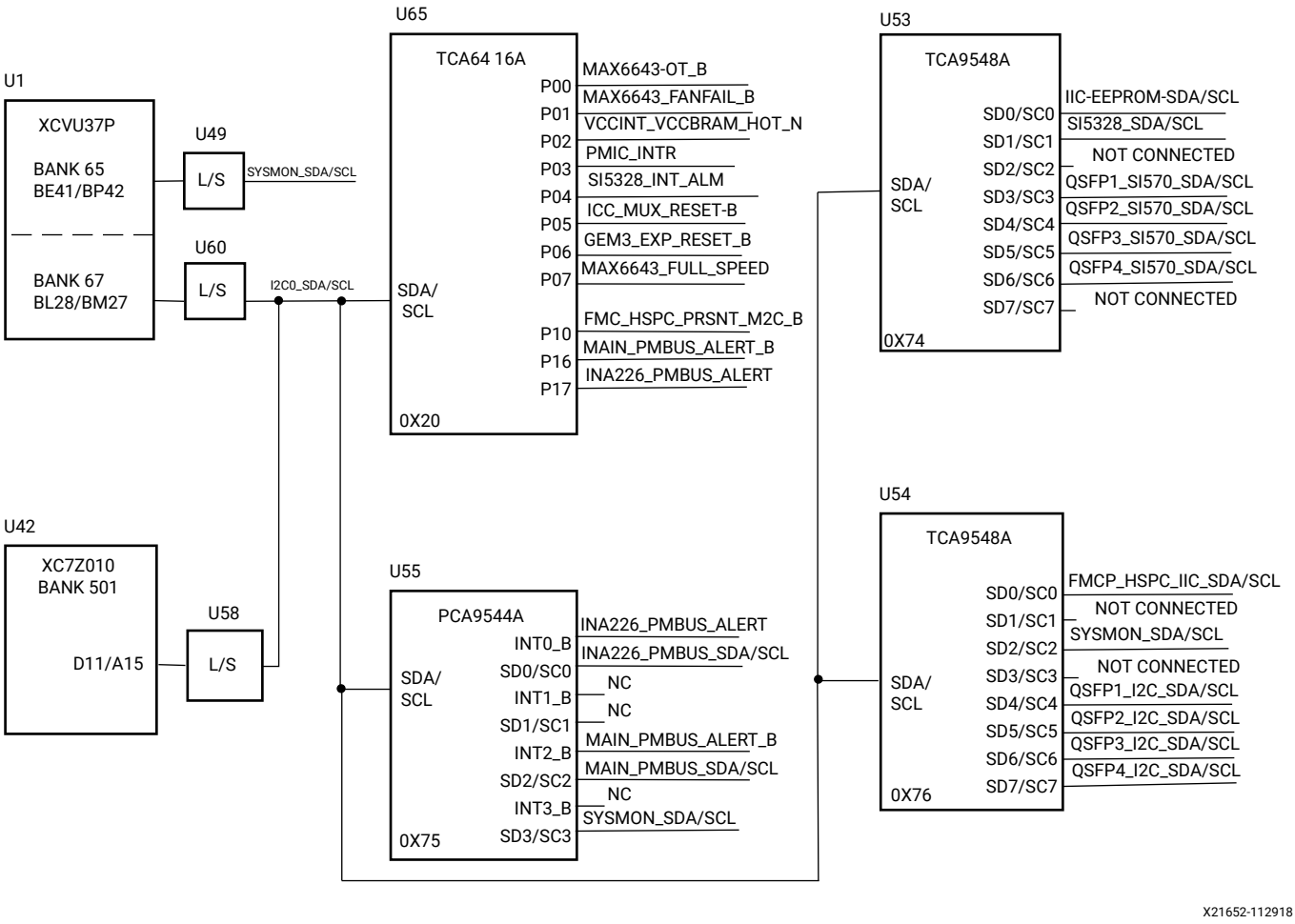
I2C Bus, Topology, and Switches

[Figure 2, callout 25, 26]

The VCU128 evaluation board I2C bus implementation consists of I2C bus I2C0. The FPGA U1 HP bank 67 (VCCO VCC1V8) and system controller U42 bank 501 are wired to I2C0 via level-shifters. I2C bus I2C0 is routed to a 1-to-4 channel TI PCA9544A bus switch U55 (address 0x75) and a dual 8-bit port TI TCA6416A IO expander U65 (address 0x20). I2C bus I2C0 is also routed to a pair of 1-to-8 channel TI TCA9548A bus switches U53 (address 0x74) and U54 (address 0x76). The bus switches can operate at speeds up to 400 kHz. The VCU128 evaluation board I2C0 I2C bus topology is shown in the following figures.

IMPORTANT! *The TCA9548 U53 and U54 RESET_B pin 3 control signal IIC_MUX_RESET_B is connected to the I2C0 bus TCA6416A U65 port expander (Addr 0x20) port P05 pin 9. The IIC_MUX_RESET_B signal must be driven hi-Z or High to enable I2C bus transactions with the target devices connected to U53 and U54.*

Figure 25: **I2C0 Bus Topology**



I2C Bus Addresses

User applications that communicate with any of the I2C bus I2C0 downstream devices must first set up a path to the desired target device through the appropriate bus switch: I2C0 U55 PCA9544A, address 0x75 (`0b111101`); U53 TCA9548A, address 0x74 (`0b1110100`), or U54 TCA9548A, address 0x76 (`0b111110`), respectively. The following table lists the address for each bus.

Table 28: **I2C Bus Addresses**

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
I2C0 Bus				
PCA9544A 4-channel bus switch	N/A	0b1110101	0x75	U55 PCA9544A
PMBus INA226 power monitor[1]	0		0x40-0x42 0x46-0x48 0x4C-0x4D	INA226 U14,U16,U20,U21, U79,U84,U85,U86
Not used	1	N/A	N/A	N/A
PMBus regulators[1]	2		0x60-0x65 0x68-0x6B	Various Intersil regulators U3,U12,U15,U22,U24,U25,U29,U31,U36,U44,U67, U68
FPGA SYSMON	3	0b0110010	0x32	U1 BANK 65
I2C0 Bus				
TCA9548 8-channel bus switch	N/A	0b1110100	0x74	U53 TCA9548A
I2C EEPROM	0	0b1010100	0x54	U48 M24C08
SI5328 clock	1	0b1101000	0x68	U87 SI5328B
Not used	2	N/A	N/A	N/A
QSFP1 Si570 clock	3	0b1011101	0x5D	U95 SI570
QSFP2 Si570 clock	4	0b1011101	0x5D	U90 SI570
QSFP3 Si570 clock	5	0b1011101	0x5D	U82 SI570
QSFP4 Si570 clock	6	0b1011101	0x5D	U80 SI570
Not used	7	N/A	N/A	N/A
I2C0 Bus				
TCA9548 8-channel bus switch	N/A	0b1110101	0x76	U54 TCA9548A
FMCP HSPC (FMC Plus)	0	0bXXXXXXX	0x##	J18 FMCP HSPC
Not used	1	N/A	N/A	N/A
FPGA SYSMON	2	0b0110010	0x32	U1 BANK 65
Not used	3	N/A	N/A	N/A
QSFP1 module	4	0b1010000	0x50	J42 28 Gb/s QSFP+
QSFP2 module	5	0b1010000	0x50	J39 28 Gb/s QSFP+
QSFP3 module	6	0b1010000	0x50	J35 28 Gb/s QSFP+
QSFP4 module	7	0b1010000	0x50	J32 28 Gb/s QSFP+

Notes:

1. See Onboard Power System Devices.

Information about the PCA9544A, TCA9548, and TCA6416A is available on the TI Semiconductor website.

Status and User LEDs

[Figure 2, callout 24]

The following table defines VCU128 board status and user LEDs.

Table 29: **Board Status and User LEDs**

Reference Designator	Description (Green unless otherwise noted)
DS1	Combined power good (red/green)
DS2	GPIO_LED_1
DS3	GPIO_LED_0
DS4	GPIO_LED_2
DS5	GPIO_LED_5
DS6	GPIO_LED_4
DS7	GPIO_LED_5
DS8	GPIO_LED_6
DS9	GPIO_LED_7
DS10	FPGA INIT (red/green)
DS11	VCCINT 0.85V Mode
DS12	VCCINT 0.72V Mode
DS13	FPGA done
DS14	VADJ_PG
DS15	SYSTEM CTLR INIT (red/green)
DS16	SYSTEM CTLR error (red)
DS17	SYSTEM CTLR status
DS18	SYSTEM CTLR done
DS19	ENET PHY link
DS20	12V On
EPHY P2 RT	ENET LINK1000
EPHY P2 LFT	ENET link activity

User GPIO

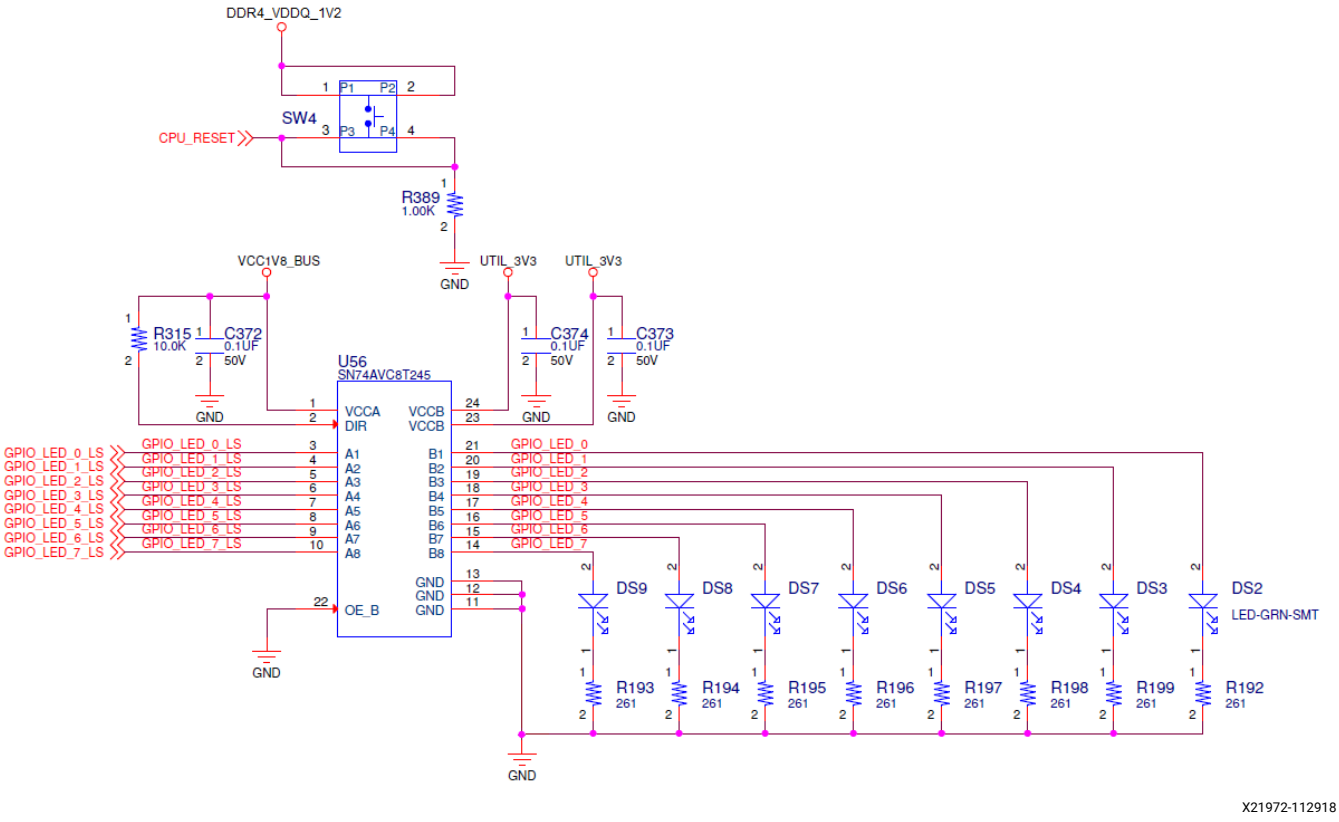
[Figure 2, callout 27, 28, 29]

The VCU128 board provides the following user and general purpose I/O capabilities.

- Eight user LEDs (callout 28)
  - GPIO_LED[7-0]: DS9, DS8, DS7, DS6, DS5, DS4, DS3, DS2
- CPU_RESET/GPIO pushbutton switch (callout 29)
  - CPU_RESET: SW4

The following figure shows the GPIO circuits.

Figure 26: **User GPIO**



GPIO Connections to FPGA U1

The following table lists the GPIO connections to FPGA U1.

Table 30: **GPIO Connections to FPGA U1**

FPGA (U1) Pin		Schematic Net Name	FPGA (U1) Direction	I/O Standard	Device
GPIO LEDs (Active-High) GPIO_LED signals are wired to LED driver U56					
BANK 67	BH24	GPIO_LED_0	Output	LVCMOS18	DS2
BANK 67	BG24	GPIO_LED_1	Output	LVCMOS18	DS3
BANK 67	BG25	GPIO_LED_2	Output	LVCMOS18	DS4
BANK 67	BF25	GPIO_LED_3	Output	LVCMOS18	DS5
BANK 67	BF26	GPIO_LED_4	Output	LVCMOS18	DS6
BANK 67	BF27	GPIO_LED_5	Output	LVCMOS18	DS7
BANK 67	BG27	GPIO_LED_6	Output	LVCMOS18	DS8
BANK 67	BG28	GPIO_LED_7	Output	LVCMOS18	DS9
CPU reset pushbutton (active-high)					
BANK 64	BM29	CPU_RESET	Input	LVCMOS12	SW4.3
GPIO SMA pair (applied voltage should not exceed 1.8V)					
BANK 67	BH27	SMA_CLK_OUTPUT_P	I/O	LVCMOS18	J12.1
BANK 67	BJ27	SMA_CLK_OUTPUT_N	I/O	LVCMOS18	J13.1

Switches

[Figure 2, callouts 30, 33]

The VCU118 evaluation board includes a power on/off slide switch and a configuration pushbutton switch.

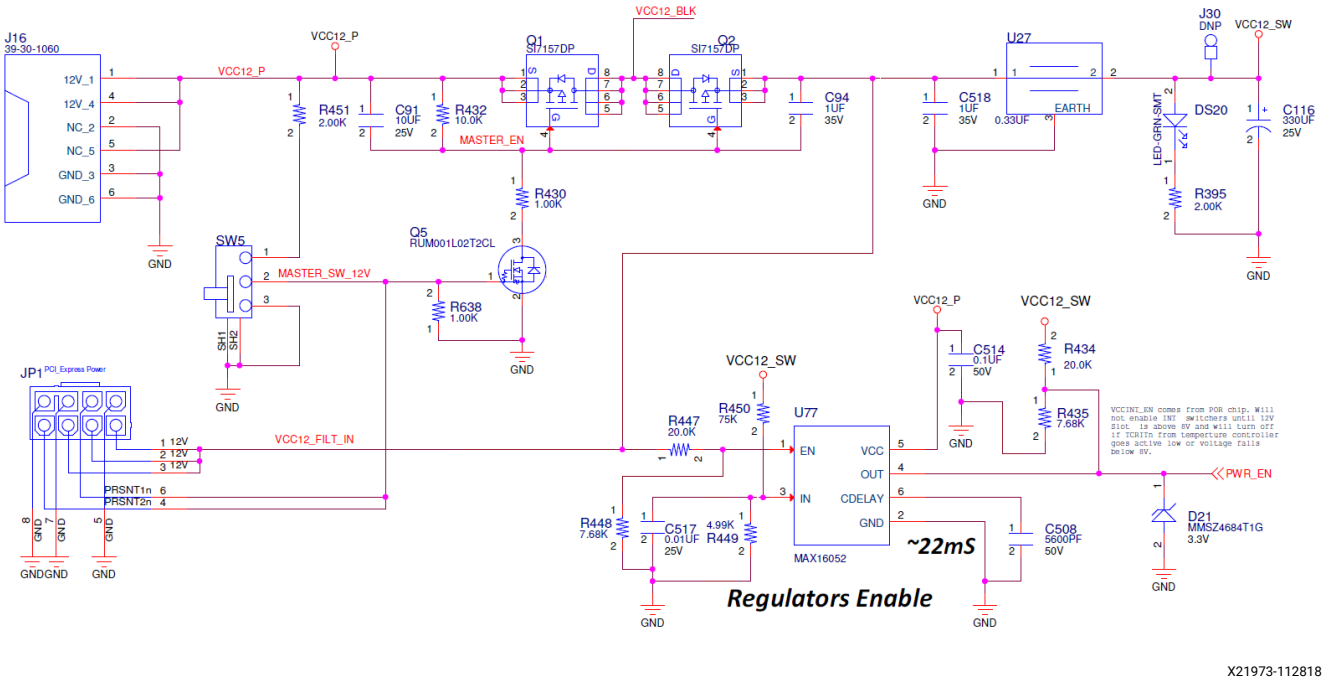
- FPGA Program_B SW4, active-Low (callout 30)
- Power on/off slide switch SW5 (callout 33)

Power On/Off Slide Switch SW5

[Figure 2, callout 33]

The VCU118 board power switch is SW5. Sliding the switch actuator from the off to the on position applies 12VDC power from the 6-pin mini-fit power input connector J16, normally used in bench-top applications with the provided power adapter. The green LED DS20 illuminates when the VCU128 board power switch is on. See Board Power System for details on the onboard power system. The following figure shows the power connector J16, power switch SW5, and indicator LED DS20.

Figure 27: **Power On/Off Switch SW5**



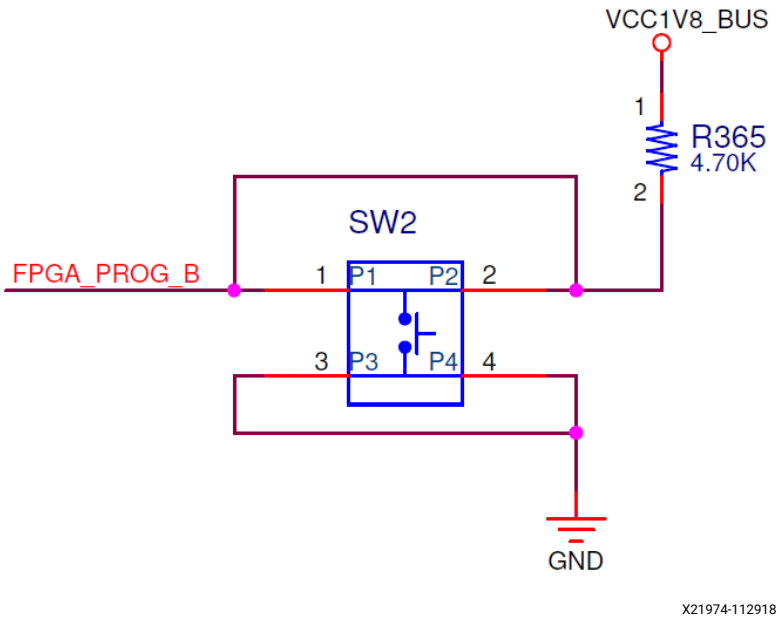
When the VCU128 board is used inside a computer chassis (i.e., plugged in to a PCIe® slot), power is normally provided from the PC ATX supply 2x4 PCIe power connector. See Installing the Board in a PC Chassis.

Program_B Pushbutton Switch

[Figure 2, callout 30]

Switch SW2 grounds the XCVU37P FPGA U1 PROGRAM_B pin when pressed. This action clears the FPGA configuration. The FPGA_PROG_B signal is connected to XCVU37P FPGA U1 pin BB15. See the *UltraScale Architecture Configuration User Guide* (UG570) for further configuration details. The following figure shows SW2.

Figure 28: **Program_B Pushbutton Switch SW2**



FPGA Mezzanine Card Interface

[Figure 2, callout 31]

The VCU128 evaluation board supports the VITA 57.4 FPGA mezzanine card plus (FMC+ or FMCP) specification by providing a subset implementation of the high pin count connector at J18 (HSPC, high serial pin connector). The VITA 57.4 standard extends the VITA 57.1 FMC standard by specifying two new connectors that increase the number of multi-gigabit interfaces from 10 to 24. Also, there is an optional extension connector (the high serial pin connector extension, or HSPCe) to boost pin-count by 80 positions, arranged in a 4x20 array. The VCU128 board does not implement the high serial pin connector/HSPCe extension.

FMC+ connectors use a 14 x 40 form factor, populated with 560 pins. The connector is keyed so that a mezzanine card, when installed on the VCU128 evaluation board, faces away from the board.

J18 FMC+/FMCP Connectors

This section describes the J18 FMC+/FMCP connectors.

- Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector. More information about SEAF series connectors is available on the Samtec website.
- The 560-pin FMC+ connector defined by the FMC specification (see Appendix A: VITA 57.4 FMCP Connector Pinouts) provides connectivity for up to:
  - 160 single-ended or 80 differential user-defined signals

- 24 transceiver differential pairs
- 6 transceiver differential clocks
- 4 differential clocks
- 239 ground and 17 power connections

FMCP Connector J18

[Figure 2, callout 33]

The HSPC connector at J18 implements a subset of the full FMCP connectivity:

- 68 single-ended or 34 differential user-defined pairs (full LA-bus: LA[00:33])
- 24 transceiver differential pairs
- 6 transceiver differential clocks
- 2 differential clocks
- 239 ground and 14 power connections

J18 VITA 57.4 FMCP HSCP Connections

The FMCP J18 connections to FPGA U1 are listed in the following table. The net names shown in the table are connected to FMCP HSCP J18 pins.

Table 31: **J18 VITA 57.4 FMCP HSCP Connections**

J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J18 Sections A/B Connections to FPGA U1							
A2	FMCP_HSPC_DP1_M2C_P	LVDS	BB51	B1	NC		
A3	FMCP_HSPC_DP1_M2C_N	LVDS	BB52	B4	FMCP_HSPC_DP9_M2C_P	LVDS	AT51
A6	FMCP_HSPC_DP2_M2C_P	LVDS	BA53	B5	FMCP_HSPC_DP9_M2C_N	LVDS	AT52
A7	FMCP_HSPC_DP2_M2C_N	LVDS	BA54	B8	FMCP_HSPC_DP8_M2C_P	LVDS	AU53
A10	FMCP_HSPC_DP3_M2C_P	LVDS	BA49	B9	FMCP_HSPC_DP8_M2C_N	LVDS	AU54
A11	FMCP_HSPC_DP3_M2C_N	LVDS	BA50	B12	FMCP_HSPC_DP7_M2C_P	LVDS	AV51
A14	FMCP_HSPC_DP4_M2C_P	LVDS	AY51	B13	FMCP_HSPC_DP7_M2C_N	LVDS	AV52
A15	FMCP_HSPC_DP4_M2C_N	LVDS	AY52	B16	FMCP_HSPC_DP6_M2C_P	LVDS	AW49
A18	FMCP_HSPC_DP5_M2C_P	LVDS	AW53	B17	FMCP_HSPC_DP6_M2C_N	LVDS	AW50
A19	FMCP_HSPC_DP5_M2C_N	LVDS	AW54	B20	FMCP_HSPC_GBTCLK1_M2C_P	LVDS	AR40
A22	FMCP_HSPC_DP1_C2M_P	LVDS	BC44	B21	FMCP_HSPC_GBTCLK1_M2C_N	LVDS	AR41
A23	FMCP_HSPC_DP1_C2M_N	LVDS	BC45	B24	FMCP_HSPC_DP9_C2M_P	LVDS	AT46
A26	FMCP_HSPC_DP2_C2M_P	LVDS	BB46	B25	FMCP_HSPC_DP9_C2M_N	LVDS	AT47
A27	FMCP_HSPC_DP2_C2M_N	LVDS	BB47	B28	FMCP_HSPC_DP8_C2M_P	LVDS	AU48
A30	FMCP_HSPC_DP3_C2M_P	LVDS	BA44	B29	FMCP_HSPC_DP8_C2M_N	LVDS	AU49
A31	FMCP_HSPC_DP3_C2M_N	LVDS	BA45	B32	FMCP_HSPC_DP7_C2M_P	LVDS	AU44
A34	FMCP_HSPC_DP4_C2M_P	LVDS	AY46	B33	FMCP_HSPC_DP7_C2M_N	LVDS	AU45
A35	FMCP_HSPC_DP4_C2M_N	LVDS	AY47	B36	FMCP_HSPC_DP6_C2M_P	LVDS	AV46
A38	FMCP_HSPC_DP5_C2M_P	LVDS	AW44	B37	FMCP_HSPC_DP6_C2M_N	LVDS	AV47
A39	FMCP_HSPC_DP5_C2M_N	LVDS	AW45	B40	NC		

Table 31: **J18 VITA 57.4 FMCP HSCP Connections** *(cont'd)*

J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J18 Sections C/D Connections to FPGA U1							
C2	FMCP_HSPC_DP0_C2M_P	LVDS	BC53	D1	VADJ_PG		
C3	FMCP_HSPC_DP0_C2M_N	LVDS	BC54	D4	FMCP_HSPC_GBTCLK0_M2C_P	LVDS	AV42
C6	FMCP_HSPC_DP0_M2C_P	LVDS	BC48	D5	FMCP_HSPC_GBTCLK0_M2C_N	LVDS	AV43
C7	FMCP_HSPC_DP0_M2C_N	LVDS	BC49	D8	FMCP_HSPC_LA01_CC_P	LVDS	F26
C10	FMCP_HSPC_LA06_P	LVDS	E22	D9	FMCP_HSPC_LA01_CC_N	LVDS	F25
C11	FMCP_HSPC_LA06_N	LVDS	D22	D11	FMCP_HSPC_LA05_P	LVDS	H27
C14	FMCP_HSPC_LA10_P	LVDS	B23	D12	FMCP_HSPC_LA05_N	LVDS	G27
C15	FMCP_HSPC_LA10_N	LVDS	A23	D14	FMCP_HSPC_LA09_P	LVDS	E26
C18	FMCP_HSPC_LA14_P	LVDS	C23	D15	FMCP_HSPC_LA09_N	LVDS	D26
C19	FMCP_HSPC_LA14_N	LVDS	B22	D17	FMCP_HSPC_LA13_P	LVDS	A25
C22	FMCP_HSPC_LA18_CC_P	LVDS	E19	D18	FMCP_HSPC_LA13_N	LVDS	A24
C23	FMCP_HSPC_LA18_CC_N	LVDS	E18	D20	FMCP_HSPC_LA17_CC_P	LVDS	F18
C26	FMCP_HSPC_LA27_P	LVDS	E21	D21	FMCP_HSPC_LA17_CC_N	LVDS	E17
C27	FMCP_HSPC_LA27_N	LVDS	D21	D23	FMCP_HSPC_LA23_P	LVDS	B21
C30	FMCP_HSPC_IIC_SCL			D24	FMCP_HSPC_LA23_N	LVDS	B20
C31	FMCP_HSPC_IIC_SDA			D26	FMCP_HSPC_LA26_P	LVDS	D17
C34	GA0 = 0 = GND			D27	FMCP_HSPC_LA26_N	LVDS	D16
C35	VCC12_SW			D29	FMCP_HSPC_TCK_BUF		
C37	VCC12_SW			D30	FPGA_TDO_FMC_TDI_BUF		
C39	UTIL_3V3			D31	FMCP_HSPC_TDO_HPC1_TDI		
				D32	UTIL_3V3		
				D33	FMCP_HSPC_TMS_BUF		
				D34	NC		
				D35	GA1 = 0 = GND		
				D36	UTIL_3V3		
				D38	UTIL_3V3		
				D40	UTIL_3V3		

Table 31: **J18 VITA 57.4 FMCP HSCP Connections** *(cont'd)*

J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J18 Sections G/H Connections to FPGA U1							
G2	FMCP_HSPC_CLK1_M2C_P	LVDS	G18	H1	FMCP_HSPC_VREF_A_M2C		
G3	FMCP_HSPC_CLK1_M2C_N	LVDS	G17	H2	FMCP_HSPC_PRSNT_M2C_B		
G6	FMCP_HSPC_LA00_CC_P	LVDS	E24	H4	FMCP_HSPC_CLK0_M2C_P	LVDS	F24
G7	FMCP_HSPC_LA00_CC_N	LVDS	E23	H5	FMCP_HSPC_CLK0_M2C_N	LVDS	F23
G9	FMCP_HSPC_LA03_P	LVDS	B27	H7	FMCP_HSPC_LA02_P	LVDS	L23
G10	FMCP_HSPC_LA03_N	LVDS	A26	H8	FMCP_HSPC_LA02_N	LVDS	K22
G12	FMCP_HSPC_LA08_P	LVDS	E27	H10	FMCP_HSPC_LA04_P	LVDS	C25
G13	FMCP_HSPC_LA08_N	LVDS	D27	H11	FMCP_HSPC_LA04_N	LVDS	C24
G15	FMCP_HSPC_LA12_P	LVDS	J22	H13	FMCP_HSPC_LA07_P	LVDS	K27
G16	FMCP_HSPC_LA12_N	LVDS	H22	H14	FMCP_HSPC_LA07_N	LVDS	J27
G18	FMCP_HSPC_LA16_P	LVDS	K24	H16	FMCP_HSPC_LA11_P	LVDS	B26
G19	FMCP_HSPC_LA16_N	LVDS	K23	H17	FMCP_HSPC_LA11_N	LVDS	B25
G21	FMCP_HSPC_LA20_P	LVDS	A21	H19	FMCP_HSPC_LA15_P	LVDS	J26
G22	FMCP_HSPC_LA20_N	LVDS	A20	H20	FMCP_HSPC_LA15_N	LVDS	J25
G24	FMCP_HSPC_LA22_P	LVDS	B16	H22	FMCP_HSPC_LA19_P	LVDS	B18
G25	FMCP_HSPC_LA22_N	LVDS	A16	H23	FMCP_HSPC_LA19_N	LVDS	B17
G27	FMCP_HSPC_LA25_P	LVDS	D20	H25	FMCP_HSPC_LA21_P	LVDS	A19
G28	FMCP_HSPC_LA25_N	LVDS	D19	H26	FMCP_HSPC_LA21_N	LVDS	A18
G30	FMCP_HSPC_LA29_P	LVDS	H19	H28	FMCP_HSPC_LA24_P	LVDS	C18
G31	FMCP_HSPC_LA29_N	LVDS	H18	H29	FMCP_HSPC_LA24_N	LVDS	C17
G33	FMCP_HSPC_LA31_P	LVDS	H17	H31	FMCP_HSPC_LA28_P	LVDS	G21
G34	FMCP_HSPC_LA31_N	LVDS	G16	H32	FMCP_HSPC_LA28_N	LVDS	F21
G36	FMCP_HSPC_LA33_P	LVDS	K21	H34	FMCP_HSPC_LA30_P	LVDS	J20
G37	FMCP_HSPC_LA33_N	LVDS	J21	H35	FMCP_HSPC_LA30_N	LVDS	J19
G39	VADJ_1V8_FPGA			H37	FMCP_HSPC_LA32_P	LVDS	H20
				H38	FMCP_HSPC_LA32_N	LVDS	G20
				H40	VADJ		

Table 31: **J18 VITA 57.4 FMCP HSCP Connections** *(cont'd)*

J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J18 Sections L/M Connections to FPGA U1							
L1	NC			M2	FMCP_HSPC_DP23_M2C_P	LVDS	AE49
L4	FMCP_HSPC_GBTCLK4_M2C_P(5)	LVDS	AJ40	M3	FMCP_HSPC_DP23_M2C_N	LVDS	AE50
L5	FMCP_HSPC_GBTCLK4_M2C_N(5)	LVDS	AJ41	M6	FMCP_HSPC_DP22_M2C_P	LVDS	AE53
L8	FMCP_HSPC_GBTCLK3_M2C_P(5)	LVDS	AL40	M7	FMCP_HSPC_DP22_M2C_N	LVDS	AE54
L9	FMCP_HSPC_GBTCLK3_M2C_N(5)	LVDS	AL41	M10	FMCP_HSPC_DP21_M2C_P	LVDS	AF51
L12	FMCP_HSPC_GBTCLK2_M2C_P(5)	LVDS	AN40	M11	FMCP_HSPC_DP21_M2C_N	LVDS	AF52
L13	FMCP_HSPC_GBTCLK2_M2C_N(5)	LVDS	AN41	M14	FMCP_HSPC_DP20_M2C_P	LVDS	AG53
L16	FMCP_HSPC_SYNC_C2M_P	LVDS	D25	M15	FMCP_HSPC_DP20_M2C_N	LVDS	AG54
L17	FMCP_HSPC_SYNC_C2M_N	LVDS	D24	M18	FMCP_HSPC_DP14_C2M_P	LVDS	AM46
L20	FMCP_HSPC_REFCLK_C2M_P	LVDS	H24	M19	FMCP_HSPC_DP14_C2M_N	LVDS	AM47
L21	FMCP_HSPC_REFCLK_C2M_N	LVDS	H23	M22	FMCP_HSPC_DP15_C2M_P	LVDS	AL44
L24	FMCP_HSPC_REFCLK_M2C_P	LVDS	G26	M23	FMCP_HSPC_DP15_C2M_N	LVDS	AL45
L25	FMCP_HSPC_REFCLK_M2C_N	LVDS	G25	M26	FMCP_HSPC_DP16_C2M_P	LVDS	AK46
L28	FMCP_HSPC_SYNC_M2C_P	LVDS	G23	M27	FMCP_HSPC_DP16_C2M_N	LVDS	AK47
L29	FMCP_HSPC_SYNC_M2C_N	LVDS	G22	M30	FMCP_HSPC_DP17_C2M_P	LVDS	AJ48
L32	NC			M31	FMCP_HSPC_DP17_C2M_N	LVDS	AJ49
L33	NC			M34	FMCP_HSPC_DP18_C2M_P	LVDS	AJ44
L36	VCC12_SW			M35	FMCP_HSPC_DP18_C2M_N	LVDS	AJ45
L37	VCC12_SW			M38	FMCP_HSPC_DP19_C2M_P	LVDS	AH46
L40	VCC12_SW			M39	FMCP_HSPC_DP19_C2M_N	LVDS	AH47

Table 31: **J18 VITA 57.4 FMCP HSCP Connections** *(cont'd)*

J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J18 FMCP HSCP Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J18 Sections Y/Z Connections to FPGA U1							
Y2	FMCP_HSPC_DP23_C2M_P	LVDS	AE44	Z1	FMCP_HSPC_PRSNT_M2C_B		
Y3	FMCP_HSPC_DP23_C2M_N	LVDS	AE45	Z4	FMCP_HSPC_DP22_C2M_P	LVDS	AF46
Y6	FMCP_HSPC_DP21_C2M_P	LVDS	AG44	Z5	FMCP_HSPC_DP22_C2M_N	LVDS	AF47
Y7	FMCP_HSPC_DP21_C2M_N	LVDS	AG45	Z8	FMCP_HSPC_DP20_C2M_P	LVDS	AG48
Y10	FMCP_HSPC_DP10_M2C_P	LVDS	AR53	Z9	FMCP_HSPC_DP20_C2M_N	LVDS	AG49
Y11	FMCP_HSPC_DP10_M2C_N	LVDS	AR54	Z12	FMCP_HSPC_DP11_M2C_P	LVDS	AP51
Y14	FMCP_HSPC_DP12_M2C_P	LVDS	AN53	Z13	FMCP_HSPC_DP11_M2C_N	LVDS	AP52
Y15	FMCP_HSPC_DP12_M2C_N	LVDS	AN54	Z16	FMCP_HSPC_DP13_M2C_P	LVDS	AN49
Y18	FMCP_HSPC_DP14_M2C_P	LVDS	AM51	Z17	FMCP_HSPC_DP13_M2C_N	LVDS	AN50
Y19	FMCP_HSPC_DP14_M2C_N	LVDS	AM52	Z20	FMCP_HSPC_GBTCLK5_M2C_P	LVDS	AG40
Y22	FMCP_HSPC_DP15_M2C_P	LVDS	AL53	Z21	FMCP_HSPC_GBTCLK5_M2C_N	LVDS	AG41
Y23	FMCP_HSPC_DP15_M2C_N	LVDS	AL54	Z24	FMCP_HSPC_DP10_C2M_P	LVDS	AR48
Y26	FMCP_HSPC_DP11_C2M_P	LVDS	AR44	Z25	FMCP_HSPC_DP10_C2M_N	LVDS	AR49
Y27	FMCP_HSPC_DP11_C2M_N	LVDS	AR45	Z28	FMCP_HSPC_DP12_C2M_P	LVDS	AP46
Y30	FMCP_HSPC_DP13_C2M_P	LVDS	AN44	Z29	FMCP_HSPC_DP12_C2M_N	LVDS	AP47
Y31	FMCP_HSPC_DP13_C2M_N	LVDS	AN45	Z32	FMCP_HSPC_DP16_M2C_P	LVDS	AL49
Y34	FMCP_HSPC_DP17_M2C_P	LVDS	AK51	Z33	FMCP_HSPC_DP16_M2C_N	LVDS	AL50
Y35	FMCP_HSPC_DP17_M2C_N	LVDS	AK52	Z36	FMCP_HSPC_DP18_M2C_P	LVDS	AJ53
Y38	FMCP_HSPC_DP19_M2C_P	LVDS	AH51	Z37	FMCP_HSPC_DP18_M2C_N	LVDS	AJ54
Y39	FMCP_HSPC_DP19_M2C_N	LVDS	AH52	Z40	UTIL_3V3		

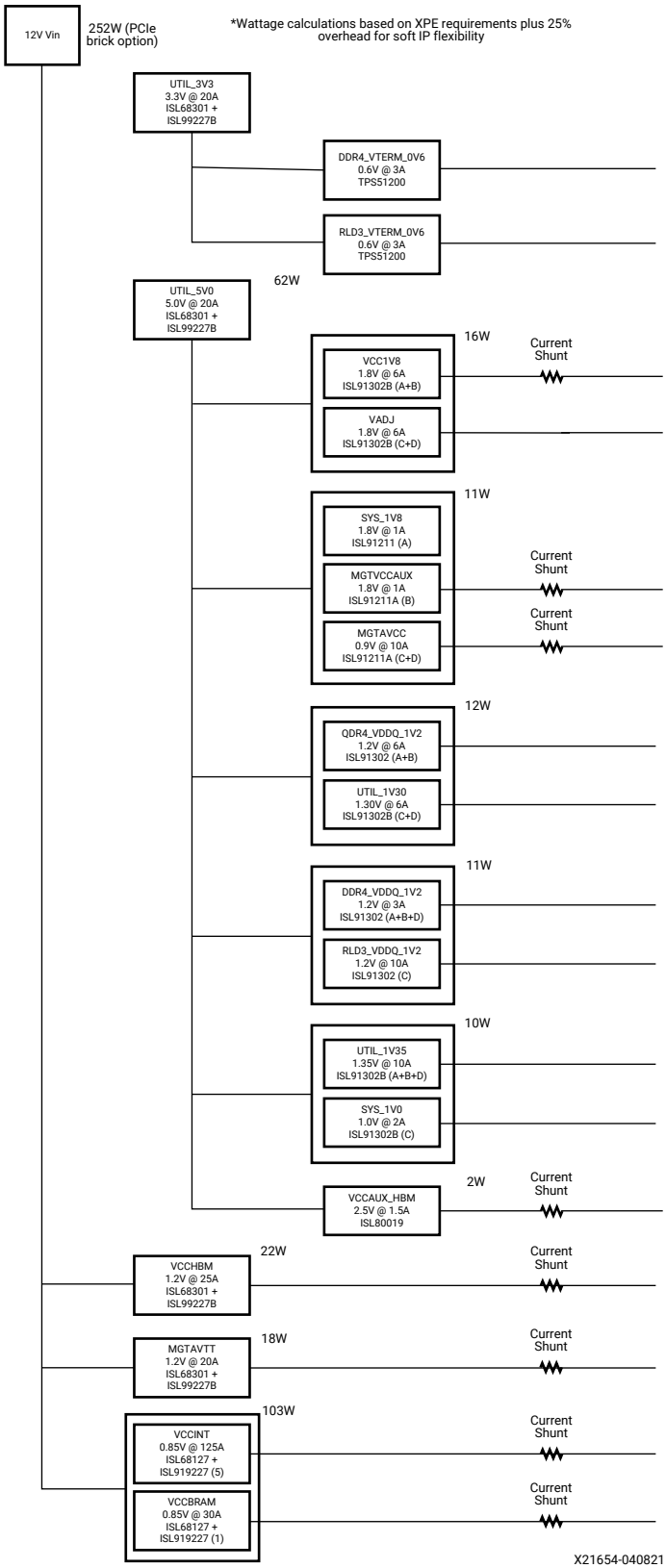
More information about the VITA 57.4 FMC+ specification is available on the VITA FMC Marketing Alliance website.

Board Power System

[Figure 2, callout 34]

The VCU128 board has an Intersil power system. The following figure shows the VCU128 board power system block diagram.

Figure 29: **Power System Block Diagram**



Onboard Power System Devices

The VCU128 evaluation board uses programmable power regulators from Intersil Corporation to supply the core and auxiliary voltages listed in the following table.

Table 32: **Onboard Power System Devices**

Schematic Page	Rail Name	Regulator Type	U#	Vout (V)	Iout Range (A)	I2C Address	INA226	
							U#	I2C Address
Programmable Regulators and INA226 Map								
Programmable Regulators								
54	VCCINT (PWM[2:6])	ISL68127IRAZ-TR5823	U31	0.72 - 0.85[1]	125	0X65	U84	0x40
54	VCCBRAM (PWM[0])	ISL68127IRAZ-TR5823	U31	0.72 - 0.85[1]	30	0X65	U86	0x41
56	VCC1V8 (PH_A/B)	ISL91302BIKZ-TR5814	U15	1.8	4 - 6	0x63	U14	0X42
56	VADJ (PH_C/D)	ISL91302BIKZ-TR5814	U15	0, 0.3 -1.8	4.5 - 6	0x63	NA	NA
57	VCCHBM	ISL68301IRAZ-TR5823	U36	1.2	25	0x68	U85	0x4C
57	MGTAVTT	ISL68301IRAZ-TR5823	U24	1.2	20	0x69	U21	0x47
58	SYS_1V8 (PH_A)	ISL91211AIKZ-TR5818	U22	1.8	0.75 - 1	0x60	NA	NA
58	MGTVCCAUX (PH_B)	ISL91211AIKZ-TR5818	U22	1.8	0.75 - 1	0x60	U20	0x48
58	MGTAVCC (PH_C/D)	ISL91211AIKZ-TR5818	U22	0.9	8 - 10	0x60	U16	0x46
59	QDR4_VDDQ (PH_A/B)	ISL91302BIKZ-TR5815	U44	1.2	5 - 6	0x62	NA	NA
59	UTIL_1V30 (PH_C/D)	ISL91302BIKZ-TR5815	U44	1.3	4.5 - 6	0x62	NA	NA
60	RLD3_VDDQ (PH_A/B/D)	ISL91302BIKZ-TR5816	U67	1.2	7 - 10	0x64	NA	NA
60	DDR4_VDDQ (PH_C)	ISL91302BIKZ-TR5816	U67	1.2	2.5 - 3	0x64	NA	NA
61	UTIL_1V35 (PH_A/B/D)	ISL91302BIKZ-TR5817	U68	1.35	6.5 - 10	0x61	NA	NA
61	SYS_1V0 (PH_C)	ISL91302BIKZ-TR5817	U68	1	1.75 - 2	0x61	NA	NA
62	UTIL_3V3	ISL68301IRAZ-TR5826	U3	3.3	30	0x6A	NA	NA
62	UTIL_5V0	ISL68301IRAZ-TR5825	U12	5	20	0x6B	NA	NA
Non-I2C Regulators								
63	VCCAUX_HBM	SL80019FRZ-T7A	U29	2.5	1.5	NA	U79	0x4D
65	VCC_3V3	ISL85415FRZ-T7A	U25	3.3	20	NA	NA	NA
33	DDR4_VTERM_0V6	TPS51200DR	U71	0.6	3	NA	NA	NA
33	RLD3_VTERM_0V6	TPS51200DR	U92	0.6	3	NA	NA	NA

Notes:

1. Jumper selectable at 3-pin header J25: 1-2=0.85V (default); 2-3=0.72V.

Documentation describing the programming of the Intersil power controllers is available on the Intersil website (see References). The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583).

FMCP HSPC Connector J18 VADJ Power Rail

The VCU128 evaluation board implements the ANSI/VITA 57.4 IPMI support functionality. The power control of the VADJ power rail is managed by the U42 system controller. This rail powers both the FMCP HSPC (J18) VADJ pins, as well as XCVU37P U1 HP banks 71 and 72 (see I/O Voltage Rails). The valid values of the VADJ rail are 1.2V, 1.5V, and 1.8V.

At power on, the system controller detects if an FMC module is connected to FMCP J18:

- If no FMC card is attached to the FMC port, the VADJ voltage is set to 0V
- When an FMC card is attached, its IIC EEPROM is read to find a VADJ voltage supported by both the VCU128 board and the FMC module, within the available choices of 1.2V, 1.5V, 1.8V, and 0.0V
- If no valid information is found in the IIC EEPROM, the VADJ rail is set to 0V

The system controller user interface allows the FMC IPMI routine to be overridden and an explicit value to be set for the VADJ rail.

Monitoring Voltage and Current

[Figure 2, callout 35]

Voltage and current monitoring and control for the Intersil power system is available through either the VCU128 system controller or the Intersil PowerNavigator software GUI. The VCU128 system controller is a simple and convenient way to monitor the voltage and current values for the power rails listed in the following table. The Intersil programmable power controllers listed in the table can also be accessed through the 2x3 male pin header J1. Using this connector requires the Intersil ZLUSBEVAL3Z USB to PMBus adapter. This adapter cable can be ordered from the Intersil website (see References). The associated Intersil PowerNavigator software GUI can be downloaded from the Intersil website. The Intersil programmable controller and INA226 power monitor I2C bus mapping is shown in the following table.

Table 33: **Programmable Controller and INA226 Power Monitor I2C Bus Mapping**

Schematic Page	Rail Name	Regulator Type	U#	Vout (V)	Iout Range (A)	I2C Address	INA226	
							U#	I2C Address
Programmable Regulators and INA226 Map								
Programmable Regulators								
54	VCCINT (PWM[2:6])	ISL68127IRAZ-TR5823	U31	0.72 - 0.85[1]	125	0X65	U84	0x40
54	VCCBRAM (PWM[0])	ISL68127IRAZ-TR5823	U31	0.72 - 0.85[1]	30	0X65	U86	0x41
56	VCC1V8 (PH_A/B)	ISL91302BIKZ-TR5814	U15	1.8	4 - 6	0x63	U14	0X42

Table 33: **Programmable Controller and INA226 Power Monitor I2C Bus Mapping** *(cont'd)*

Schematic Page	Rail Name	Regulator Type	U#	Vout (V)	Iout Range (A)	I2C Address	INA226	
							U#	I2C Address
56	VADJ (PH_C/D)	ISL91302BIKZ-TR5814	U15	0, 0.3 -1.8	4.5 - 6	0x63	NA	NA
57	VCCHBM	ISL68301IRAZ-TR5823	U36	1.2	25	0x68	U85	0x4C
57	MGTAVTT	ISL68301IRAZ-TR5823	U24	1.2	20	0x69	U21	0x47
58	SYS_1V8 (PH_A)	ISL91211AIKZ-TR5818	U22	1.8	0.75 - 1	0x60	NA	NA
58	MGTVCCAUX (PH_B)	ISL91211AIKZ-TR5818	U22	1.8	0.75 - 1	0x60	U20	0x48
58	MGTAVCC (PH_C/D)	ISL91211AIKZ-TR5818	U22	0.9	8 - 10	0x60	U16	0x46
59	QDR4_VDDQ (PH_A/B)	ISL91302BIKZ-TR5815	U44	1.2	5 - 6	0x62	NA	NA
59	UTIL_1V30 (PH_C/D)	ISL91302BIKZ-TR5815	U44	1.3	4.5 - 6	0x62	NA	NA
60	RLD3_VDDQ (PH_A/B/D)	ISL91302BIKZ-TR5816	U67	1.2	7 - 10	0x64	NA	NA
60	DDR4_VDDQ (PH_C)	ISL91302BIKZ-TR5816	U67	1.2	2.5 - 3	0x64	NA	NA
61	UTIL_1V35 (PH_A/B/D)	ISL91302BIKZ-TR5817	U68	1.35	6.5 - 10	0x61	NA	NA
61	SYS_1V0 (PH_C)	ISL91302BIKZ-TR5817	U68	1	1.75 - 2	0x61	NA	NA
62	UTIL_3V3	ISL68301IRAZ-TR5826	U3	3.3	30	0x6A	NA	NA
62	UTIL_5V0	ISL68301IRAZ-TR5825	U12	5	20	0x6B	NA	NA
Non-I2C Regulators								
63	VCCAUX_HBM	SL80019FRZ-T7A	U29	2.5	1.5	NA	U79	0x4D
65	VCC_3V3	ISL85415FRZ-T7A	U25	3.3	20	NA	NA	NA
33	DDR4_VTERM_0V6	TPS51200DR	U71	0.6	3	NA	NA	NA
33	RLD3_VTERM_0V6	TPS51200DR	U92	0.6	3	NA	NA	NA

Notes:

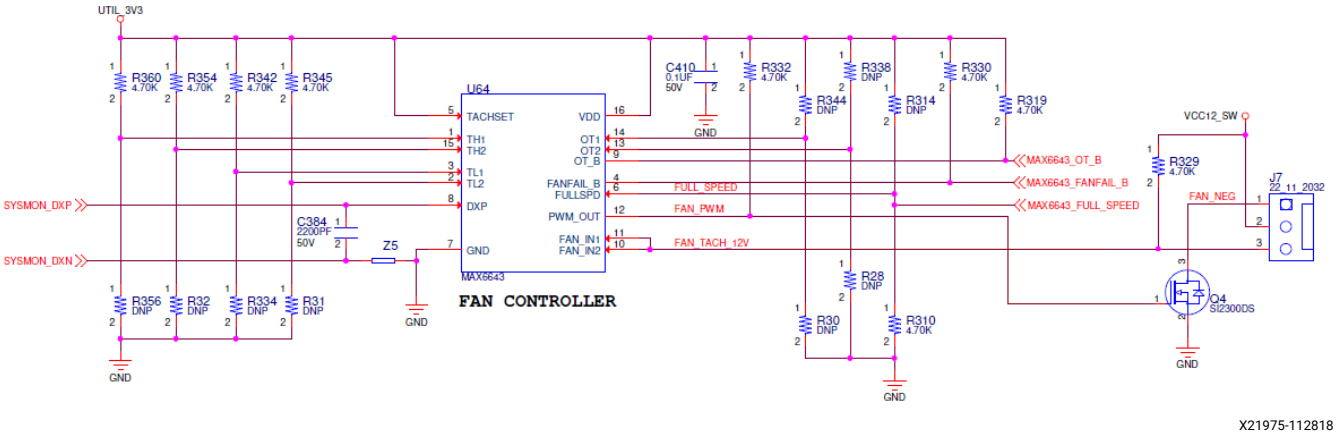
1. Jumper selectable at 3-pin header J25: 1-2 = 0.85V (default); 2-3 = 0.72V.

Cooling Fan

The XCVU37P FPGA U1 cooling fan connector is shown in the following figure. The VCU128 fan circuit uses a Maxim MAX6643 fan controller that autonomously monitors the FPGA die temperature pins DXP and DXN. The fan circuit is set up to increase fan speed as the FPGA temperature increases.

***Note*:** At initial power on, it is normal for the fan controller to energize at full speed for a few seconds.

Figure 30: **Cooling Fan Circuit**

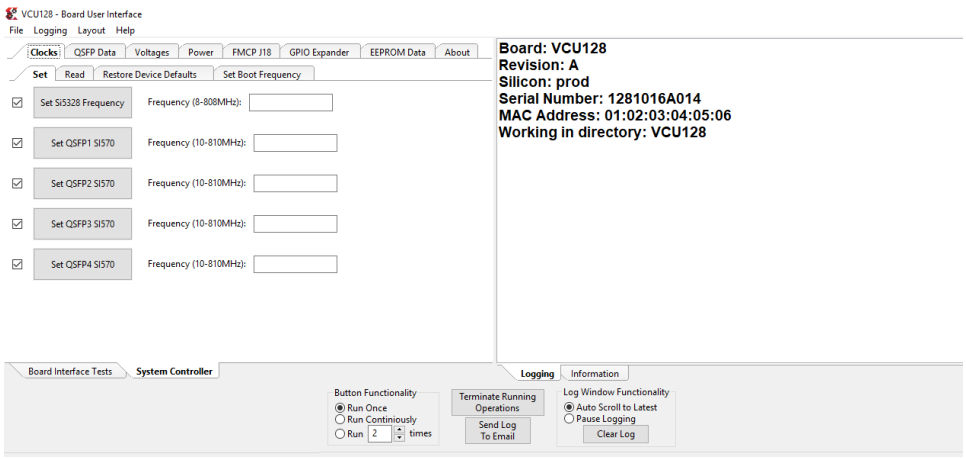


System Controller

[Figure 2, callout 8]

The VCU128 board includes an onboard Zynq®-7000 SoC U42 as the system controller. A host PC resident graphical user interface for the system controller (SCUI) is provided on the VCU128 website. The SCUI can be used to query and control select programmable features such as clocks, FMC functionality, and power systems. The VCU128 evaluation kit website also includes a *VCU128 System Controller Tutorial* (XTP534) and the *VCU128 Software Install and Board Setup Tutorial* (XTP535). A summary of the steps is as follows.

1. Ensure the Silicon Labs VCP USB-UART drivers are installed on the host PC. See the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033).
2. Download the SCUI host PC application.
3. Connect the micro-B USB cable between the VCU128 board USB-UART connector (J2) and the host PC.
4. Power-cycle the VCU128 board.
5. Launch the SCUI as shown in the following example.



X21976-112818

See the *VCU128 System Controller Tutorial* (XTP534) and the *VCU128 Software Install and Board Setup Tutorial* (XTP535) for more information on installing and using the System Controller utility.

Configuration Options

[Figure 2, callout 36]

The VCU128 board supports two of the seven UltraScale™ FPGA configuration modes.

- Master SPI using the onboard 2 Gbit Quad SPI flash memory
- JTAG using:
  - USB JTAG configuration port J2 (FTDI FT4232H bridge U8)
  - Xilinx® platform cable 2 mm, keyed flat cable header (J4)

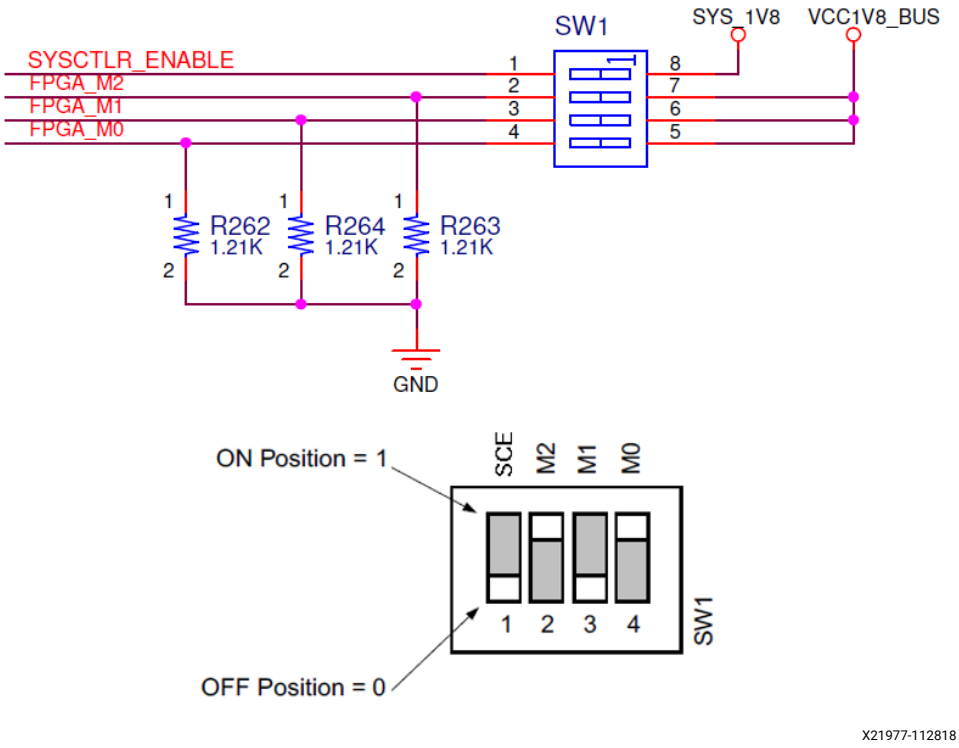
Each configuration interface corresponds to one or more configuration modes and bus widths as listed in the following table. The mode switches M2, M1, and M0 are on 4-pole DIP SW1 positions 2, 3, and 4, respectively. The FPGA default mode setting M[2:0] = 001, selecting the master SPI configuration mode.

Table 34: **Board FPGA Configuration Modes**

Configuration Mode	SW16 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master SPI	1	x1, x2, x4	Output
JTAG	101	x1	Not applicable

The following figure shows mode switch SW1.

Figure 31: **SW1 JTAG Settings**



The mode pins settings on SW1 determine if the Quad SPI flash is used for configuring the FPGA. DIP switch SW1 also includes a system controller enable switch in position 1. See the *UltraScale Architecture Configuration User Guide* (UG570) for further details on configuration modes.

VITA 57.4 FMCP Connector Pinouts

Overview

The following figure shows the pinout of the FPGA mezzanine card plus (FMCP) connector J18 defined by the VITA 57.4 FMC specification. For a description of how the VCU128 evaluation board implements the FMCP specification, see FPGA Mezzanine Card Interface.

Figure 32: **FMCP Connector Pinouts**

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

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Appendix B

Xilinx Constraints File

Overview

The Xilinx® design constraints (XDC) file template for the VCU128 board provides for designs targeting the VCU128 evaluation board. Net names in the constraints listed correlate with net names on the latest VCU128 evaluation board schematic. Identify the appropriate pins and replace the net names with the net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.

The FMCP connector J18 (HSCP) is connected to 1.8V (nominal) VADJ banks 70 and 71. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT! *See VCU128 board documentation for the XDC file.*

Appendix C

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

VCU128 Evaluation Kit - Master Answer Record 71849

For Technical Support, open a Support Service Request.

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

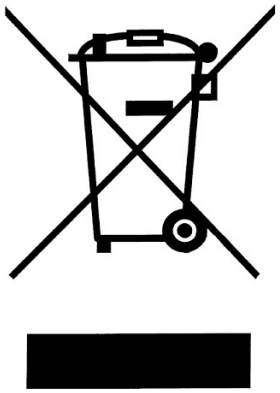
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the VCU128 board and its documentation is available on the following websites.

VCU128 Evaluation Kit

VCU128 Evaluation Kit - Master Answer Record 71849

These documents provide supplemental material useful with this guide:

1. *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923)
2. *UltraScale Architecture Configuration User Guide* (UG570)
3. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
4. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
5. *UltraScale Architecture Clocking Resources User Guide* (UG572)
6. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
7. *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182)
8. *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156)
9. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
10. *AXI UART Lite LogiCORE IP Product Guide* (PG142)
11. *Vivado Design Suite User Guide: Using Constraints* (UG903)
12. *UltraScale Architecture PCB Design User Guide* (UG583)
13. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
14. *VCU128 System Controller Tutorial* (XTP534)
15. *VCU128 Software Install and Board Setup Tutorial* (XTP535)
16. *VCU128 Restoring Flash Tutorial* (XTP533)
17. For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

    These websites provide supplemental material useful with this guide:

18. Xilinx, Inc.

    (XCVU37P-2FSVH2892E)

19. Micron Technology

    (MT40A512M16LY-075E, MT44K32M36RB-083E, MT25QU02GCBB8E12-0SIT)

20. http://www.cypress.com (CY7C4142KV13_106FCXC)

21. Silicon Labs (Si570, Si5328B)
22. SiTime Corp. (SIT9120AI)
23. Future Technology Devices International Ltd. (FT232HL)
24. SNIA Technology Affiliates (SFF-8663, SFF-8679)
25. PCI Express® standard
26. Texas Instruments (TCA9548, PCA9544, DP83867ISRGZ)
27. Samtec, Inc.
28. VITA FMC Marketing Alliance

    (FPGA Mezzanine Card (FMC) VITA 57.4 specification) This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28 Gb/s. It also describes FMC+ I/O modules that support this enhanced version of the FMC electro-mechanical standard. This is between the front panel I/O, on the mezzanine module, and an FPGA processing device on the carrier card, which accepts the mezzanine module. Additional signals to support backplane reference clock and synchronization have been added. The VITA 57.4 specification is backwards compatible in that a VITA 57.4 carrier card can still support a VITA 57 FMC.

29. Intersil Corporation (a wholly owned subsidiary of Renesas Electronics Corporation)

    The Intersil PowerNavigator software is available at: https://www.intersil.com/en/products/power-management/zilker-labs-digital-power/powernavigator.html

    The Intersil USB to PMBUS ZLUSBEVAL3Z Dongle is available at: https://www.intersil.com/en/tools/reference-designs/zlusbeval3z.html

ATX Power Supply Adapter Cable

The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009.

Sourcegate only manufactures the latest revision, which is currently A4. To order, contact Aries Ang, aries.ang@sourcegate.net, +65 6483 2878 for price and availability. This is a custom cable and cannot be ordered from the Sourcegate website.