ZCU111 Evaluation Board

User Guide

UG1271 (v1.2) October 2, 2018

XILINX

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
10/02/2018 Version 1.2	
Electrostatic Discharge Caution	Added new electrostatic discharge information.
PS-Side: DDR4 SODIMM Socket	Revised first paragraph.
PL-Side: DDR4 Component Memory	Added reference to DS926.
RFMC Plug-in Card Interface	Revised paragraph following Figure 3-20 and added reference to Appendix D, HW-FMC-XM500.
Overview in Appendix D	Revised bulleted list.
Table D-3	Added a note.
8/06/2018 Version 1.1	
RF Data Converter Clocking	Removed RF Clocking Overview figure.
Figure 3-18	Added capacitor option.
Table 3-18 and Table 3-19	Added optional RFMC and SYSREF capacitor options.
SFP28 Module Connectors	Added note and reference to SNIA Technology Affiliates website.
06/28/2018 Version 1.0	
	Initial Xilinx release.

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Appendix E: Additional Resources and Legal Notices

Introduction

Overview

The ZCU111 evaluation board features the Zynq® UltraScale+™ RFSoC ZCU28DR device. This board enables the evaluation of the integrated RF-DAC and RF-ADC functionality, soft decision forward error correction (SDFEC), and FPGA fabric and RFSoC features, such as the quad core Arm® Cortex™-A53 processing system (PS) and the dual-core Arm Cortex-R5 real-time processors. The ZCU111 evaluation board is equipped with many of the common board-level features needed for design development, such as DDR4 memory, networking interfaces, FMC+ expansion port, and access to the new RF-FMC interface.

The ZCU111 evaluation board kit includes an out-of-the-box FMC XM500 balun transformer add-on card to support signal analysis and loopback evaluation. This card includes on-board high-frequency and low frequency baluns and SMAs for custom baluns and filtering. For more information on this card, see Appendix D, HW-FMC-XM500.

Additional Resources

See Appendix E, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the ZCU111 evaluation board.

Block Diagram

The ZCU111 board block diagram is shown in Figure 1-1.

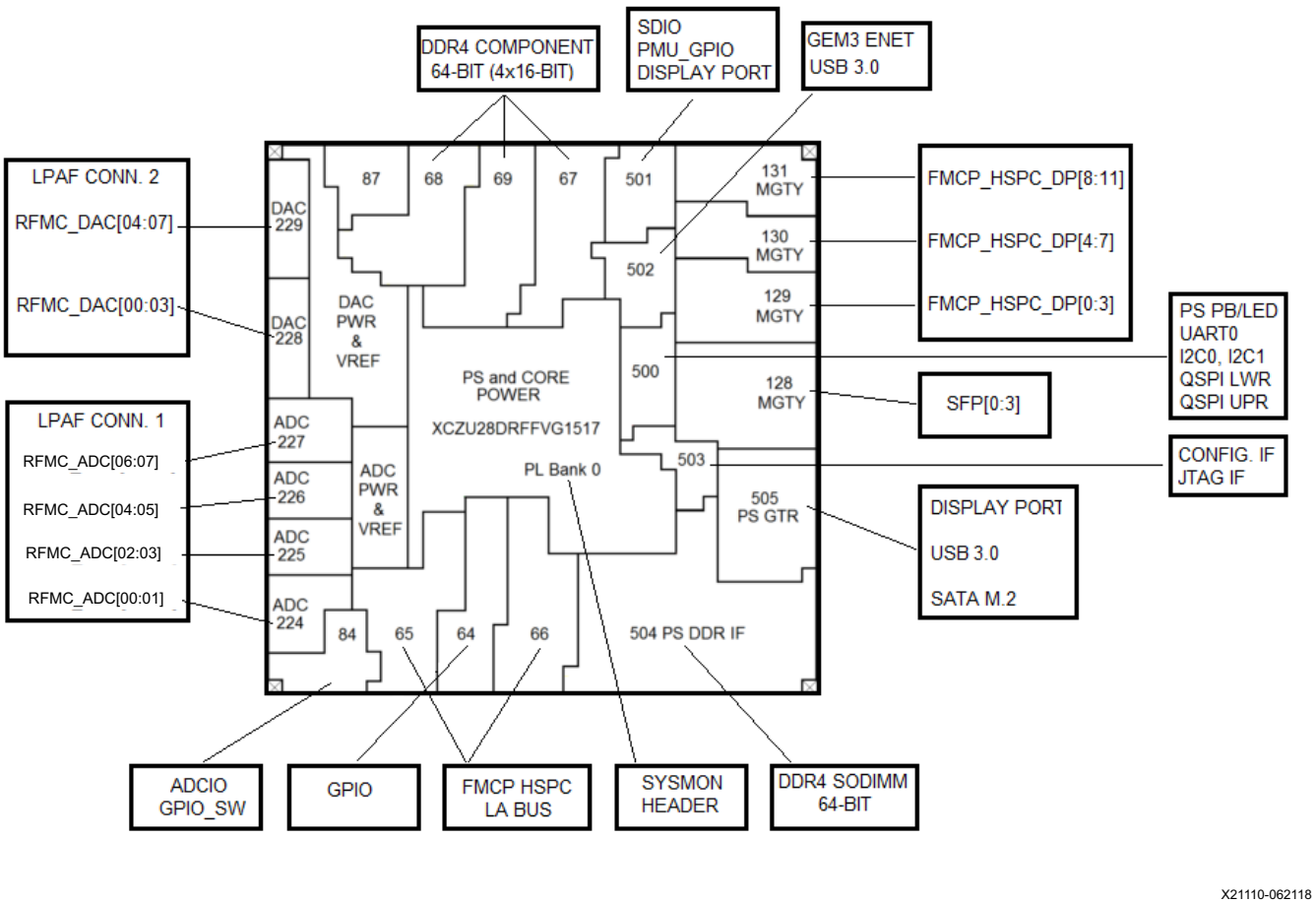

Figure 1-1: **ZCU111 Evaluation Board Block Diagram**

Board Features

The ZCU111 evaluation board features are listed here. Detailed information for each feature is provided in Board Component Descriptions in Chapter 3.

- XCZU28DR-2E, FFVG1517 package
- Form factor: rectangular 11.811 in. x 7.874 in. x 0.1 in.
- Configuration from:
  - Dual Quad SPI

  - Micro SD card
  - USB-to-JTAG bridge
- Clocks
  - GTR_REF_CLK_DP 27 MHz
  - GTR_REF_CLK_USB3 26 MHz
  - GTR_REF_CLK_SATA 125 MHz
  - CLK_100 100 MHz
  - CLK_125 125 MHz
  - PS_REF_CLK 33.33 MHz
  - USER_MGT_SI570 (default 156.25 MHz)
  - USER_SI570 (default 300 MHz)
- PS DDR4 4 GB 64-bit SODIMM
- PL DDR4 4 GB 64-bit component (4x16-bit)
- PS GTR (bank 505) assignment
  - DisplayPort 1.2 transmit only (two GTR)
  - USB3 (one GTR)
  - SATA with M2 connector (one GTR)
- PL GTY assignment (16 total)
  - SFP28 (four, bank GTY128)
  - FMCP HSCP DP (four, bank GTY129)
  - FMCP HSCP DP (four, bank GTY130)
  - FMCP HSCP DP (four, bank GTY131)
- PL FMCP HSCP (FMC+) connectivity - full LA[00:33] bus
- PS MIO connectivity
  - PS MIO[0:5, 7:12]: dual Quad SPI flash memory
  - PS MIO[13]: PS_GPIO2
  - PS MIO[14:17]: two channels of I2C
  - PS MIO[18:19]: UART (one of three FT4232 UART channels)
  - PS MIO[22:23]: PS_PB, PS_LED I/F
  - PS MIO[26]: platform management unit (PMU)
  - PS MIO[27:30]: DisplayPort control

  - PS MIO[32:37]: PMU_GPIO[0:5]
  - PS MIO[38]: PS_GPIO1
  - PS MIO[44:51]: SD I/F
  - PS MIO[52:63]: USB3.0
  - PS MIO[64:77]: GEM3 Ethernet
- PL I/O connections:
  - PL-side user DIP switch (8-position)
  - PL-side CPU reset pushbutton
  - PL-side user LEDs (eight)
  - PL-side user pushbuttons (five, geographic N, S, E, W, C)
  - PL-side PMOD0/1 (two R.A. 2x6 receptacles)
- Security - PSBATT button battery backup
- SYSMON header
- Operational switches (power on/off, PROG_B, boot mode DIP switch)
- Operational status LEDs (INIT, DONE, PS STATUS, PGOOD)
- Power management
- System controller (MSP430)

The ZCU111 provides a rapid prototyping platform using the XCZU28DR-2EFFVG1517 device. See the *Zynq UltraScale+ RFSoC Data Sheet: Overview* (DS889) [Ref 1] for a feature set overview, description, and ordering information.

Board Specifications

Dimensions

Height: 11.811 inches (30.0 cm)

Width: 7.874 inches (20.0 cm)

Thickness: 100.8 mil (0.2743 cm)

Note: A 3D model of this board is not available.

See ZCU111 board documentation for the XDC listing and board schematics.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the ZCU111 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic (0381811) page numbers, and links to a detailed functional description of the components and board features in Chapter 3.

IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT: *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific ZCU111 version of interest for such details.*

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.

- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

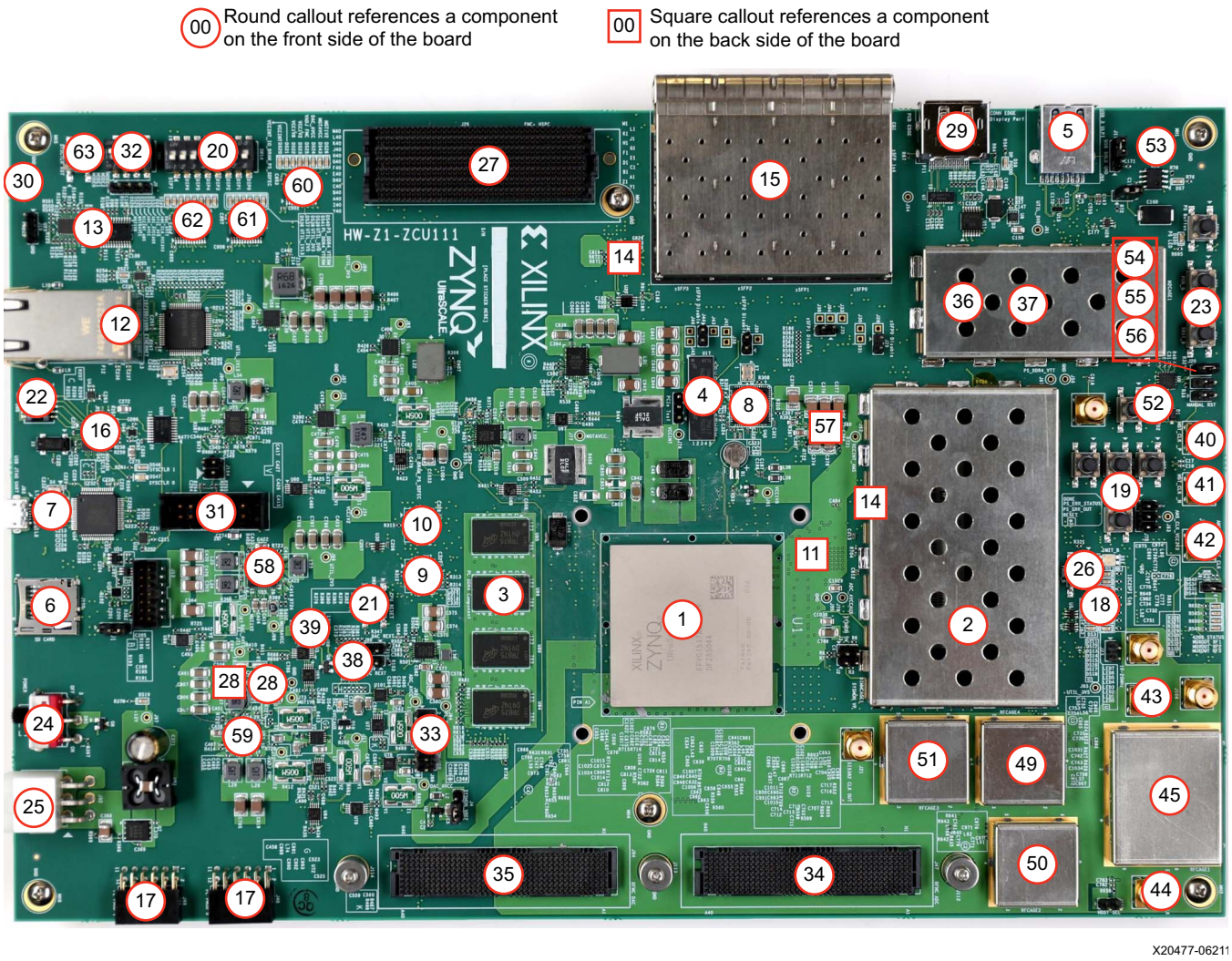

Figure 2-1: **ZCU111 Evaluation Board Components**

Table 2-1: **Board Component Locations**

Callout	Ref. Des.	Feature [B] = Bottom	Notes	Schematic Page
1	U1	Zynq UltraScale+ XCZU28DR RFSoC fansink	XCZU28DR-2FFVG1517 COFAN 30-4988-10	
2	J50	PS-Side: DDR4 SODIMM Socket, w/64-bit DDR4 SODIMM	LOTES ADDR0067-P001A with MICRON MTA4ATF51264HZ-2G6E1	43
3	U80, U94-U96	PL-Side: DDR4 Component Memory	Micron MT40A512M16JY-075E	72-75
4	U17, U18	Quad SPI Flash Memory (MIO 0–12)	Micron MT25QU02CBB8E-0SIT	25
5	U12, J96	USB 3.0 Transceiver and USB 2.0 ULPI PHY [B]	SMSC USB3320-EZK, WURTH 692122030100	24
6	J100	SD Card Interface	MOLEX 5025700893	28
7	U34, J83	UART0 (MIO 18-19)	FTDI FT4232Hx-REEL, Hirose ZX62D-AB-5P8	29
8	U46	SI5341B 10 Independent Output Any-Frequency Clock Generator	Silicon Labs SI5341B-D07833-GM	40
9	U47	Programmable User SI570 Clock	Silicon Labs SI570BAB001614DG	45
10	U49	Programmable User MGT SI570 Clock, user MGT clock, 156.250 MHz, 3.3V LVDS	Silicon Labs SI570BAB000544DG	45
11	U48	SI5382A SFP28 Clock Recovery [B]	Silicon Labs SI5382B-C-GMR	39
12	U37, P12	10/100/1000 MHz Tri-Speed Ethernet PHY, RJ45 with mag	TI DP83867IRPAP, Wurth 7499111221A	30
13	U22, U23	I2C0 (MIO 14-15), expander	TI TCA6416APWR, TI PCA9544ARGYR	26
14	U26, U27	I2C1 (MIO 16-17) [B]	Two each TI TCA9548APWR	27
15	J27, J32, J37, J42	SFP28 Module Connectors	Molex 170382-0001	38
16	U42	ZCU111 System Controller	TI MSP430F5342	32
17	J48, J49	User PMOD GPIO Connectors, PMOD0/1 RA receptacles	SULLINS PPPC062LJBN-RC	42
18	DS11-DS18	User I/O, eight user LEDs, active High	GPIO LEDs, GREEN 0603	41
19	SW9-SW13	User I/O, user pushbutton switches, active High	E-Switch TL3301EP100QG (N,S,W,E,C pattern)	41
20	SW14	User I/O, user 8-pole DIP switch, active High	C&K SDA08H1SBD	41
21	SW20	User I/O, CPU_RESET pushbutton, active High	E-switch TL3301EP100QG	41
22	SW8	System controller	5-pole C&K SDA05H1SBD	32
23	SW3, SW4	Switches, PS_SRST_B, PS_POR_B pushbuttons	E-switch TL3301EP100QG	12

Table 2-1: **Board Component Locations *(Cont'd)***

Callout	Ref. Des.	Feature [B] = Bottom	Notes	Schematic Page
24	SW16	Power On/Off Slide Switch, power ON/OFF slide switch	C&K 1201M2S3AQE2	46
25	J52	Power On/Off Slide Switch, power connector	MOLEX 39-30-1060	46
26	SW2	Program_B Pushbutton, PS_PROG pushbutton	E-switch TL3301EP100QG	12
27	J26	FPGA Mezzanine Card Interface, FMCP HSPC connector	Samtec ASP_184329_01	33-37
28	-	Board Power System, (top, [B])	Infineon regulators	47-61
29	P11	DPAUX (MIO 27-30), DisplayPort	MOLEX 0472720001	22-23
30	J19	Monitoring Voltage and Current, PMBUS connector	SULLINS PBC36SAAN	26
31	J92	System controller, MSP430 SC emulation cable connector	TYCO 5103308-2	32
32	SW6	RFSoC Device Configuration, FPGA MODE 4-pole DIP switch	4-pole C&K SDA04H1SBD	12
33	J5	SYSMON 2X6 vertical male pin header	SULLINS PBC36DAAN	3
34	J47	RF Data Converters, low profile array (LPAF) socket	Samtec LPAF-40-03.0-S-08-2-K-TR	63
35	J94	RF Data Converters, low profile array (LPAF) socket	Samtec LPAF-40-03.0-S-08-2-K-TR	64
36	U40	PS M.2 SATA Connector	Amphenol MDT420M02001	31
37	M2CAGE1	PS M.2 SATA Connector, M.2 conn. EMI cage	Leader Tech 20S-CBSFNSV-1.0x2.25x0.40	31
38	U52	Cooling Fan Connector, fan controller	Maxim MAX6643LBBAEE++	46
39	J60	Cooling Fan Connector, fan controller	Molex 22-11-2032	46
40	J14	User SMA MGT Clock, SMA USER_SMA_MGT_CLOCK_P	Rosenberger 32K10K-400L5	8
41	J15	User SMA MGT Clock, SMA USER_SMA_MGT_CLOCK_N	Rosenberger 32K10K-400L5	8
42	J95	User SMA MGT Clock, SMA RF_FPGA_REF_CLK	Rosenberger 32K10K-400L5	4
43	J108	RF clocking, U90 LMK04208 RF REFCLK SMA	Rosenberger 32K10K-400L5	67
44	J109	RF clocking, U90 LMK04208 RF external REFCLK SMA	Rosenberger 32K10K-400L5	67
45	U90	RF clocking, LMK04208 RF REFCLK	TI LMK04208	67

Table 2-1: **Board Component Locations *(Cont'd)***

Callout	Ref. Des.	Feature [B] = Bottom	Notes	Schematic Page
49	U102	RF clocking, ADC RFPLL	TI LMX2594RHAT	68
50	U103	RF clocking, DAC RFPLL	TI LMX2594RHAT	69
51	U104	RF clocking, ADC RFPLL	TI LMX2594RHAT	70
52	U6	System Reset Pushbuttons, power-on reset	Maxim MAX16025TE+	12
53	U13	USB 3.0 Transceiver and USB 2.0 ULPI PHY, USB3 power switch,	Micrel MIC2544A-1YM	24
54	J20	System Reset Pushbuttons, 2-pin HDR PS_POR_B	SULLINS PBC36SAAN	12
55	J8	System Reset Pushbuttons, 2-pin HDR PS_SRST_B	SULLINS PBC36SAAN	12
56	J9	System Reset Pushbuttons, 2-pin HDR MR_B (U6 MAX16025 POR)	SULLINS PBC36SAAN	12
57	U53	Board Power System, INFINEON PMIC1	Infineon IRPS5401MXI04TRP	47
58	U55	Board Power System, INFINEON PMIC2	Infineon IRPS5401MXI04TRP	49
59	U57	Board Power System, INFINEON PMIC3	Infineon IRPS5401MXI04TRP	51
60	U83	Power and Status LEDs, LED driver	TI SN74AVC8T245PWR	62
61	U84	Power and Status LEDs, LED driver	TI SN74AVC8T245PWR	62
62	U85	Power and Status LEDs, LED driver	TI SN74AVC8T245PWR	62
63	SW7	PB U42 MSP430 reset, PB reset (U42 MSP430).	E-switch TL3301EP100QG	32

Default Jumper and Switch Settings

Figure 2-2 shows the ZCU111 board jumper header and switch locations. Each numbered component shown in the figure is keyed to Table 2-2 (for default jumper settings) or Table 2-3 (for default switch settings). Both tables reference the respective schematic page numbers.

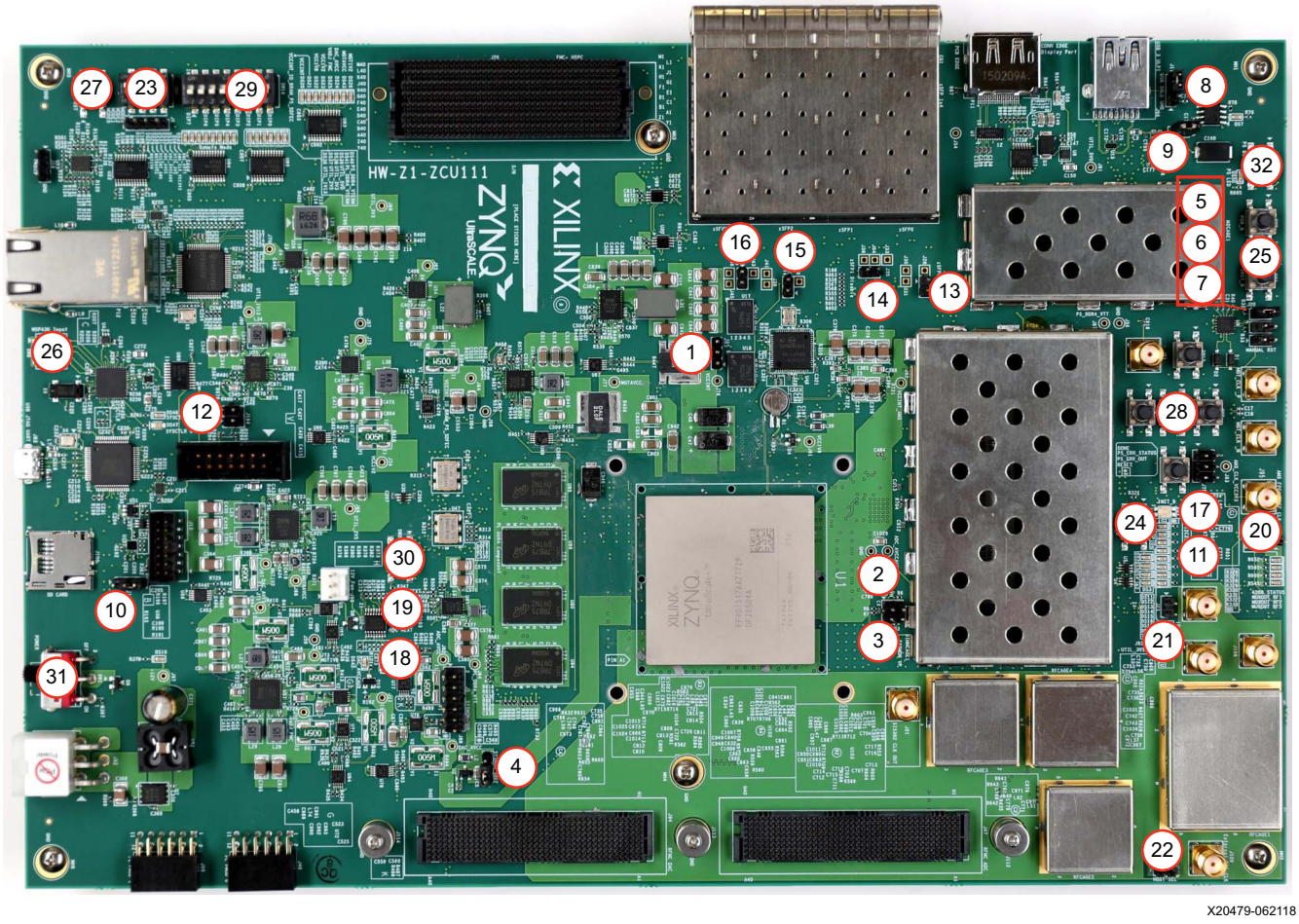

Figure 2-2: **Board Jumper Header and Switch Locations**

Jumpers

Table 2-2: **Default Jumper Settings**

Callout Number	Ref Des	Function	Default	Schematic Page
1	J85	POR_OVERRIDE	2-3	3
		1-2: Enable		
		2-3: Disable		
2	J2	SYSMON I2C address	On	3
		Off: SYSMON_VP_R floating		
		On: SYSMON_VP_P pulled down		
3	J3	SYSMON I2C Address	On	3
		Off: SYSMON_VN_R floating		
		On: SYSMON_VP_N pulled down		
4	J4	SYSMON VREFP	1-2	3
		1-2: 1.25V VREFP connected to fpga		
		2-3: VREFP connected to GND		
5	J20	Reset sequencer PS_POR_B	On	12
		Off: sequencer does not control PS_POR_B		
		On: sequencer can control PS_POR_B		
6	J8	Reset sequencer PS_SRST_B	On	12
		Off: sequencer does not control PS_SRST_B		
		On: sequencer can control PS_SRST_B		
7	J9	Reset sequencer inhibit	Off	12
		Off: sequencer normal operation		
		On: sequencer inhibit (resets will stay asserted)		
8	J17	USB 3.0 connector J96 shield connection options	2-3	24
		1-2: J96 shield capacitor C171 to GND		
		2-3: J96 shield directly to GND		
9	J18	ULPI USB3320 U12 ULPIO_VBUS_SEL option jumper	Off	24
		On: Selects U13 MIC2544A switch 5V for VBUS		
		Off: normal operation, VBUS from J96 USB3.0 conn.		
10	J1	SD3.0 U107 IP4856CX25 level-trans. ref. voltage select	1-2	28
		1-2: track SD3.0 J100 socket UTIL_3V3 3.3V		
		2-3: GND = revert to internal voltage reference		
11	J23	U93 SC18IS602IPW I2C-to-SPI bridge enable	Off	66
		On: U93 bridge RESET_B to GND, U93 inhibited		

Table 2-2: **Default Jumper Settings *(Cont'd)***

Callout Number	Ref Des	Function	Default	Schematic Page
		Off: U93 bridge enabled		
12	J164	U111 MPS430 RST_B and test pin options		32
		1-2: MSP430_RST_B connected to PMOD1_0	Open	
		2-3: MSP430_TEST connected to PMOD1_1	Open	
13	J29	SFP0 J29 enable jumper	On	38
		On: SFP0 TX_DISABLE = GND = enabled		
		Off: SFP0 TX_DISABLE = high = disabled		
14	J35	SFP1 J35 enable jumper	On	38
		On: SFP1 TX_DISABLE = GND = enabled		
		Off: SFP1 TX_DISABLE = high = disabled		
15	J40	SFP2 J40 enable jumper	On	38
		On: SFP2 TX_DISABLE = GND = enabled		
		Off: SFP2 TX_DISABLE = high = disabled		
16	J44	SFP3 J44 enable jumper	On	38
		On: SFP3 TX_DISABLE = GND = enabled		
		Off: SFP3 TX_DISABLE = high = disabled		
17	J87	USB2ANY cable select jumper	Off	66
		On: USBANY_SDO connected to I2CSPI_SDO		
		Off: USBANY_SDO not connected to I2CSPI_SDO		
18	J89	ZU28DR RFSoC U1 ADC bank 224 ADC_REXT select	Off	9
		On: bank 224 ADC_REXT pin AB8 = GND		
		Off: bank 224 ADC_REXT pin AB8 = 2.49K to GND		
19	J90	ZU28DR RFSoC U1 DAC bank 228 DAC_REXT select	Off	10
		On: bank 228 DAC_REXT pin W8 = GND		
		Off: bank 228 DAC_REXT pin W8 = 2.49K to GND		
20	J101	SPI CS select header		66
		1-2:		
		3-4:		
		5-6:		
		7-8:		
21	J111	SPI SDO select header		66
		1-2:		
		3-4:		
		5-6:		

Table 2-2: **Default Jumper Settings *(Cont'd)***

Callout Number	Ref Des	Function	Default	Schematic Page
		7-8:		
22	J110	U92 12.8MHz TXCO power	On	67
		On: U92 is on		
		Off: U92 is off		

Switches

Table 2-3: **Default Switch Settings**

Callout Number	Ref Des	Function	Default	Schematic Page
23	SW6	RFSoC U1 Mode 4-Pole DIP Switch	0010	12
		Switch OFF = 1 = High; ON = 0 = Low		
		Mode = SW6[4:1] = Mode[3:0]		
		JTAG = ON,ON,ON,ON = 0000		
		QSPI32 = ON,ON,OFF,ON = 0010		
		SD = OFF,OFF,OFF,ON = 1110		
24	SW2	PS_PROG_B pushbutton	(1)	12
25	SW3	PS_POR_B pushbutton	(1)	12
	SW4	PS_SRST_B pushbutton	(1)	12
26	SW8	MSP430 U42 5-Pole GPIO DIP switch Switch Off = 1 = High; On = 0 = Low	11111	32
27	SW8	RST_B pushbutton for MSP430 U42/MSP430 EMUL. cable J92	(1)	32
28	SW9	GPIO pushbutton (geographic) GPIO_SW_N	(1)	41
	SW10	GPIO pushbutton (geographic) GPIO_SW_W	(1)	41
	SW11	GPIO pushbutton (geographic) GPIO_SW_C	(1)	41
	SW12	GPIO pushbutton (geographic) GPIO_SW_E	(1)	41
	SW13	GPIO pushbutton (geographic) GPIO_SW_S	(1)	41
29	SW14	GPIO 8-Pole DIP switch Switch Off = 0 = Low; On = 1 = High	00000000	41
30	SW15	CPU_RESET pushbutton	(1)	41
31	SW16	Main power slide switch	off	46
32	SW19	PS MIO22_BUTTON pushbutton	(1)	11

Notes:

1. Pushbutton switch default = open (not pressed).

RFSoC Device Configuration

Zynq UltraScale+ XCZU28DR-2E RFSoC devices use a multi-stage boot process as described in the "Boot and Configuration" chapter of the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3]. Switch SW6 configuration option settings are listed in Table 2-4.

Table 2-4: **Switch SW6 Configuration Option Settings**

Boot Mode	Mode Pins [3:0]	Mode SW6 [4:1]
JTAG	0000	ON,ON,ON,ON
QSPI32	0010(1)	ON,ON,OFF,ON
SD	1110	OFF,OFF,OFF,ON

Notes:
1. Default switch setting.

JTAG

Vivado®, Xilinx SDK, or third-party tools can establish a JTAG connection to the Zynq UltraScale+ RFSoC device through the FTDI FT4232 USB-to-JTAG/USB UART device (U34) connected to micro-USB connector (J83).

Quad SPI

To boot from the dual Quad SPI nonvolatile configuration memory:

1. Store a valid Zynq UltraScale+ RFSoC boot image in the Quad SPI flash devices connected to the MIO Quad SPI interface. See the *ZCU111 Restoring Flash Tutorial* XTP515 [Ref 13] for information on programming the QSPI.
2. Set the boot mode pins SW6 [3:0] PS_MODE[3:0] as indicated in Table 2-4 for Quad SPI32.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW6 is callout 46 in Figure 2-1.

SD

To boot from an SD card:

1. Store a valid Zynq UltraScale+ RFSoC boot image file on to an SD card (and then plug the SD card into ZCU111 board socket J100).
2. Set the boot mode pins SW6 [3:0] PS_MODE[3:0] as indicated in Table 2-4 for SD.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW6 is callout 46 in Figure 2-1.

See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] for more information about Zynq UltraScale+ RFSoC configuration options.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 13 identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Figure 2-1, page 12.

Component Descriptions

Zynq UltraScale+ XCZU28DR RFSoC

[Figure 2-1, callout 1]

The ZCU111 board is populated with the Zynq UltraScale+ XCZU28DR-2FFVG1517 RFSoC, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Zynq UltraScale+ RFSoC features the Arm® flagship Cortex®-A53 64-bit quad-core processor and Cortex-R5 dual-core real-time processor.

For additional information on the Zynq UltraScale+ XCZU28DR-2FFVG1517 RFSoC, see the *Zynq UltraScale+ RFSoC Data Sheet* (DS926) [Ref 2]. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] for more information about Zynq UltraScale+ RFSoC configuration options.

Encryption Key Battery Backup Circuit

The XCZU28DR RFSoC U1 implements bitstream encryption key technology. The ZCU111 board provides the encryption key backup battery circuit shown in Figure 3-1.

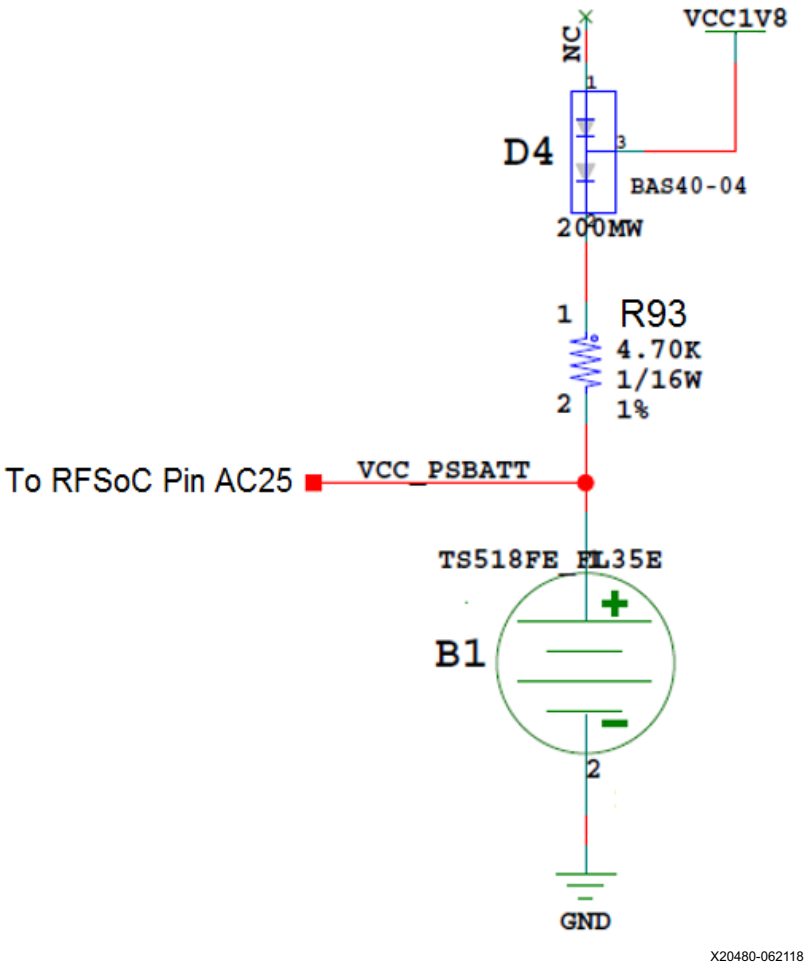

Figure 3-1: **Encryption Key Backup Circuit**

The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCZU28DR-2E RFSoC U1 V_{CC_PSBATT} pin Y23. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the UTIL_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 ΩK current limit resistor. The nominal charging voltage is 1.42V.

I/O Voltage Rails

The XCZU28DR RFSoC PL I/O bank voltages on the ZCU111 board are listed in Table 3-1.

Table 3-1: **I/O Voltage Rails**

XCZU28DR	Power Net Name	Voltage	Connected To
PL bank 64	VCC1V8	1.8V	GPIO
PL bank 65	VADJ_FMC(1)	1.8V	FMCP_HSPC LA BUS [0:16]
PL bank 66	VADJ_FMC(1)	1.8V	FMCP_HSPC LA BUS [17:32]
PL bank 67	VCC1V2	1.2V	PL_DDR4_DQ[32:63]
PL bank 68	VCCIV2	1.2V	PL_DDR4_DQ[0:31], SFPx_TX_DISABLE, SYSMON_SDA/SCL
PL bank 69	VCC1V2	1.2V	PL_DDR4 ADDR/CTRL, PMOD0&1[0:7],MSP430_GPIO[0:3]
PL bank 84	VCC1V8	1.8V	ADCIO[0:19], GPIO_SW[N,E,C,W]
PL bank 87	VCC1V8	1.8V	DACIO[0:19], GPIO_SW[S], SFP_SI5382_CLK_IN_SEL
PS bank 500	VCC1V8	1.8V	QSPI LWR/UPR, PS_GPIO2, I2Cx_SDA/SCL, UART0_RXD/TXD
PS bank 501	VCC1V8	1.8V	DP CTRL, PMU_GPO[0:5], SDIO I/F, PS_GPIO1
PS bank 502	VCC1V8	1.8V	USB I/F, ENET I/F
PS bank 503	VCC1V8	1.8V	PS CONFIG I/F
PS bank 504	VCC1V2	1.2V	PS_DDR4 64-BIT SODIMM I/F

Notes:
1. The ZCU111 board is shipped with VADJ_FMC set to 1.8V by the MSP430 system controller.

PS-Side: DDR4 SODIMM Socket

[Figure 2-1, callout 2]

The PS-side memory is wired to the Zynq UltraScale+ DDRC bank 504 hard memory controller. The PS-side bank 504 memory interface supports 260-pin 64-bit DDR4 SODIMM socket J50. The ZCU111 board is shipped with a DDR4 SODIMM installed:

- Manufacturer: Micron
- Part Number: MTA4ATF51264HZ-2G6E1
- Description:
  - 4 GByte 260-pin DDR4 SODIMM
  - Single rank x16
  - 512 Mbit x 64-bit
  - Supports 1333 MT/s – 2666 MT/s

The ZCU111 XCZU28DR RFSoC PS DDR interface performance is documented in the *Zynq UltraScale+ RFSoC Data Sheet* (DS926)[Ref 2].

The ZCU111 DDR4 SODIMM interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 4]. The DDR4 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150) [Ref 5]. For more details, see the Micron MTA4ATF51264HZ-2G6E1 data sheet at the Micron website [Ref 15].

The connections between the DDR4 SODIMM socket J50 and XCZU28DR PS bank 504 are referenced in Appendix B, Xilinx Design Constraints.

PL-Side: DDR4 Component Memory

[Figure 2-1, callout 3]

The 4 GB, 64-bit wide DDR4 memory system is comprised of four 512 Mb x 16 SDRAM, U80 and U94-U96.

- Manufacturer: Micron
- Part Number: MT40A512M16JY-075E
- Description:
  - 8 Gb (512 Mb x 16)
  - 1.2V 96-ball TFBGA
  - DDR4-2666

The ZCU111 XCZU28DR RFSoC PL DDR interface performance is documented in the *Zynq UltraScale+ RFSoC Data Sheet* (DS926)[Ref 2].

This memory system is connected to PL-side XCZU28DR banks 67, 68, and 69. The DDR4 0.6V VTT termination voltage is supplied from sink-source regulator U81.

The ZCU111 board DDR4 64-bit component memory interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 4]. The ZCU111 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150) [Ref 5]. For more details, see the Micron MTA4ATF51264HZ-2G6E1 data sheet at the Micron website [Ref 15]

The connections between the DDR4 component memories and the XCZU28DR banks are referenced in Appendix B, Xilinx Design Constraints.

PSMIO

Table 3-2 provides PS MIO peripheral mapping implemented on the ZCU111 board. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] for more information on PS MIO peripheral mapping.

Table 3-2: **MIO Peripheral Mapping**

MIO[0:25] Bank 500		MIO[26:51] Bank 501		MIO[52:77] Bank 502	
0	QSPI	26	PMU IN	52	USB0
1	QSPI	27	DPAUX	53	USB0
2	QSPI	28	DPAUX	54	USB0
3	QSPI	29	DPAUX	55	USB0
4	QSPI	30	DPAUX	56	USB0
5	QSPI	31	Not assigned/no connect	57	USB0
6	Not assigned/no connect	32	PMU OUT	58	USB0
7	QSPI	33	PMU OUT	59	USB0
8	QSPI	34	PMU OUT	60	USB0
9	QSPI	35	PMU OUT	61	USB0
10	QSPI	36	PMU OUT	62	USB0
11	QSPI	37	PMU OUT	63	USB0
12	QSPI	38	GPIO	64	GEM3
13	GPIO	39	SD1	65	GEM3
14	I2C0	40	SD1	66	GEM3
15	I2C0	41	SD1	67	GEM3
16	I2C1	42	SD1	68	GEM3
17	I2C1	43	Not assigned/no connect	69	GEM3
18	UART0	44	Not assigned/no connect	70	GEM3
19	UART0	45	SD1	71	GEM3
20	Not assigned/no connect	46	SD1	72	GEM3
21	Not assigned/no connect	46	SD1	73	GEM3
22	GPIO	48	SD1	74	GEM3
23	GPIO	49	SD1	75	GEM3
24	Not assigned/no connect	50	SD1	76	MDI03
25	Not assigned/no connect	51	SD1	77	MDI03

Quad SPI Flash Memory (MIO 0–12)

[Figure 2-1, callout 4]

The Micron dual MT25QU02GCBB8E12-0sit serial NOR flash Quad SPI flash memory can hold the boot image for the RFSoC system. This interface is used to support QSPI32 boot mode as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3].

The dual Quad SPI flash memory located at U17/U18 provides 4 Gb of non-volatile storage that can be used for configuration and data storage.

- Part number: MT25QU02GCBB8E12-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 8 bits
- Data rate: various depending on single, dual, or quad mode

The configuration and Quad SPI flash memory section of the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] provides details on using the memory. For more Quad SPI details, see the Micron MT25QU02GCBB8E12-0SIT data sheet at the Micron website [Ref 15].

The connections between the Quad SPI flash memory and XCZU28DR PS bank 500 are referenced in Appendix B, Xilinx Design Constraints.

GPIO (MIO 13, 38)

These two GPIO bits are connected to the U42 MSP430 system controller for general purpose signaling or communications between the Zynq UltraScale+ RFSoC device and the MSP430 system controller. These signals are level-shifted by TSX0108E U41. The connections between the U42 system controller and the XCZU28DR RFSoC are listed in Table 3-3.

Table 3-3: **System Controller U42 GPIO Connections to XCZU28DR U1**

XCZU28DR (U1) Pin	Net Name	MSP430 U42	
		Pin Name	Pin #
E27	MIO38_PS_GPIO1	P1_6	19
R28	MIO13_PS_GPIO2	P1_7	20

I2C0 (MIO 14-15), I2C1 (MIO 16-17)

Figure 3-2 shows a high-level view of the I2C0 and I2C1 bus connectivity.

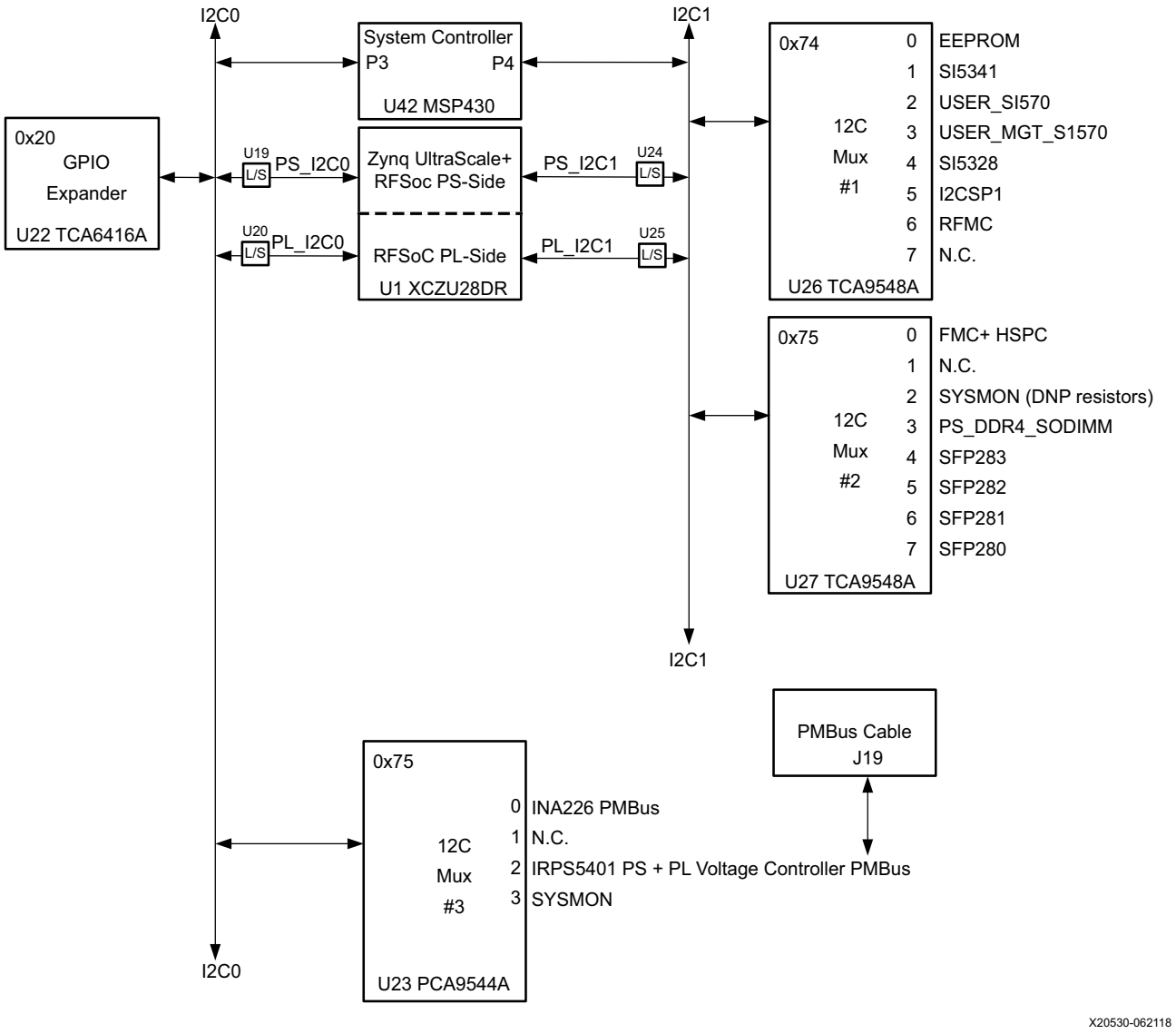

Figure 3-2: **I2C0 and I2C1 Bus Connectivity Overview**

I2C0 (MIO 14-15)

[Figure 2-1, callout 13]

The I2C bus I2C0 connects the RFSoC U1 PS bank 500, PL bank 64, and the system controller U42 to a GPIO 16-bit port expander (TCA6416A U22) and I2C switch (PCA9544A U23). The port expander enables controlling resets and power system enable pins, and accepting various alarm inputs without requiring the PL-side to be configured. The I2C0 bus also provides access to the PMBus power controllers and the INA226 power monitors via the U23 PCA9544A switch. TCA6416A U22 is pin-strapped to respond to I2C address `0x20`. The PCA9544A U23 switch is set to `0x75`.

The devices on each port of the I2C0 U22 TCA6416A port expander are listed in Table 3-4, and the devices on each bus of the I2C0 U23 PCA9544A switch are listed in Table 3-5. Figure 3-3 shows a high-level view of the I2C0 bus connectivity represented in Table 3-4 and Table 3-5.

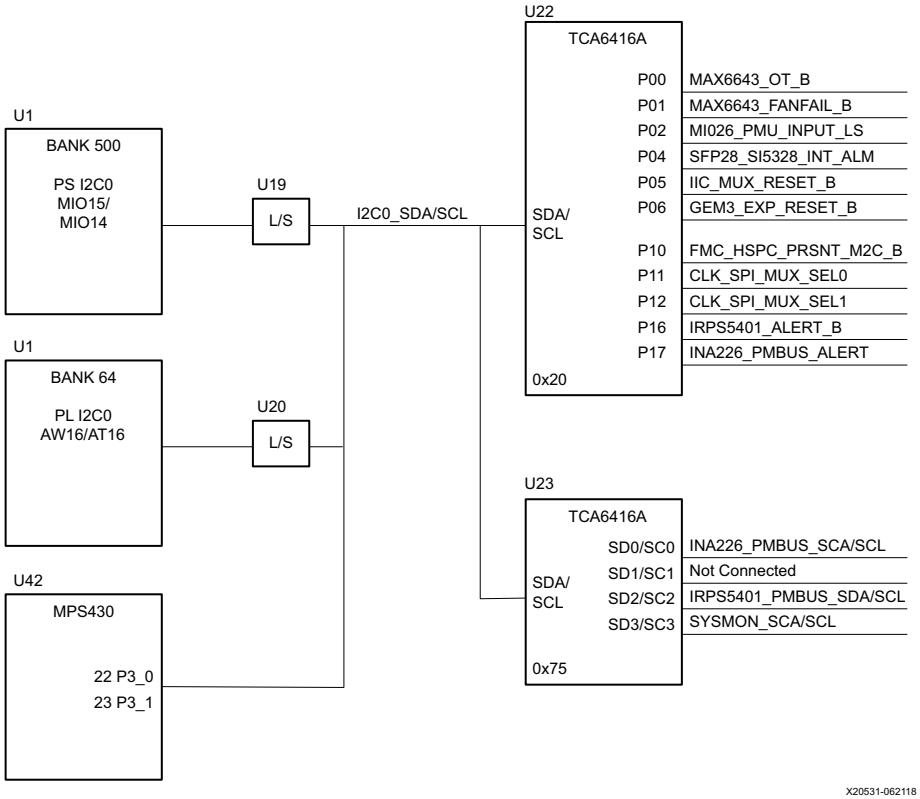

Figure 3-3: **I2C0 Bus Topology**

Table 3-4: **I2C0 Port Expander TCA6416A U22 Addr. 0x20 Connections**

TCA6416A U22		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin No.	Pin Name	Reference Designator	Device
SDA	23	I2C0_SDA	Refer to connections shown in Figure 3-3. TCA6416A U22 Addr. 0x20			
SCL	22	I2C0_SCL				
P00	4	MAX6643_OT_B	9	OT_B	U52	MAX6643
P01	5	MAX6643_FANFAIL_B	4	FANFAIL_B	U52	MAX6643
P02	6	MIO26_PMU_INPUT_LS	G25	PS_MIO26	U1	XCZU28DR
P04	8	SFP_SI5382_INT_ALM	12	INTRB	U48	SI5382A
P05	9	IIC_MUX_RESET_B	3	RESET_B	U26,U27	TCA9548A
P06	10	GEN3_EXP_RESET_B	2	B	U14	SN74LVC1G08
P10	13	FMCP_HSPC_PRSNT_M2C_B	4	OE	U45	NC7SZ66P5X
			H2	PRSNT_M2C_L	J26(H)	ASP_184329_01
			Z1	PRSNT_M2C_L	J26(Z)	ASP_184329_01
P11	14	CLK_SPI_MUX_SEL0	14	S0	U97	IDTQS3VH253QG8
P12	15	CLK_SPI_MUX_SEL1	2	S1	U97	IDTQS3VH253QG8
P16	19	IRPS5401_ALERT_B	11	INT2_B	U23	PCA9544A
			17	ALERT_B	U53,U55,U57	IRPS5401
			17	SALERT_B	U68,U70,U74,U75	IR38060
P17	20	INA226_PMBUS_ALERT	4	INT0_B	U23	PCA9544A
			3	ALERT	U3,U59-U61 U63-U66	INA226
			3	ALERT	U67,U69,U71,U73, U77,U79	

Table 3-5: **I2C0 Multiplexer PCA9544A U23 Addr. 0x75 Connections**

PCA9544A U23		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin No.	Pin Name	Reference Designator	Device
SDA	19	I2C0_SDA	Refer to connections shown in Figure 3-3. PCA9544A U23 Addr. 0x75			
SCL	18	I2C0_SCL				
Port		Mux'd I2C Bus				
0		INA226_PMBUS_SDA/SCL	4/5	SDA/SCL	See P17 in Table 3-4	INA226
2		IRPS5401_SDA/SCL	19/18	DATA/CLK	U53,U55,U57	IRPS5401
3		SYSMON_SDA/SCL	D11/B12	Bank 68	U1(1)	XCZU28DR

Notes:
1. SYSMON SDA/SCL are level-shifted via U99.

I2C1 (MIO 16-17)

[Figure 2-1, callout 14]

The I2C bus I2C1 connects the RFSoC U1 PS bank 500, PL bank 64, and system controller U42 to two I2C switches (TCA9548A U26 and U27). These I2C1 connections enable I2C communications with other I2C capable target devices. TCA9548A U26 is pin-strapped to respond to I2C address 0x74. TCA9548A U27 is pin-strapped to respond to I2C address 0x75. Figure 3-4 shows a high-level view of the I2C1 bus connectivity represented in Table 3-6 and Table 3-7.

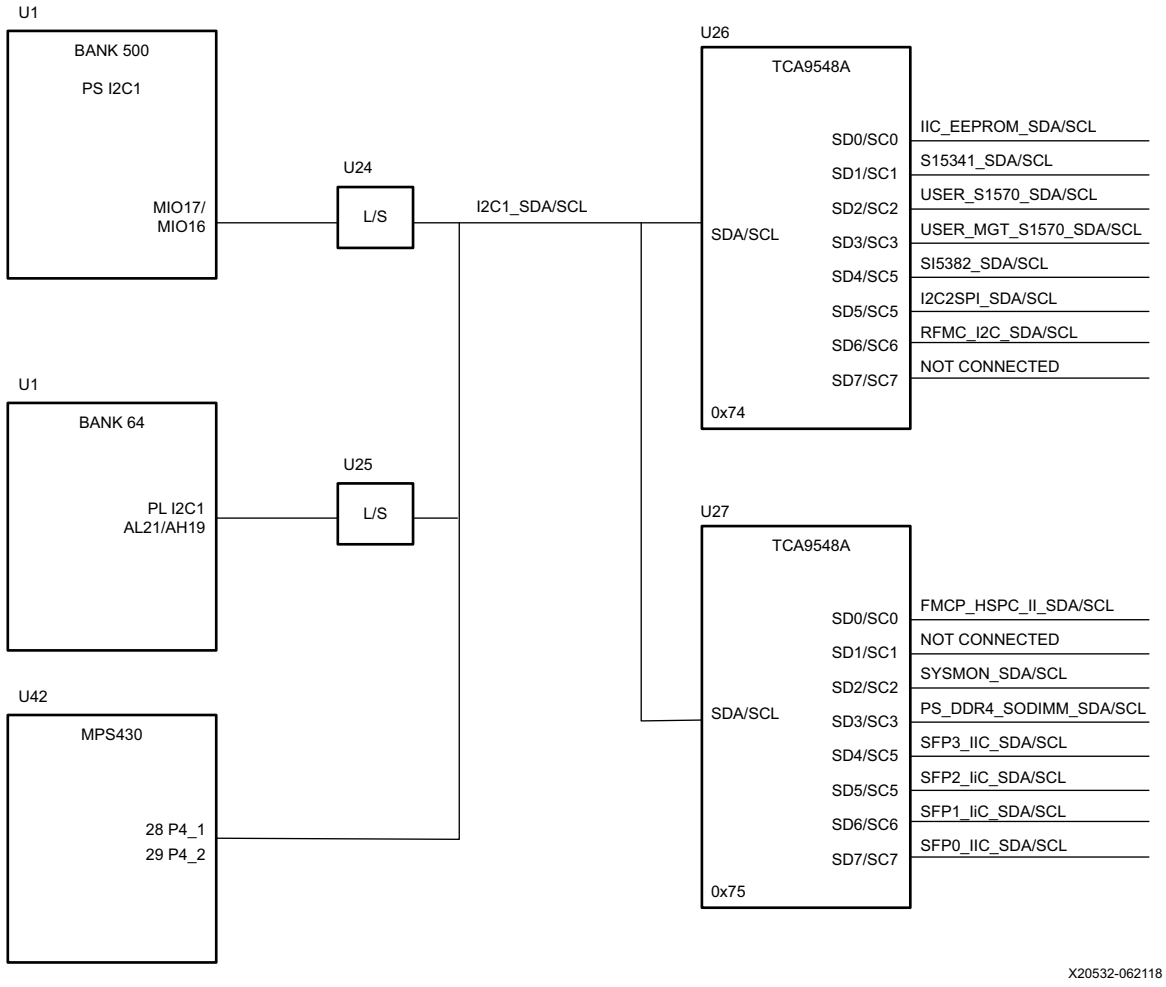

Figure 3-4: **I2C1 Bus Topology**

Table 3-6: **I2C1 TCA9548A U26 Adr. 0x74 Connections**

TCA9548A U26 (Addr 0x74) Port	I2C1 Bus Device	Target Device Address
0	EEPROM U88	0X54
1	Si5341 clock U46	0x36
2	USER Si570 clock U47	0X5D
3	USER MGT Si570 clock U49	0X5D
4	Si5382 (SFP28 ClK recovery) U48	0x68
5	SC18IS602B U93	0x2F
6	LPAF-40 J47 connector	USER
7	No connection	NA

Table 3-7: **I2C1 TCA9548A U27 Adr. 0x75 Connections**

TCA9548A U27 (Addr 0x75) Port	I2C1 Bus Device	Target Device Address
0	FMCP HSPC J26	0x##
1	Not connected	NA
2	SYSMON U1 BANK 68	0x32
3	PS DDR4 SODIMM SKT. J50	0x51
4	SFP3 P2	0x50
5	SFP2 P1	0x50
6	SFP1 P2	0x50
7	SFP0 P1	0x50

For more information on the TCA9548A and PCA9544A, see the Texas Instruments website [Ref 20].

UART0 (MIO 18-19)

[Figure 2-1, callout 7]

This is the primary Zynq UltraScale+ RFSoC PS-side UART interface and is connected to the FTDI U34 FT4232HL USB-to-Quad-UART bridge port B through TXS0108E level-shifter U21. The FT4232HL U34 port assignments are listed in Table 3-8. The FT4232HL UART interface circuit is shown in Figure 3-5.

Table 3-8: **FT4232HL Port Assignments**

FT4232HL U34	Zynq UltraScale+ RFSoC U1
Port A JTAG	ZCU111 JTAG chain
Port B UART0	PS_UART0 (MIO 18-19)
Port C UART2	PL_UART2 bank 64
Port D UART3	U42 system controller UART

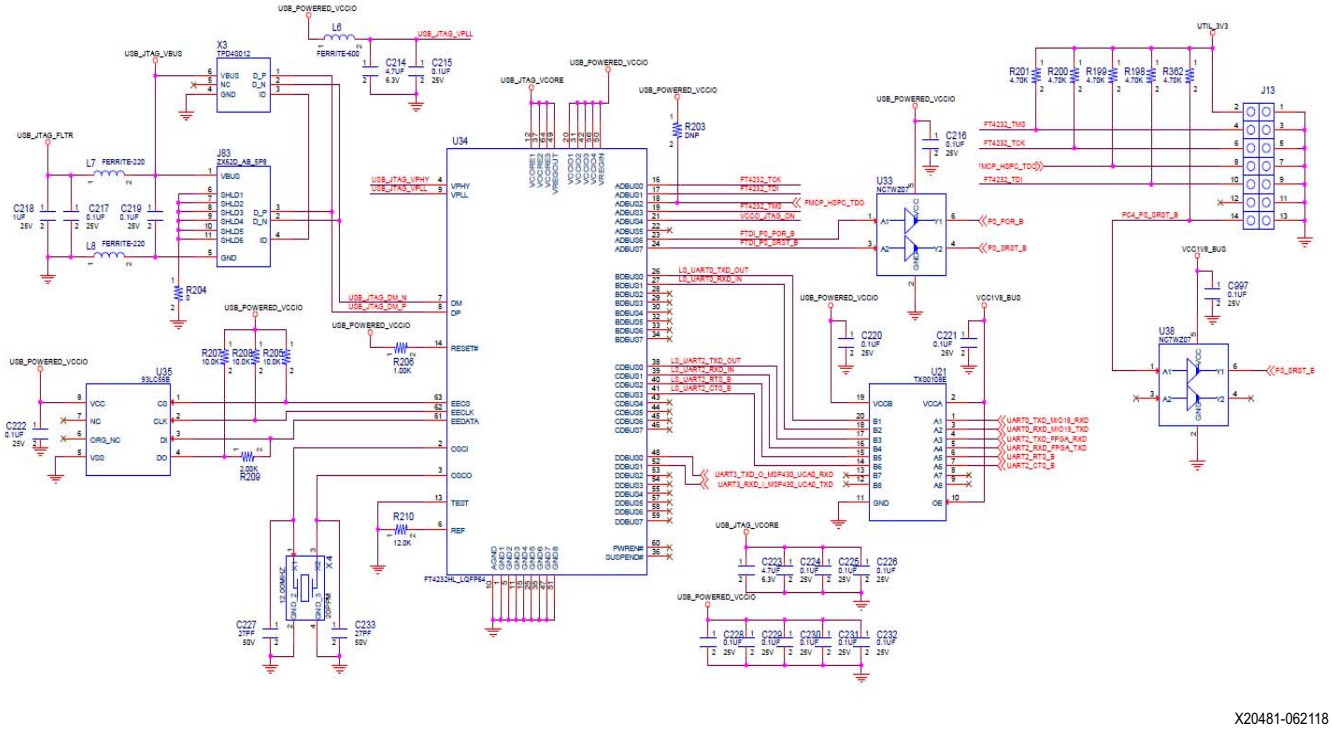

Figure 3-5: **ZCU111 FT4232HL UART Connections**

The FT4232HL U34 UART connections are listed in Table 3-9.

Table 3-9: **FT4232HL UART Connections**

FT4232HL U34 Pin	Schematic Net Name	Level Shifter	Level-Shifted Net Name	Target UART Ref Des., Pin	
26	LS_UART0_TXD_OUT	U21	UART0_TXD_MIO18_RXD	U1	Y27
27	LS_UART0_RXD_IN	U21	UART0_RXD_MIO19_TXD	U1	W28
38	LS_UART2_TXD_OUT	U21	UART2_TXD_FPGA_RXD	U1	AT15
39	LS_UART0_RXD_IN	U21	UART2_RXD_FPGA_TXD	U1	AU15
40	LS_UART2_RTS_B	U21	UART2_RTS_B	U1	AU14
41	LS_UART2_CTS_B	U21	UART2_CTS_B	U1	AT14
48	UART3_TXD_O_MSP430_UCA0_RXD	NA	NA	U42	26
52	UART3_RXD_I_MSP430_UCA0_TXD	NA	NA	U42	25

For more information on the FT4232HL, see the Future Technology Devices International Ltd website [Ref 26].

UART1 (MIO 20-21)

The PS-side UART1 is not connected.

GPIO (MIO 22-23)

The PS-side pushbutton SW19 is connected to MIO22 (pin U1.Y28). The PS-side LED DS50, which is physically placed adjacent to the pushbutton, is connected to MIO23 (pin U1.U29).

CAN1 (MIO 24-25)

The PS-side CAN bus TX and RX MIO pins are not connected.

PMU GPI (MIO 26)

The PS-side MIO 26 is reserved as an input to the PMU for indicating a warm boot. PS bank 501 MIO26 (U1.G25) is connected to the I2C0 U22 TCA6416A bus expander (port P02 U22.6) through a 0Ω series resistor R92. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] for more details about the PMU interface.

DPAUX (MIO 27-30)

[Figure 2-1, callout 29]

The Zynq UltraScale+ RFSoC provides a VESA DisplayPort 1.2 source-only controller that supports up to two lanes of main link data at rates of 1.62 Gb/s, 2.70 Gb/s, or 5.40 Gb/s. The

DisplayPort standard defines an auxiliary channel that uses LVDS signaling at a 1 Mb/s data rate, which is translated from single-ended MIO signals to the differential DisplayPort AUX channel, DPAUX (see Table 3-10). The DisplayPort circuit is shown in Figure 3-6.

Table 3-10: **DPAUX/MIO Connections**

XCZU28DR (U1) Pin	Net Name	SN74AVC4T245 Level Shifter U10	
		Pin Name	Pin #
D25	MIO30_DP_AUX_IN	2A1	8
B25	MIO29_DP_OE	1A2	7
F25	MIO28_DP_HPD	2A2	9
C25	MIO27_DP_AUX_OUT	1A1	6

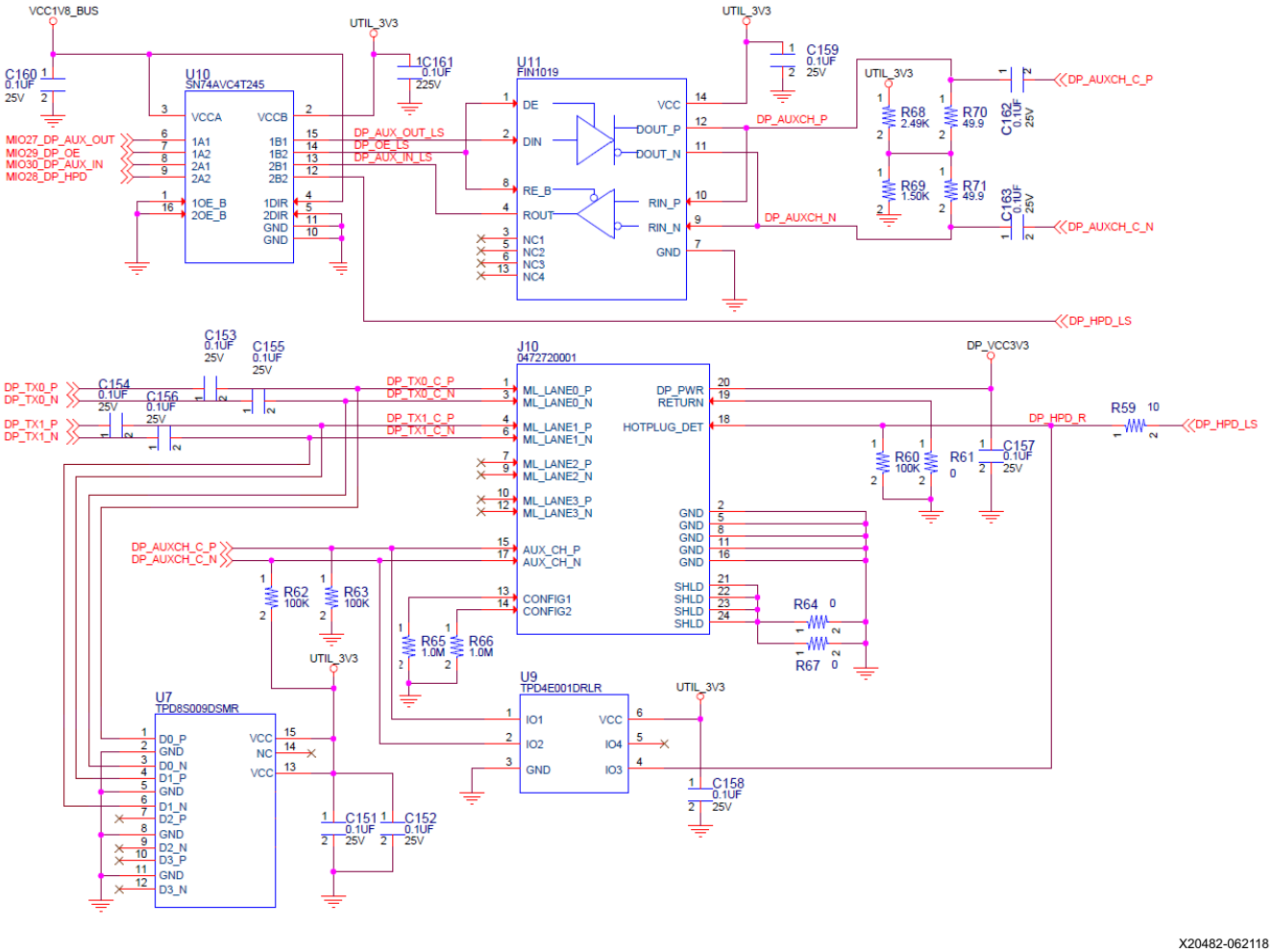

Figure 3-6: **DisplayPort Circuit**

PMU GPO (MIO 32-37)

The platform management unit (PMU) in the Zynq UltraScale+ RFSoC device signals power domain changes using the PMU output pins. The Zynq UltraScale+ RFSoC device PMU GPO pins are connected to inputs of the MSP430 system controller via TXS0108E level-shifter U41. The RFSoC U1 bank 501 and MSP430 U42 pin numbers are listed in Table 3-11.

Table 3-11: **XCZU28DR U1 to MSP430 Connections**

XCZU28DR (U1) Pin	Net Name	MSP430 U42	
		Pin Name	Pin #
F26	MIO37_PMU_GPO5	P1_0	13
C27	MIO36_PMU_GPO4	P1_1	14
E26	MIO35_PMU_GPO3	P1_2	15
B27	MIO34_PMU_GPO2	P1_3	16
A27	MIO33_PMU_GPO1	P1_4	17
A26	MIO32_PMU_GPO0	P1_5	18

Through the I2C0 bus RFSoC MIO pins, the PMU has access to the board power controllers and power monitors. See Figure 3-3, page 29 for more details.

See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] for more details about the PMU interface.

SD1 (MIO 39-51)

A PS-side interface to an SD card connector is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD3.0 access post boot.

SD Card Interface

[Figure 2-1, callout 6]

The ZCU111 board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and devices. Information for the SD I/O card specification can be found at the SanDisk Corporation [Ref 17] or SD Association [Ref 18] websites. The ZCU111 SD card interface supports the SD1_LS configuration boot mode documented in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3].

The SDIO signals are connected to XCZU28DR RFSoC PS bank 501, which has its VCCMIO set to 1.8V. The six SD interface nets MIOxx_SDIO_DAT[0:3], MIO50_SDIO_CMD, and MIO51_SDAIO_CLK each have a series 30Ω resistor at the bank 501 source. An NXP IP4856CX25 SD 3.0-compliant voltage level-translator U107 is present between the XCZU28DR RFSoC and the SD card connector (J100). The NXP IP4856CX25 U107 device provides SD3.0 capability with SDR104 performance.

Figure 3-7 shows the connections of the SD card interface on the ZCU111 board.

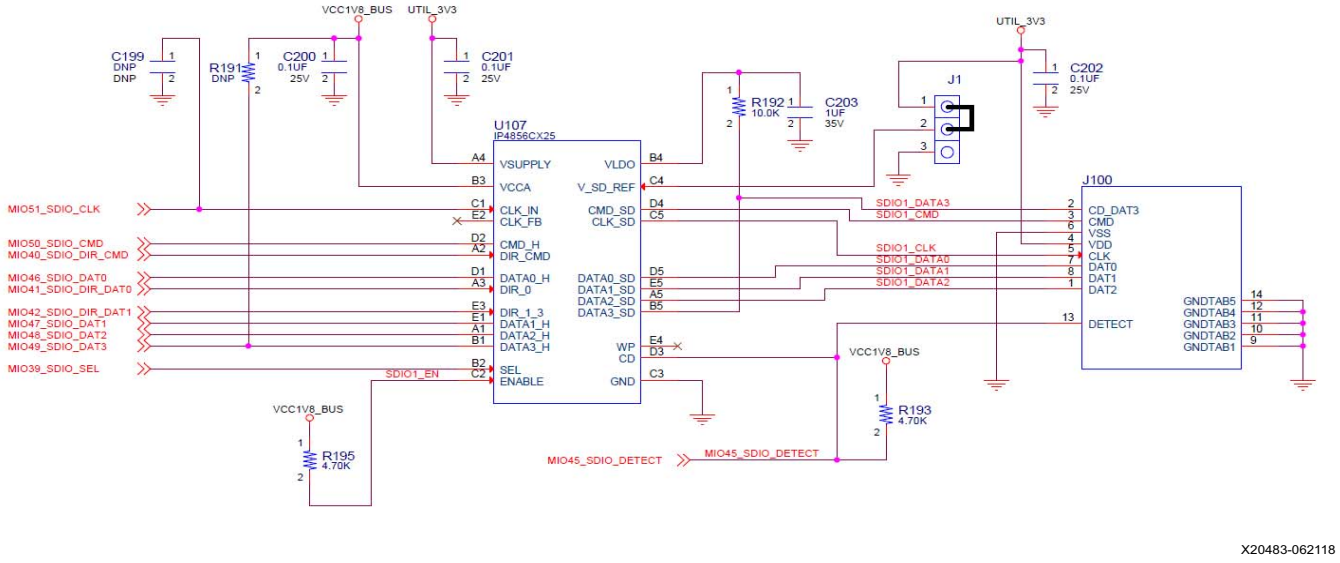

Figure 3-7: **SD Card Interface**

The NXP SD3.0 level shifter is mounted on an Aries adapter board that has the pin mapping shown in Table 3-12.

Table 3-12: **IP4856CX25 U107 Adapter Pin-Out**

Aires Adapter Pin Number	IP4856CX25 U107 Pin Number	IP4856CX25 U107 Pin Name
1	C1	CLK_IN
2	C3	GND
3	D3	CD
4	D2	CMD_H
5	E2	CLK_FB
6	E4	WP
7	B4	VLDO
8	C4	VSD_REF
9	A3	DIR_0
10	A4	VSUPPLY
11	B3	VCCA
12	A2	DIR_CMD
13	D1	DATA0_H
14	B2	SEL
15	B1	DATA3_H

Table 3-12: **IP4856CX25 U107 Adapter Pin-Out *(Cont'd)***

Aires Adapter Pin Number	IP4856CX25 U107 Pin Number	IP4856CX25 U107 Pin Name
16	E1	DATA1_H
17	E3	DIR_1_3
18	A1	DATA2_H
19	E5	DATA1_SD
20	D5	DATA0_SD
21	C5	CLK_SD
22	D4	CMD_SD
23	B5	DATA3_SD
24	A5	DATA2_SD
25	C2	ENABLE

The connections between the SD NXP IP4856CX25 (U107) level-shifter and the XCZU28DR RFSoC PS bank 501 are referenced in Appendix B, Xilinx Design Constraints.

USB0 (MIO 52-63)

The USB interface on the PS-side serves multiple roles as a host or device controller. The USB 3.0 interface is supported by the RFSoC GTR interface while the USB 2.0 capabilities of the SMSC USB3320C controller are shared on a common USB 3.0 micro USB type A connector (J96).

USB 3.0 Transceiver and USB 2.0 ULPI PHY

[Figure 2-1, callout 5]

The ZCU111 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI transceiver at U12 to support a USB connection to the host computer (see Figure 3-8). A USB cable is supplied in the ZCU111 evaluation kit (standard-A connector to host computer, USB 3.0 A connector to ZCU111 board connector J96). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device, which drives the physical USB bus. Using the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

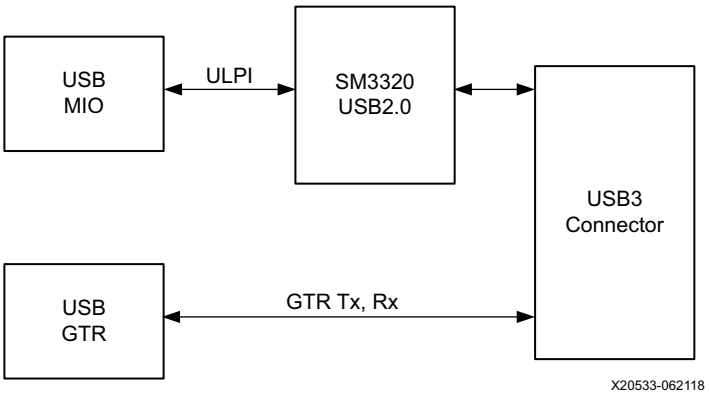

Figure 3-8: **USB Interface**

The USB3320 is clocked by a 24 MHz crystal (X2). See the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details [Ref 16]. The interface to the USB3320 PHY is implemented through the IP in the XCZU28DR RFSoC PS.

Table 3-13 describes the jumper settings for the USB 2.0 circuit.

Note: The bold text in Table 3-13 identifies the default shunt positions for USB 2.0 high-speed on-the-go (OTG) mode.

Table 3-13: **USB Jumper Settings**

Header	Function	Shunt Position	Notes
J18	VBUS select	ON = Device mode (150 µF) and VBus power source **OFF = Device mode (5.7 µF)**	VBUS load capacitance
J17	Shield select	**Position 2-3 = Shield connected to GND** Position 1-2 = Shield floating	Optional C171 in position 1-2

Note: The shield for the USB 3.0 micro-B connector (J96) can be tied to GND by a jumper on header J17 pins 2-3 (default). The USB shield can optionally be connected through a series capacitor to GND by installing a capacitor (body size 0402) at location C171 and jumping pins 1-2 on header J17.

The USB3320 ULPI U12 transceiver circuit (see Figure 3-9) has a Micrel MIC2544 high-side programmable current limit switch (U13). This switch has an open-drain output fault flag on pin 2, which turns on LED DS7 if over current or thermal shutdown conditions are detected. DS7 is located in the U13 circuit area (Figure 2-1, callout 53). Figure 3-9 shows the ULPI U12 transceiver circuit.

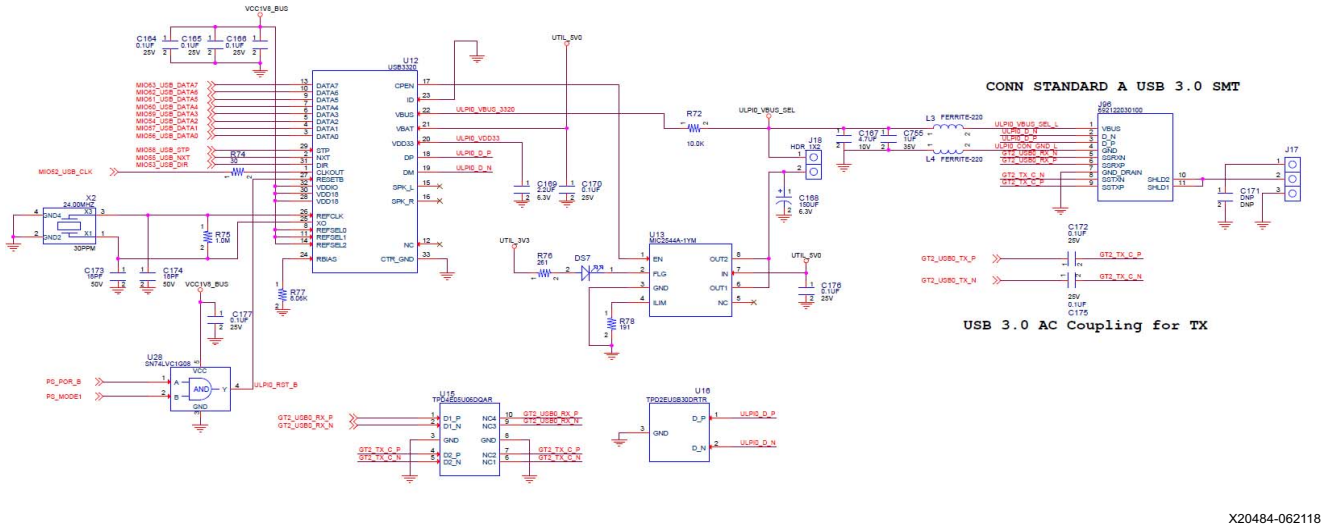

Figure 3-9: **USB3320 ULPI Transceiver Circuit**

The connections between the USB 2.0 PHY (U12) and the XCZU28DR RFSoC PS bank 502 are referenced in Appendix B, Xilinx Design Constraints.

GEM3 Ethernet (MIO 64-77)

The PS-side Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface (see Figure 3-10), which connects to a TI DP83867IRPAP Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector. The RGMII Ethernet PHY is boot strapped to PHY address `5'b01100` (`0x0C`) and Auto Negotiation is set to *Enable*. The communication with the device is described in the DP83867 RGMII PHY data sheet [Ref 20].

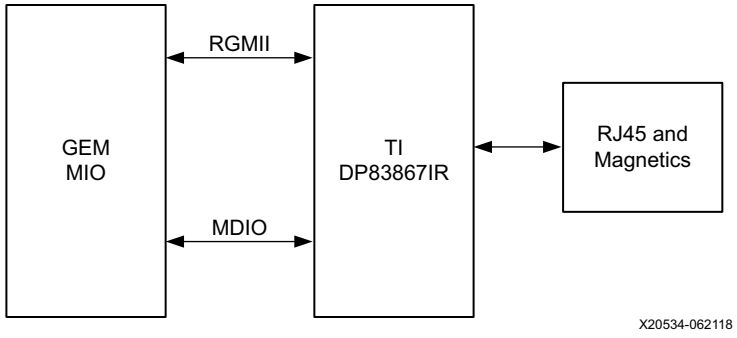

Figure 3-10: **Ethernet Block Diagram**

10/100/1000 MHz Tri-Speed Ethernet PHY

[Figure 2-1, callout 12]

The ZCU111 board uses the TI DP83867IRPAP Ethernet RGMII PHY [Ref 20] (U37) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Wurth 7499111221A RJ-45 connector (P12) with built-in magnetics. The Ethernet connections from XCZU28DR RFSoC U1 to the DP83867IRPAP PHY device at U37 are listed in Table 3-14.

Table 3-14: **DP83867 PHY Connections to XCZU28DR RFSoC**

XCZU28DR (U1) Pin	Net Name	DP83867 PHY U37	
		Pin #	Pin Name
J31	MIO64_ENET_TX_CLK	40	GTX_CLK
J32	MIO65_ENET_TX_D0	38	TX_DO
J34	MIO66_ENET_TX_D1	37	TX_D1
K28	MIO67_ENET_TX_D2	36	TX_D2
K29	MIO68_ENET_TX_D3	35	TX_D3
K30	MIO69_ENET_TX_CTRL	52	TX_EN_TX_CTRL
K31	MIO70_ENET_RX_CLK	43	RX_CLK
K32	MIO71_ENET_RX_D0	44	RX_DO
K33	MIO72_ENET_RX_D1	45	RX_D1
K34	MIO73_ENET_RX_D2	46	RX_D2
L29	MIO74_ENET_RX_D3	47	RX_D3
L30	MIO75_ENET_RX_CTRL	53	RX_DV_RX_CTRL
L33	MIO76_ENET_MDC	20	MDC
L34	MIO77_ENET_MDIO	21	MDIO

Ethernet PHY Reset

[Figure 2-1, callout 12]

The DP83867IRPAP PHY U37 LED interface is shown in Figure 3-11. The DP83867IRPAP can be reset by the GEN3_EXP_RESET_B signal via the I2C0 TCA6416A U22 bus expander P06 pin 10 or the PS_POR_B signal generated by the MAX16025 U6 POR device pin 11. The SW3 pushbutton at the MAX16025 U6 pin 6 input also triggers a PS_POR_B signal.

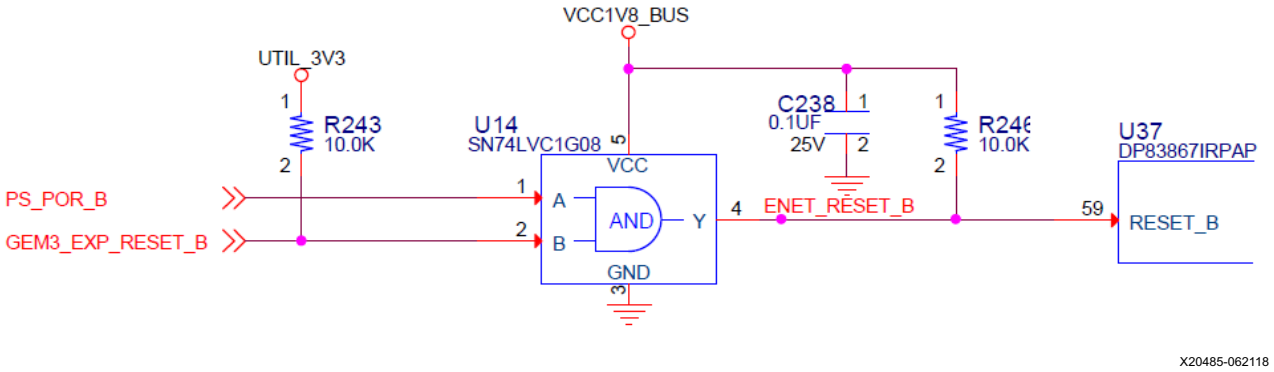

Figure 3-11: **Ethernet PHY Reset Circuit**

Ethernet PHY LED Interface

[Figure 2-1, callout 9]

The DP83867IRPAP PHY U37 LED interface (LED_0, LED_2) uses the two LEDs embedded in the P12 RJ45 connector bezel. The LED functional description is listed in Table 3-15.

Table 3-15: **Ethernet PHY LED Functional Description**

DP83867IR PHY U37 Pin		Type	Description
Name	Number		
LED_2	61	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits. ***Note:*** This pin is a strap configuration pin for RGZ devices only.
LED_1	62	S, I/O, PD	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	63	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be repurposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC. LED_2 is assigned to ACT (activity indicator) and LED_0 indicates link established. For more Ethernet PHY details, see the TI DP83867 data sheet [Ref 20]. LED_1 (100BASE-T link established) is a separate LED DS27 located on the top side of the board near the RJ45 P12 connector (Figure 2-1, callout 12).

Programmable Logic JTAG Programming Options

[Figure 2-1, callouts 7 and 63]

ZCU111 JTAG chain:

- J83 USB micro AB connector connected to U34 FT4232HL USB-JTAG bridge
- J13 2x7 2 mm shrouded, keyed JTAG pod flat cable connector

The ZCU111 board JTAG chain is shown in Figure 3-12.

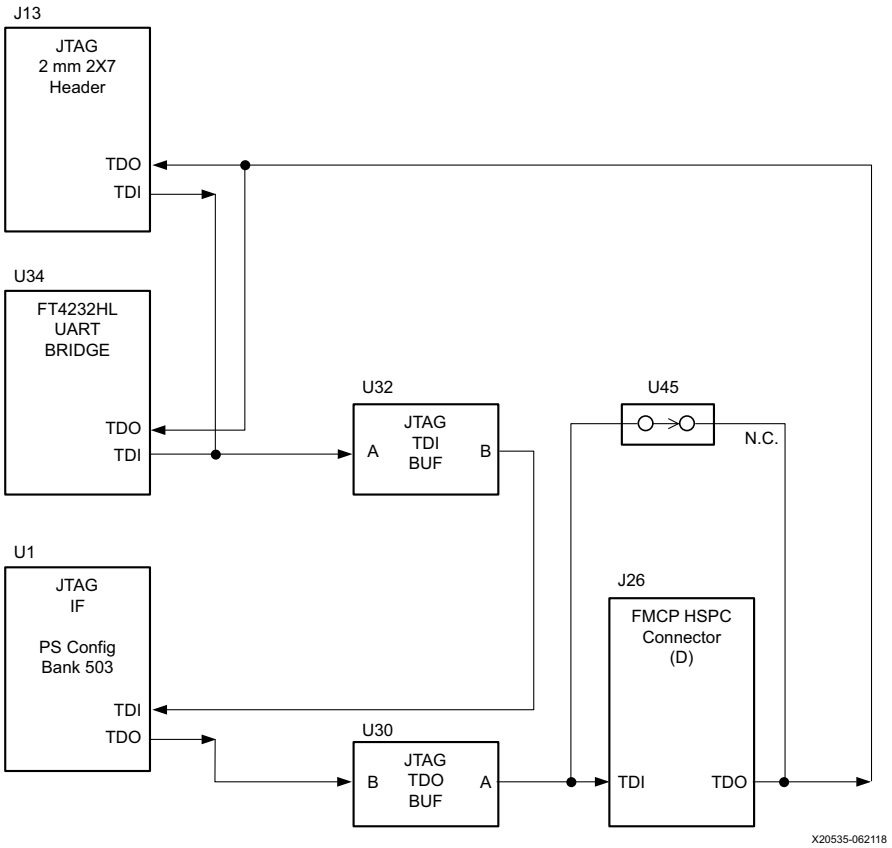

Figure 3-12: **JTAG Chain Block Diagram**

FMC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to J26, it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switch U45. The SPST switch is normally closed and transitions to an open state when an FMC is attached. Switch U45 adds an attached FMC to the JTAG chain as determined by the FMCP_HSPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection using a device or bypass jumper to ensure that the JTAG chain connects to the U1 XCZU28DR RFSoC.

Clock Generation

The ZCU111 board provides fixed and variable clock sources for the XCZU28DR RFSoC. Table 3-16 lists the source devices for each clock.

Table 3-16: **Clock Sources**

Clock (Net) Name	Frequency	Clock Source
Fixed Frequency Clocks		
PS_REF_CLK	33.33 MHz	U46 SI5341B clock generator
CLK_100	100 MHz	
CLK_125	125 MHz	
GTR_REF_CLK_SATA	125 MHz	
GTR_REF_CLK_USB3	26 MHz	
GTR_REF_CLK_DP	27 MHz	
Programmable Frequency Clocks		
USER_SI570	300 MHz (default)	U47 SI570 I2C PROG. OSC.
USER_MGT_SI570	156.25 MHz (default)	U49 SI570 I2C PROG. OSC.
USER_SMA_MGT_CLOCK	User-provided source	J14 (P)/J15 (N) SMA CONN.
SFP_SI5382_CLOCKS	Variable	U48 SI5382A clock recovery

Table 3-17 lists the connections for each clock.

Table 3-17: **Clock Connections to XCZU28DR U1**

Clock Source Ref. Des. and Pin	Net Name	I/O Standard	XCZU28DR (U1) Pin
U46 SI5341B Clock Generator			
U46.59	PS_REF_CLK (series R310)	(1)	AC30
U46.45	CLK_125_P	LVDS	AL17
U46.44	CLK_125_N	LVDS	AM17
U46.42	CLK_100_P	LVDS	AM15
U46.41	CLK_100_N	LVDS	AN15
U46.35	GTR_REF_CLK_SATA_P	(2)	AC34
U46.34	GTR_REF_CLK_SATA_N	(2)	AC35
U46.31	GTR_REF_CLK_USB3_P	(2)	AE34
U46.30	GTR_REF_CLK_USB3_N	(2)	AE35
U46.24	GTR_REF_CLK_DP_P	(2)	AG34
U46.23	GTR_REF_CLK_DP_N	(2)	AG35
U47 SI570 I2C Prog. Oscillator (300 MHz default)			
U47.4	USER_SI570_P	LVDS	J19
U47.5	USER_SI570_N	LVDS	J18
U49 SI570 I2C Prog. Oscillator (156.250 MHz default)			
U49.4	USER_MGT_SI570_P	(2)	V31
U49.5	USER_MGT_SI570_N	(2)	V32
J14 (P)/J15 (N) SMA Connectors			
J14	USER_SMA_MGT_CLOCK_P	(2)	T31
J15	USER_SMA_MGT_CLOCK_N	(2)	T32
U48 SI5382A Clock Recovery			
U48.1	SFP_SI5382_IN1_P	(2)	AA33
U48.2	SFP_SI5382_IN1_N	(2)	AA34
U48.21	SFP_SI5382_OUT_P	(2)	Y31
U48.20	SFP_SI5382_OUT_N	(2)	Y32
U48.63	SFP_REC_CLOCK_P	LVDS(3)	AW14
U48.64	SFP_REC_CLOCK_N	LVDS(3)	AW13

Notes:

1. U1 XCZU28DR bank 503 supports LVCMOS18 level inputs.
2. Series capacitor coupled, U1 MGT (I/O standards do not apply).
3. Series capacitor coupled.

SI5341B 10 Independent Output Any-Frequency Clock Generator

[Figure 2-1, callout 8]

- Clock generator: Silicon Labs SI5341B-D07833-GM
- Jitter: <100 fs RMS typical
- Differential and single-ended outputs

The SI5341B is a one-time programmable clock source. The clock circuit is shown in Figure 3-13.

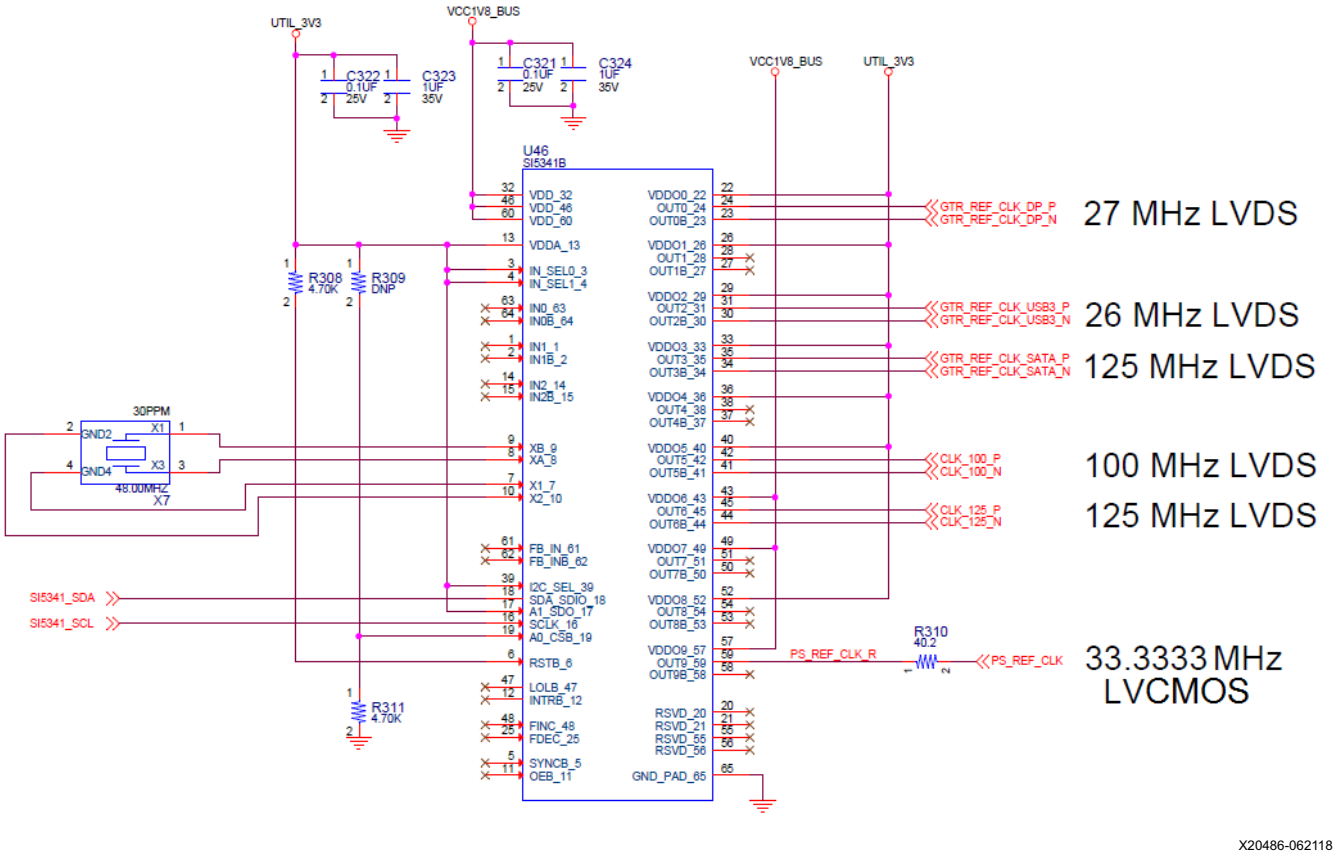

Figure 3-13: **SI5341B Clock Generator**

Programmable User SI570 Clock

[Figure 2-1, callout 9]

The ZCU111 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U47) connected to the GC inputs of PL bank 69. The USER_SI570_P and USER_SI570_N clock signals are connected to XCZU28DR RFSoC U1 pins J19 and J18, respectively. At power-up, the user clock defaults to an output frequency of 300.000 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through the I2C1 bus interface. Power cycling the ZCU111 board reverts this user clock to the default frequency of 300.000 MHz.

This oscillator can be reprogrammed from MSP430 system controller U42 (see TI MSP430 System Controller, page 88 for more system controller information and the ZCU111 web page for the tutorial on the system controller user interface (XTP517) [Ref 11].

- Programmable oscillator: Silicon Labs Si570BAB001614DG (10 MHz-810 MHz, 300 MHz default)
- LVDS differential output
- Total Stability: 61.5 ppm

The programmable user clock circuit is shown in Figure 3-14.

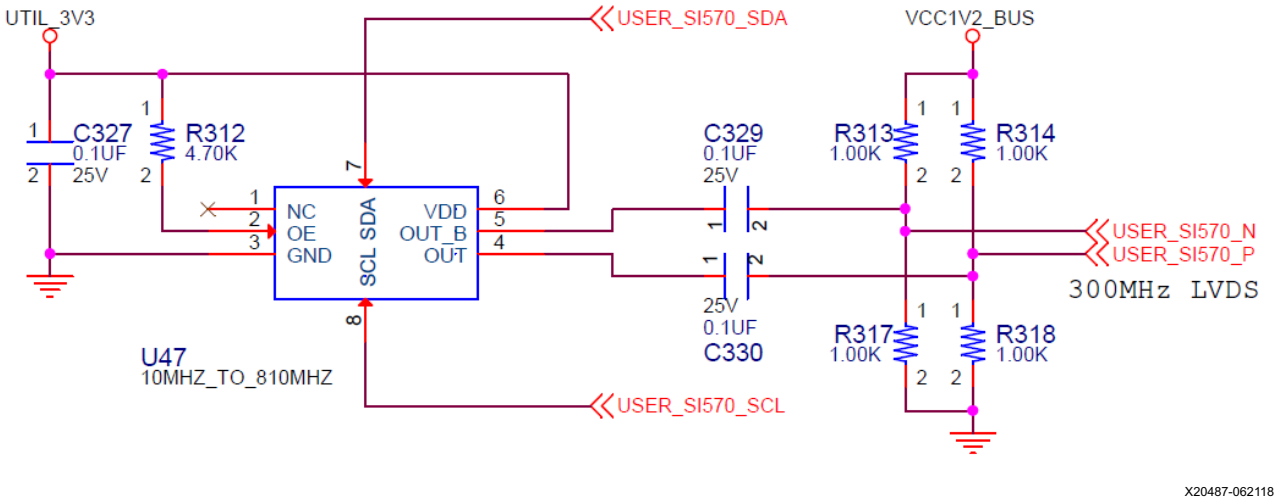

Figure 3-14: **Programmable User Clock**

Programmable User MGT SI570 Clock

[Figure 2-1, callout 10]

The ZCU111 board has a programmable low-jitter 3.3V LVDS SI570 differential oscillator (U49) connected to the XCZU28DR U1 GTY bank 129. The USER_MGT_SI570_CLOCK_P and USER_MGT_SI570_CLOCK_N clock signals are connected through series capacitors to XCZU28DR RFSoC U1 pins V31 and V32, respectively. At power-up, the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the ZCU111 board reverts this user clock to the default frequency of 156.250 MHz.

This oscillator can be reprogrammed from MSP430 system controller U41 (see TI MSP430 System Controller, page 95 for more system controller information and the ZCU111 web page for the tutorial on the system controller user interface (XTP517) [Ref 11].

- Programmable oscillator: Silicon Labs Si570BAB000544DG (10 MHz-810 MHz, 156.250 MHz default)
- LVDS differential output
- Total stability: 61.5 ppm

The programmable user clock MGT circuit is shown in Figure 3-15.

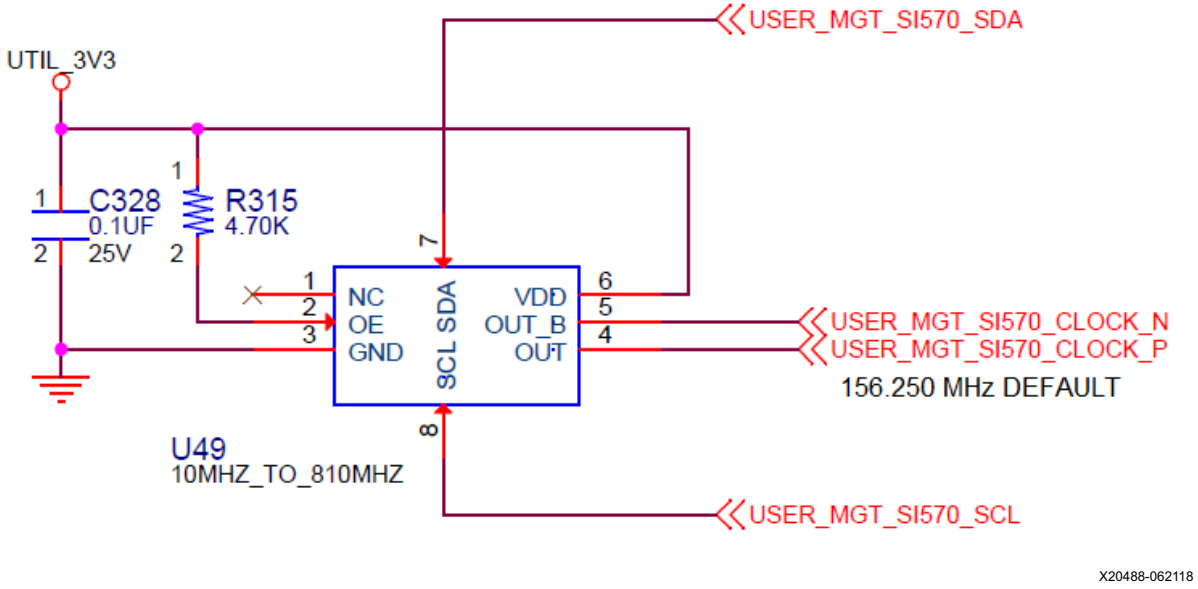

Figure 3-15: **Programmable User MGT Clock**

User SMA MGT Clock

[Figure 2-1, callout 48]

The ZCU111 board provides a pair of SMAs for differential AC coupled user MGT clock input into FPGA U1 GTY bank 130. This differential signal pair is series-capacitor coupled. The P-side SMA J14 signal USER_SMA_MGT_CLOCK_P is connected to U1 MGTREFCLK1P pin T31, and the N-side SMA J15 signal USER_SMA_MGT_CLOCK_N is connected to U1 MGTREFCLK1N pin T32. The transceiver reference clock pin absolute input voltage range is –0.5V min. to 1.3V max. The user SMA MGT clock circuit is shown in Figure 3-16.

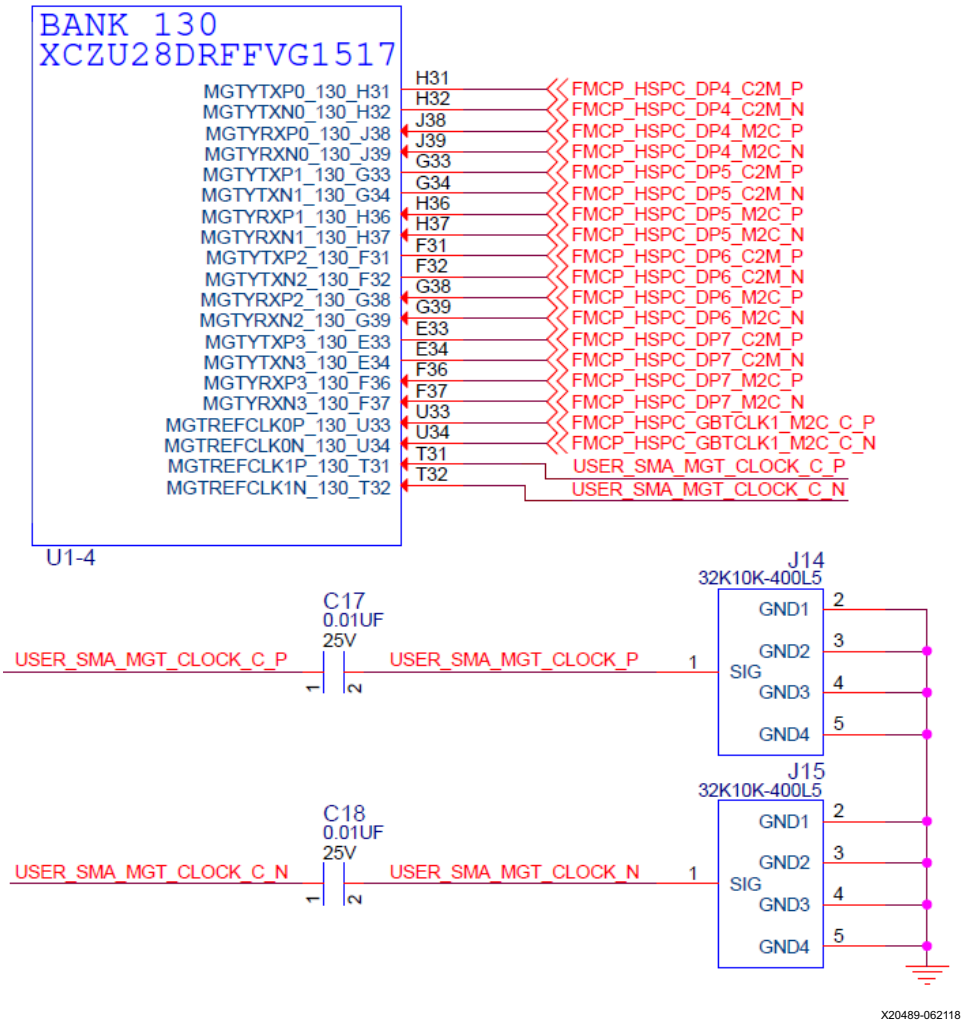

Figure 3-16: **User SMA MGT Clock**

SI5382A SFP28 Clock Recovery

[Figure 2-1, callout 8]

The ZCU111 board includes a Silicon Labs SI5382A jitter attenuator U48. The RFSoC U1 PL user logic can implement a clock recovery circuit and output this series capacitor coupled clock from a differential pair on I/O bank 64 (SFP_REC_CLOCK_P U1 pin AW14 and SFP_REC_CLOCK_N U1 pin AW13) for jitter attenuation. The jitter attenuated clock (SFP_SI5382_OUT_P (U48 pin 21), SFP_SI5382_OUT_N (U48 pin 20)) is then routed as a series capacitor coupled reference clock to GTY bank 128 inputs MGTREFCLK1P (U1 pin Y31) and MGTREFCLK1N (U1 pin Y32).

The primary purpose of this clock is to support common packet radio interface/open base station architecture initiative (CPRI/OBSAI) applications that perform clock recovery from a user-supplied SFP28 module, and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTY transceiver. The jitter attenuated clock circuit is shown in Figure 3-17.

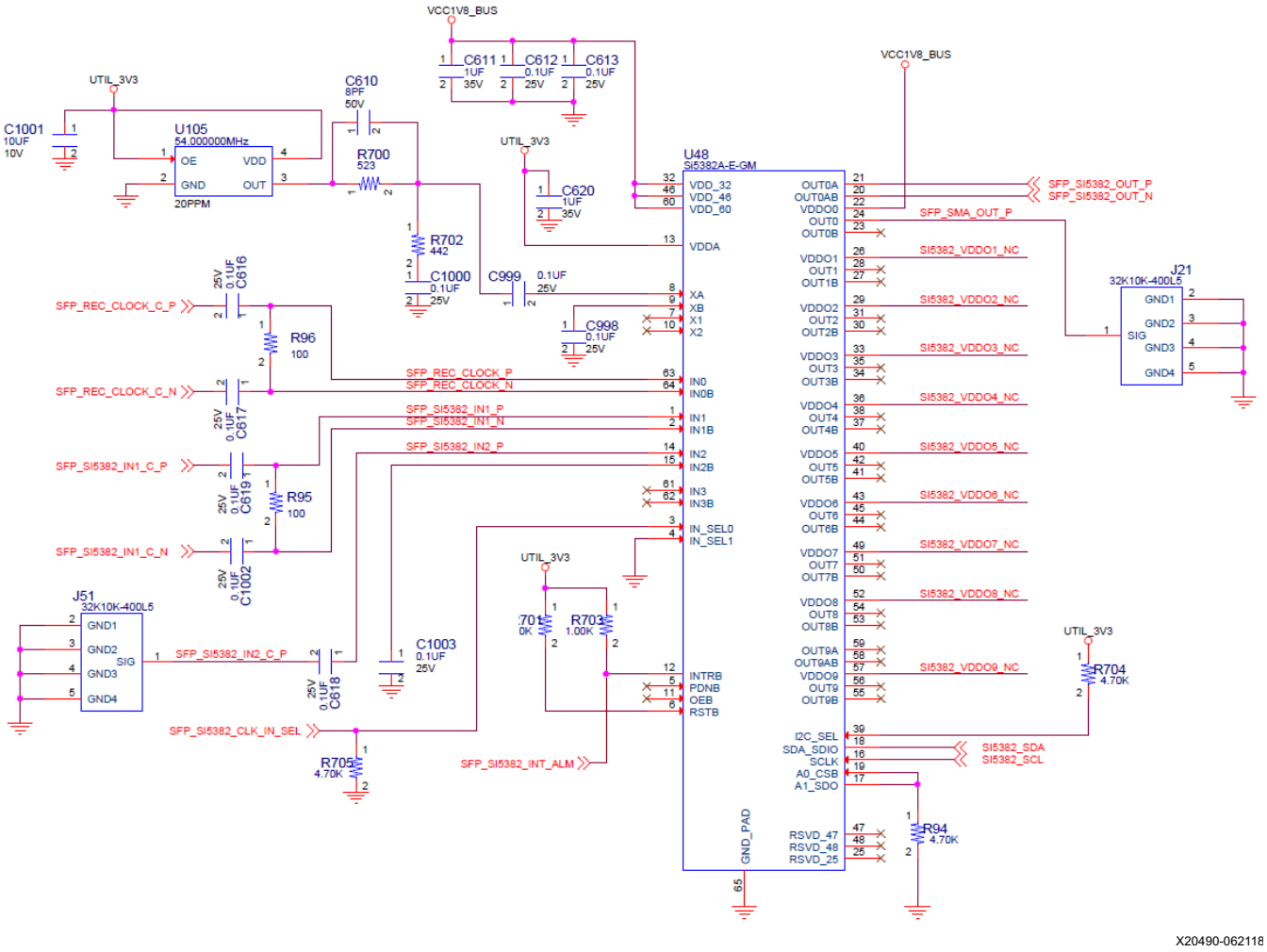

Figure 3-17: **SFP28 Jitter Attenuated Clock**

For more details on the Silicon Labs SI5341B, SI570, and SI5382A devices, see [Ref 14].

For UltraScale FPGA clocking information, see the *UltraScale Architecture Clocking Resources User Guide* (UG572) [Ref 10].

RF Data Converters

The ZU28DRF-FFVG1517 contains eight multi-gigasample (4 GSPS), 12-bit RF analog-to-digital converter (RF-ADC) channels across four banks and eight multi-gigasample (6.544 GSPS), 14-bit RF digital-to-analog (RF-DAC) converter channels across two banks. The ZCU111 board provides a pair of Samtec LPAF connectors (J47: ADC; J94: DAC) for the RF-ADC/RF-DAC clock and RF signals.

	Channels per Bank	Banks	Channel Count
RF-ADC	2	4 (224-227)	8
RF-DAC	4	2 (228, 229)	8

RF Data Converter Clocking

The RF data converter clocking includes primary on-board reference PLL (LMK04208) and on-board RF PLLs (LMX2594) to generate RF-ADC and RF-DAC sample clocks. With careful board modification, external equipment can also directly drive ADC bank clocks and DAC bank clocks through the Samtec LPAF (8x40) connector.

The LMX2594 clocks can be configured either as direct RF clocks or as reference clock sources for the internal PLL contained within the RFSoC data converter tile.

See *ZCU111 System Controller Tutorial* (XTP517) [Ref 11] for information on programming the LMK and LMX PLLs.

Two Samtec LPAF (8x40) connectors provide an RFMC system interface for plug-in cards. Figure 3-20 and Figure 3-21 illustrate the connector pinout and plug-in card dimensions.

Figure 3-18 shows the bank view of the ZCU111 RF clocking structure.

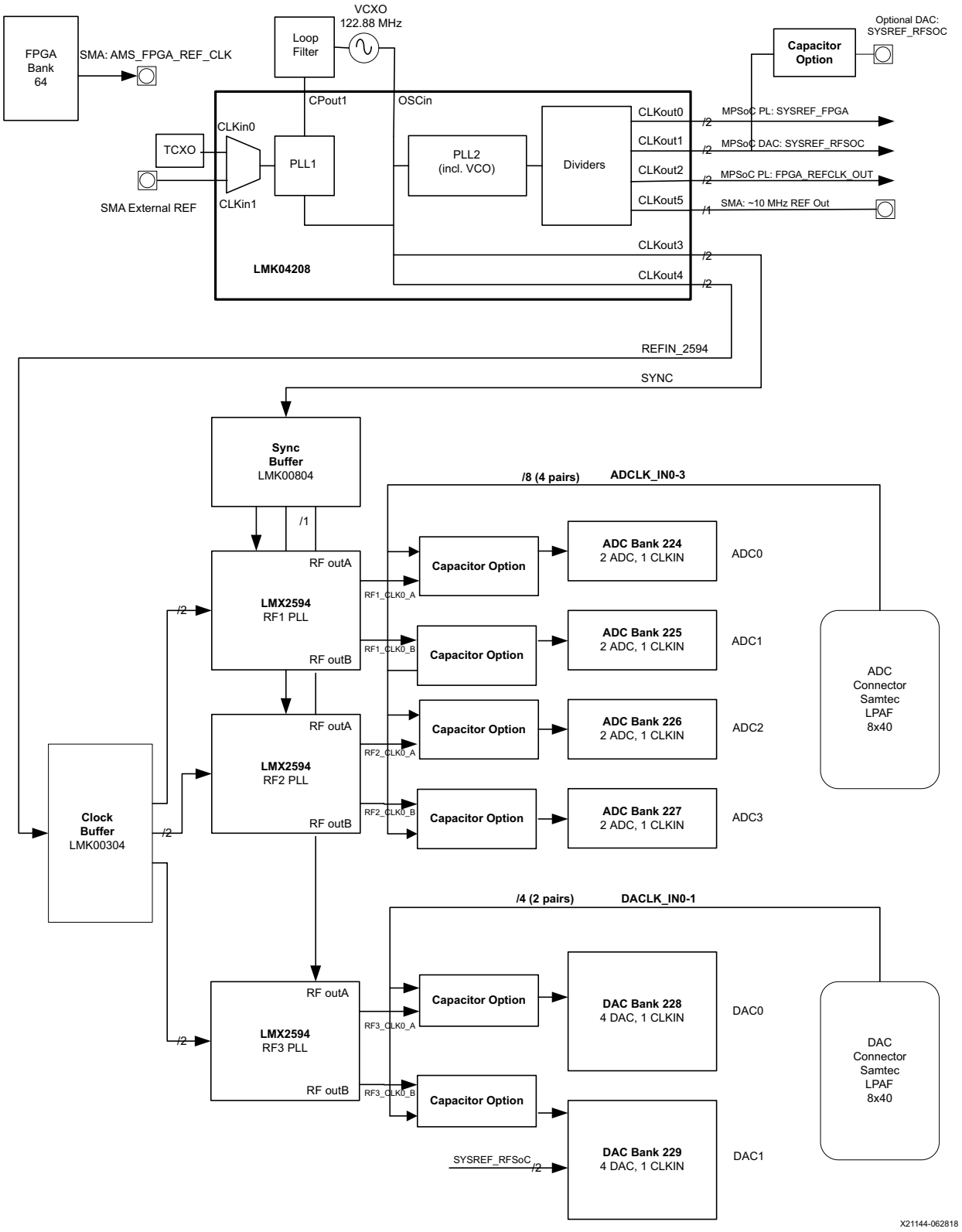

Figure 3-18: **RF Clocking Structure for ADC and DAC Banks**

Table 3-18 and Table 3-19 provides guidance on external clocking modifications.

IMPORTANT: *To provide external sources from the RFMC connector, the default capacitors must be carefully moved to optional capacitor locations.*

Table 3-18: **RFMC External Clocking Modifications**

LMX2594 Device and Channel	Output Net Name	FPGA Net Name	FPGA Bank	RFMC Optional External Clock Net Name	Default Capacitors	Optional External Source Capacitors
U102 Channel A	RF1_CLKO_A_P/N	RF1_CLKO_A_C_P/N	224	ADCLK_IN0_P/N	C632 / C640	C948 / C949
U102 Channel B	RF1_CLKO_B_P/N	RF1_CLKO_B_C_P/N	225	ADCLK_IN1_P/N	C646 / C718	C1018 / C1019
U103 Channel A	RF2_CLKO_A_P/N	RF2_CLKO_A_C_P/N	227	ADCLK_IN2_P/N	C683 / C690	C951 / C950
U103 Channel B	RF2_CLKO_B_P/N	RF2_CLKO_B_C_P/N	226	ADCLK_IN3_P/N	C692 / C699	C1020 / C1021
U104 Channel A	RF3_CLKO_A_P/N	RF3_CLKO_A_C_P/N	228	DACLK_IN0_P/N	C666 / C673	C1024 / C1025
U104 Channel B	RF3_CLKO_B_P/N	RF3_CLKO_B_C_P/N	229	DACLK_IN1_P/N	C675 / C682	C1022 / C1023

By default, the LMK04208 provides a clock to the DAC bank 228 SYSREF clock input pins.

IMPORTANT: *To provide an external SYSREF clock with the onboard optional SMAs, the default capacitors must be carefully moved to optional capacitor locations.*

Table 3-19: **SYSREF External Clocking Modifications**

LMK04208 Device and Channel	Output Net Name	FPGA Net Name	FPGA Bank	ZCU111 SYSREF SMA	Default Capacitors	Optional External Source Capacitors
U90 OUT1 P	CLK_4208_OUT1_P	SYSREF_RFSOC_C_P	228	J7	C742	C1031
U90 OUT1 N	CLK_4208_OUT1_N	SYSREF_RFSOC_C_N	228	J10	C743	C1034

Before making ZCU111 RF clock capacitor modifications, refer to the PC board layout and identify the metal RF cage associated with the capacitors of interest:

- C632/C640, C646/C718: RFCAGE2
- C683/C690, C692/C699: REFCAGE3
- C666/C673, C675/C682: RFCAGE4
- C742 and C743: RFCAGE1

The appropriate cage lid must be removed to make the capacitor modifications, and replaced upon completion.

To implement the external clock source capability, remove (desolder) the *default capacitors* and solder them onto the pads at the *optional external source capacitors* locations shown in the above tables (e.g., for Table 3-18, U102 Channel A, remove C632 and solder it at C948, remove C640 and solder it at C949, and so on). Due to via-in-pad component footprints, Xilinx recommends the rework be implemented by an expert rework technician.

The I2C_to_SPI bridge connectivity for PLL readback is shown in Figure 3-19.

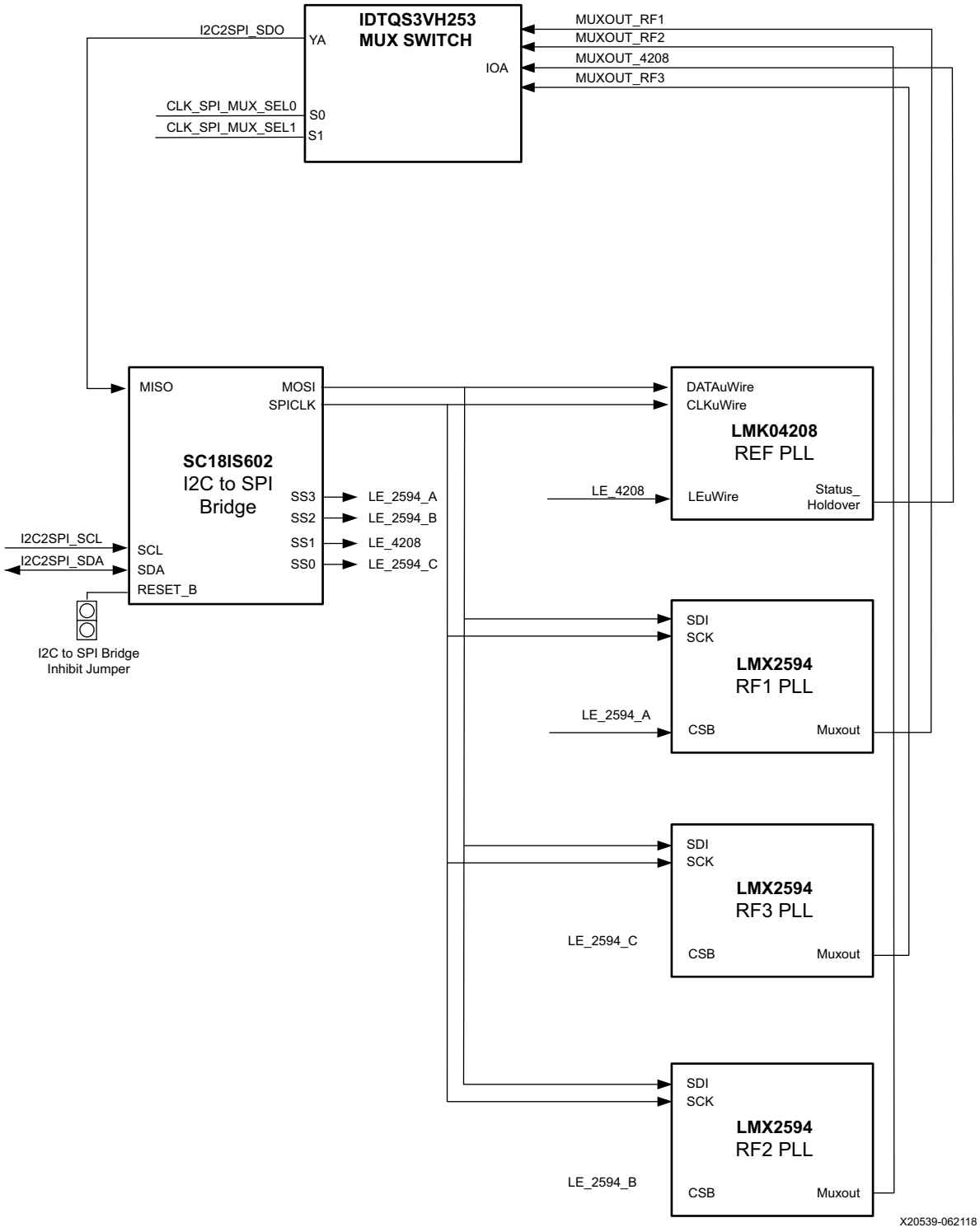

Figure 3-19: **I2C_to_SPI Bridge Connectivity for PLL Readback**

RFMC Plug-in Card Interface

Two Samtec LPAF (8x40) connectors provide access to the ADC/DAC clocking and data path signals. The Samtec part number is LPAF-40-03.0-S-08-2-K-TR. See Table 3-20 and Figure 3-20.

Table 3-20: **RF RFMC Plug-in Card Interface**

Technical Details	
Part number	LPAF-40-03.0-S-08-2-K-TR
Series	LPAF
Number of positions	–40
Lead style	–03.0 = 3.0 mm
Plating option	Non-standard option Contact SAMTEC: –S = 30µ Selective gold in contact area, matte tin on tail
Row option	–08 = eight row
Solder type	–2 = 95.5% tin/3.8% silver/.7% copper crimp tail
Pick and place pad	–K - polyamide file pad
Tape and reel packaging	–TR = tape and reel packaging

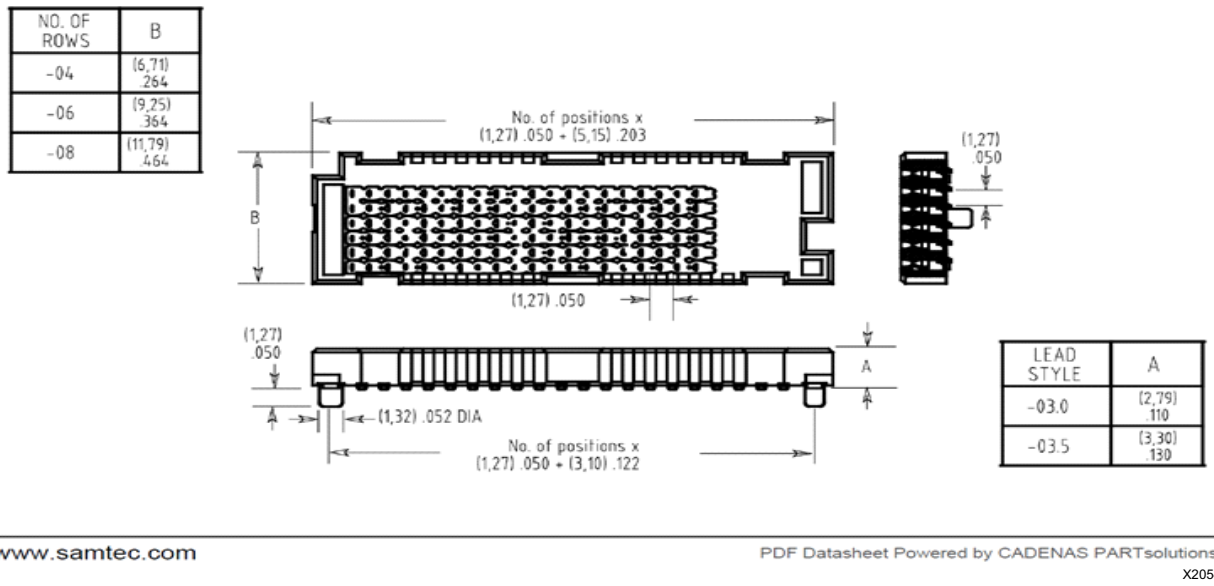

Figure 3-20: **SAMTEC Connector**

The RFMC LPAF connector pin definitions are shown in Figure 3-21 (RF-ADC J47) and Figure 3-22 (RF-DAC J94). RF-ADC banks 224-227 and RF-DAC banks 228-229 are fully pinned out to J47 and J94, respectively.

	H	G	F	E	D	C	B	A
1	ADCIO_17	GND	ADCIO_12	GND	ADCIO_07	GND	ADCIO_02	GND
2	GND	ADCIO_15	GND	ADCIO_10	GND	ADCIO_05	GND	ADCIO_00
3	ADCIO_18	GND	ADCIO_13	GND	ADCIO_08	GND	ADCIO_03	GND
4	GND	ADCIO_16	GND	ADCIO_11	GND	ADCIO_06	GND	ADCIO_01
5	ADCIO_19	GND	ADCIO_14	GND	ADCIO_09	GND	ADCIO_04	GND
6	GND	I2C_SCL	GND	I2C_SDA	GND	ADCIO_VADJ	GND	ADCIO_VADJ
7	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3
8	GND	GND	GND	GND	GND	GND	GND	GND
9	GND	ADC_00_P	ADC_00_N	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	GND	ADC_01_P	ADC_01_N	GND
11	GND	GND	GND	GND	GND	GND	GND	GND
12	GND	ADC_02_P	ADC_02_N	GND	GND	GND	GND	GND
13	GND	GND	GND	GND	GND	ADC_03_P	ADC_03_N	GND
14	GND	GND	GND	GND	GND	GND	GND	GND
15	GND	ADC_04_P	ADC_04_N	GND	GND	GND	GND	GND
16	GND	GND	GND	GND	GND	ADC_05_P	ADC_05_N	GND
17	GND	GND	GND	GND	GND	GND	GND	GND
18	GND	ADC_06_P	ADC_06_N	GND	GND	GND	GND	GND
19	GND	GND	GND	GND	GND	ADC_07_P	ADC_07_N	GND
20	GND	GND	GND	GND	GND	GND	GND	GND
21	VCM	VCM	VCM	VCM	VCM	VCM	VCM	VCM
22	GND	GND	GND	GND	GND	GND	GND	GND
23	GND	ADC_08_P	ADC_08_N	GND	GND	GND	GND	GND
24	GND	GND	GND	GND	GND	ADC_09_P	ADC_09_N	GND
25	GND	GND	GND	GND	GND	GND	GND	GND
26	GND	ADC_10_P	ADC_10_N	GND	GND	GND	GND	GND
27	GND	GND	GND	GND	GND	ADC_11_P	ADC_11_N	GND
28	GND	GND	GND	GND	GND	GND	GND	GND
29	GND	ADC_12_P	ADC_12_N	GND	GND	GND	GND	GND
30	GND	GND	GND	GND	GND	ADC_13_P	ADC_13_N	GND
31	GND	GND	GND	GND	GND	GND	GND	GND
32	GND	ADC_14_P	ADC_14_N	GND	GND	GND	GND	GND
33	GND	GND	GND	GND	GND	ADC_15_P	ADC_15_N	GND
34	GND	GND	GND	GND	GND	GND	GND	GND
35	GND	ADC_CLKIN_1_P	ADC_CLKIN_1_N	GND	GND	GND	GND	GND
36	GND	GND	GND	GND	GND	ADC_CLKIN_0_P	ADC_CLKIN_0_N	GND
37	GND	GND	GND	GND	GND	GND	GND	GND
38	GND	ADC_CLKIN_3_P	ADC_CLKIN_3_N	GND	GND	GND	GND	GND
39	GND	GND	GND	GND	GND	ADC_CLKIN_2_P	ADC_CLKIN_2_N	GND
40	GND	GND	GND	GND	GND	GND	GND	GND

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Figure 3-21: **RFMC RF-ADC LPAF Connector, Vertical Orientation (A1 in Upper Right Corner)**

	H	G	F	E	D	C	B	A
1	DAC_AVTT	DAC_AVTT	GND	12V	12V	12V	12V	12V
2	DAC_AVTT	DAC_AVTT	GND	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND	GND	GND
4	GND	GND	GND	GND	GND	DAC_CLKIN_0_P	DAC_CLKIN_0_N	GND
5	GND	DAC_CLKIN_1_P	DAC_CLKIN_1_N	GND	GND	GND	GND	GND
6	GND	GND	GND	GND	GND	GND	GND	GND
7	GND	GND	GND	GND	GND	DAC_CLKIN_2_P	DAC_CLKIN_2_N	GND
8	GND	DAC_CLKIN_3_P	DAC_CLKIN_3_N	GND	GND	GND	GND	GND
9	GND	GND	GND	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	GND	DAC_00_P	DAC_00_N	GND
11	GND	DAC_01_P	DAC_01_N	GND	GND	GND	GND	GND
12	GND	GND	GND	GND	GND	GND	GND	GND
13	GND	GND	GND	GND	GND	DAC_02_P	DAC_02_N	GND
14	GND	DAC_03_P	DAC_03_N	GND	GND	GND	GND	GND
15	GND	GND	GND	GND	GND	GND	GND	GND
16	GND	GND	GND	GND	GND	DAC_04_P	DAC_04_N	GND
17	GND	DAC_05_P	DAC_05_N	GND	GND	GND	GND	GND
18	GND	GND	GND	GND	GND	GND	GND	GND
19	GND	GND	GND	GND	GND	DAC_06_P	DAC_06_N	GND
20	GND	DAC_07_P	DAC_07_N	GND	GND	GND	GND	GND
21	GND	GND	GND	GND	GND	GND	GND	GND
22	GND	GND	GND	GND	GND	DAC_08_P	DAC_08_N	GND
23	GND	DAC_09_P	DAC_09_N	GND	GND	GND	GND	GND
24	GND	GND	GND	GND	GND	GND	GND	GND
25	GND	GND	GND	GND	GND	DAC_10_P	DAC_10_N	GND
26	GND	DAC_11_P	DAC_11_N	GND	GND	GND	GND	GND
27	GND	GND	GND	GND	GND	GND	GND	GND
28	GND	GND	GND	GND	GND	DAC_12_P	DAC_12_N	GND
29	GND	DAC_13_P	DAC_13_N	GND	GND	GND	GND	GND
30	GND	GND	GND	GND	GND	GND	GND	GND
31	GND	GND	GND	GND	GND	DAC_14_P	DAC_14_N	GND
32	GND	DAC_15_P	DAC_15_N	GND	GND	GND	GND	GND
33	GND	GND	GND	GND	GND	GND	GND	GND
34	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3
35	GND	SPARE_02	GND	SPARE_01	GND	DACIO_VADJ	GND	DACIO_VADJ
36	DACIO_17	GND	DACIO_12	GND	DACIO_07	GND	DACIO_02	GND
37	GND	DACIO_15	GND	DACIO_10	GND	DACIO_05	GND	DACIO_00
38	DACIO_18	GND	DACIO_13	GND	DACIO_08	GND	DACIO_03	GND
39	GND	DACIO_16	GND	DACIO_11	GND	DACIO_06	GND	DACIO_01
40	DACIO_19	GND	DACIO_14	GND	DACIO_09	GND	DACIO_04	GND

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Figure 3-22: **RFMC DAC LPAF Connector, Vertical Orientation (A1 Upper Right Corner)**

See Appendix D, HW-FMC-XM500 for information about the Xilinx HW-FMC-XM500 RFMC plug-in card.

SFP28 Module Connectors

[Figure 2-1, callouts 14, 15]

The ZCU111 board hosts four SFP28 connectors J27, J32, J37, and J42. The connectors are housed within a single quad SFP28 cage assembly. The ganged SFP28 cage supports up to four SFP/SFP+/SFP28 modules. Figure 3-23 shows the SFP28 module connector circuitry typical of the four implementations.

Note: The SFPx_TX_DISABLE default 2-pin jumper is On, which means the SFPx_TX_DISABLE net is pulled Low, enabling the TX output of the SFP module.

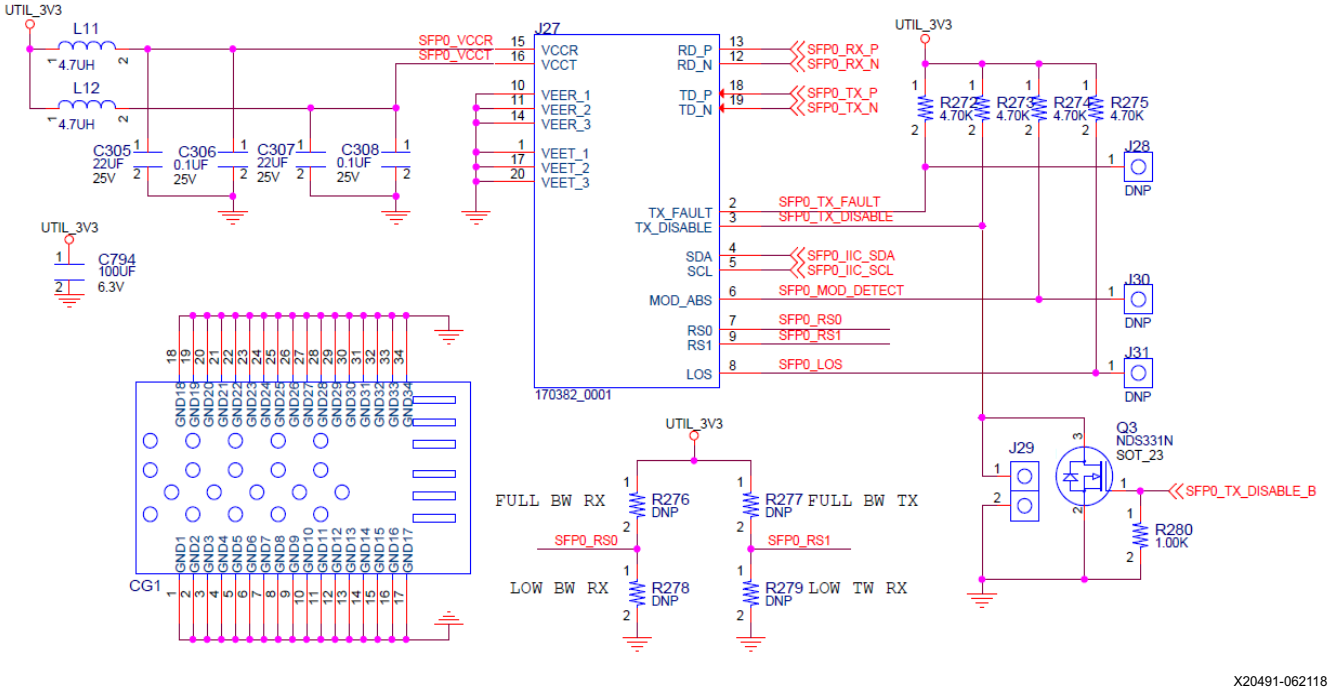

Figure 3-23: **SFP28 Module Connectivity**

Table 3-21 lists the SFP28 module connections to RFSoC U1.

Table 3-21: **SFP28 Control and Status Board Test Points**

SFP28 Control/ Status Signal	Board Connection	
SFP0 J27[(1)(2)]		
SFP_TX_FAULT	Test point J28	High = Fault
		Low = Normal operation
SFP_TX_DISABLE	Jumper J29	Off = SFP disabled
		On = SFP enabled
SFP_MOD_DETECT	Test point J30	High = Module not present
		Low = Module present
SFP_RS0	PU R276/PD R278	PU R276 = Full RX bandwidth
		PD R278 = Reduced RX bandwidth
SFP_RS1	PU R277/PD R279	PU R277 = Full TX bandwidth
		PD R279 = Reduced TX bandwidth
SFP_LOS	Test point J31	High = Loss of receiver signal
		Low = Normal operation
SFP1 J32[(1)(2)]		
SFP_TX_FAULT	Test point J33	High = Fault
		Low = Normal operation
SFP_TX_DISABLE	Jumper J35	Off = SFP disabled
		On = SFP enabled
SFP_MOD_DETECT	Test point J34	High = Module not present
		Low = Module present
SFP_RS0	PU R281/PD R283	PU R281 = Full RX bandwidth
		PD R283 = Reduced RX bandwidth
SFP_RS1	PU R282/PD R284	PU R282 = Full TX bandwidth
		PD R284 = Reduced TX bandwidth
SFP_LOS	Test point J36	High = Loss of receiver signal
		Low = Normal operation
SFP2 J37[(1)(2)]		
SFP_TX_FAULT	Test point J38	High = Fault
		Low = Normal operation
SFP_TX_DISABLE	Jumper J40	Off = SFP disabled
		On = SFP enabled

Table 3-21: **SFP28 Control and Status Board Test Points *(Cont'd)***

SFP28 Control/ Status Signal	Board Connection	
SFP_MOD_DETECT	Test point J39	High = Module not present
		Low = Module present
SFP_RS0	PU R289/PD R291	PU R289 = Full RX bandwidth
		PD R291 = Reduced RX bandwidth
SFP_RS1	PU R290/PD R292	PU R290 = Full TX bandwidth
		PD R292 = Reduced TX bandwidth
SFP_LOS	Test point J41	High = Loss of receiver signal
		Low = Normal operation
SFP3 J42[(1)(2)]		
SFP_TX_FAULT	Test point J43	High = Fault
		Low = Normal operation
SFP_TX_DISABLE	Jumper J44	Off = SFP disabled
		On = SFP enabled
SFP_MOD_DETECT	Test point J45	High = Module not present
		Low = Module present
SFP_RS0	PU R294/PD R300	PU R294 = Full RX bandwidth
		PD R300 = Reduced RX bandwidth
SFP_RS1	PU R295/PD R301	PU R295 = Full TX bandwidth
		PD R301 = Reduced TX bandwidth
SFP_LOS	Test point J46	High = Loss of receiver signal
		Low = Normal operation

Notes:

1. The RS0/RS1 PU/PD resistors are not populated.There are pull-down resistors built into the SFP28 modules that select the lower bandwidth mode of the module.
2. BW selection is also available via I2C control. For this and additional information about the SFP28 module, see SFF-8402 and SFF-8432 at the specification website [Ref 28].

Table 3-22 lists the SFP28 module connections to the Zynq UltraScale+ RFSoC U1.

Table 3-22: **SFP28 RFSoC Connections**

XCZU28DR Pin (U1)	Schematic Net Name	I/O Standard	SFP+ Pin	SFP+ Pin Name
SFP0 J27				
Y35	SFP0_TX_P	(1)	18	TD_P
Y36	SFP0_TX_N	(1)	19	TD_N
AA38	SFP0_RX_P	(1)	13	RD_P
AA39	SFP0_RX_N	(1)	12	RD_N
G12	SFP0_TX_DISABLE_B	LVCMOS12	3	TX_DISABLE
SFP1 J32				
V35	SFP1_TX_P	(1)	18	TD_P
V36	SFP1_TX_N	(1)	19	TD_N
W38	SFP1_RX_P	(1)	13	RD_P
W39	SFP1_RX_N	(1)	12	RD_N
G10	SFP0_TX_DISABLE_B	LVCMOS12	3	TX_DISABLE
SFP2 J37				
T35	SFP2_TX_P	(1)	18	TD_P
T36	SFP2_TX_N	(1)	19	TD_N
U38	SFP2_RX_P	(1)	13	RD_P
U39	SFP2_RX_N	(1)	12	RD_N
K12	SFP0_TX_DISABLE_B	LVCMOS12	3	TX_DISABLE
SFP3 J42				
R33	SFP3_TX_P	(1)	18	TD_P
R34	SFP3_TX_N	(1)	19	TD_N
R38	SFP3_RX_P	(1)	13	RD_P
R39	SFP3_RX_N	(1)	12	RD_N
J7	SFP0_TX_DISABLE_B	LVCMOS12	3	TX_DISABLE

Notes:

1. Bank 128 GTY connections, I/O standards not applicable.

For additional information about the small form factor pluggable SFP28 module, see the SFF-8402 and SFF-8432 specifications at the SNIA Technology Affiliates website [Ref 28].

User PMOD GPIO Connectors

[Figure 2-1, callout 20, 21]

The ZCU111 evaluation board supports two right-angle PMOD GPIO receptacles J48 and J49. The 3.3V PMOD nets are level-shifted and are wired to the XCZU28DR device U1 banks 28, 66, and 68. Figure 3-24 shows the GPIO PMOD connector circuits.

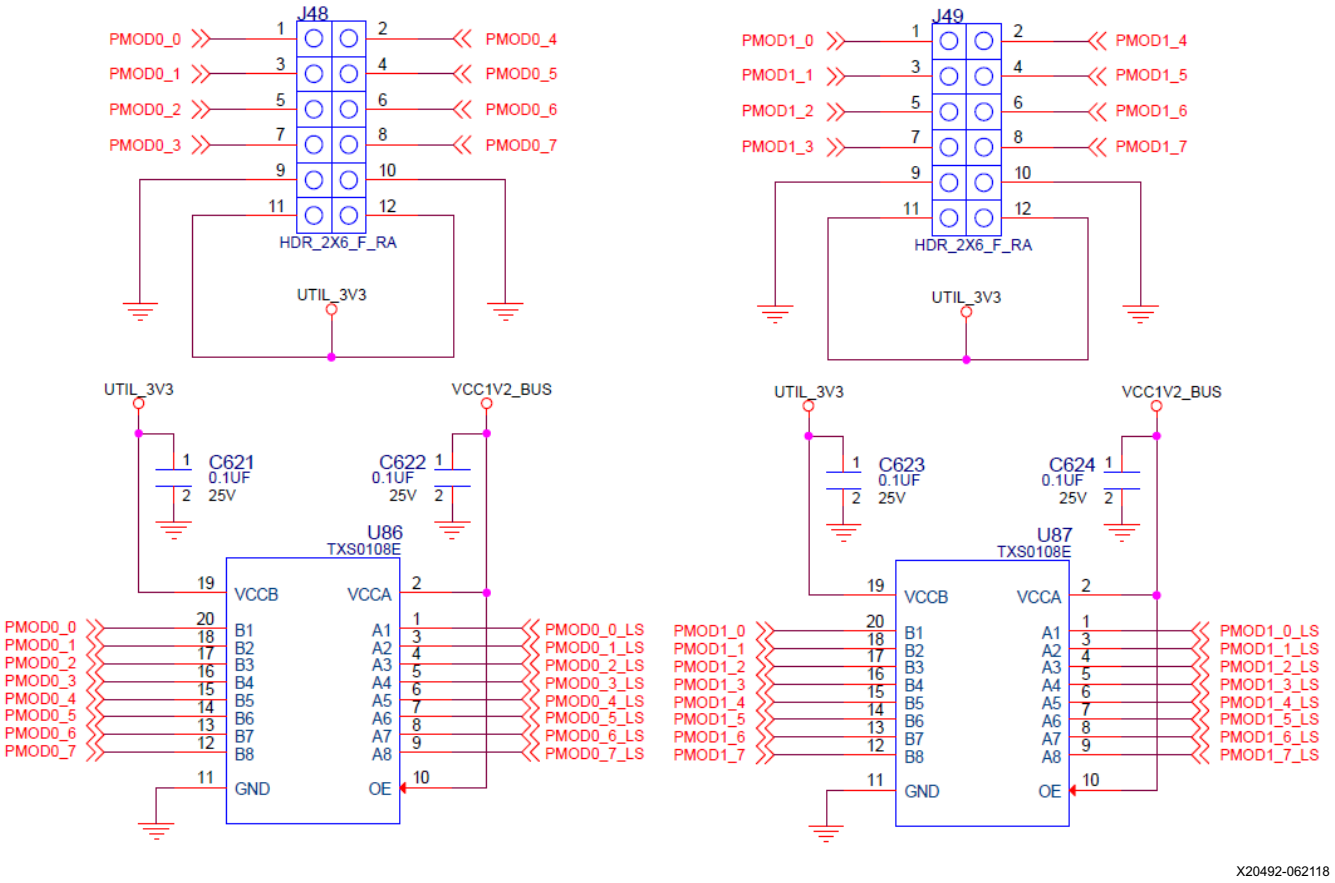

Figure 3-24: **PMOD Connectors**

Table 3-23 lists the connections between the XCZU28DR RFSoC and the PMOD

Table 3-23: **PMOD Connections to XCZU28DR**

XCZU28DR (U1) Pin	Net Name(1)	I/O Standard	PMOD Pin
C17	PMOD0_0	LVCMOS12	J48.1
M18	PMOD0_1	LVCMOS12	J48.3
H16	PMOD0_2	LVCMOS12	J48.5
H17	PMOD0_3	LVCMOS12	J48.7
J16	PMOD0_4	LVCMOS12	J48.2
K16	PMOD0_5	LVCMOS12	J48.4
H15	PMOD0_6	LVCMOS12	J48.6
J15	PMOD0_7	LVCMOS12	J48.8
L14	PMOD1_0	LVCMOS12	J49.1
L15	PMOD1_1	LVCMOS12	J49.3
M13	PMOD1_2	LVCMOS12	J49.5
N13	PMOD1_3	LVCMOS12	J49.7
M15	PMOD1_4	LVCMOS12	J49.2
N15	PMOD1_5	LVCMOS12	J49.4
M14	PMOD1_6	LVCMOS12	J49.6
N14	PMOD1_7	LVCMOS12	J49.8

Notes:
1. Level-shifted net names at XCZU28DR have _LS appended.

For more information on the PMOD interface, see the Digilent website [Ref 27].

User I/O

[Figure 2-1, callouts 22-25]

The ZCU111 board provides these user and general purpose I/O capabilities:

- Eight user LEDs (callout 22)
  - GPIO_LED[7-0]: DS11, DS12, DS13, DS14, DS15, DS16, DS17, DS18
- 8-position user DIP Switch (callout 23)
  - GPIO_DIP_SW[7:0]: SW14
- Five user pushbuttons and CPU reset switch (callouts 24 and 25)
  - GPIO_SW_[NWCES]: SW9, SW10, SW11, SW12, SW13
  - CPU_RESET: SW15

Figure 3-25 through Figure 3-27 show the GPIO circuits. Table 3-24 lists the GPIO connections to XCZU28DR U1 connections.

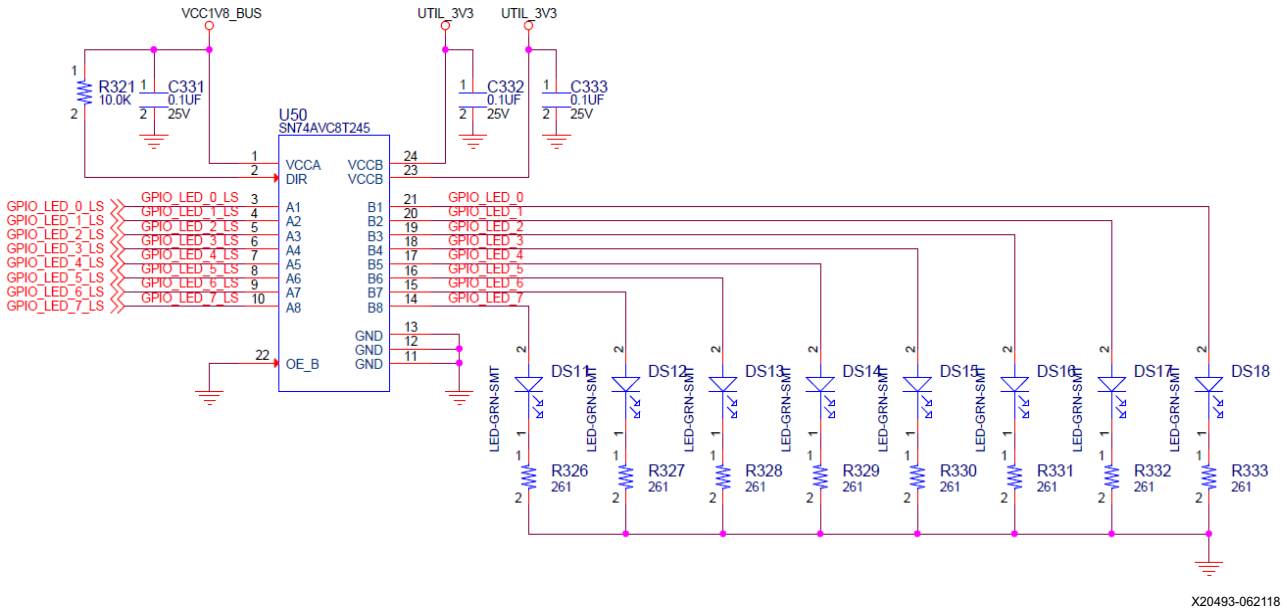

Figure 3-25: **GPIO LEDs**

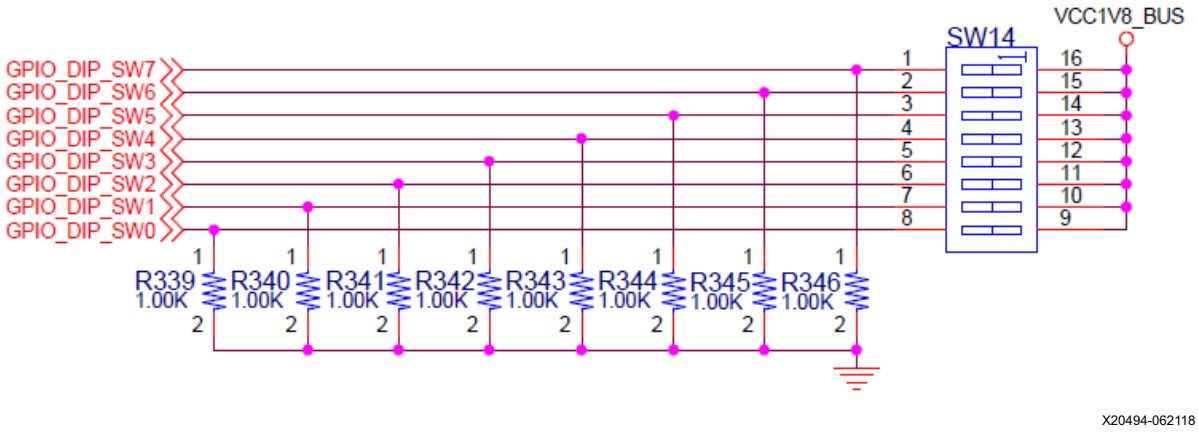

Figure 3-26: **GPIO 8-Pole DIP Switch**

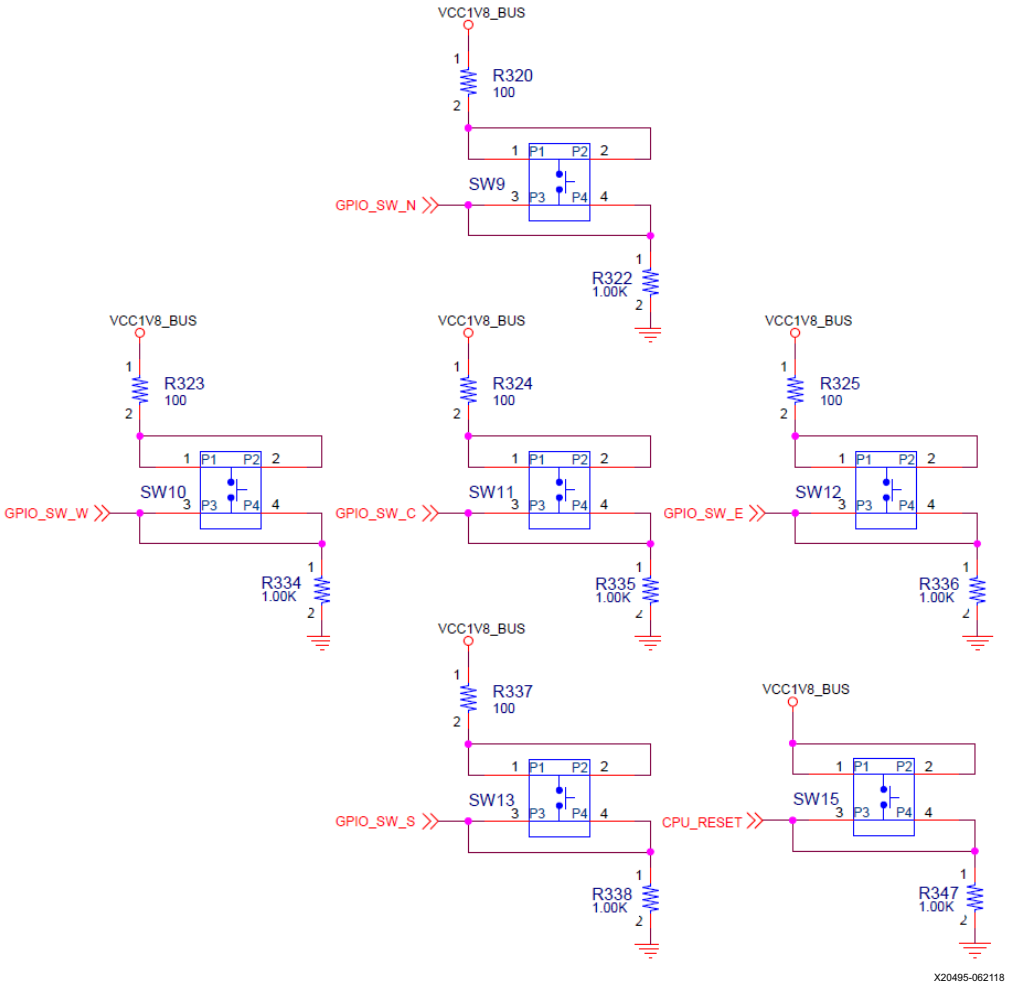

Figure 3-27: **GPIO Pushbutton Switches**

Table 3-24: **GPIO Connections to XCZU28DR**

XCZU28DR (U1) Pin	Net Name	I/O Standard	Device
GPIO LEDs (Active High)[1]			
AR13	GPIO_LED_0	LVCMOS18	DS11.2
AP13	GPIO_LED_1	LVCMOS18	DS12.2
AR16	GPIO_LED_2	LVCMOS18	DS13.2
AP16	GPIO_LED_3	LVCMOS18	DS14.2
AP15	GPIO_LED_4	LVCMOS18	DS15.2
AN16	GPIO_LED_5	LVCMOS18	DS16.2
AN17	GPIO_LED_6	LVCMOS18	DS17.2
AV15	GPIO_LED_7	LVCMOS18	DS18.2
GPIO DIP SW (Active High)			
AF16	GPIO_DIP_SW0	LVCMOS18	SW14.8

Table 3-24: **GPIO Connections to XCZU28DR *(Cont'd)***

XCZU28DR (U1) Pin	Net Name	I/O Standard	Device
AF17	GPIO_DIP_SW1	LVCMOS18	SW14.7
AH15	GPIO_DIP_SW2	LVCMOS18	SW14.6
AH16	GPIO_DIP_SW3	LVCMOS18	SW14.5
AH17	GPIO_DIP_SW4	LVCMOS18	SW14.4
AG17	GPIO_DIP_SW5	LVCMOS18	SW14.3
AJ15	GPIO_DIP_SW6	LVCMOS18	SW14.2
AJ16	GPIO_DIP_SW7	LVCMOS18	SW14.1
Directional Pushbuttons (Active High)			
AW3	GPIO_SW_N	LVCMOS18	SW9.3
AW6	GPIO_SW_W	LVCMOS18	SW10.3
AW5	GPIO_SW_C	LVCMOS18	SW11.3
AW4	GPIO_SW_E	LVCMOS18	SW12.3
E8	GPIO_SW_S	LVCMOS18	SW13.3
CPU Reset Pushbutton (Active High)			
AF15	CPU_RESET	LVCMOS18	SW15.3

Notes:

1. Level-shifted net names at ZU28DR U1 have _LS appended.

Power and Status LEDs

[Figure 2-1, area of callout 22]

Table 3-25 defines the power and status LEDs. For user-controlled GPIO LED details, see User I/O, page 65.

Table 3-25: **Power and Status LEDs**

Ref. Des.	Schematic Net Name	LED Color	Description
DS1	PS_INIT_B	Green/ Red	Green: FPGA initialization was successful. Red: FPGA initialization is in progress.
DS2	PS_DONE	Green	RFSoC U1 bit file download is complete.
DS3	PS_RESET_B	Red	POR U6 asserts RESET_B low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes low, or MR is asserted.
DS4	PS_ERR_OUT	Red	PS error out is asserted for accidental loss of power, an error in the PMU that holds the CSU in reset, or an exception in the PMU.
DS5	PS_ERR_STATUS	Red	PS error status indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.
DS6	PS_VCC3V3_PG	Green	DisplayPort 3.3V power on
DS7	USB3 MIC2544 U13 FLG	Green	PS USB 3.0 ULPI VBUS power error
DS27	ENET_LED_1	Green	EHPY U37 1000BASE-T link is established.
DS47	MSP430_LED0	Green	MSP430 U41 GPIO LED
DS46	MSP430_LED1	Green	MSP430 U41 GPIO LED
DS11	GPIO_LED_7	Green	USER GPIO LED
DS12	GPIO_LED_6	Green	USER GPIO LED
DS13	GPIO_LED_5	Green	USER GPIO LED
DS14	GPIO_LED_4	Green	USER GPIO LED
DS15	GPIO_LED_3	Green	USER GPIO LED
DS16	GPIO_LED_2	Green	USER GPIO LED
DS17	GPIO_LED_1	Green	USER GPIO LED
DS18	GPIO_LED_0	Green	USER GPIO LED
DS19	VCC12_SW	Green	12VDC power on
DS20	VCCINT_PG	Green	VCCINT 0.85VDC power on
DS21	VCCPSINTFP_PG	Green	VCCPSINTFP 0.85VDC power on
DS22	VCC1V8	Green	VCC1V8 1.8VDC power on
DS23	VCC1V2_PG	Green	VCC1V2 1.2VDC power on

Table 3-25: **Power and Status LEDs *(Cont'd)***

Ref. Des.	Schematic Net Name	LED Color	Description
DS24	DAC_AVCC_PG	Green	ADC_AVCC 0.925V power on
DS25	VADJ_FMC_PG	Green	VADJ_FMC 1.8VDC (Nom.) power on
DS26	MGT1V2_PG	Green	MGT1V2 1.2VDC power on
DS43	MGTAVCC_PG	Green	MGTAVCC 0.9VDC power on
DS28	MGT1V8_PG	Green	MGT1V8 1.8VDC power on
DS29	MGTRAVCC_PG	Green	MGTRAVCC 0.85VDC power on
DS30	VCCINT_RF_PG	Green	VCCINT_RF 0.85VDC power on
DS31	ADC_AVCC_PG	Green	ADC_AVCC 0.925VDC power on
DS32	UTIL_3V5_PG	Green	UTIL_3V5 3.5VDC power on
DS33	ADC_AVCCAUX_PG	Green	ADC_AVCCAUX 1.8VDC power on
DS34	MUXOUT_RF1	Green	LMX2594 U102 lock detect
DS35	MUXOUT_RF2	Green	LMX2594 U103 lock detect
DS36	UTIL_1V13_PG	Green	UTIL_1V13 1.13VDC power on
DS37	UTIL_2V5_PG	Green	UTIL_2V5 2.5VDC power on
DS38	UTIL_3V3_PG	Green	UTIL_3V3 3.3VDC power on
DS39	UTIL_5V0_PG	Green	UTIL_5V0 5VDC power on
DS40	PS_DDR4_VTERM_0V60_PGOOD	Green	PS_DDR4_VTERM 0.6VDC power on
DS41	PL_DDR4_VTERM_0V60_PGOOD	Green	PL_DDR4_VTERM 0.6VDC power on
DS42	DAC_AVCCAUX_ON	Green	DAC_AVCCAUX 1.8VDC power on
DS44	MUXOUT_RF3	Green	LMX2594 U104 lock detect
DS45	STATUS_4208	Green	LMK04208 status
DS49	DAC_AVTT_PG	Green	DAC_AVTT 2.5VDC power on
DS8	RF_CLK_VCC3V3_PG	Green	RF_CLK_VCC3V3 3.3VDC power on
DS50	MIO23_LED	Green	RFSoC U1 bank 500 GPIO LED

Figure 3-28 shows the power and status LEDs area of the board.

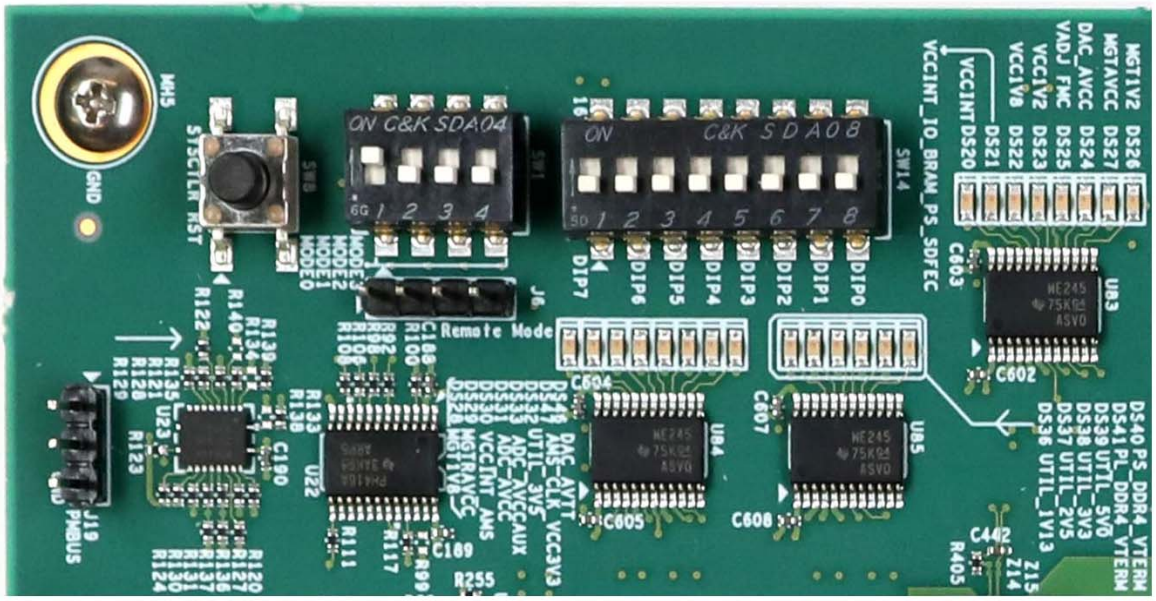

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Figure 3-28: **Power and Status LEDs**

GTY Transceivers

[Figure 2-1, callout 1]

The XCZU28DR provides 16 GTY transceivers (32.75 Gb/s capable) on the PL-side.

The GTY transceivers in the XCZU28DR are grouped into four channels or quads. The reference clock for a quad can be sourced from the quad above or the quad below the GTY quad of interest. The four GTY quads used on the ZCU111 board have the connectivity listed in this section.

- Quad 128:
- MGTREFCLK0 - SFP_SI5382_IN1_C_P/N
- MGTREFCLK1 - SFP_SI5382_OUT_C_P/N
- Contains four GTY transceivers allocated to SFP[0:3] TX/RX lanes
- Quad 129:
- MGTREFCLK0 - FMCP_HSPC_GBTCLK0_M2C_C_P/N
- MGTREFCLK1 - USER_MGT_SI570_CLOCK_C_P/N
- Contains four GTY transceivers allocated to FMCP_HSPC_DP[0:3] TX/RX
- Quad 130:
- MGTREFCLK0 - FMCP_HSPC_GBTCLK1_M2C_C_P/N

- MGTREFCLK1 - USER_SMA_MGT_CLOCK_C_P/N
- Contains four GTY transceivers allocated to FMCP_HSPC_DP[4:7] TX/RX
- Quad 131:
- MGTREFCLK0 - FMCP_HSPC_GBTCLK2_M2C_C_P/N
- MGTREFCLK1 - not connected
- Contains four GTY transceivers allocated to FMCP_HSPC_DP[8:11] TX/RX

Figure 3-29 shows the MGTY assignments.

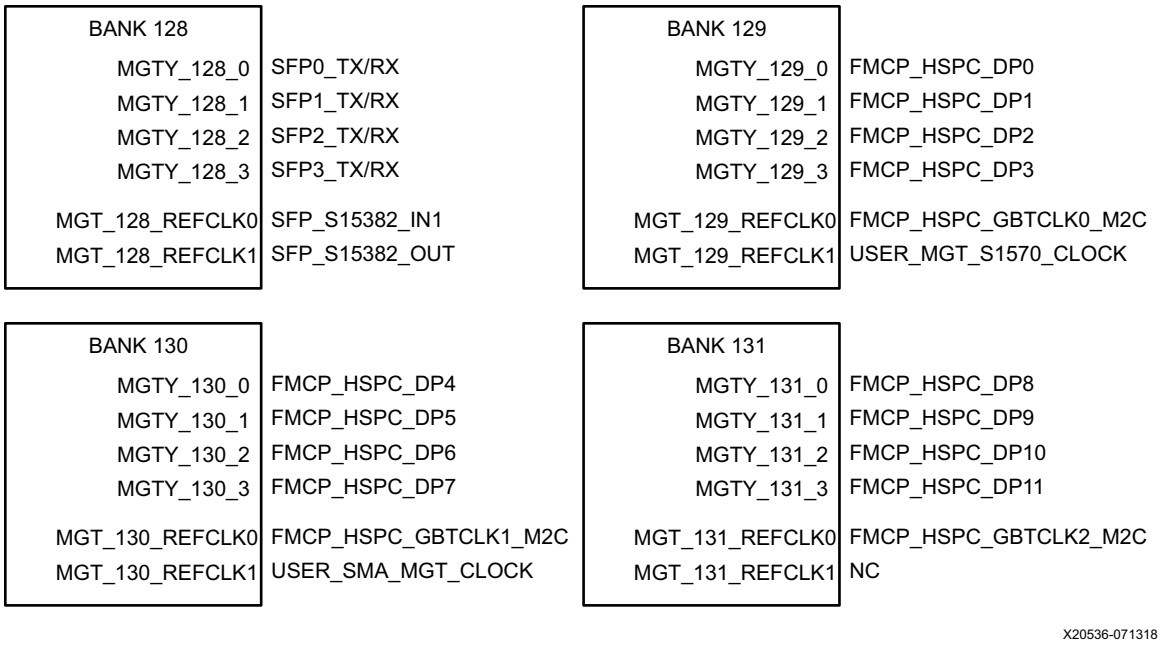

Figure 3-29: **GTY Bank Assignments**

FMCP HSPC

Twelve MGTs are provided by PL-side MGT banks 129, 130, and 131. Available MGT reference clocks include the FMC defined GBT clocks 0, 1 and 2, a programmable SI570 clock and an SMA clock.

SFP28

One PL-side GTY transceiver in bank 128 is provided for the quad SFP28 interface. Available GTY reference clocks include a jitter attenuated recovered clock from a Si5382. SFP+ modules typically provide an I2C based control interface. This I2C interface is accessible for each individual SFP28 module through the I2C multiplexer topology on the ZCU111 board. The RFSoC U1 connections for each quad are referenced in Appendix B, Xilinx Design Constraints.

For additional information on GTY transceivers, see the *UltraScale Architecture GTY Transceivers User Guide* (UG578) [Ref 6].

PS-Side: GTR Transceivers

[Figure 2-1, callout 1]

The PS-side GTR transceiver bank 505 supports two DisplayPort transmit channels, USB (3.0) and SATA, as shown in Figure 3-30.

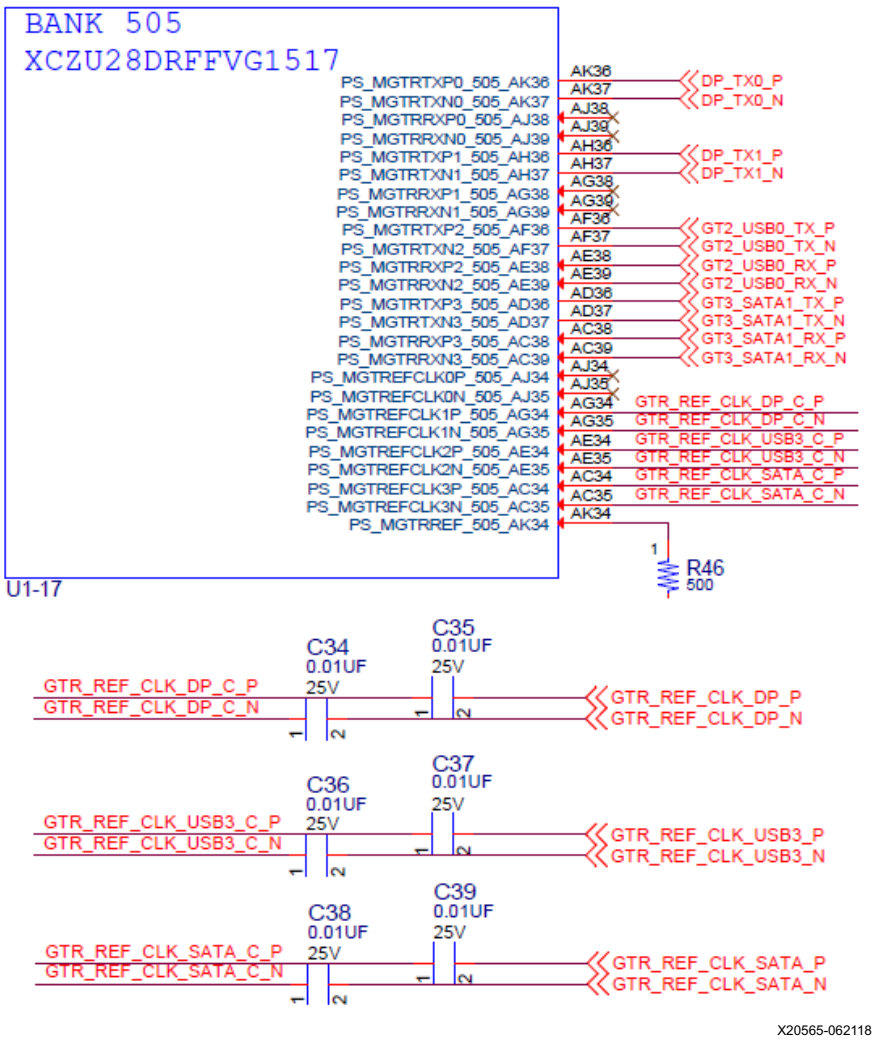

Figure 3-30: **PS-GTR Lane Assignments**

Bank 505 DP (DisplayPort) lanes 0 and 1 TX support the 2-channel source only PS-side DisplayPort circuitry described in DPAUX (MIO 27-30), page 35.

Bank 505 USB0 lane 2 supports the USB3.0 interface described in USB 3.0 Transceiver and USB 2.0 ULPI PHY, page 39.

Bank 505 SATA1 lane 3 supports the M.2 SATA connector U170 as shown in Figure 3-31.

Bank 505 reference clocks are connected to the U46 SI5341B clock generator as detailed in SI5341B 10 Independent Output Any-Frequency Clock Generator, page 47.

Bank 505 connections are referenced in Appendix B, Xilinx Design Constraints.

PS M.2 SATA Connector

[Figure 2-1, callout 34]

The M.2 SATA interface is provided for SATA SSD access using the PS-side bank 505 GTR transceiver. Figure 3-31 shows M.2 connector U40.

The socket 2 SATA adapter pinout with key M is shown in Table 3-26. SATA-A data connection is used for TX and SATA-B for RX. The M.2 connector U40 is a type 2242 (active component section 22 mm wide with overall length 42 mm form factor) used on socket 2.

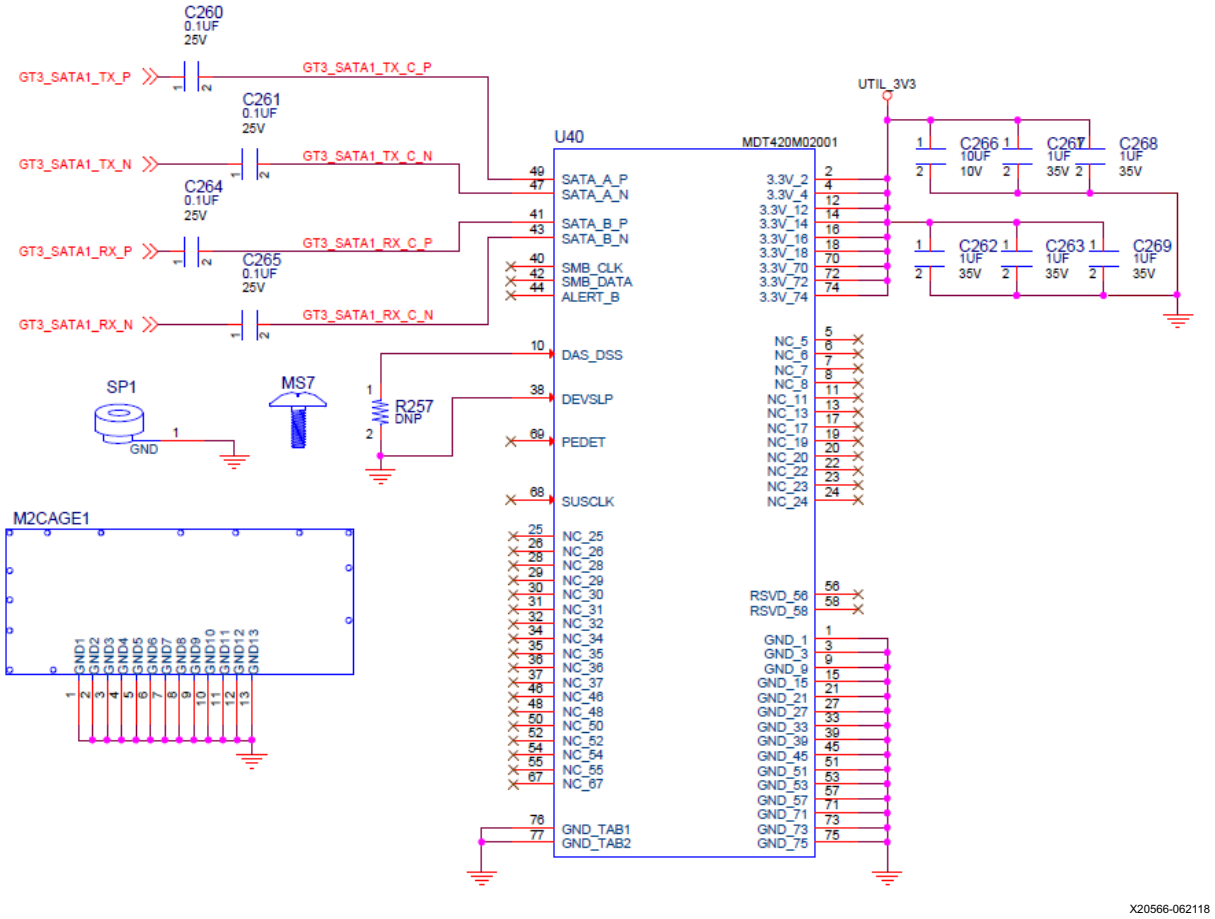

Figure 3-31: **M.2 Connector U170**

Table 3-26: **M.2 Connector U40 Pinout**

Pin	Signal
74	3.3V
72	3.3V
70	3.3V
68	SUSCLK(32 kHz) (I)(0/3.3V)
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
58	Reserved for MGFG_CLOCK
56	Reserved for MGFG_DATA
54	NC
52	NC
50	NC
48	NC
46	NC
44	ALERT# (O) (0/1.8V)
42	SMB_DATA (I/O) (0/1.8V)
40	SMB_CLK (I/O) (0/1.8V)
38	DEVSLP (I)
36	NC
34	NC
32	NC
30	NC
28	NC
26	NC
24	NC
22	NC
20	NC
18	3.3V
16	3.3V
14	3.3V
12	3.3V
10	DAS/DSS (I/O)
8	NC
6	NC

Table 3-26: **M.2 Connector U40 Pinout *(Cont'd)***

Pin	Signal
4	3.3V
2	3.3V
75	GND
73	GND
71	GND
69	PEDET (GND-SATA)
67	NC
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
	ADD_IN CARD KEY M
57	GND
55	NC
53	NC
51	GND
49	SATA-A+
47	SATA-A-
45	GND
43	SATA-B+
41	SATA-B-
39	GND
37	NC
35	NC
33	GND
31	NC
29	NC
27	GND
25	NC
23	NC
21	GND
19	NC
17	NC
15	GND
13	NC
11	NC

Table 3-26: **M.2 Connector U40 Pinout *(Cont'd)***

Pin	Signal
9	GND
7	NC
5	NC
3	GND
1	GND

The M.2 adapter tie-offs as implemented on the ZCU111 board are listed in Table 3-27.

Table 3-27: **M.2 U40 Connector Tie-offs**

M.2 Signal Name	ZCU111 Tie-Off	U40 Pin
SUSCLK	No connect	68
ALERT#	No connect	44
SMB_DATA	No connect	42
SMB_CLK	No connect	40
DEVSLP	GND	38
DAS/DSS	DNP Res to GND	10
PEDET	No connect	69
SATA-A	GTR TX	49, 47
SATA-B	GTR RX	43, 41

The M.2 U40 connector to RFSoC connections are listed in Table 3-28.

Table 3-28: **M.2 U40 Connections to the XCZU28DR RFSoC**

XCZU28DR (U1) Pin	Net Name	I/O Standard	M.2 Connector U40	
			Pin Number	Pin Name
AD36	GT3_SATA1_TX_P	(1)	49	SATA-A+
AD37	GT3_SATA1_TX_N	(1)	47	SATA-A-
AC38	GT3_SATA1_RX_P	(1)	41	SATA-B+
AC39	GT3_SATA1_RX_N	(1)	43	SATA-B-

Notes:

1. Series capacitor coupled, MGT I/F, I/O standards do not apply.

For more information, see PCI_Express_M.2_Specification_Rev1.1_TS_12092016_NCB [Ref 21].

FPGA Mezzanine Card Interface

[Figure 2-1, callouts 33,34]

The ZCU111 evaluation board supports the VITA 57.4 FPGA mezzanine card (FMC+ or FMCP) specification by providing a subset implementation of the high pin count connector at J26 (HSPC). FMC+ connectors use a 14 x 40 form factor, populated with 560 pins. The connector is keyed so that a mezzanine card, when installed on the ZCU111 evaluation board, faces away from the board

J26 FMC+ Connector Type

- Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector. For more information about SEAF series connectors, see the Samtec website [Ref 22]. For more information about the VITA 57.4 FMC+ specification, see the VITA FMC Marketing Alliance website [Ref 23].
- The 560-pin FMC+ connector defined by the FMC specification (see Appendix A, VITA 57.4 FMCP Connector Pinouts) provides connectivity for up to:
  - 160 single-ended or 80 differential user-defined signals
  - 24 transceiver differential pairs
  - 6 transceiver differential clocks
  - 4 differential clocks
  - 239 ground and 19 power connections

FMCP Connector J26

[Figure 2-1, callout 27]

The HSPC connector J26 implements a subset of the full FMCP connectivity:

- 68 single-ended or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 12 transceiver differential pairs
- 3 transceiver differential clocks
- 2 differential clocks
- 239 ground and 16 power connections

The FMCP HSPC J26 connections to RFSoC U1 are referenced in Appendix B, Xilinx Design Constraints. See the FPGA Mezzanine Card (FMC) VITA 57.4 specification [Ref 23] for additional information on the FMCP HSPC connector.

Cooling Fan Connector

[Figure 2-1, near callout 10]

The ZCU111 cooling fan connector is shown in Figure 3-32.

The ZCU111 uses the Infineon MAX6643 (U52) fan controller, which autonomously controls the fan speed by controlling the pulse width modulation (PWM) signal to the fan based on the die temperature sensed via the FPGA's DXP and DXN pins. The fan rotates slowly (acoustically quiet) when the RFSoC is cool and rotates faster as the FPGA heats up (acoustically noisy).

The fan speed (PWM) versus the RFSoC die temperature algorithm along with the over temperature set point and fan failure alarm mechanisms are defined by the strapping resistors on the MAX6643 device. The over temperature and fan failures alarms can be monitored by any available processor in the RFSoC by polling the I2C expander U22 on the I2C0 bus. See the MAX6643 [Ref 24] data sheet for more information on the device circuit implementation on this board.

Note: At initial power on, it is normal for the fan controller to energize at full speed for a few seconds.

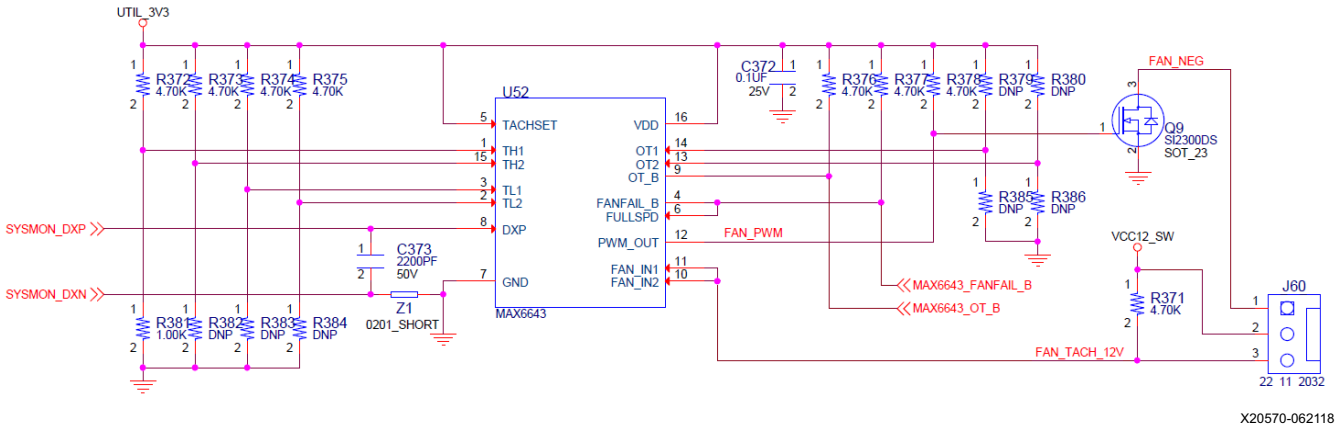

Figure 3-32: **12V Fan Header**

VADJ_FMC Power Rail

The ZCU111 evaluation board implements the ANSI/VITA 57.4 IPMI support functionality. The power control of the VADJ_FMC power rail is managed by the U42 system controller. This rail powers the FMCP HSPC (J26) VADJ pins, as well as the XCZU28DR HP banks 65, 66. The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V.

At power on, the system controller detects if an FMC module is installed on J26:

- If no card is attached to the FMCP connector, the VADJ voltage is set to 1.8V

- When an FMC card is attached, its IIC EEPROM is read to find a VADJ voltage supported by both the ZCU111 board and the FMC module, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V
- If no valid information is found in an FMC card IIC EEPROM, the VADJ_FMC rail is set to 0.0V

The system controller user interface allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ_FMC rail. Override mode is useful for FMC mezzanine cards that do not contain valid IPMI EPROM data defined by the ANSI/VITA57.1 specification.

ZCU111 System Controller

[Figure 2-1, callout 19]

The ZCU111 board includes an on-board system controller. A host PC resident system controller user interface (SCUI) is provided on the ZCU111 Evaluation Kit website. This GUI enables the query and control of select programmable features such as clocks, FMC functionality, and power system parameters. The ZCU111 web page also includes a tutorial on the SCUI (XTP517) [Ref 11] and board setup instructions (XTP518) [Ref 12].

A brief summary of these instructions are provided here:

1. Ensure that the Silicon Labs VCP USB-UART drivers are installed. See the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033) [Ref 14].
2. Download the SCUI host PC application.
3. Connect the micro-USB to ZCU111 USB-UART connector (J83).
4. Power-cycle the ZCU111.
5. Launch the SCUI.

The SCUI GUI is shown in Figure 3-33.

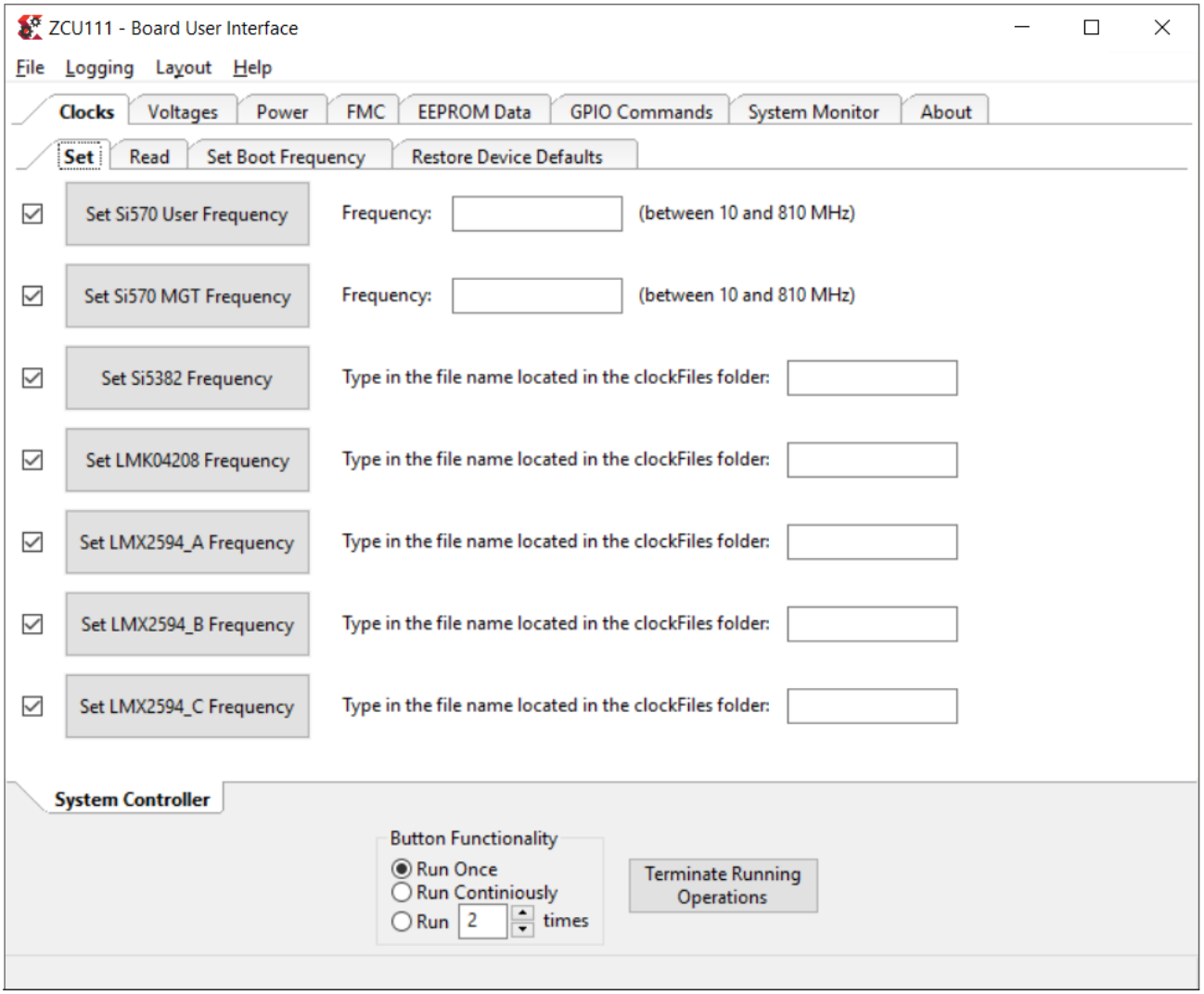

Figure 3-33: **System Controller User Interface**

On first use of the SCUI, go to the **FMC** > **Set VADJ** > **Boot-up** tab and click **USE FMC EEPROM Voltage**. The SCUI buttons gray-out during command execution and return to their original appearance when ready to accept a new command.

See the *System Controller Tutorial* (XTP517) [Ref 11] and the *ZCU111 Software Install and Board Setup Tutorial* (XTP518) [Ref 12] for more information on installing and using the system controller utility.

Switches

[Figure 2-1, callouts 27, 29, 31, and 46]

The ZCU111 board includes power, configuration, and reset switches:

- SW1 power on/off slide switch (callout 29)
- SW2 (PS_PROG_B), active-Low pushbutton (callout 31)
- SW3 (SRST_B), active-Low pushbutton (callout 27)
- SW4 (POR_B), active-Low pushbutton (callout 27)
- SW6 U1 RFSoC PS bank 503 4-pole mode DIP switch (callout 32)

Power On/Off Slide Switch

[Figure 2-1, callout 29]

The ZCU111 board power switch is SW1. Sliding the switch actuator from the off to on position applies 12V power from J52, a 6-pin mini-fit connector. Green LED DS19 illuminates when the ZCU111 board power is on. See Board Power System for details on the on-board power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the ZCU111 board power connector J52. The ATX 6-pin connector has a different pin-out than J52. Connecting an ATX 6-pin connector into J52 damages the ZCU111 board and voids the board warranty.*

Figure 3-34 shows the power connector J52, power switch SW16, and LED indicator DS19.

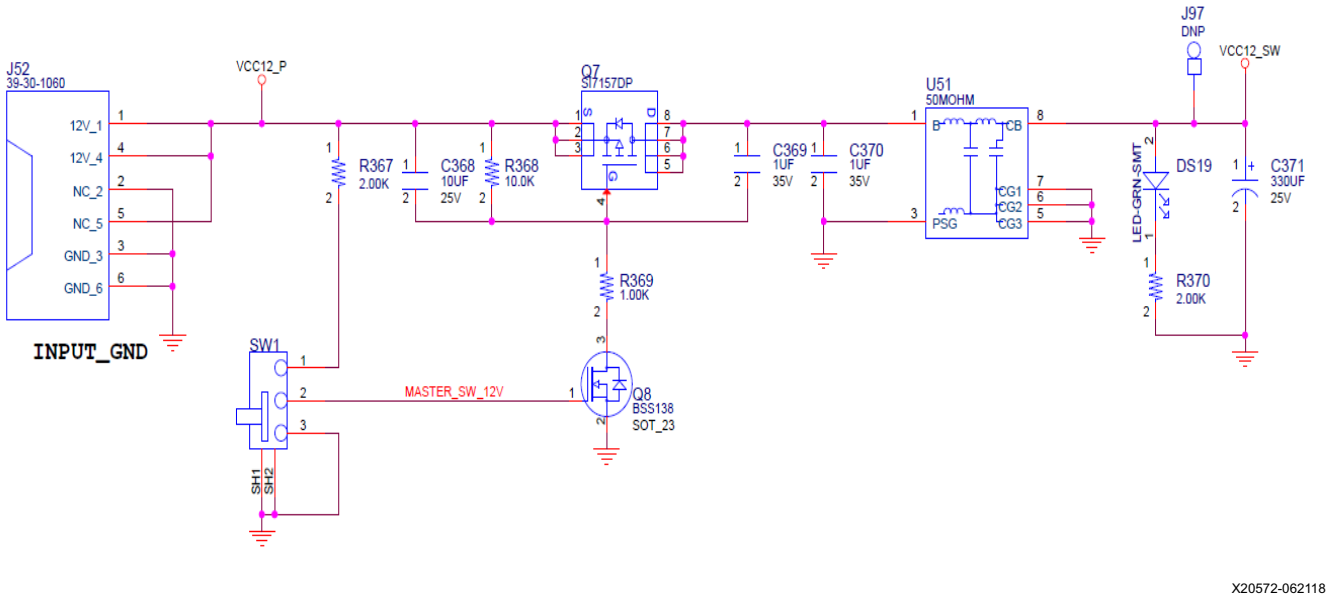

Figure 3-34: **Power Input**

Program_B Pushbutton

[Figure 2-1, callout 31]

PS_PROG_B pushbutton switch SW2 grounds the XCZU28DR RFSoC PS_PROG_B pin AA27 when pressed (see Figure 3-35). This action clears the programmable logic configuration, which can then be acted on by the PS software. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] for information about Zynq UltraScale+ RFSoC configuration.

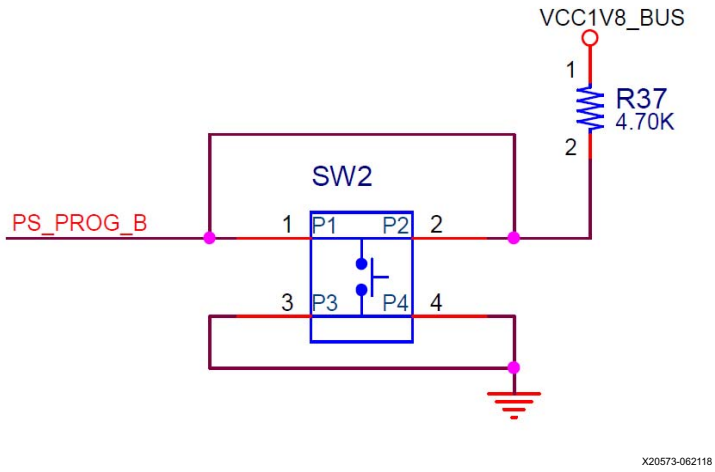

Figure 3-35: **PS_PROG_B Pushbutton Switch**

System Reset Pushbuttons

[Figure 2-1, callout 54]

Figure 3-36 shows the reset circuitry for the PS.

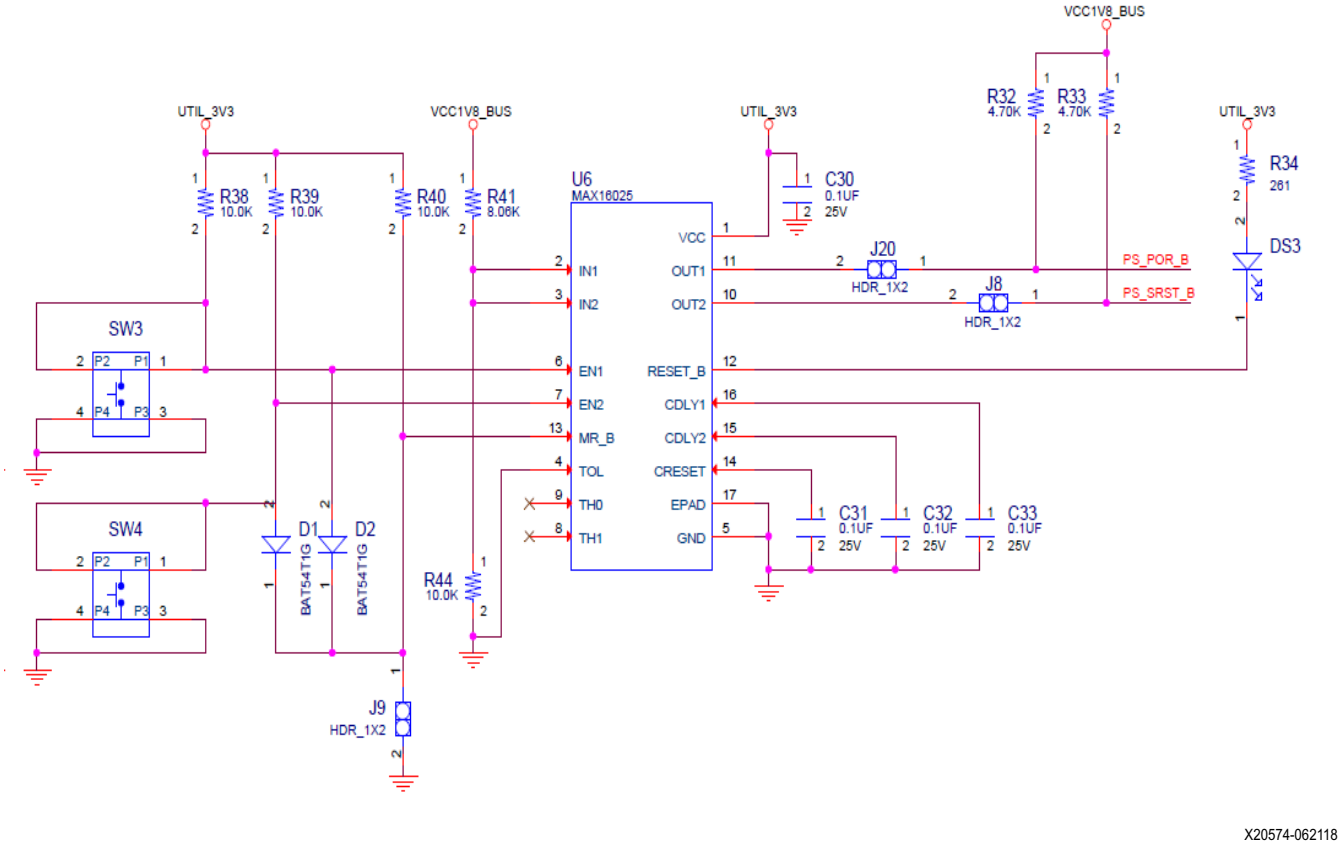

Figure 3-36: **PS SRST_B and POR_B Pushbutton Switches SW3 and SW4**

PS_POR_B Reset

Depressing and then releasing pushbutton SW4 causes net PS_POR_B to strobe Low. This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply power-good signal. When the voltage at IN1 is below its threshold or EN1 (P.B. switch SW4 is pressed) goes Low, OUT1 (PS_POR_B) goes Low.

PS_SRST_B Reset

Depressing and then releasing pushbutton SW3 causes net PS_SRST_B to strobe Low. This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps. When the voltage at IN2 is below its threshold or EN2 (P.B. switch SW3 is pressed) goes Low, OUT2 (PS_SRST_B) goes Low.

Active-Low reset output RST_B asserts when any of the monitored voltages (IN_) falls below the respective threshold, any EN_ goes Low, or MR is asserted. RST_B remains asserted for the reset time-out period after all of the monitored voltages exceed their respective threshold, all EN_ are High, all OUT_ are High, and MR is deasserted. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) [Ref 3] for information on the resets.

Board Power System

[Figure 2-15, callout 35]

The ZCU111 evaluation board uses power management ICs (PMIC) and power regulators from Infineon [Ref 25] to supply the core and auxiliary voltages listed in Table 3-29. See schematic 0381811.

Table 3-29: **Power System Devices**

Ref Des, PMBus ADDR	Controller or Regulator	Rail Name	Voltage (V)	Max Current (A)	INA226 Sensor	INA226 PMBus ADDR	Sense Resistor (Ω)	0381811 Schem. Page
U53 (0X43)	IRPS5401_A	VCCINT_IO_BRAM_PS_SDFEC	0.85	10	U59	0x41	R394: 0.005	47
	IRPS5401_B	VCC1V8	1.8	2	U61	0x42	R388: 0.005	
	IRPS5401_C	VCCINT_RF	0.85	7	U63	0x49	R389: 0.005	
	IRPS5401_D	Tied to chan. C						
	IRPS5401_LDO	N.C.						
U55 (0X44)	IRPS5401_A	UTIL_3V3	3.3	10.5				49
	IRPS5401_B	UTIL_2V5	2.5	2				
	IRPS5401_C	MGT1V2	1.2	6	U66	0x47	R398: 0.005	
	IRPS5401_D	Tied to chan. C						
	IRPS5401_LDO	MGTRAVCC	0.85	0.5	DVM on R399		R399: 0.005	

Table 3-29: **Power System Devices *(Cont'd)***

Ref Des, PMBus ADDR	Controller or Regulator	Rail Name	Voltage (V)	Max Current (A)	INA226 Sensor	INA226 PMBus ADDR	Sense Resistor (Ω)	0381811 Schem. Page
U57 (0X45)	IRPS5401_A	VCC1V2	1.2	6	U60	0x43	R418: 0.005	51
	IRPS5401_B	DAC_AVTT	2.5/3.0	0.5	U3	0x4A	R409: 0.005	
	IRPS5401_C	VADJ_FMC	1.8	5	U64	0x45	R412: 0.005	
	IRPS5401_D	Tied to 3C						
	IRPS5401_LDO	MGT1V8	1.8	0.5	U65	0x48	R413: 0.005	
U68	IR38064	VCCINT	0.85	30	U67	0x40	R447: 0.002	54
U70	IR38060	MGTAVCC	0.9	3	U69	0x46	R456: 0.002	55
U72	IFX1763	DAC_AVCCAUX	1.8	0.5	U71	0x4B	R463: 0.005	56
U74	IR38060	ADC_AVCCAUX	1.8	2	U73	0x4D	R471: 0.005	57
U75	IR38060	UTIL_1V13	1.13	4				58
U76	IR3883	UTIL_5V0	5	2.7				59
U101	ISL80112	ADC_AVCC	0.925	2	U77	0x4C	R489: 0.005	60
U78	ISL80112	DAC_AVCC	0.925	1	U79	0x4E	R494: 0.005	60
U81	IR3897	PL_DDR4_VTT	0.6	±3.0				61
U82	IR3897	PS_DDR4_VTT	0.6	±3.0				61

The FMCP HSPC (J26) and VADJ pins are wired to the programmable rail VADJ_FMC. The VADJ_FMC rail is programmed to 1.80V by default. The VADJ_FMC rail also powers the XCZU28DR HP banks 65 and 66 (see Table 3-1). Documentation describing PMBus programming for the Infineon power controllers is available at the Infineon website [Ref 25]. The PCB layout and power system design meets the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 4].

Monitoring Voltage and Current

Voltage and current monitoring and control are available for the Infineon power system controllers through the Infineon PowIRCenter graphical user interface. The PMBus interface controllers and regulators listed in Table 3-29 are accessed through the 1x3 PMBus connector J19, which is provided for use with the Infineon PowIRCenter USB cable (Infineon part number USB005) and can be ordered from the Infineon website [Ref 25]. The associated Infineon PowerTool GUI can be downloaded from the Infineon website. This is the simplest and most convenient way to monitor the voltage and current values for the Infineon PMBus programmed power rails listed in Table 3-29.

Each Infineon PMIC controller can report the voltage and current of its controlled rail to the Infineon GUI for display to the user. Fourteen rails have a TI INA226 PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA226 to report the sensed parameters separately on the PMBus. The rails configured with the INA226 power monitors are shown in Table 3-29.

As described in I2C0 (MIO 14-15), page 29, the I2C0 bus provides access to the PMBus power controllers and the INA226 power monitors via the U23 PCA9544A bus switch. All PMBus controlled Infineon regulators are tied to the IRPS5401_SDA/SCL PMBUS, while the INA226 power monitors are separated on to INA226_PMBUS.

Figure 3-3, page 29 and Table 3-5, page 31 document the I2C0 bus access path to the Infineon PMBus controllers and INA226 power monitor op amps. Also, see schematic 0381881. Power rail measurements are accessible to the system controller and RFSoC PL logic through their respective I2C0 bus connections.

VITA 57.4 FMCP Connector Pinouts

Overview

Figure A-1 shows the pinout of the FPGA plus mezzanine card (FMCP) high pin count (HSPC) connector defined by the VITA 57.4 FMC specification. For a description of how the ZCU111 evaluation board implements the FMCP specification, see FPGA Mezzanine Card Interface, page 79.

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

X20518-062118

Figure A-1: **FMCP HSPC Connector Pinout**

Appendix B

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the ZCU111 board provides for designs targeting the ZCU111 evaluation board. Net names in the constraints listed correlate with net names on the latest ZCU111 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 8] for more information.

The HSPC FMCP connector J26 is connected to RFSoC banks powered by the variable voltage V_{AJ_FMC}. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT: *See ZCU111 board documentation for the XDC file.*

Appendix C

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

ZCU111 Evaluation Kit — Master Answer Record 70958

For Technical Support, open a Support Service Request.

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

HW-FMC-XM500

Overview

The ZU28DRF-FFVG1517 contains eight multi-gigasample (4 GSPS), 12-bit RF analog-to-digital converter (RF-ADC) channels across four banks and eight multi-gigasample (6.544 GSPS), 14-bit RF digital-to-analog (RF-DAC) converter channels across two banks. The ZCU111 board provides a pair of Samtec LPAF connectors for the RF-ADC/RF-DAC clock and RF signals. The FMC-XM500 is an out-of-the-box AMS RFMC plug-in card that mates with the ZCU111 board via two Samtec LPAM (8x40) connectors on the bottom of the XM500 card with connectivity featuring:

- Two DACs and two ADCs routed to HF baluns with –1dB Pi pad attenuators and then to SMAs
- Two DACs and two ADCs routed to LF baluns with –3dB Pi pad attenuators and then to SMAs
- Four DACs and four ADCs routed to SMAs for use with external custom baluns and filters
- Four pairs external input clocks for ADCs
- Four pairs external input clocks for DACs
- While the ZCU111 board RFSoC bank 224-227 VCM nets are wired to the ZCU111 LPAF J47 connector, the RFMC XM500 plug-in board mating LPAM J333 connector does not break out these VCM nets

AMS RFMC Plug-in Card Interface

On the bottom of the XM500 card, two Samtec LPAM (8x40) terminals provide access to the ADC/DAC clocking and data path signals. The Samtec part number is LPAM-40-010-S-08-2-K-TR. Figure D-1 shows the Samtec LPAM connector.

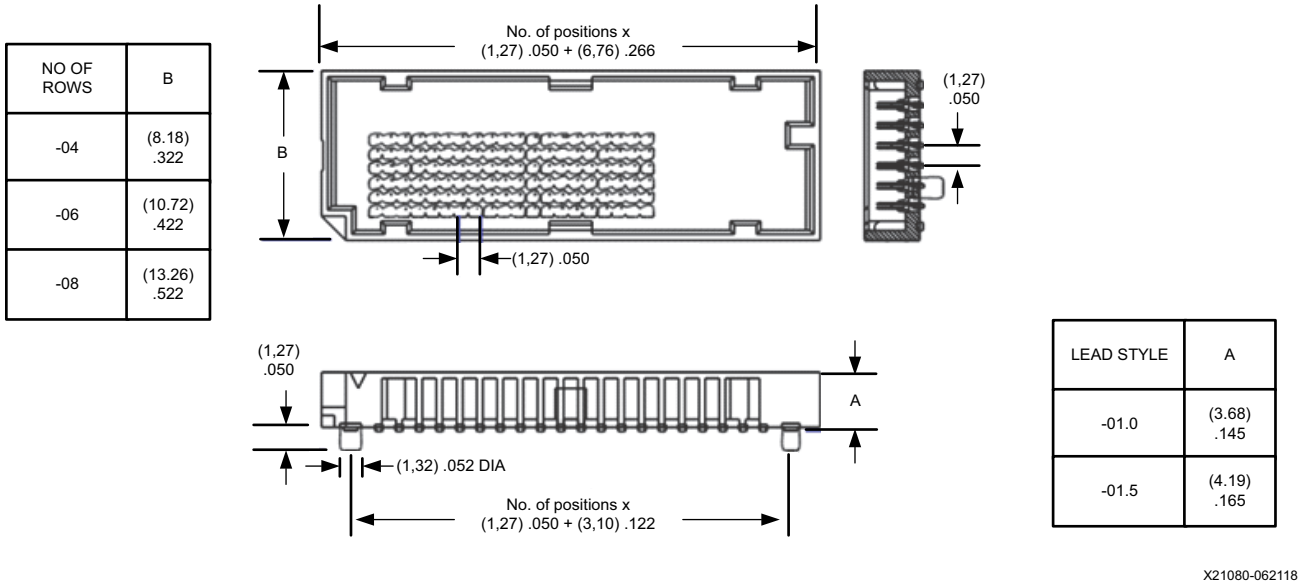

Figure D-1: **Samtec LPAM Connector**

XM500 Card Components

The XM500 card component locations are shown in Figure D-2 and listed in Table D-1.

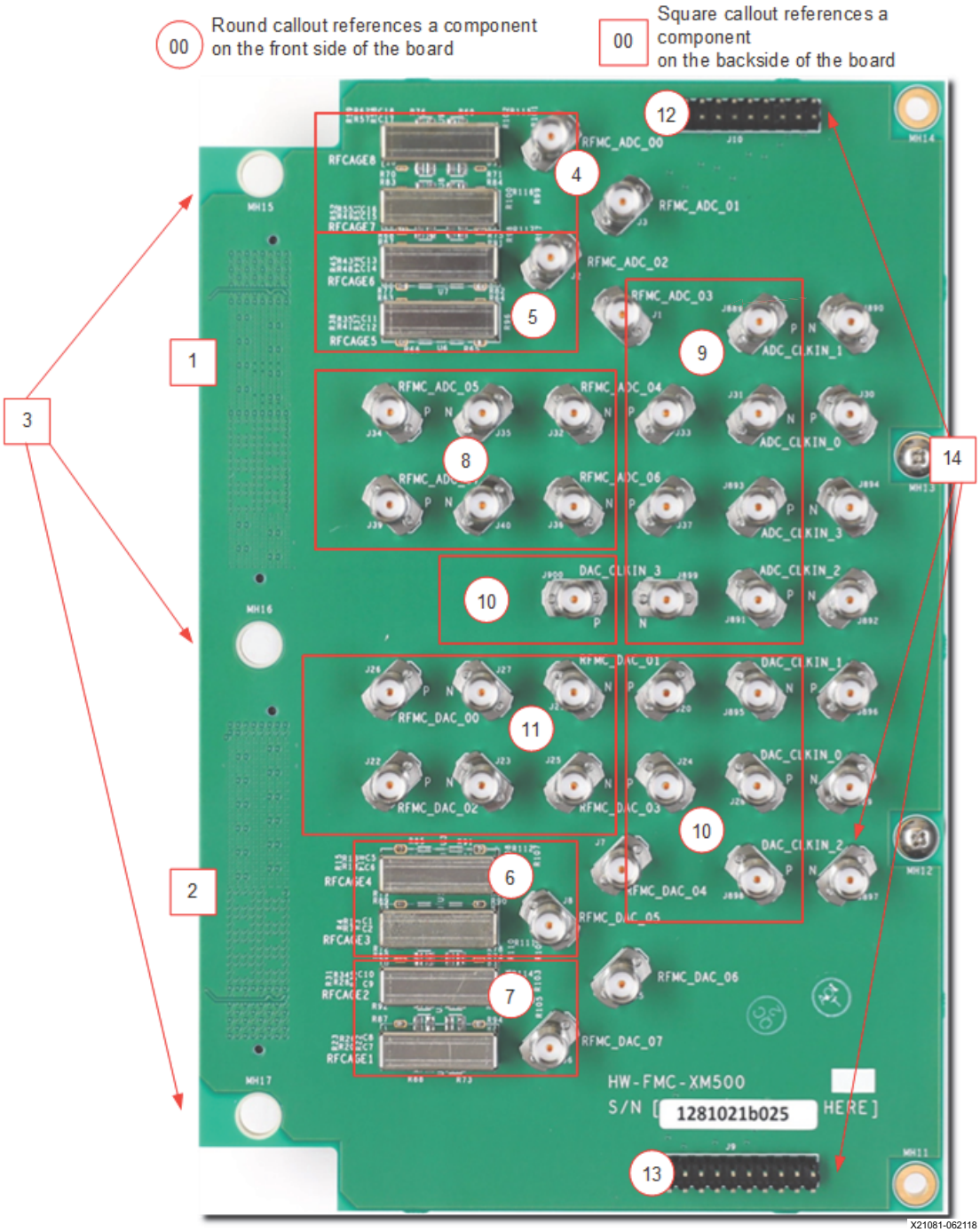

Figure D-2: **XM500 Card Components**

Table D-1: **XM500 Card Components Locations**

Callout No.	Ref Des.	Feature	Notes	Schematic 0381858 Page
1	J333	ADC connector, low profile array (LPAM) terminal	Samtec LPAM-40-010-S-08-2-K-TR	3
2	J888	DAC connector, low profile array (LPAM) terminal	Samtec LPAM-40-010-S-08-2-K-TR	4
3	MH15,16,17	Mounting holes for the jackscrew of LPAF connector mounting system	Jackscrew attached with ZCU111 board	2
4	U8, U9, J3, J4	Two channels ADC Low frequency baluns with -3dB attenuators to SMAs	Mini-Circuits TCM2-33WX+	2
5	U6, U7, J1, J2	Two channels ADC High frequency baluns with -1dB attenuators to SMAs	Anaren BD1631J50100AHF	2
6	U1, U3, J7, J8	Two channels DAC High frequency baluns with -1dB attenuators to SMAs	Anaren BD1631J50100AHF	2
7	U4, U5, J5, J6	Two channels DAC Low frequency baluns with -3dB attenuators to SMAs	Mini-Circuits TCM2-33WX+	2
8	J32-J37, J39, J40	Four channels ADCs to SMAs	Molex Screw-on SMA: 0732513481	3
9	J30, J31, J891-J894, J889, J890	Four pairs external input clock SMAs for ADC	Molex Screw-on SMA: 0732513481	3
10	J28, J29, J895-J900	Four pairs external input clock SMAs for DAC	Molex Screw-on SMA: 0732513481	4
11	J20-J27	Four channels DACs to SMAs	Molex Screw-on SMA: 0732513481	4
12	J10	20 ADC I/Os to 2x10 header	2.54mm 2x10 header	3
13	J9	20 DAC I/Os to 2x10 header	2.54mm 2x10 header	4
14	MH11-MH14	Mounting holes for standoff	#4-40 0.625" alum standoffs (5/8" or 15.9mm)	2

ADC/DAC Bank Data and Clock Channel Mapping

This section provides details on the ZCU111 board U1 RFSoC ZCU28DR ADC/DAC bank data and clock channel mapping. Figure D-3 and Figure D-4 show the ZCU111 board U1 RFSoC ZC28DR bank RF channel mapping and RF bank connectivity.

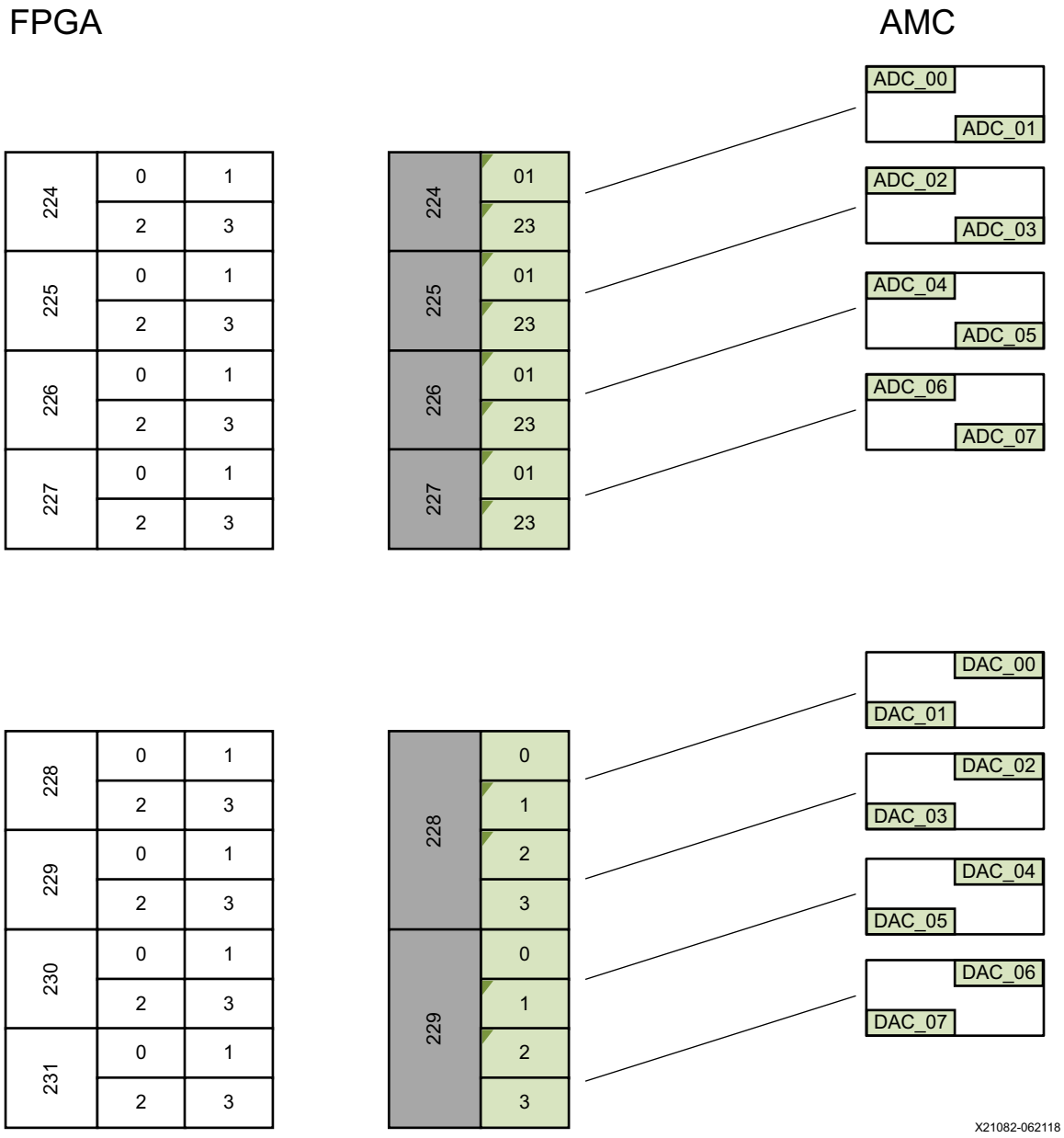

Figure D-3: **RFSoC ZCU28DR ADC/DAC Bank Channel Mapping**

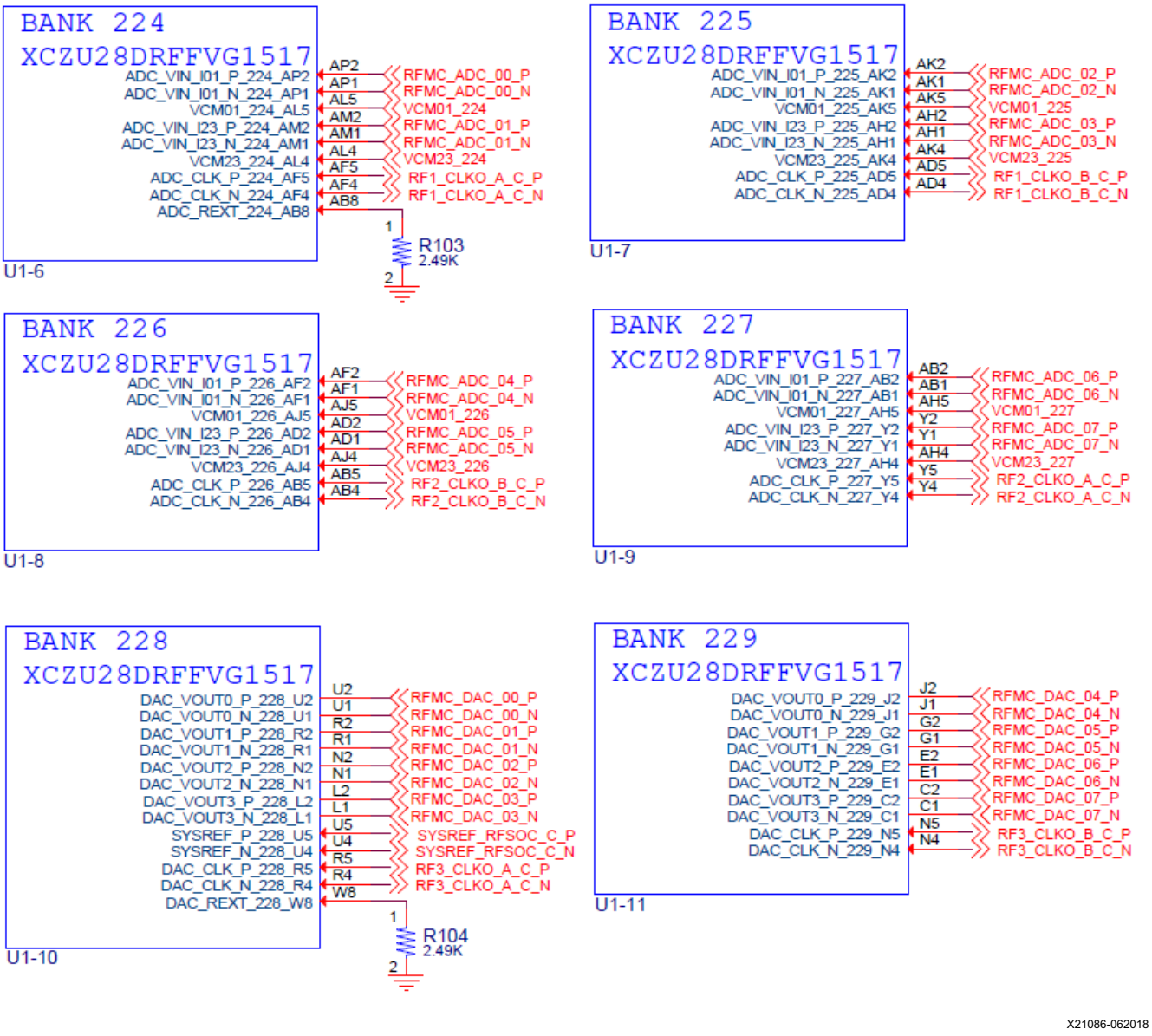

Figure D-4: **RFSoC ZCU28DR ADC/DAC Banks 224-229 Connectivity**

XM500 ADC/DAC Data and Clock SMA

This section provides details on the XM500 ADC/DAC data and clock SMA, and I/O 2x10 header connectors to the ZCU111 board U1 RFSoC ZCU28DR channel mapping. Table D-2 provides the XM500 ADC/DAC data and clock mapping.

Table D-2: **XM500 ADC/DAC Data and Clock Mapping**

SMA Ref. Des.	ADC/DAC Data or Clock
J26(P)/J27(N)	DAC228_T0_Ch0
J20(P)/J21(N)	DAC228_T0_Ch1
J22(P)/J23(N)	DAC228_T0_Ch2
J24(P)/J25(N)	DAC228_T0_Ch3
J7	DAC229_T1_Ch0
J8	DAC229_T1_Ch1
J5	DAC229_T1_Ch2
J6	DAC229_T1_Ch3
J4	ADC224_T0_Ch0
J3	ADC224_T0_Ch1
J2	ADC225_T1_Ch0
J1	ADC225_T1_Ch1
J33(P)/J32(N)	ADC226_T2_Ch0
J34(P)/J35(N)	ADC226_T2_Ch1
J37(P)/J36(N)	ADC227_T3_Ch0
J39(P)/J40(N)	ADC227_T3_Ch1
J30(P)/J31(N)	ADC224_T0_CLKIN
J889(P)/J890(N)	ADC225_T1_CLKIN
J891(P)/J892(N)	ADC226_T2_CLKIN
J893(P)/J894(N)	ADC227_T3_CLKIN
J28(P)/J29(N)	DAC228_T0_CLKIN
J896(P)/J895(N)	DAC229_T1_CLKIN
J898(P)/J897(N)	DAC230_T2_CLKIN
J900(P)/J899(N)	DAC231_T3_CLKIN
J9 2x10 header	See Figure D-5
J10 2x10 header	See Figure D-5

Figure D-5 shows the XM500 2x10 header connector J10 ADCIO and J9 DACIO to the ZCU111 board U1 RFSoC ZC28DR bank 84 and 87 mapping.

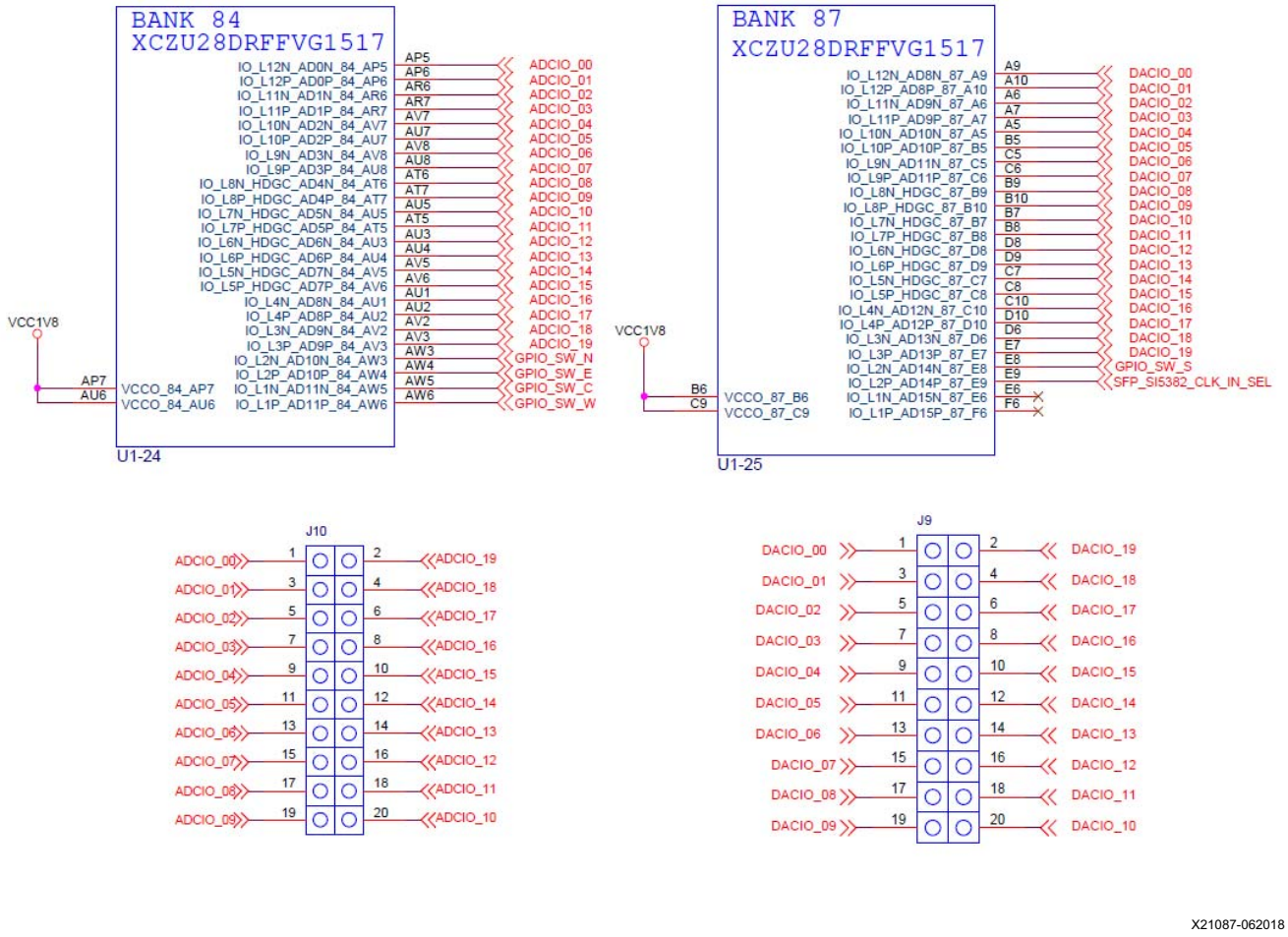

Figure D-5: **XM500 J10, J9 2x10 Header to ZCU111 Board U1 RFSoC ZCU28DR ADC/DAC Banks 84, 87 Connectivity**

Table D-3 and Table D-4 show end-to-end ZCU111 U1 RFSoC pin number to LPAF/M connector pin number to XM500 connectors pin number.

Table D-3: **ZCU111 U1 RFSoC RF Bank 224-229 Connections to XM500**

ZCU111 Board (with LPAF)					Mated Conns	XM500 RFMC Card (with LPAM)		
ZU28DR U1 Bank	ZU28DR U1 Pin Name	ZU28DR U1 Pin	ZCU111 Net Name	ZCU111 LPAF	LPAF/ M Pin	XM500 LPAM	SE-to-Diff Element	XM500 SMA Ref Des
224	ADC_VIN_I01_P_224_AP2	AP2	RFMC_ADC_00_P	J47	G9	J333	U9 Mini-Circuits Xfmr 0-1 GHz	J4
	ADC_VIN_I01_N_224_AP1	AP1	RFMC_ADC_00_N		F9			
	VCM01_224_AL5	AL5	VCM01_224(1)		A21			NC
	ADC_VIN_I23_P_224_AM2	AM2	RFMC_ADC_01_P		C10		U8 Mini-Circuits Xfmr 0-1 GHz	J3
	ADC_VIN_I23_N_224_AM1	AM1	RFMC_ADC_01_N		B10			
	VCM23_224_AL4	AL4	VCM23_224(1)		B21			NC
225	ADC_VIN_I01_P_225_AK2	AK2	RFMC_ADC_02_P	J47	G12	J333	U7 Anaren Balun 1-4 GHz	J2
	ADC_VIN_I01_N_225_AK1	AK1	RFMC_ADC_02_N		F12			
	VCM01_225_AK5	AK5	VCM01_225(1)		C21			NC
	ADC_VIN_I23_P_225_AH2	AH2	RFMC_ADC_03_P		C13		U6 Anaren Balun 1-4 GHz	J1
	ADC_VIN_I23_N_225_AH1	AH1	RFMC_ADC_03_N		B13			
	VCM23_225_AK4	AK4	VCM23_225(1)		D21			NC
226	ADC_VIN_I01_P_226_AF2	AF2	RFMC_ADC_04_P	J47	G15	J333	None, Direct	J33
	ADC_VIN_I01_N_226_AF1	AF1	RFMC_ADC_04_N		F15			J32
	VCM01_226_AJ5	AJ5	VCM01_226(1)		E21			NC
	ADC_VIN_I23_P_226_AD2	AD2	RFMC_ADC_05_P		C16		None, Direct	J34
	ADC_VIN_I23_N_226_AD1	AD1	RFMC_ADC_05_N		B16			J35
	VCM23_226_AJ4	AJ4	VCM23_226(1)		F21			NC
227	ADC_VIN_I01_P_227_AB2	AB2	RFMC_ADC_06_P	J47	G18	J333	None, Direct	J37
	ADC_VIN_I01_N_227_AB1	AB1	RFMC_ADC_06_N		F18			J36
	VCM01_227_AH5	AH5	VCM01_227(1)		G21			NC
	ADC_VIN_I23_P_227_Y2	Y2	RFMC_ADC_07_P		C19		None, Direct	J39
	ADC_VIN_I23_N_227_Y1	Y1	RFMC_ADC_07_N		B19			J40
	VCM23_227_AH4	AH4	VCM23_227(1)		H21			NC

Notes:

1. While the ZCU111 board RFSoC bank 224-227 VCM nets are wired to the LPAF J47 connector, the RFMC XM500 plug-in board mating LPAM J333 connector does not break out these nets.

Table D-3: **ZCU111 U1 RFSoC RF Bank 224-229 Connections to XM500 *(Cont'd)***

ZCU111 Board (with LPAF)					Mated Conns	XM500 RFMC Card (with LPAM)		
ZU28DR U1 Bank	ZU28DR U1 Pin Name	ZU28DR U1 Pin	ZCU111 Net Name	ZCU111 LPAF	LPAF/ M Pin	XM500 LPAM	SE-to-Diff Element	XM500 SMA Ref Des
228	DAC_VOUT0_P_228_U2	U2	RFMC_DAC_00_P	J94	C10	J888	None, Direct	J26
	DAC_VOUT0_N_228_U1	U1	RFMC_DAC_00_N		B10			J27
	DAC_VOUT1_P_228_R2	R2	RFMC_DAC_01_P		G11		None, Direct	J20
	DAC_VOUT1_N_228_R1	R1	RFMC_DAC_01_N		F11			J21
	DAC_VOUT2_P_228_N2	N2	RFMC_DAC_02_P		C13		None, Direct	J22
	DAC_VOUT2_N_228_N1	N1	RFMC_DAC_02_N		B13			J23
	DAC_VOUT3_P_228_L2	L2	RFMC_DAC_03_P		G14		None, Direct	J24
	DAC_VOUT3_N_228_L1	L1	RFMC_DAC_03_N		F14			J25
229	DAC_VOUT0_P_229_J2	J2	RFMC_DAC_04_P	J94	C16	J888	U3 Anaren Balun 1-4 GHz	J7
	DAC_VOUT0_N_229_J1	J1	RFMC_DAC_04_N		B16			
	DAC_VOUT1_P_229_G2	G2	RFMC_DAC_05_P		G17		U1 Anaren Balun 1-4 GHz	J8
	DAC_VOUT1_N_229_G1	G1	RFMC_DAC_05_N		F17			
	DAC_VOUT2_P_229_E2	E2	RFMC_DAC_06_P		C19		U5 Mini-Circuits Xfmr 0-1 GHz	J5
	DAC_VOUT2_N_229_E1	E1	RFMC_DAC_06_N		B19			
	DAC_VOUT3_P_229_C2	C2	RFMC_DAC_07_P		G20		U4 Mini-Circuits Xfmr 0-1 GHz	J6
	DAC_VOUT3_N_229_C1	C1	RFMC_DAC_07_N		F20			

Table D-4: **ZCU111 U1 RFSoC Bank 84 ADCIO and Bank 87 DACIO Connections to XM500**

ZCU111 Board (with LPAF)					Mated Conns	XM500 RFMC Card (with LPAM)		
ZU28DR U1 Bank	ZU28DR U1 Pin Name	ZU28DR U1 Pin	ZCU111 Net Name	ZCU111 LPAF	LPAF/M Pin	XM500 LPAM	2x10 Header Pin	XM500 Header
84	IO_L12N_AD0N_84_AP5	AP5	ADCIO_00	J47	A2	J333	1	J10 2x10 Male-Pin Header
	IO_L12P_AD0P_84_AP6	AP6	ADCIO_01		A4		3	
	IO_L11N_AD1N_84_AR6	AR6	ADCIO_02		B1		5	
	IO_L11P_AD1P_84_AR7	AR7	ADCIO_03		B3		7	
	IO_L10N_AD2N_84_AV7	AV7	ADCIO_04		B5		9	
	IO_L10P_AD2P_84_AU7	AU7	ADCIO_05		C2		11	
	IO_L9N_AD3N_84_AV8	AV8	ADCIO_06		C4		13	
	IO_L9P_AD3P_84_AU8	AU8	ADCIO_07		D1		15	
	IO_L8N_HDGC_AD4N_84_AT6	AT6	ADCIO_08		D3		17	
	IO_L8P_HDGC_AD4P_84_AT7	AT7	ADCIO_09		D5		19	
	IO_L7N_HDGC_AD5N_84_AU5	AU5	ADCIO_10		E2		20	
	IO_L7P_HDGC_AD5P_84_AT5	AT5	ADCIO_11		E4		18	
	IO_L6N_HDGC_AD6N_84_AU3	AU3	ADCIO_12		F1		16	
	IO_L6P_HDGC_AD6P_84_AU4	AU4	ADCIO_13		F3		14	
	IO_L5N_HDGC_AD7N_84_AV5	AV5	ADCIO_14		F5		12	
	IO_L5P_HDGC_AD7P_84_AV6	AV6	ADCIO_15		G2		10	
	IO_L4N_AD8N_84_AU1	AU1	ADCIO_16		G4		8	
	IO_L4P_AD8P_84_AU2	AU2	ADCIO_17		H1		6	
	IO_L3N_AD9N_84_AV2	AV2	ADCIO_18		H3		4	
	IO_L3P_AD9P_84_AV3	AV3	ADCIO_19		H5		2	

Table D-4: **ZCU111 U1 RFSoC Bank 84 ADCIO and Bank 87 DACIO Connections to XM500 *(Cont'd)***

ZCU111 Board (with LPAF)					Mated Conns	XM500 RFMC Card (with LPAM)		
ZU28DR U1 Bank	ZU28DR U1 Pin Name	ZU28DR U1 Pin	ZCU111 Net Name	ZCU111 LPAF	LPAF/M Pin	XM500 LPAM	2x10 Header Pin	XM500 Header
87	IO_L12N_AD8N_87_A9	A9	DACIO_00	J94	A37	J888	1	J9 2x10 Male-Pin Header
	IO_L12P_AD8P_87_A10	A10	DACIO_01		A39		3	
	IO_L11N_AD9N_87_A6	A6	DACIO_02		B36		5	
	IO_L11P_AD9P_87_A7	A7	DACIO_03		B38		7	
	IO_L10N_AD10N_87_A5	A5	DACIO_04		B40		9	
	IO_L10P_AD10P_87_B5	B5	DACIO_05		C37		11	
	IO_L9N_AD11N_87_C5	C5	DACIO_06		C39		13	
	IO_L9P_AD11P_87_C6	C6	DACIO_07		D36		15	
	IO_L8N_HDGC_87_B9	B9	DACIO_08		D28		17	
	IO_L8P_HDGC_87_B10	B10	DACIO_09		D40		19	
	IO_L7N_HDGC_87_B7	B7	DACIO_10		E37		20	
	IO_L7P_HDGC_87_B8	B8	DACIO_11		E39		18	
	IO_L6N_HDGC_87_D8	D8	DACIO_12		F36		16	
	IO_L6P_HDGC_87_D9	D9	DACIO_13		F38		14	
	IO_L5N_HDGC_87_C7	C7	DACIO_14		F40		12	
	IO_L5P_HDGC_87_C8	C8	DACIO_15		G37		10	
	IO_L4N_AD12N_87_C10	C10	DACIO_16		G39		8	
	IO_L4P_AD12P_87_D10	D10	DACIO_17		H36		6	
	IO_L3N_AD13N_87_D6	D6	DACIO_18		H38		4	
	IO_L3P_AD13P_87_E7	E7	DACIO_19		H40		2	

Appendix E

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the ZCU111 board and its documentation is available on the following websites.

ZCU111 Evaluation Kit

ZCU111 Evaluation Kit — Master Answer Record 70958

These Xilinx documents provide supplemental material useful with this guide:

1. *Zynq UltraScale+ RFSoC Data Sheet: Overview* (DS889)
2. *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
3. *Zynq UltraScale+ Device Technical Reference Manual* (UG1085)
4. *UltraScale Architecture PCB Design User Guide* (UG583)
5. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
6. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
7. *Tera Term Terminal Emulator Installation Guide* (UG1036)
8. *Vivado Design Suite User Guide: Using Constraints* (UG903)
9. *UltraScale Architecture System Monitor User Guide* (UG580)
10. *UltraScale Architecture Clocking Resources User Guide* (UG572)
11. *ZCU111 System Controller Tutorial* (XTP517)
12. *ZCU111 Software Install and Board Setup Tutorial* (XTP518)
13. *ZCU111 Restoring Flash Tutorial* (XTP515)
14. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)

The following websites provide supplemental material useful with this guide:

15. Micron Technology: www.micron.com
    (MTA4ATF51264HZ-2G6E1, MT40A512M16JY-075E, MT25QU02GCBB8E12-0SIT data sheets)
16. Standard Microsystems Corporation (SMSC): www.microchip.com
    (USB3320 data sheet)
17. SanDisk Corporation: www.sandisk.com
18. SD Association: www.sdcard.org
19. Silicon Labs: www.silabs.com/Pages/default.aspx
    (SI570, SI5341B, SI5382A)

20. Texas Instruments: www.ti.com/product/DP83867IR
(TCA9548A, PCA9544A, DP83867, LMK04208, LMK00304, LMK00804, LMX2594)

21. PCI: https://pcisig.com/specifications/pciexpress/M.2_Specification/

22. Samtec, Inc.: www.samtec.com
(SEAF series connectors, LPAF connectors)

23. VITA FMC Marketing Alliance: www.vita.com/fmc
(FPGA Mezzanine Card (FMC) VITA 57.1, 57.4 specifications)

24. Maxim Integrated Circuits: https://www.maximintegrated.com
(MAX16025TE+, MAX6643)

25. Infineon Integrated Circuits: https://www.infineonintegrated.com/

26. Future Technology Devices International Ltd.: www.ftdichip.com
(FT4232HL)

27. Digilent: www.digilentinc.com
(Pmod peripheral modules)

28. SNIA Technology Affiliates: https://ta.snia.org/higherlogic/ws/public
(SFF-8402, SFF-8432)

29. NXP Semiconductors: www.nxp.com
(SC18IS602)

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