PE29100 Evaluation Kit (EVK) User's Manual

UltraCMOS® High-speed FET Driver, 33 MHz

PE29100 Evaluation Kit

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Introduction

Introduction

The PE29100 evaluation board allows the user to evaluate the PE29100 gate driver in a half-bridge configuration. The PE29100 integrated high-speed driver is designated to control the gates of external power devices, such as enhancement mode gallium nitride (eGaN®) FETs. The outputs of the PE29100 are capable of providing switching transition speeds in the sub nano-second range for hard switching applications up to 33 MHz.

The PE29100 evaluation kit (EVK) user's manual includes the evaluation board schematic, circuit description, quick start guide, measurement results and a Bill of Materials (BoM).

Application Support

For any technical inquiries regarding the evaluation kit or software, please visit applications support at www.psemi.com (fastest response) or call (858) 731-9400.

Evaluation Kit Contents and Requirements

Kit Contents

The PE29100 EVK includes the following hardware required to evaluate the FET driver.

Table 1 • *PE29100 Evaluation Kit Contents*

Quality	Description
1	PE29100 FET driver evaluation board assembly (PRT-66476)

Hardware Requirements

In order to evaluate the performance of the evaluation board, the following equipment is required:

- High speed digital oscilloscope
- Functional generator (PWM)
- High voltage DC power supply
- DC power supply
- DC test leads

Safety Precautions

Caution: The PE29100 FET driver EVK contains components that might be damaged by exposure to voltages in excess of the specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals or signal inputs or outputs.

Caution: PCB surface can become hot. Contact may cause burns do not touch!

Evaluation Board Assembly

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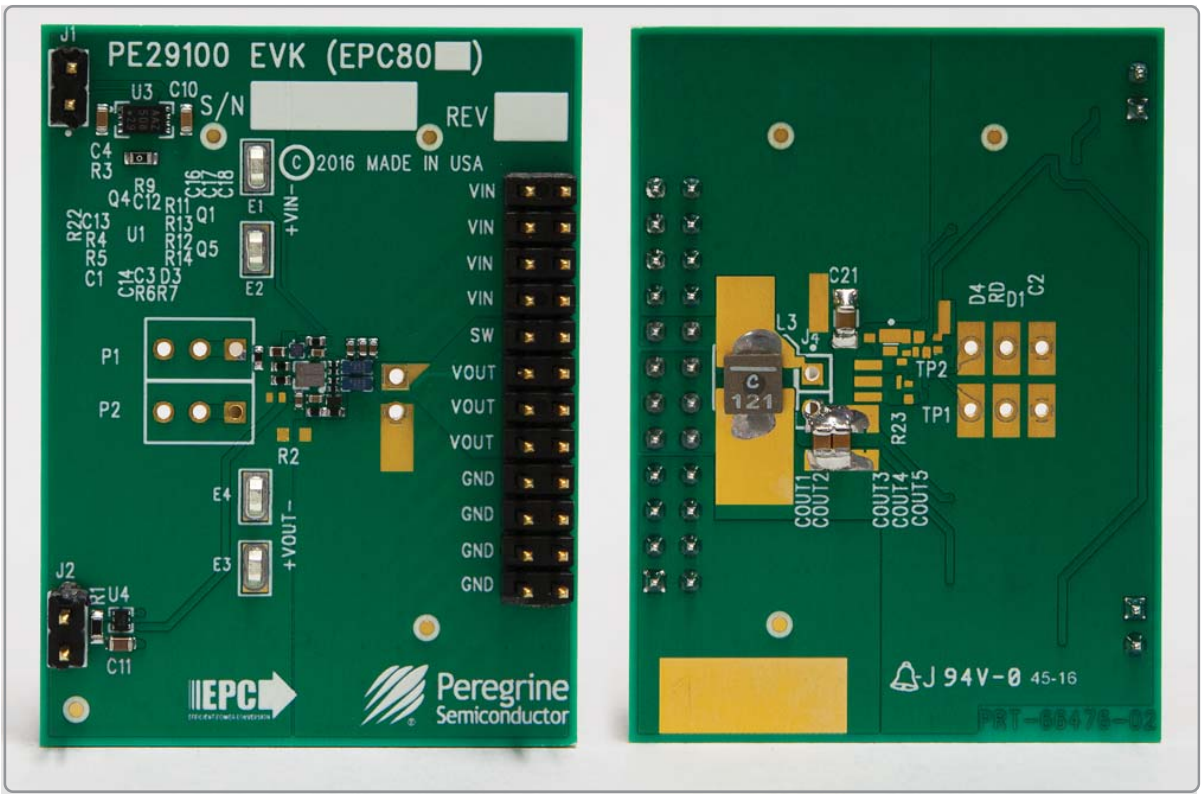
Evaluation Board Assembly Overview

The evaluation board (EVB) is assembled with a PE29100 FET driver and two EPC8009 eGaN FETs. Headers are included for signal input and power connections and probe points are included for waveform measurements.

Figure 1 • ***PE29100 Evaluation Board Assembly***



Block Diagram and Schematic

The block diagram and schematic of the evaluation board are shown in **Figure 2** and **Figure 3**.

Figure 2 • ***PE29100 Evaluation Board Block Diagram***

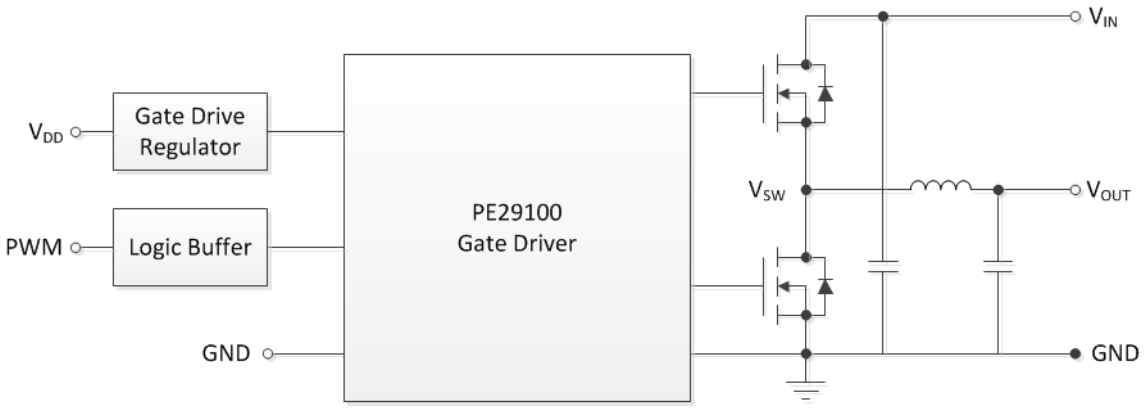
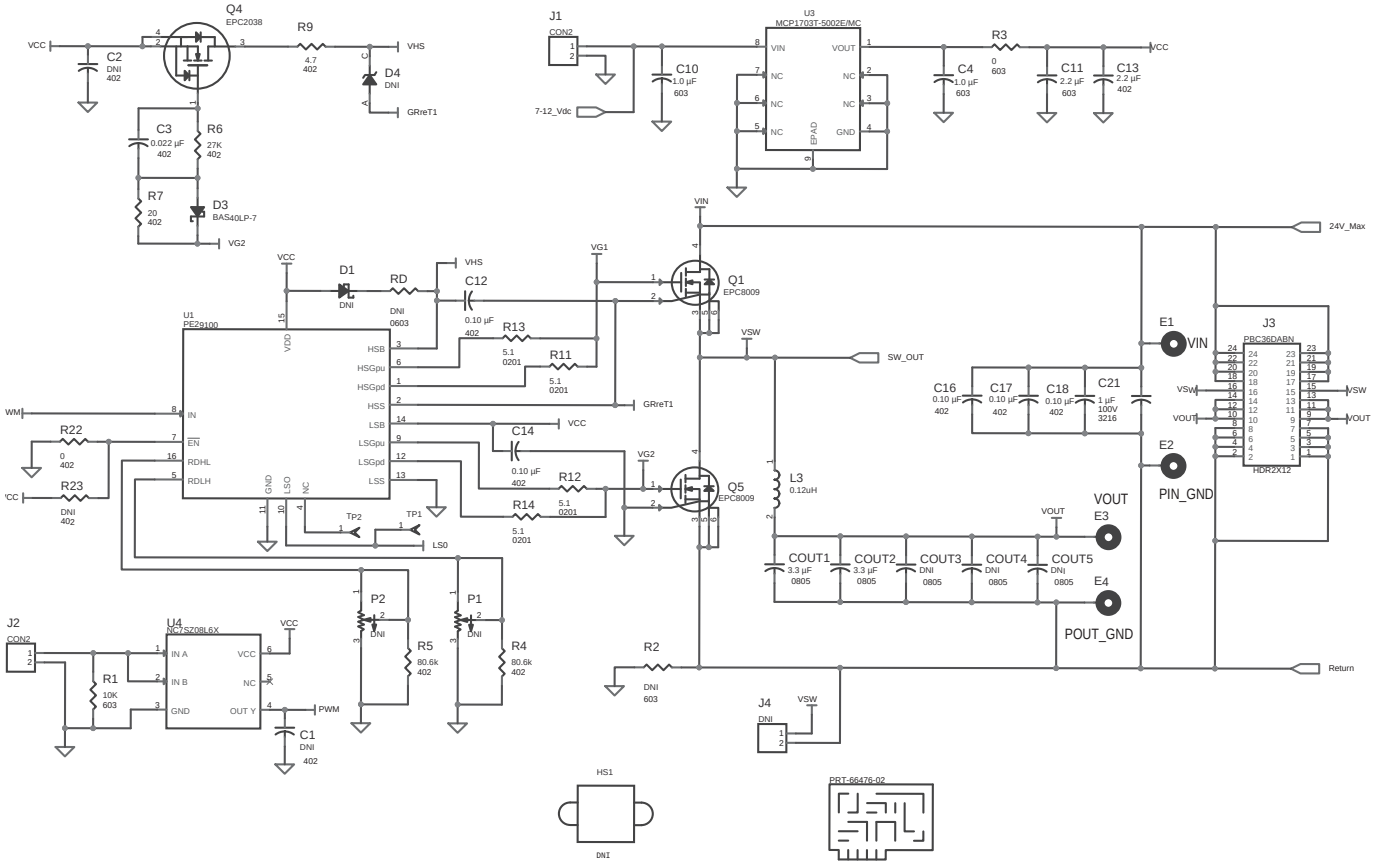


Figure 3 • *PE29100 Evaluation Board Schematic*(*)



Note: * CAUTION: Parts and assemblies susceptible to damage by electrostatic discharge (ESD).

Circuit Description

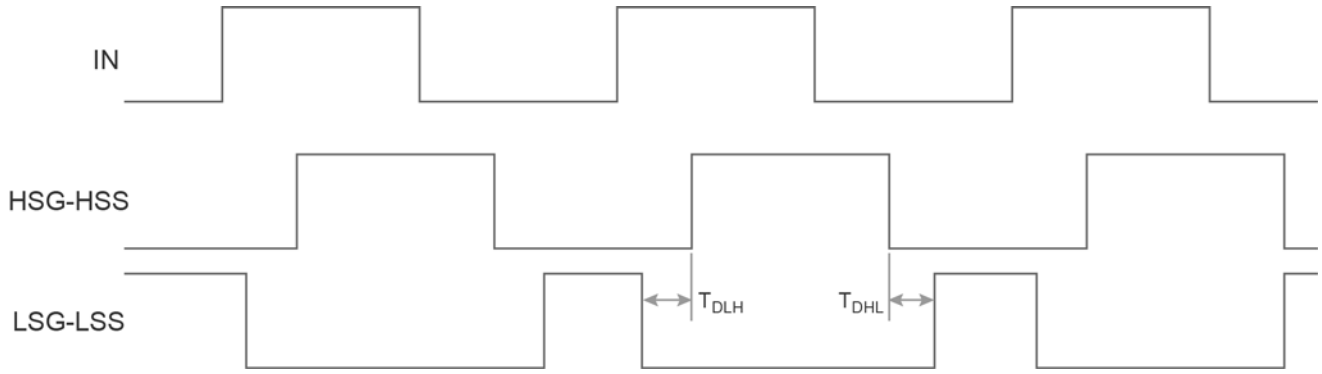
The evaluation board is configured with a PE29100 gate driver (U1) and two EPC8009 eGaN FETs (Q1 and Q5) in half-bridge configuration. An additional eGaN FET (Q4) is used as a synchronous bootstrap diode to prevent overvoltage to the gate of Q1. Gate resistors (R11–R14) are required to de-Q the inductance in the gate loop and dampen any ringing on the FET gates and the SW node.

The PE29100 features an external dead-time adjustment that allows the user to control the timing of the low-side and high-side gates to eliminate any large shoot-through currents, which could dramatically reduce the efficiency of the circuit and potentially damage the eGaN FETs. Resistors R4 and R5 are used to adjust the timing of the output waveforms and have been configured to provide approximately 4 ns of dead-time.

Note: During low-to-high switching transitions, the dead-time should be limited to 4 ns when reverse current is present on the switch node. Above 4 ns and under no load conditions, reverse current can cause cycle skipping of the high-side gate.

The dead-time resistors only affect the low-side output; the high-side output will always equal the duty-cycle of the input. The high-side FET gate node will track the duty cycle of the PWM input with a shift in the response as shown in **Figure 4**, as both rising and falling edges are shifted in the same direction. The low-side FET node duty cycle can be controlled with the dead-time resistors as each resistor will move the rising and falling edges in opposite directions. R5 will change the dead-time from LSG falling to HSG rising and R4 will change the dead-time from HSG falling to LSG rising.

Figure 4 • *PE29100 Dead-time Waveforms*



Quick Start Guide

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Quick Start Overview

This chapter will guide the user through the operating specifications, hardware configuration, test setup and test results. Operating the EVB beyond the operating specifications can result in damage to the high-speed driver and/or the power transistors.

Evaluation Board Overview

The evaluation board is designed to ease customer evaluation of Peregrine's products. The board contains:

- Header pins and jumpers for power supply and PWM connections
- Test points for performance verification

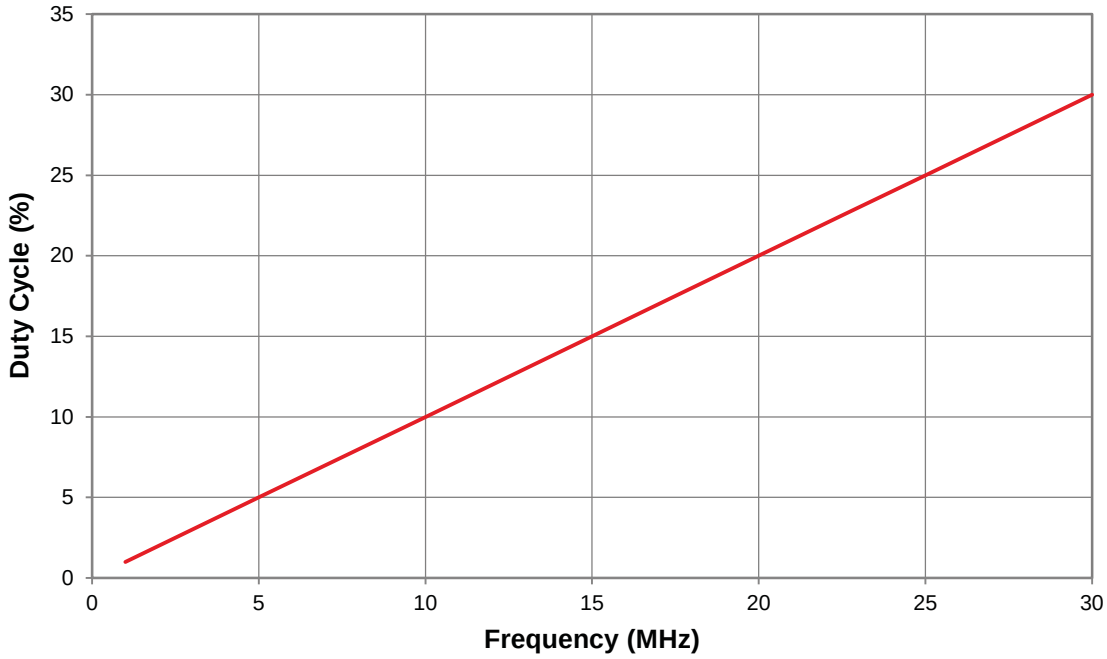
The operating specifications of the evaluation board are:

- Maximum input operating voltage of 30V(1)
- Maximum output current of 2.5A continuous(1)
- Switching frequency, 5–33 MHz(1)(2)
- Minimum high-side ouput pulse width of 10 ns(2)
- Minimum low-side ouput pulse width of 10 ns(2)

Notes:

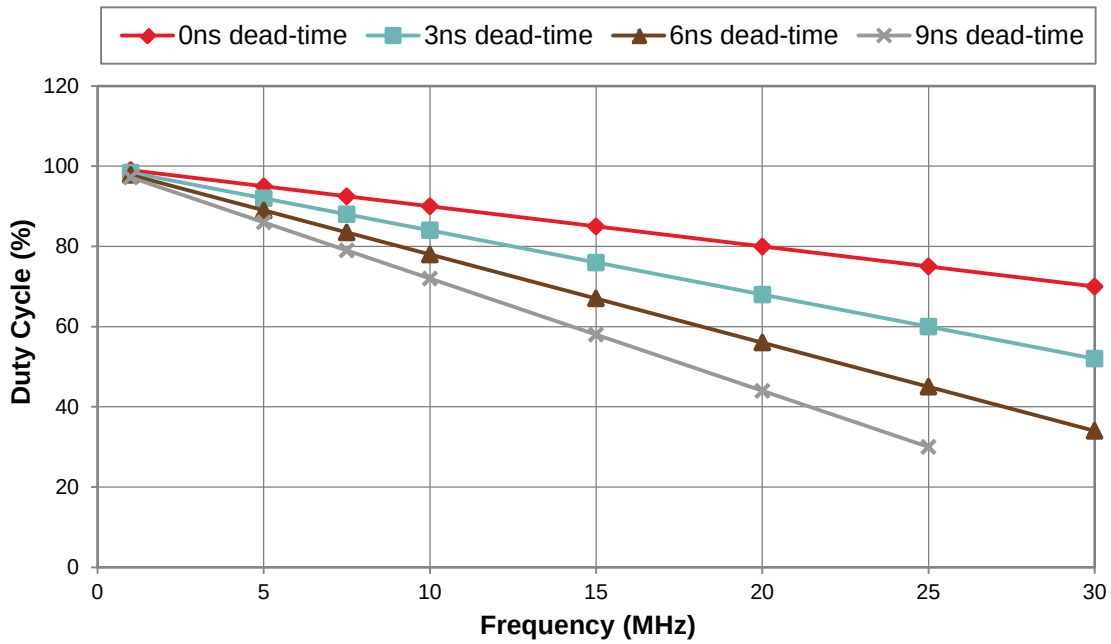
1) Assumes inductive load, maximum current depends on die temperature—actual maximum current with subject to switching frequency, bus voltage and thermals.
2) The minimum positive output pulse width should be limited to 10 ns. Operating the positive pulse width below 10 ns can result in a steady ON state condition to the high-side gate; therefore, potentially damaging the high-side device. A similar condition can result in the low-side output if the minimum negative pulse width extends below 10 ns. **Figure 5** and **Figure 6** show the relationship between operating frequency and duty cycle for the high-side and low-side minimum output pulse widths.

Figure 5 • *Duty-cycle Limit for 10 ns High-side Output Pulse Width Independent of Dead-time Setting*(*)



Note: * Area above line safe.

Figure 6 • *Duty-cycle Limit for 10 ns Low-side Output Pulse Width*(*)

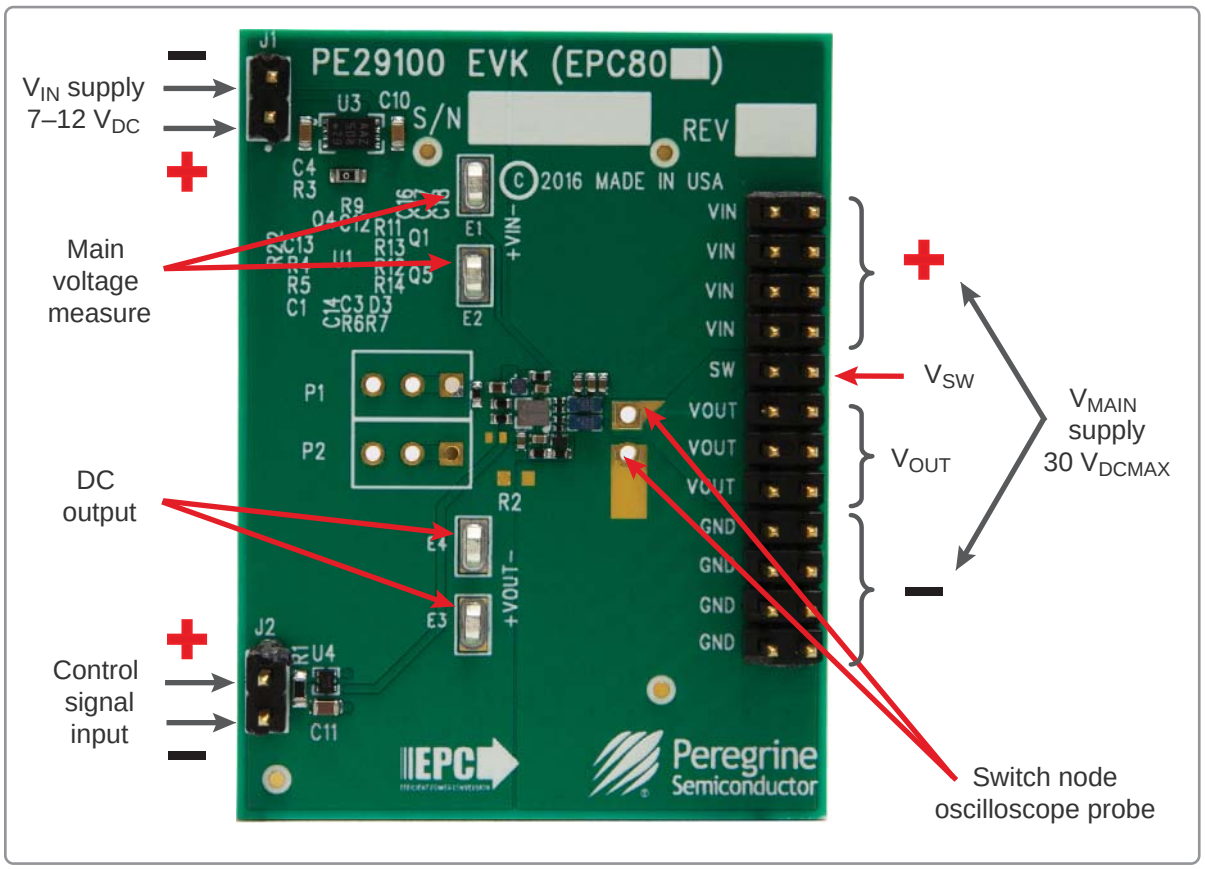


Note: * Area below line safe.

Evaluation Test Setup

Figure 7 shows the test setup for the PE29100 evaluation board. Make sure that the specified safety precautions mentioned in "Safety Precautions" on page 2 are followed.

Figure 7 • *PE29100 Evaluation Board Test Setup*



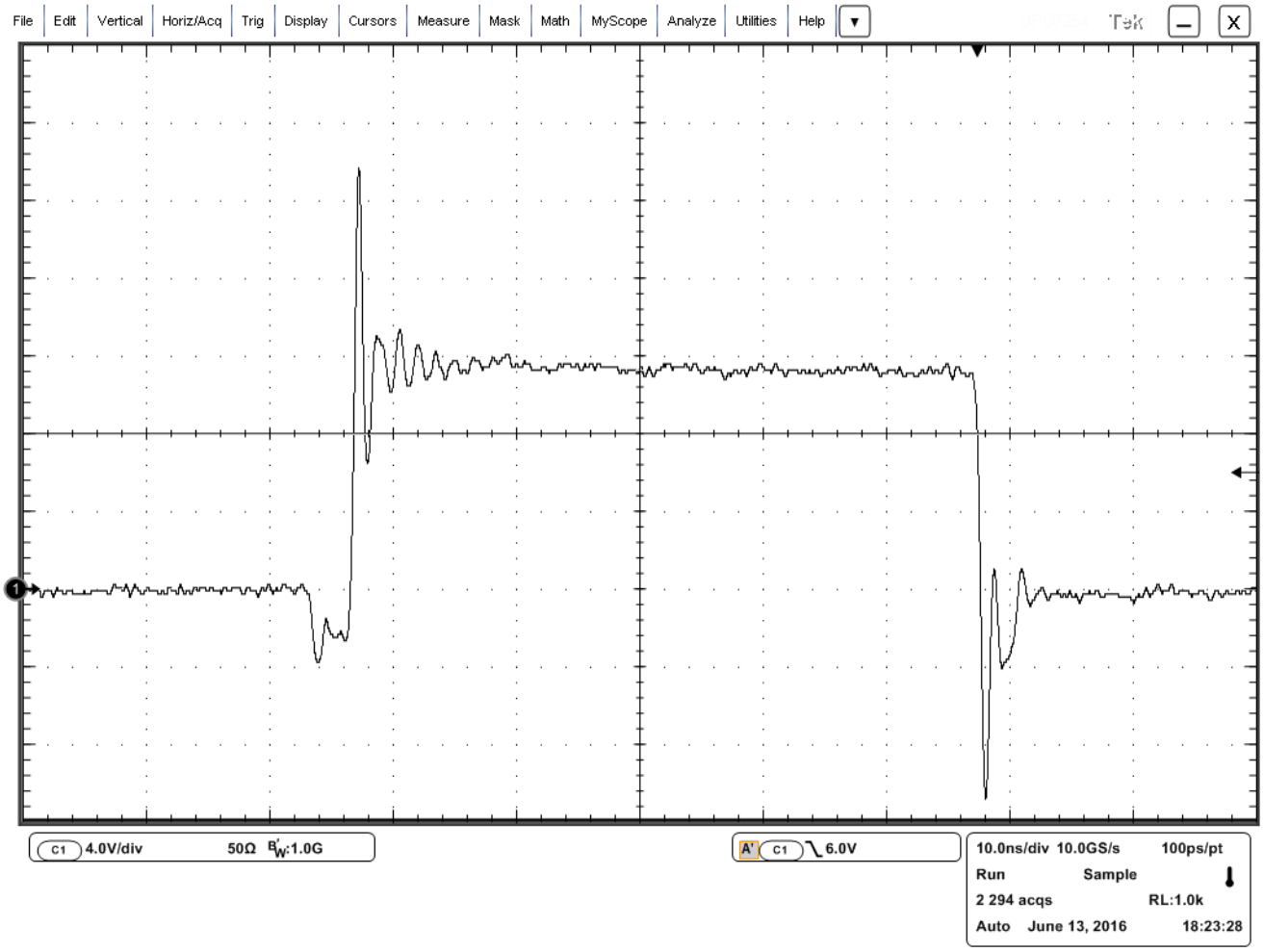
Hardware Operation

The general guidelines for operating the hardware evaluation board are listed in this section. Follow the steps to configure the hardware properly for the performance.

1) Verify that all DC power supplies are turned off before proceeding.
2) Connect the PE29100 power supply to pin 1 (J1) and ground return to pin 2 (J1).
3) Connect the input PWM control signal to pin 1 (J2) and ground return to pin 2 (J2).
4) Connect the main input power supply to VIN (J3) and the ground return to GND (J3).
5) Monitor the main supply with a voltmeter connected across test points E1 (+) and E2 (–).
6) Monitor the DC output with a voltmeter connected across test points E3 (+) and E4 (–).
7) Apply between 7V and 12V to power the PE29100 driver.
8) Set the function generator to supply a 50% duty cycle at 10 MHz with a maximum amplitude of 3 V_{PP} and a 1.5V offset.
9) Adjust the bus voltage to the required value making sure not to exceed the absolute maximum voltage of 30V on VIN (E1 and E2). Increase voltage slowly while monitoring operation to ensure the FETs are operating within their datasheet parameters.
10) Once operational, adjust the bus voltage PWM control within the operating range and observe the output switching behavior.
11) A DC load can be attached to the V_{OUT} and GND pins of J3.
12) Using a high frequency probe, carefully measure the driver output to achieve the waveforms shown in **Figure 8**. Be careful not to damage the FETs if trying to measure the signals on the eGaN FET gates.
13) Follow the above steps in reverse to power down the evaluation board.

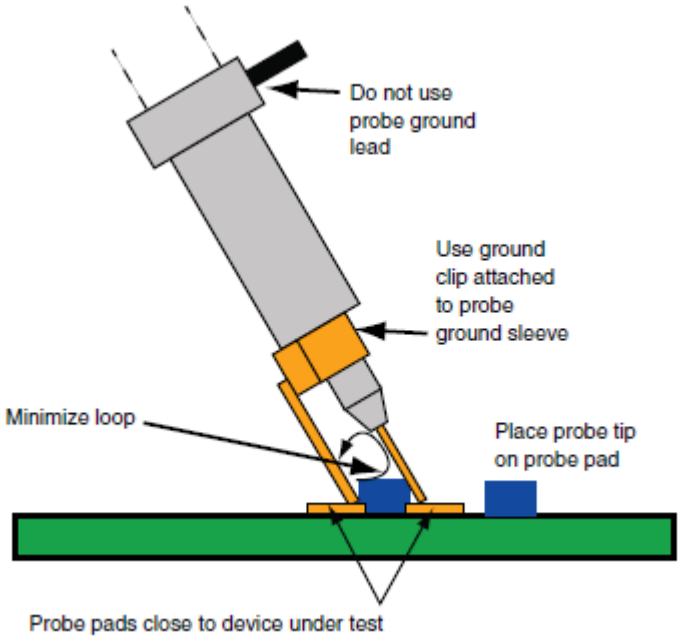
Note: When measuring the high frequency content of switch node, care must be taken to avoid long ground leads. Measure the switch node by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminal provided. See **Figure 9** for proper scope probe technique.

Figure 8 • *Oscilloscope Plot Showing SW Node Signals*(*)



Note: * V_{IN} = 12V, F_{SW} = 10 MHz, I_{LOAD} = 2A

Figure 9 • *Proper Oscilloscope Probe Measurements Technique*



Thermal Considerations

The PE29100 evaluation board includes two EPC8009 eGaN FETs. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The evaluation board is intended for bench evaluation with low ambient temperature and convection cooling. The addition of the heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125 °C.

Note: The PE29100 evaluation board does not have any current or thermal protection on board.

Technical Resources

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Technical Resources

Additional technical resources are available for download in the Products section at www.psemi.com. These include the Product Specification datasheet, S-parameters, zip file, evaluation kit schematic and bill of materials, material declaration form and PC-compatible software file.