Peregrine Semiconductor

Product Specification

PE423422

UltraCMOS® SPDT RF Switch 100–6000 MHz

Features

- AEC-Q100 Grade 2 certified
- Supports operating temperature up to +105°C
- Low insertion loss
  - 0.25 dB @ 1000 MHz
  - 0.40 dB @ 3000 MHz
  - 0.65 dB @ 5000 MHz
  - 0.90 dB @ 6000 MHz
- High isolation
  - 41 dB @ 1000 MHz
  - 28 dB @ 3000 MHz
  - 20 dB @ 5000 MHz
  - 16 dB @ 6000 MHz
- Excellent linearity
  - IIP2 of 115 dBm
  - IIP3 of 73.5 dBm
- High ESD tolerance
  - 1kV HBM on all pins
  - 200V MM on all pins
  - 1kV CDM on all pins
- Wide supply range of 2.3V to 5.5V

Product Description

The PE423422 is a HaRP™ technology-enhanced reflective SPDT RF switch. It has received AEC-Q100 Grade 2 certification and meets the quality and performance standards that makes it suitable for use in harsh automotive environments. It is designed to cover a wide range of wireless applications from 100 MHz through 6 GHz such as automotive infotainment and traffic safety applications. No blocking capacitors are required if DC voltage is not present on the RF ports.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

The PE423422 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance.

Figure 1. Functional Diagram

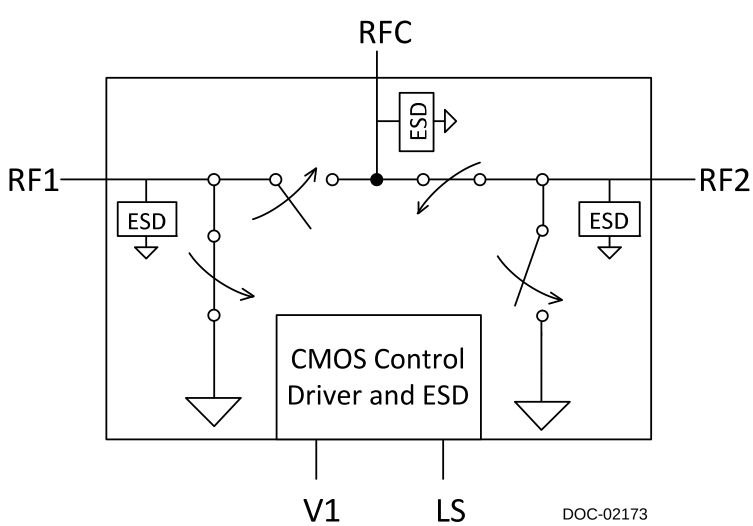


Figure 2. Package Type

12-lead 2x2 mm QFN

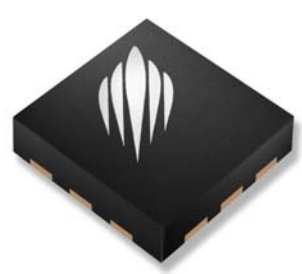


Table 1. Electrical Specifications @ 25°C, V_{DD} = 2.3V to 5.5V ($Z_S = Z_L$ = 50Ω)

Parameter	Path	Condition	Min	Typ	Max	Unit
Operational frequency			100		6000	MHz
Insertion loss	RFC–RFX	100–1000 MHz		0.25	0.35	dB
		1000–2000 MHz		0.30	0.40	dB
		2000–3000 MHz		0.40	0.50	dB
		3000–4000 MHz		0.50	0.70	dB
		4000–5000 MHz		0.65	0.90[1]	dB
		5000–6000 MHz		0.90	1.25[1]	dB
Isolation	RFX–RFX	100–1000 MHz	39	41		dB
		1000–2000 MHz	32	33		dB
		2000–3000 MHz	26	28		dB
		3000–4000 MHz	22	24		dB
		4000–5000 MHz	18	20		dB
		5000–6000 MHz	15	16		dB
Isolation	RFC–RFX	100–1000 MHz	41	44		dB
		1000–2000 MHz	33	35		dB
		2000–3000 MHz	27	29		dB
		3000–4000 MHz	22	24		dB
		4000–5000 MHz	18	20		dB
		5000–6000 MHz	15	17		dB
Return loss	RFC–RFX	100–1000 MHz		28		dB
		1000–2000 MHz		21		dB
		2000–3000 MHz		20		dB
		3000–4000 MHz		18		dB
		4000–5000 MHz		16[1]		dB
		5000–6000 MHz		13[1]		dB
2nd Harmonic, 2fo	RFC–RFX	+32 dBm output power, 850 / 900 MHz		-99		dBc
		+32 dBm output power, 1800 / 1900 MHz		-101		dBc
3rd Harmonic, 3fo	RFC–RFX	+32 dBm output power, 850 / 900 MHz		-93		dBc
		+32 dBm output power, 1800 / 1900 MHz		-87		dBc
IMD3		Bands I, II, V, VIII +20 dBm CW @ TX freq at RFC, -15 dBm CW @ 2Tx-Rx at RFC, 50Ω		-122		dBm
Input IP2	RFC–RFX	100–6000 MHz		115		dBm
Input IP3	RFC–RFX	100–6000 MHz		73.5		dBm
Input 0.1 dB compression point[2]	RFC–RFX	100–6000 MHz		34		dBm
Switching time		50% CTRL to 90% or 10% RF		2	4	µs

Notes: 1. High frequency performance can be improved by external matching
2. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 4* for the RF input power $P_{MAX,CW}$ (50Ω)

Table 1A. Electrical Specifications @ -40°C to +105°C, V_{DD} = 2.3V to 5.5V (Z_S = Z_L = 50Ω)

Parameter	Path	Condition	Min	Typ	Max	Unit
Operational frequency			100		6000	MHz
Insertion loss	RFC–RFX	100–1000 MHz		0.25	0.55	dB
		1000–2000 MHz		0.30	0.65	dB
		2000–3000 MHz		0.40	0.75	dB
		3000–4000 MHz		0.50	0.85	dB
		4000–5000 MHz		0.65	1.05[1]	dB
		5000–6000 MHz		0.90	1.45[1]	dB
Isolation	RFX–RFX	100–1000 MHz	38	41		dB
		1000–2000 MHz	31	33		dB
		2000–3000 MHz	25	28		dB
		3000–4000 MHz	21	24		dB
		4000–5000 MHz	17	20		dB
		5000–6000 MHz	14	16		dB
Isolation	RFC–RFX	100–1000 MHz	40	44		dB
		1000–2000 MHz	32	35		dB
		2000–3000 MHz	26	29		dB
		3000–4000 MHz	21	24		dB
		4000–5000 MHz	17	20		dB
		5000–6000 MHz	14	17		dB
Return loss	RFC–RFX	100–1000 MHz		28		dB
		1000–2000 MHz		21		dB
		2000–3000 MHz		20		dB
		3000–4000 MHz		18		dB
		4000–5000 MHz		16[1]		dB
		5000–6000 MHz		13[1]		dB
2nd Harmonic, 2fo	RFC–RFX	+32 dBm output power, 850 / 900 MHz		-99		dBc
		+32 dBm output power, 1800 / 1900 MHz		-101		dBc
3rd Harmonic, 3fo	RFC–RFX	+32 dBm output power, 850 / 900 MHz		-93		dBc
		+32 dBm output power, 1800 / 1900 MHz		-87		dBc
IMD3		Bands I, II, V, VIII +20 dBm CW @ TX freq at RFC, -15 dBm CW @ 2Tx-Rx at RFC, 50Ω		-122		dBm
Input IP2	RFC–RFX	100–6000 MHz		115		dBm
Input IP3	RFC–RFX	100–6000 MHz		73.5		dBm
Input 0.1 dB compression point[2]	RFC–RFX	100–6000 MHz		34		dBm
Switching time		50% CTRL to 90% or 10% RF		2	5	µs

Notes: 1. High frequency performance can be improved by external matching
2. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 4* for the RF input power $P_{MAX,CW}$ (50Ω)

Figure 3. Pin Configuration (Top View)

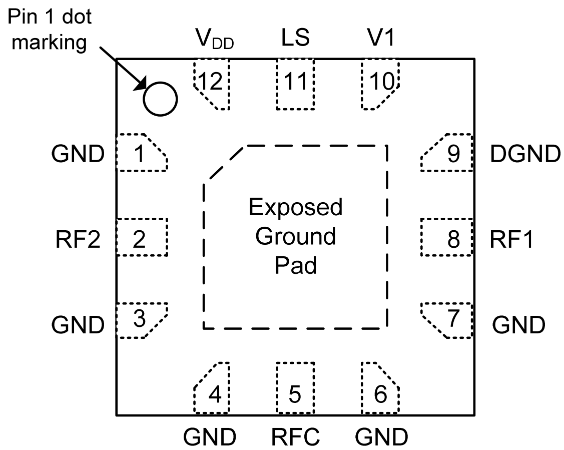


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3, 4, 6, 7	GND	Ground
2	RF2[1]	RF port 2
5	RFC[1]	RF common
8	RF1[1]	RF port 1
9	DGND	Digital ground
10	V1	Digital control logic input 1
11	LS	Logic Select
12	V_{DD}	Supply voltage
Pad	GND	Exposed pad: Ground for proper operation

Note 1: RF pins 2, 5 and 8 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	3.3	5.5	V
Supply current	I_{DD}		120	200	µA
Digital input high (V1, LS)	V_{IH}	1.2	1.5	3.3	V
Digital input low (V1,LS)	V_{IL}	0	0	0.5	V
RF input power, CW (RFC-RFX)[1]	$P_{MAX,CW}$			*Fig. 4*	dBm
Operating temperature range	T_{OP}	-40	+25	+105	°C

Note 1: 100% duty cycle, all bands, 50Ω

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (V1, LS)	V_I	-0.3	3.3	V
RF input power, Max	$P_{MAX,ABS}$		*Fig. 4*	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM, all pins[1]	$V_{ESD,HBM}$		1000	V
ESD voltage MM, all pins[2]	$V_{ESD,MM}$		200	V
ESD voltage CDM, all pins[3]	$V_{ESD,CDM}$		1000	V

Notes: 1. Human Body Model (MIL_STD-883 Method 3015)
2. Machine Model (JEDEC JESD22-A115)
3. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

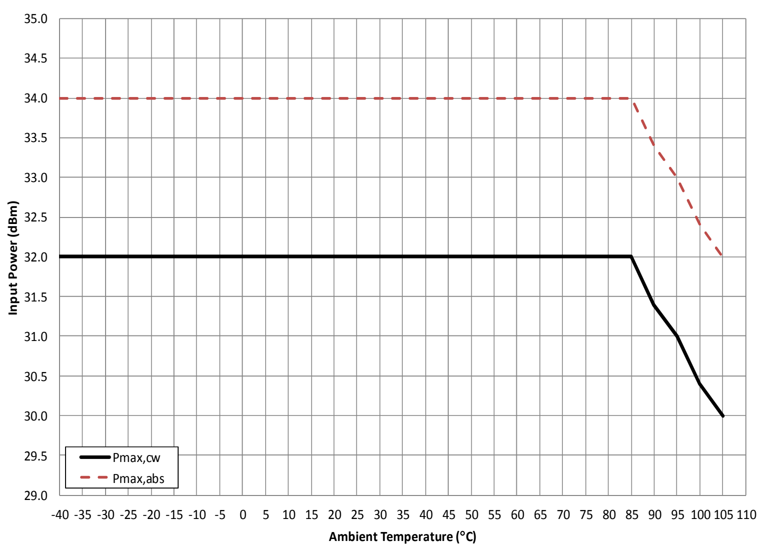
Table 5. Truth Table

Path	V1	LS
RFC–RF2	1	1
RFC–RF1	0	1
RFC–RF1	1	0
RFC–RF2	0	0

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE423422 in the 12-lead 2x2 mm QFN package is MSL1.

Figure 4. Power De-rating Curve for 100–6000 MHz vs Ambient Temperature (50Ω)



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 5. Insertion Loss RFX

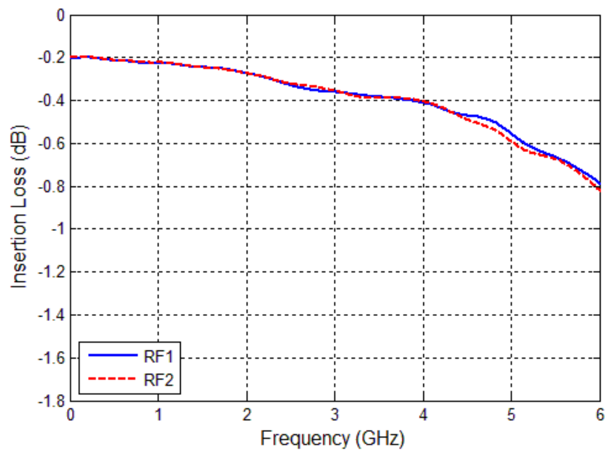


Figure 6. Insertion Loss vs Temp (RFC–RF1)

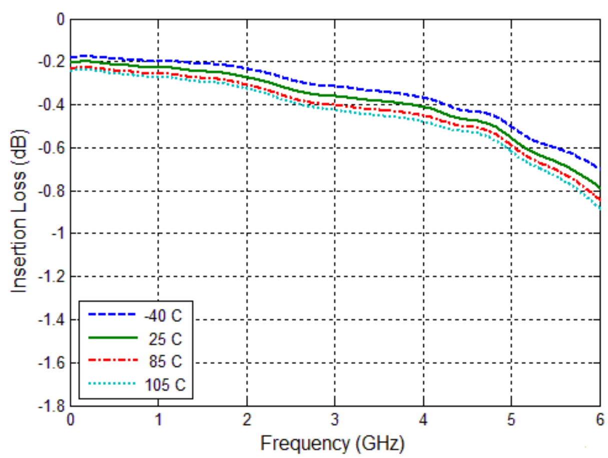


Figure 7. Insertion Loss vs V_{DD} (RFC–RF1)

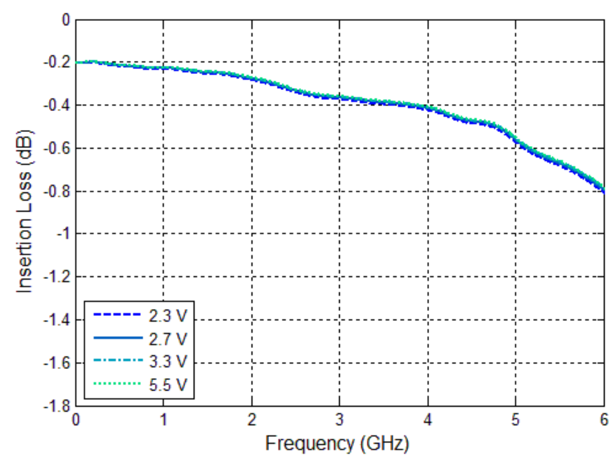


Figure 8. Insertion Loss vs Temp (RFC–RF2)

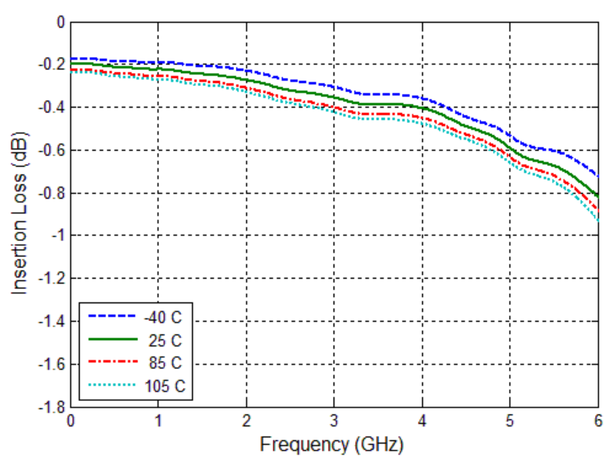
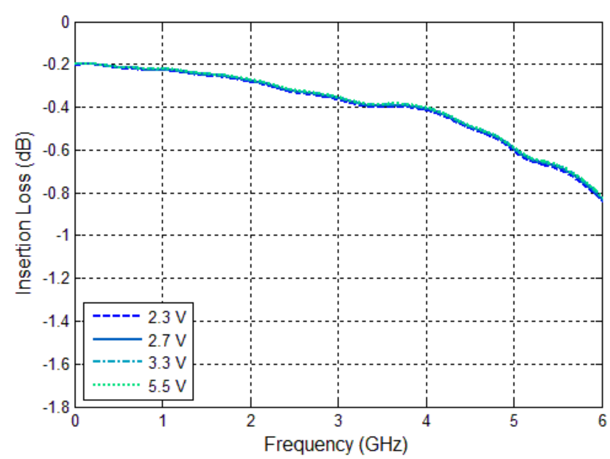


Figure 9. Insertion Loss vs V_{DD} (RFC–RF2)



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 10. RFC Port Return Loss vs Temp (RF1 Active)

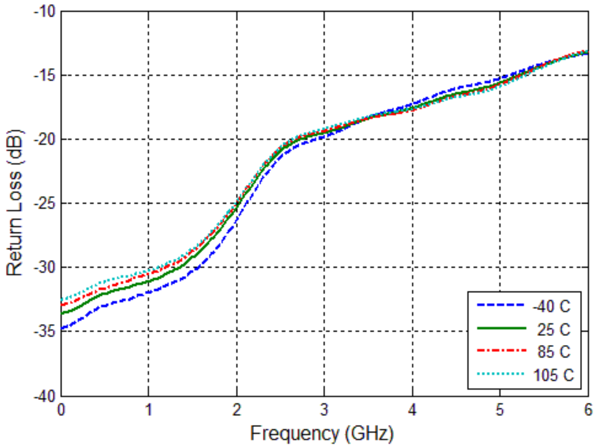


Figure 11. RFC Port Return Loss vs V_{DD} (RF1 Active)

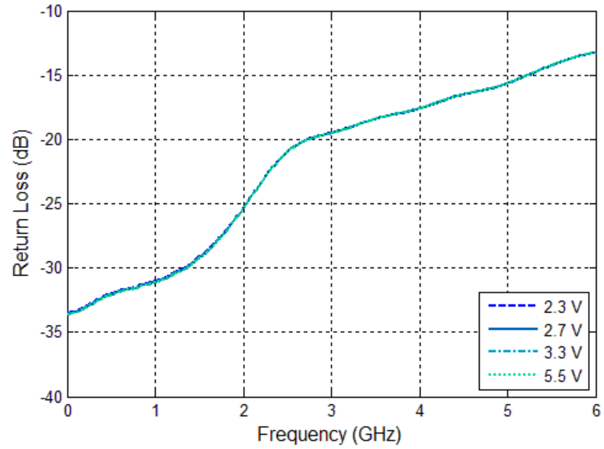


Figure 12. RFC Port Return Loss vs Temp (RF2 Active)

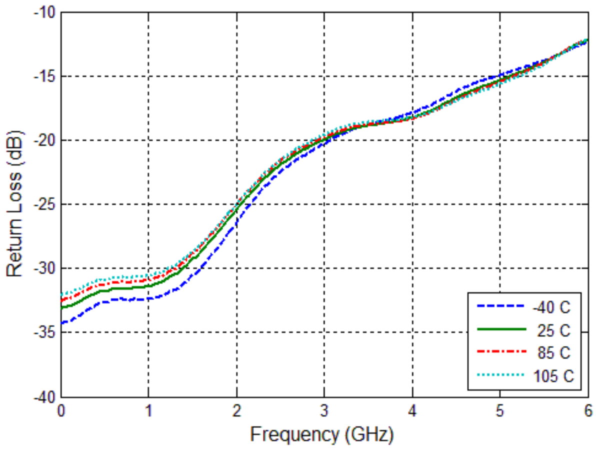
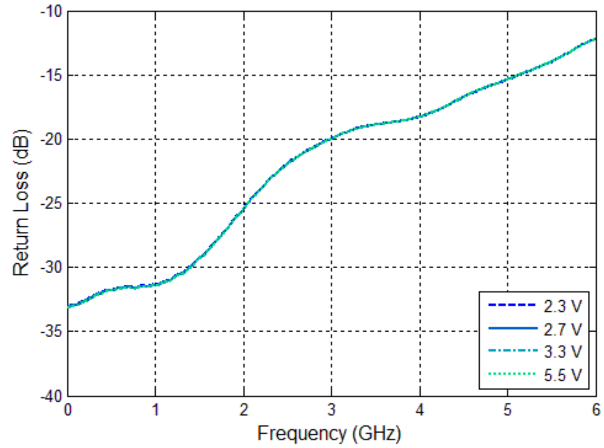


Figure 13. RFC Port Return Loss vs V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 14. Active Port Return Loss vs Temp (RF1 Active)

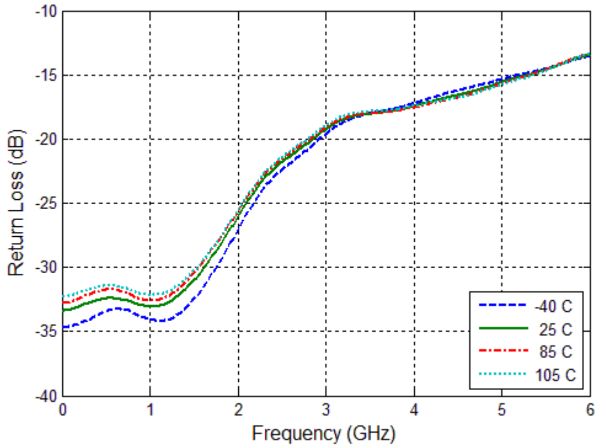


Figure 15. Active Port Return Loss vs V_{DD} (RF1 Active)

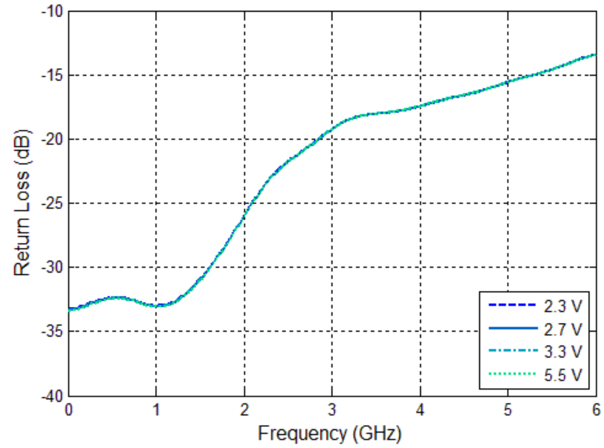


Figure 16. Active Port Return Loss vs Temp (RF2 Active)

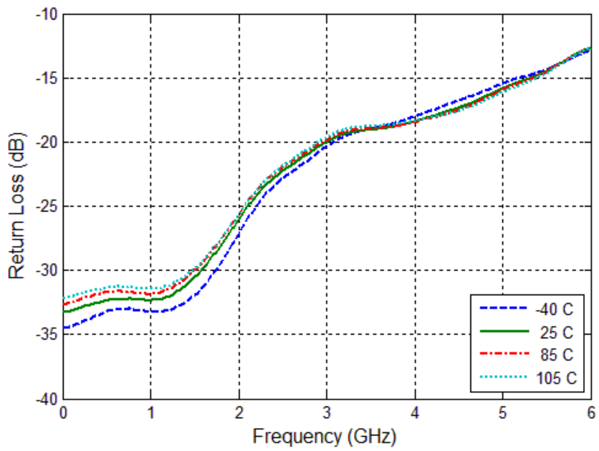
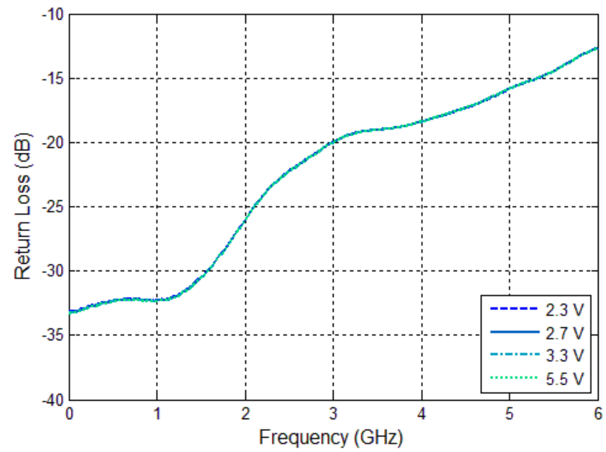


Figure 17. Active Port Return Loss vs V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 18. Isolation vs Temp (RF1–RF2, RF1 Active)

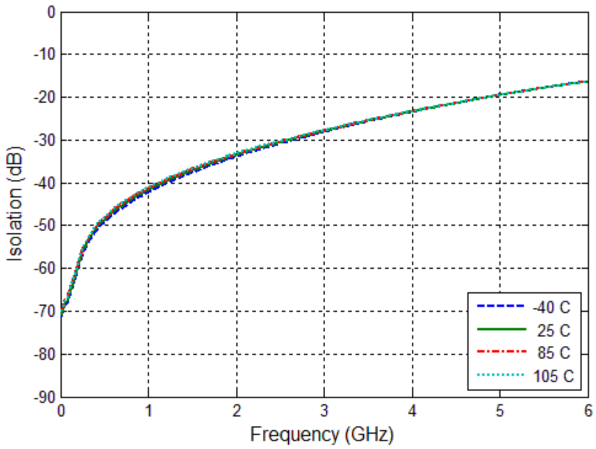


Figure 19. Isolation vs V_{DD} (RF1–RF2, RF1 Active)

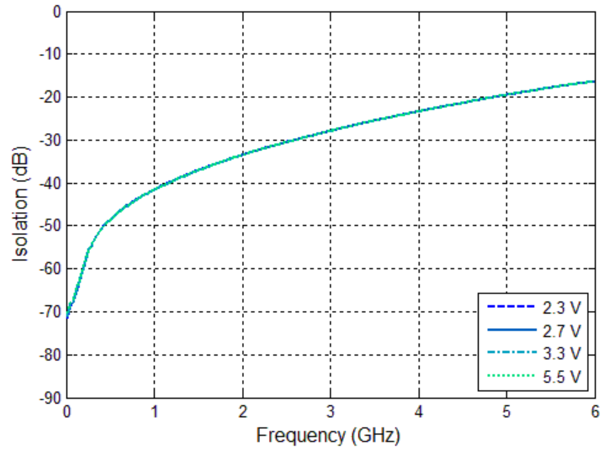


Figure 20. Isolation vs Temp (RFC–RF2, RF1 Active)

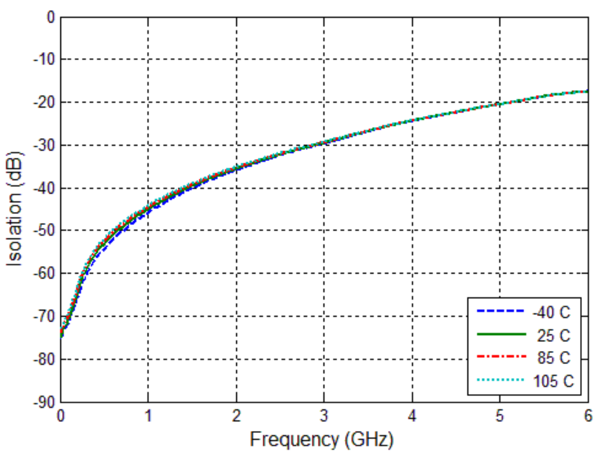
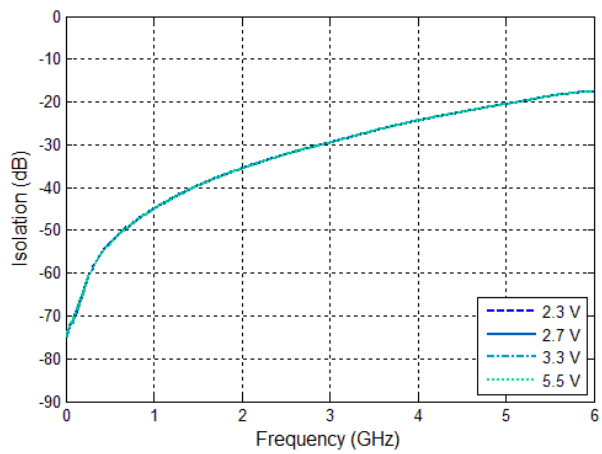


Figure 21. Isolation vs V_{DD} (RFC–RF2, RF1 Active)

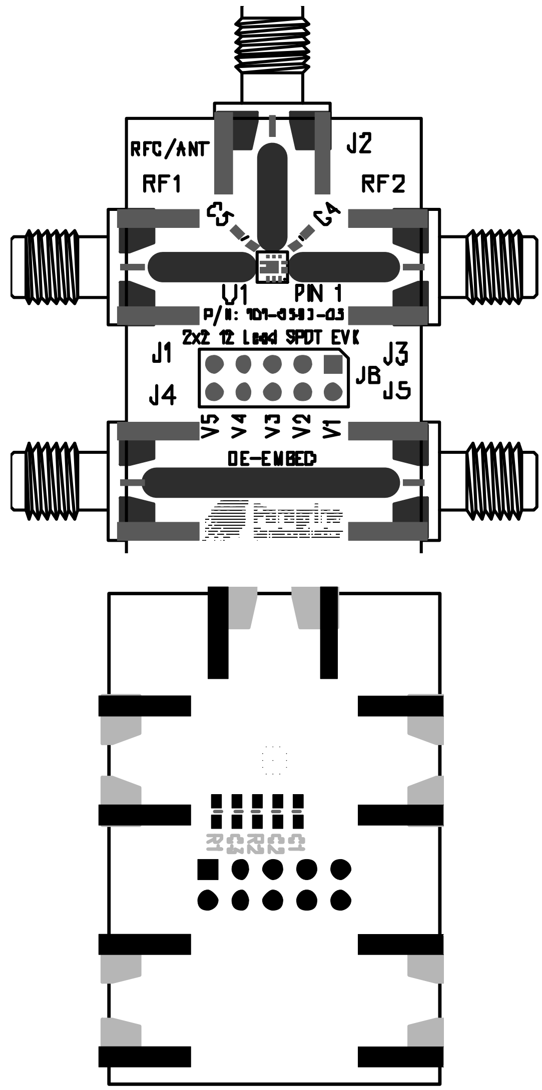


Evaluation Board

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE423422. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J2. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J1 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. J8 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top and bottom RF layers are Rogers RO4350 material with a 10 mil RF core. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 22 mils, trace gaps of 7 mils, and metal thickness of 2.1 mils.

Figure 22. Evaluation Board Layout



PRT-29005

Figure 23. Evaluation Board Schematic

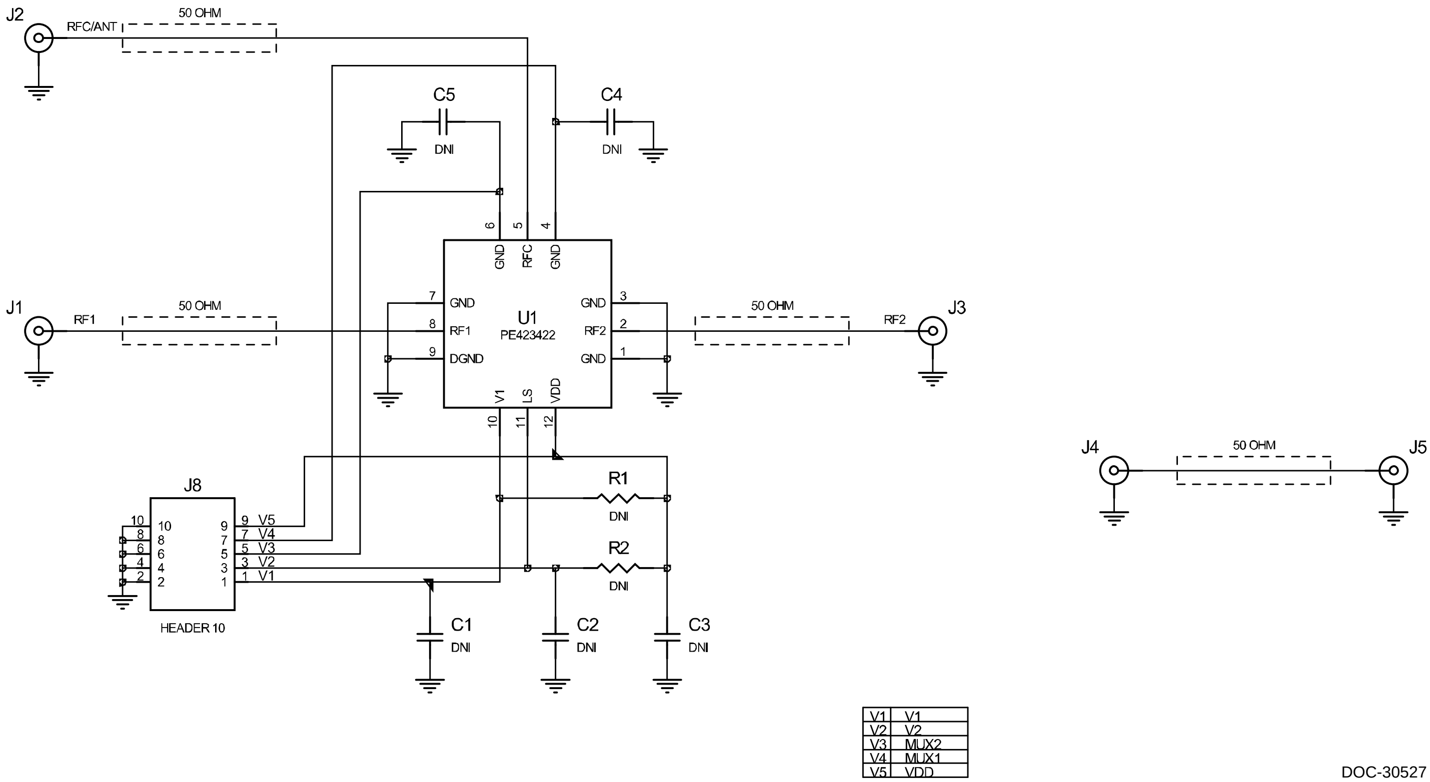


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Figure 24. Package Drawing
12-lead 2x2 mm QFN

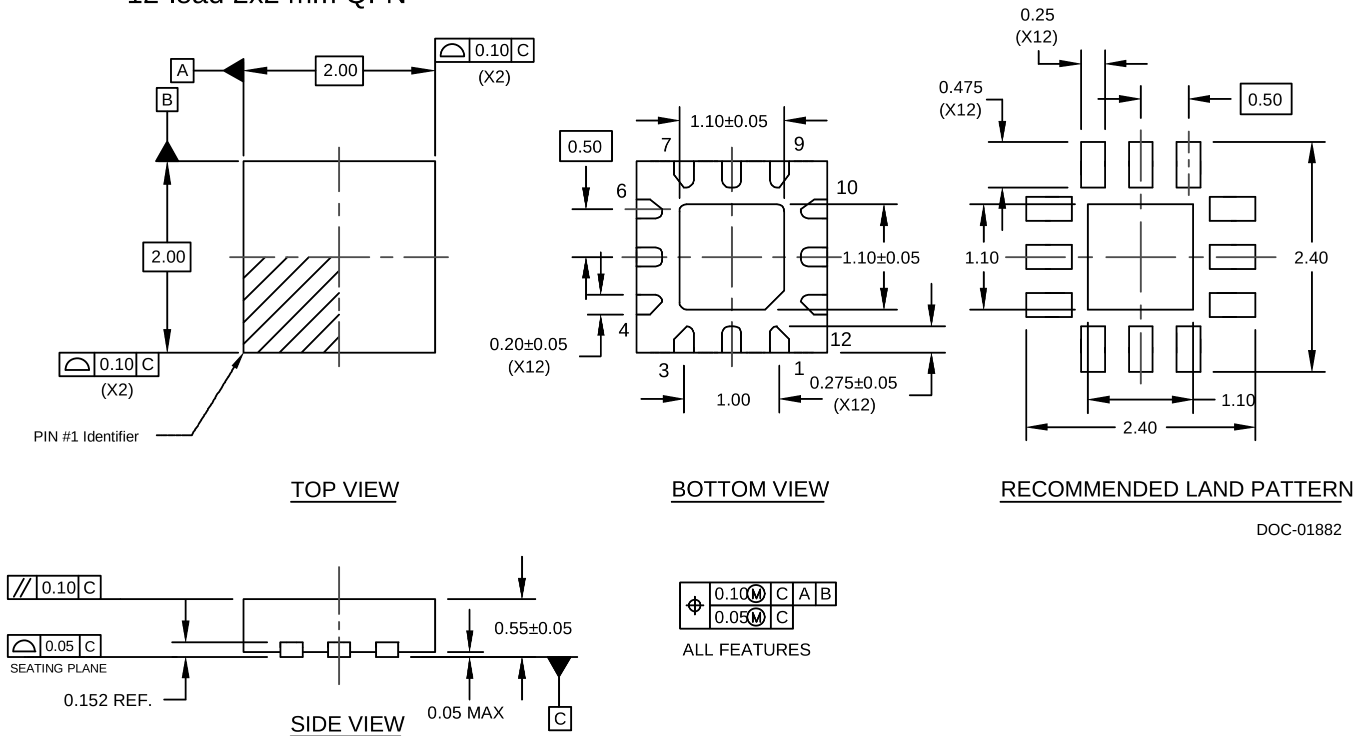
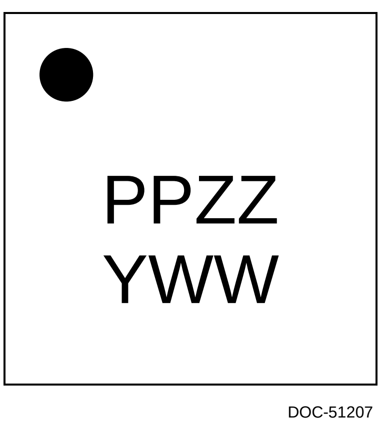


Figure 25. Top Marking Specifications



Marking Spec Symbol	Package Marking	Definition
PP	DU	Part number marking for PE423422
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week