Product Specification

PE42422

UltraCMOS® SPDT RF Switch 5–6000 MHz

Product Description

The PE42422 is a HaRP™ technology-enhanced SPDT RF switch designed to cover a broad range of applications from 5–6000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface and requires no external components.

Peregrine's HaRP technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS® process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Features

- Symmetric SPDT reflective switch
- Low insertion loss
  - 0.23 dB typical @ 100 MHz
  - 0.25 dB typical @ 1000 MHz
  - 0.40 dB typical @ 3000 MHz
  - 0.65 dB typical @ 5000 MHz
  - 0.90 dB typical @ 6000 MHz
- Wide supply range of 2.3–5.5V
- Excellent linearity
  - IIP2 of 105 dBm @ 17 MHz
  - IIP3 of 81 dBm @ 17 MHz
- High ESD tolerance
  - 4 kV HBM on RF pins to GND
  - 1 kV on all other pins
- Logic Select (LS) pin provides maximum flexibility of control logic
- 12-lead 2 × 2 mm QFN package

Figure 1. Functional Diagram

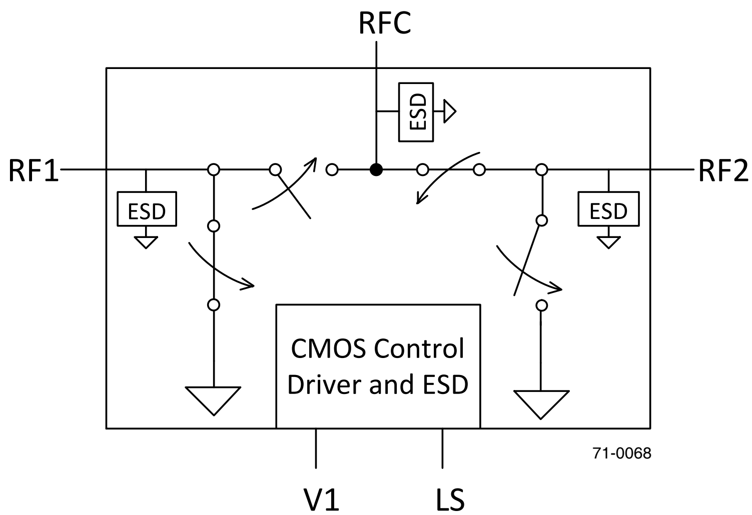


Figure 2. Package Type

12-lead 2 x 2 x 0.55 mm QFN

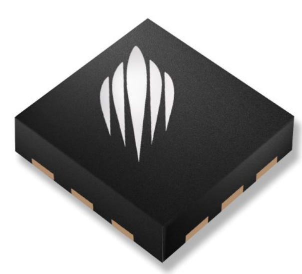


Table 1. Electrical Specifications @ +25 °C[1], V_{DD} = 2.3–5.5V (Z_S = Z_L = 50Ω), unless otherwise specified

Parameter	Path	Condition	Min	Typ	Max	Unit
Operational frequency			5		6000	MHz
Insertion loss[2]	RFX–RFC	5–100 MHz		0.23		dB
		100–1000 MHz		0.25	0.35	dB
		1000–2000 MHz		0.30	0.40	dB
		2000–3000 MHz		0.40	0.50	dB
		3000–4000 MHz		0.50	0.70	dB
		4000–5000 MHz		0.65	0.90[2]	dB
		5000–6000 MHz		0.90	1.25[2]	dB
Isolation	RFX–RFC	5–100 MHz		68		dB
		100–1000 MHz	42	44		dB
		1000–2000 MHz	33	35		dB
		2000–3000 MHz	27	29		dB
		3000–4000 MHz	22	24		dB
		4000–5000 MHz	18	20		dB
		5000–6000 MHz	15	17		dB
Isolation	RFX–RFX	5–100 MHz		61		dB
		100–1000 MHz	40	41		dB
		1000–2000 MHz	32	33		dB
		2000–3000 MHz	26	28		dB
		3000–4000 MHz	22	24		dB
		4000–5000 MHz	18	20		dB
		5000–6000 MHz	15	16		dB
Return loss[2]	RFX–RFC	5–100 MHz		33		dB
		100-1000 MHz		28		dB
		1000–2000 MHz		21		dB
		2000–3000 MHz		20		dB
		3000–4000 MHz		18		dB
		4000–5000 MHz		16[2]		dB
		5000–6000 MHz		13[2]		dB
2nd harmonic	RFX–RFC	+18 dBm input power, 17–204 MHz		–92		dBc
		+32 dBm output power, 850 / 900 MHz		–99		dBc
		+32 dBm output power, 1800 / 1900 MHz		–101		dBc
3rd harmonic	RFX–RFC	+18 dBm input power, 17–204 MHz		–125		dBc
		+32 dBm output power, 850 / 900 MHz		–93		dBc
		+32 dBm output power, 1800 / 1900 MHz		–87		dBc
IMD3	RF–RFC	Bands I, II, V, VIII +17 dBm CW @ TX freq at RFC, –15 dBm CW @ 2Tx-Rx at RFC, 50Ω		–115		dBm

Table 1. Electrical Specifications @ +25 °C[1], V_{DD} = 2.3–5.5V ($Z_S = Z_L = 50\Omega$), unless otherwise specified

Parameter	Path	Condition	Min	Typ	Max	Unit
IIP2	RFX	5 MHz 17 MHz 100–6000 MHz		96 105 115		dBm dBm dBm
IIP3	RFX	5 MHz 17 MHz 100–6000 MHz		75 81 75		dBm dBm dBm
Input 0.1dB compression point[3]	RFX or RFC	5–100 MHz 100–6000 MHz		33 34		dBm dBm
Switching time		50% CTRL to (10%–90%) or (90%–10%) RF		2	4	µs

Notes: 1. Typical performance over temperature and V_{DD} shown in *Figure 5* through *Figure 21.*
2. High frequency performance can be improved by external matching (see *Figure 22* through *Figure 27 and Figure 30*).
3. The input P0.1dB compression point is a linearity figure of merit. Refer to *Table 4* for the operating RF input power.

Figure 3. Pin Configuration (Top View)

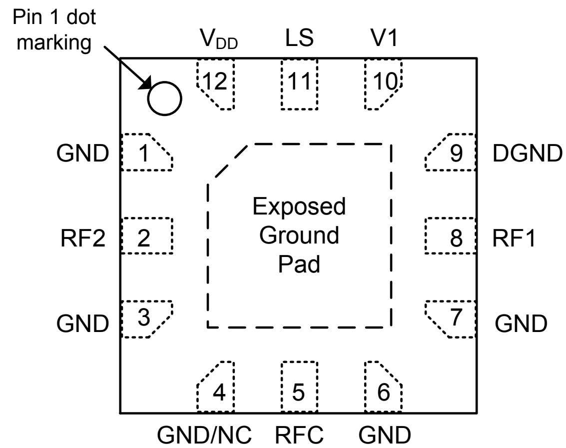


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	RF2[1]	RF port 2
3	GND	Ground
4	GND/NC[2]	Ground or no connect
5	RFC[1]	RF common
6	GND	Ground
7	GND	Ground
8	RF1[1]	RF port 1
9	DGND	Digital Ground
10	V1	Switch control input, CMOS logic level
11	LS	Logic Select, CMOS logic level
12	V_{DD}	Supply
Pad	GND	Exposed pad: ground for proper operation

Notes: 1. RF pins 2, 5 and 8 must be at 0 VDC. The RF pins do not required DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pin 4 can be grounded or left unconnected externally.

Table 3. Truth Table

Path	V1	LS
RFC–RF2	1	1
RFC–RF1	0	1
RFC–RF1	1	0
RFC–RF2	0	0

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Supply voltage	2.3	3.3	5.5	V
I_{DD} Power supply current		120	200	µA
RFX–RFC input power			*Fig. 4*	dBm
Control voltage high	1.2	1.5	3.3	V
Control voltage low	0	0	0.5	V
Operating temperature range	–40	+25	+85	°C

Table 5. Absolute Maximum Ratings

Parameter/Condition	Min	Max	Unit
RF input power, 50Ω[1]			
5–100 MHz		33	dBm
100–6000 MHz		34	dBm
ESD voltage HBM[2]			
RF pins to GND		4000	V
All other pins		1000	V
ESD voltage MM, all pins[3]		200	V
T_{ST} Storage temperature	–65	+150	°C

Notes: 1. V_{DD} within operating range specified in *Table 4.*
2. Human Body Model (MIL_STD 883 Method 3015.7).
3. Machine Model (JEDEC JESD22-A115-A).

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the *Operating Ranges* table.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

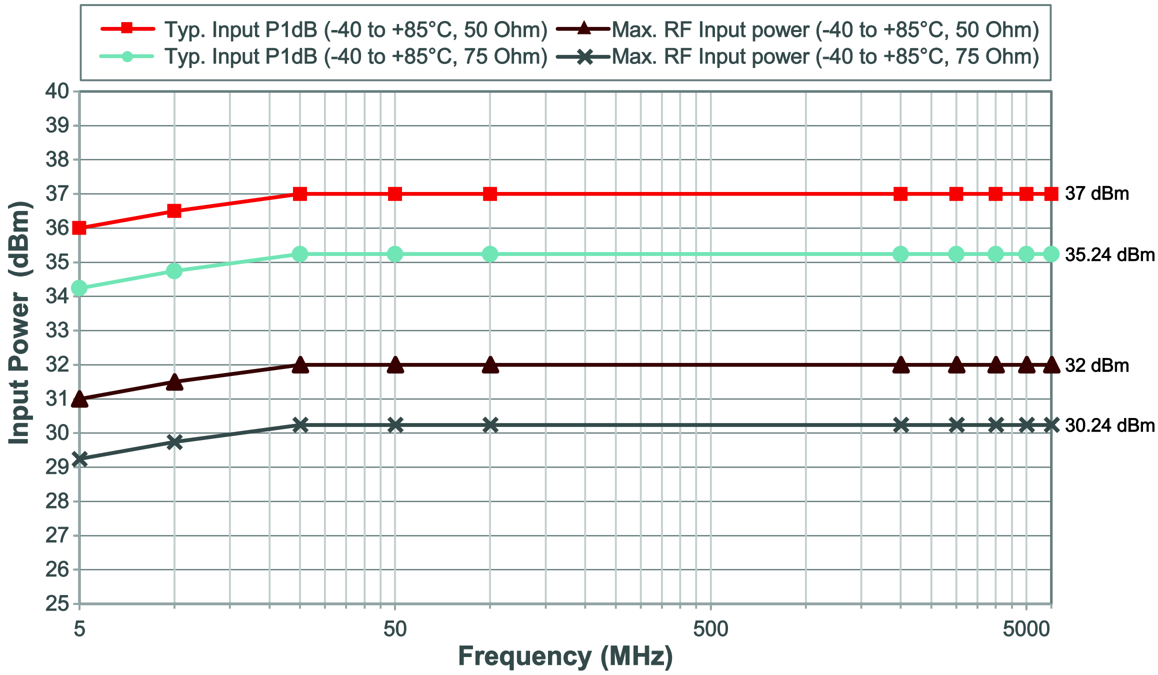
Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42422 in the 12-lead 2 × 2 × 0.55 mm QFN package is MSL1.

Figure 4. Power De-rating Curve for 5–6000 MHz



Typical Performance Data @ +25 °C and V_{DD} = 3.3V, unless otherwise specified

Figure 5. Insertion Loss RFX*

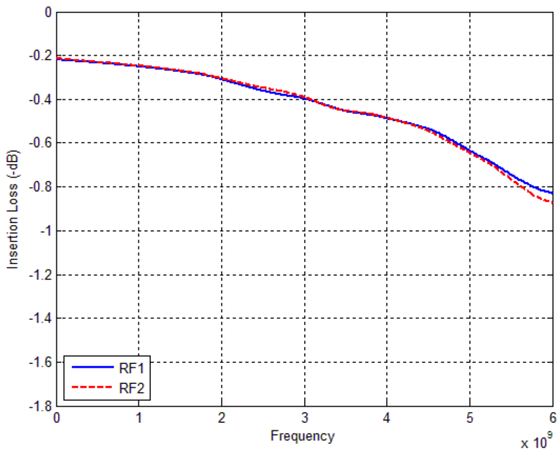


Figure 6. Insertion Loss vs Temp (RF1–RFC)*

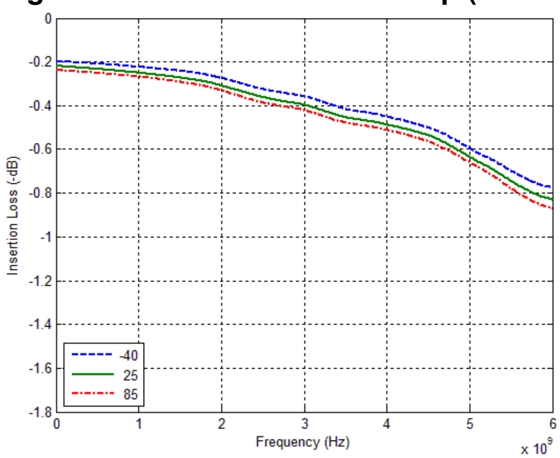


Figure 8. Insertion Loss vs V_{DD} (RF1–RFC)*

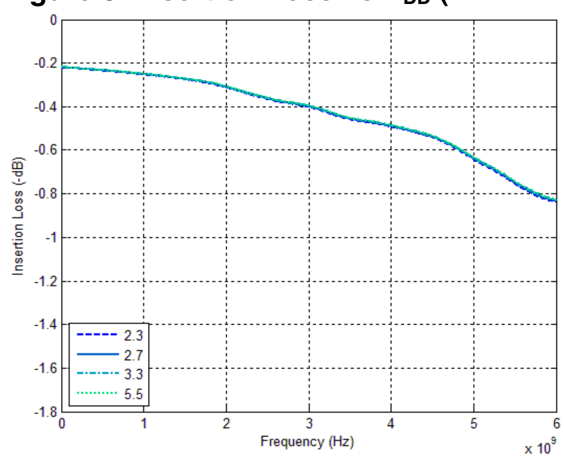


Figure 7. Insertion Loss vs Temp (RF2–RFC)*

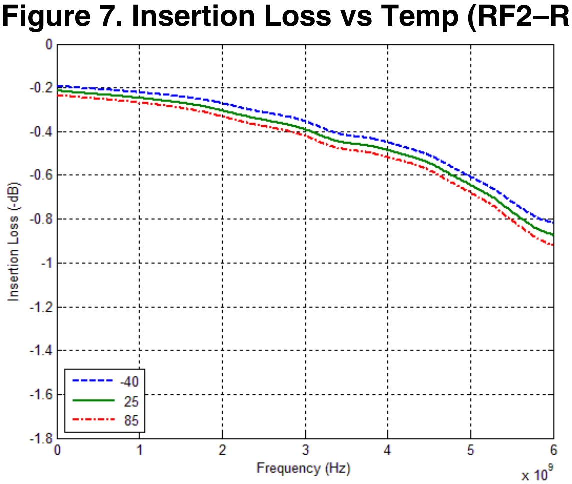
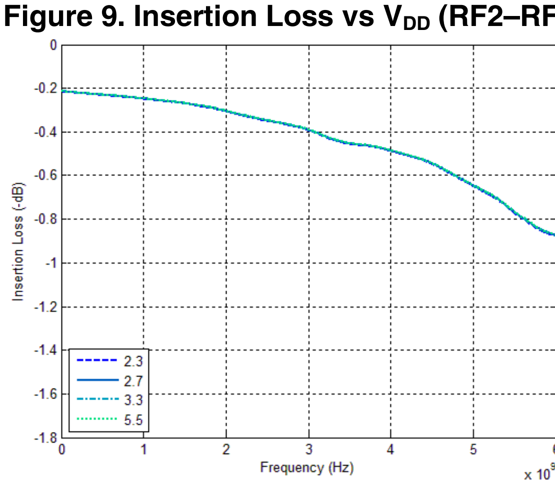


Figure 9. Insertion Loss vs V_{DD} (RF2–RFC)*



Note: * High frequency performance can be improved by external matching (see *Figure 22* through *Figure 27* and *Figure 30*).

Typical Performance Data @ +25 °C and V_{DD} = 3.3V, unless otherwise specified (cont.)

Figure 10. RFX–RFX Isolation vs Temp

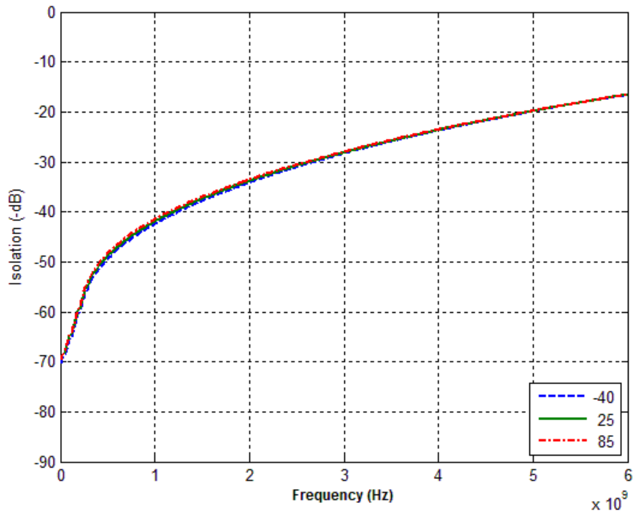


Figure 11. RFC–RFX Isolation vs Temp

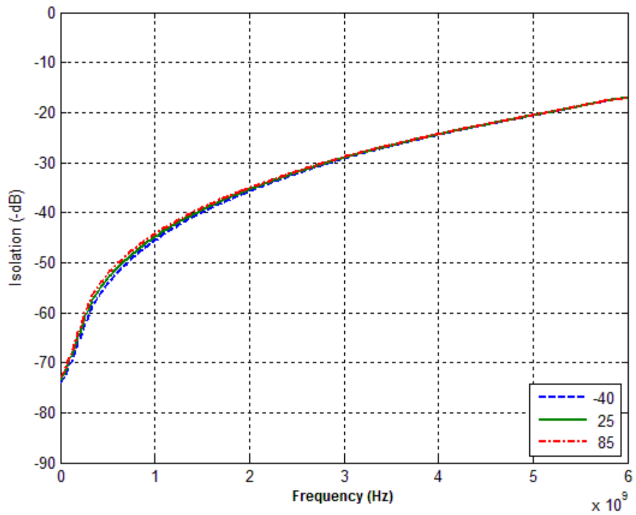


Figure 12. RFX–RFX Isolation vs V_{DD}

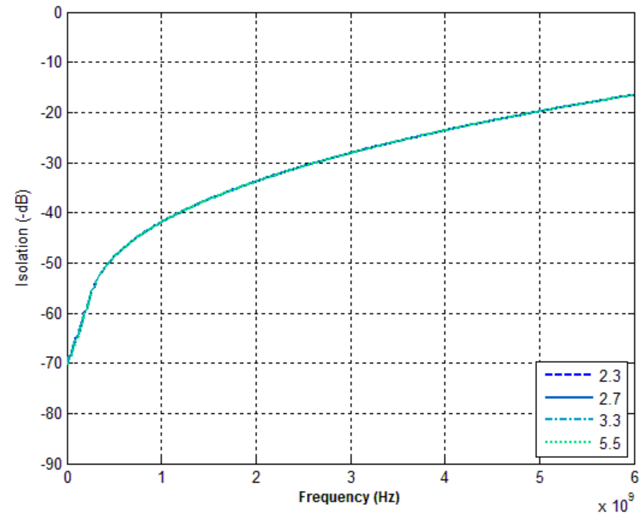
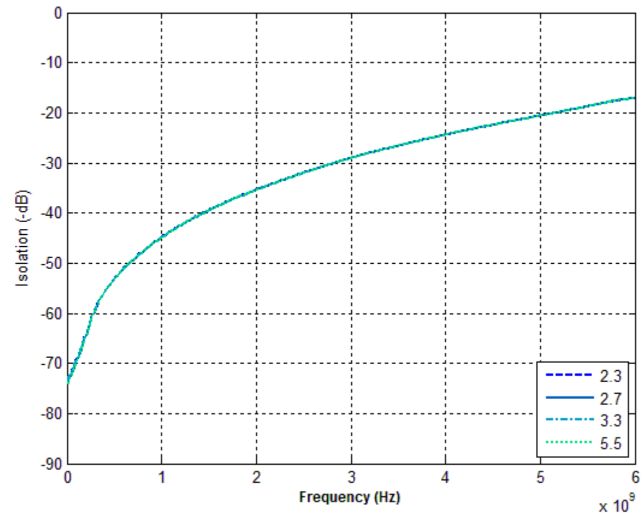


Figure 13. RFC–RFX Isolation vs V_{DD}



Typical Performance Data @ +25 °C and V_{DD} = 3.3V, unless otherwise specified (cont.)

Figure 14. RFC Port Return Loss vs Temp (RF1 Active)*

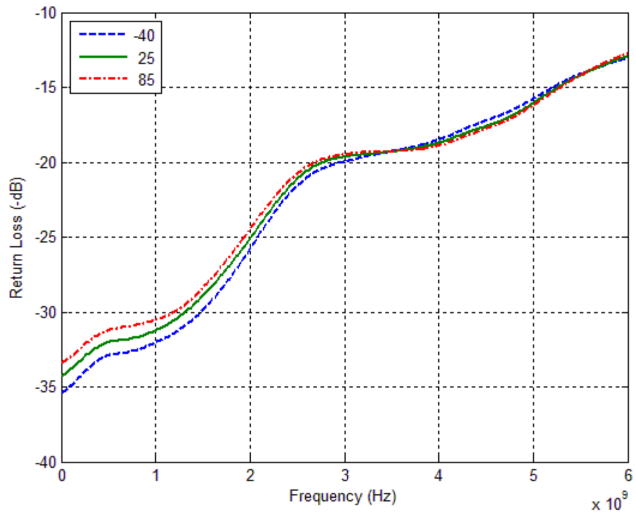


Figure 16. RFC Port Return Loss vs V_{DD} (RF1 Active)*

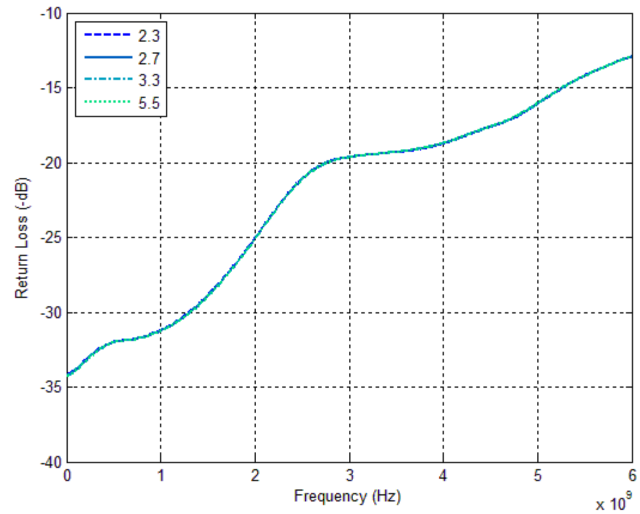


Figure 15. RFC Port Return Loss vs Temp (RF2 Active)*

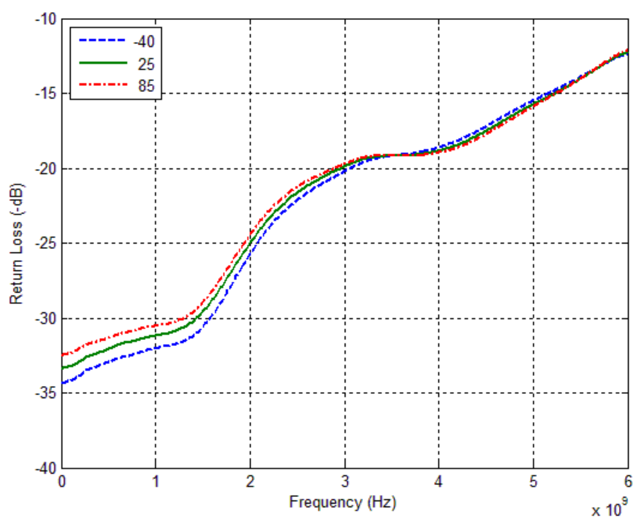
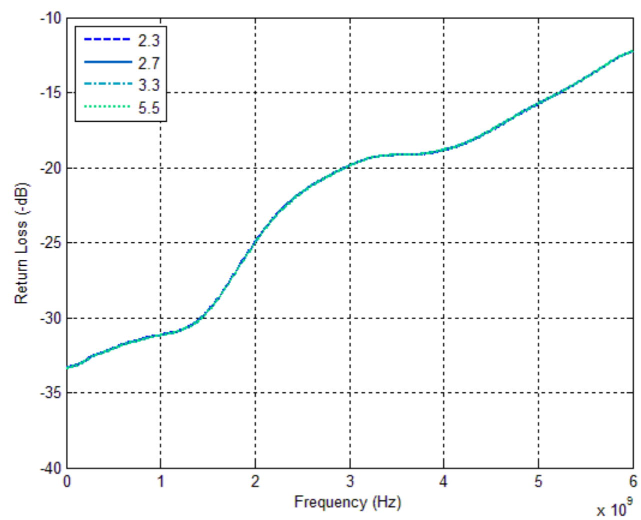


Figure 17. RFC Port Return Loss vs V_{DD} (RF2 Active)*



Note: * High frequency performance can be improved by external matching (see *Figure 22* through *Figure 27* and *Figure 30*).

Typical Performance Data @ +25 °C and V_{DD} = 3.3V, unless otherwise specified (cont.)

Figure 18. Active Port Return Loss vs Temp (RF1 Active)*

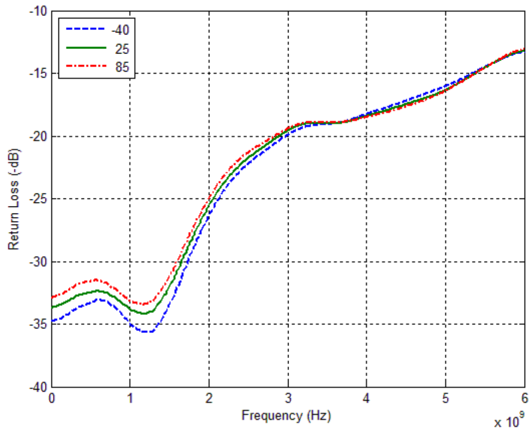


Figure 19. Active Port Return Loss vs Temp (RF2 Active)*

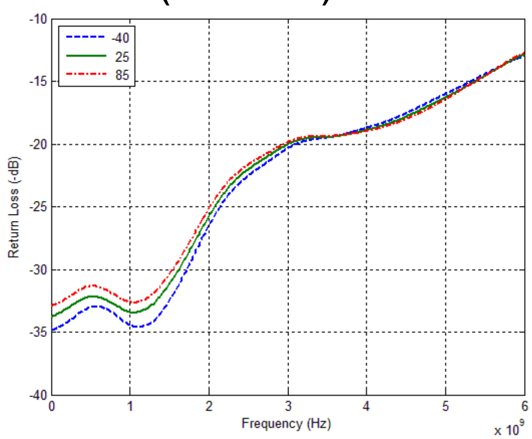


Figure 20. Active Port Return Loss vs V_{DD} (RF1 Active)*

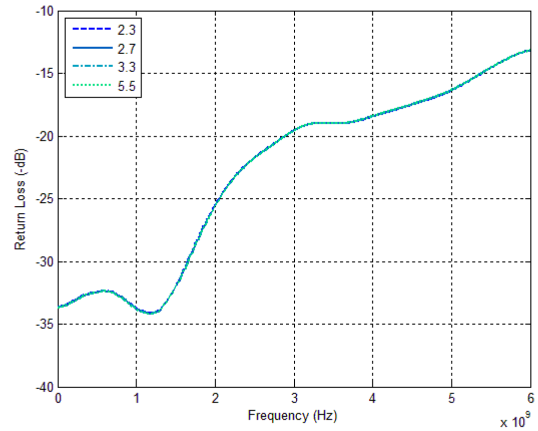
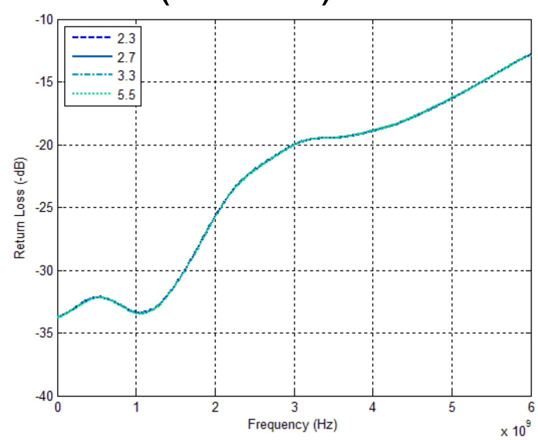


Figure 21. Active Port Return Loss vs V_{DD} (RF2 Active)*



Note: * High frequency performance can be improved by external matching (see *Figure 22* through *Figure 27* and *Figure 30*).

Performance Comparison @ +25 °C and V_{DD} = 3.3V, with or without matching

Figure 22. Insertion Loss RF1*

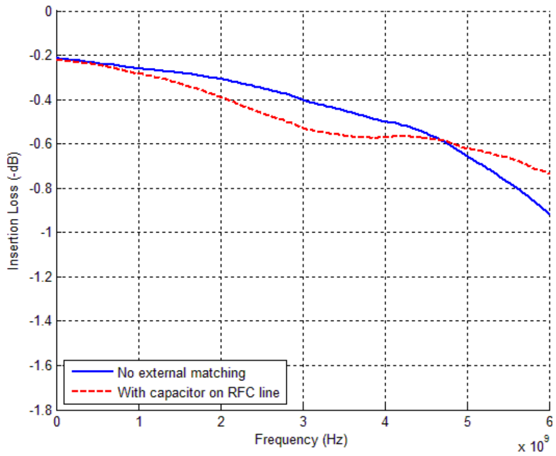


Figure 25. Insertion Loss RF2*

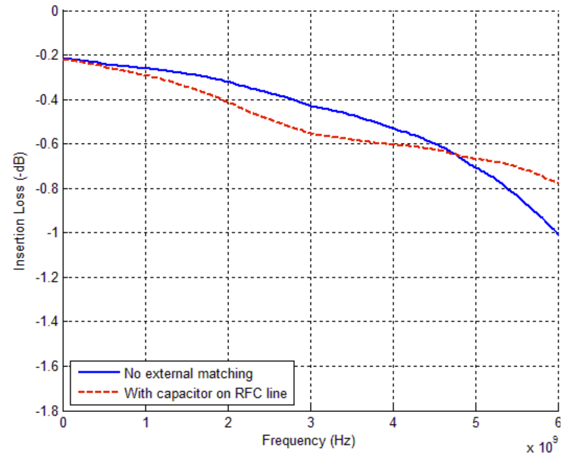


Figure 23. Active Port Return Loss (RF1 Active)*

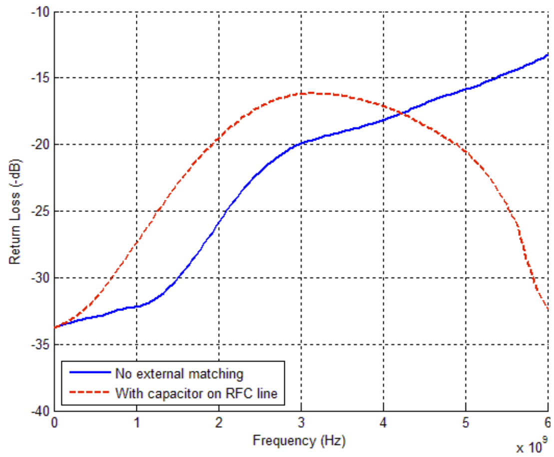


Figure 26. Active Port Return Loss (RF2 Active)*

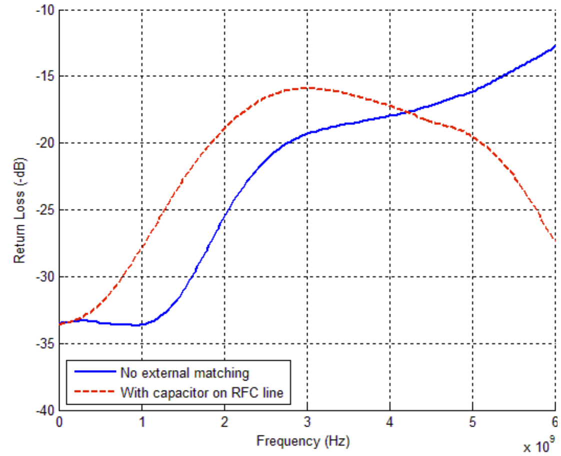


Figure 24. RFC Port Return Loss (RF1 Active)*

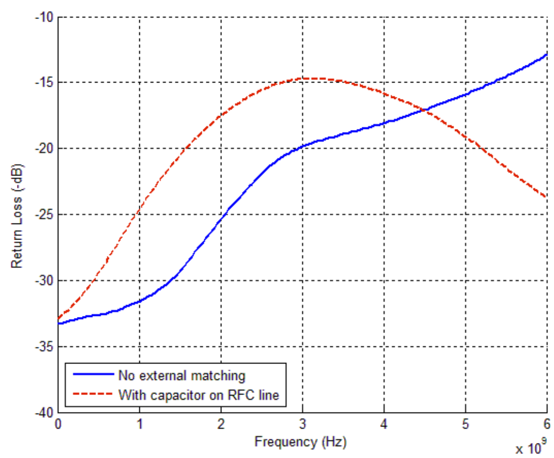
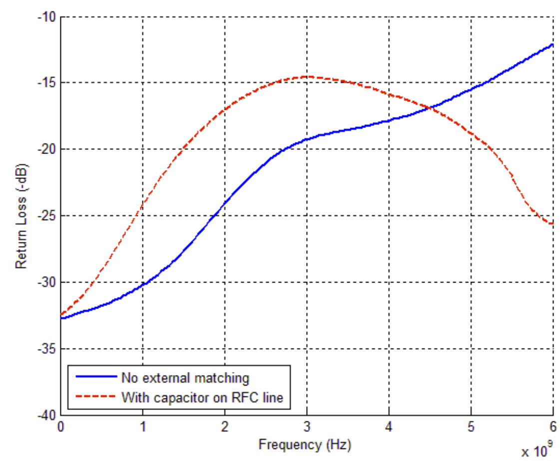


Figure 27. RFC Port Return Loss (RF2 Active)*



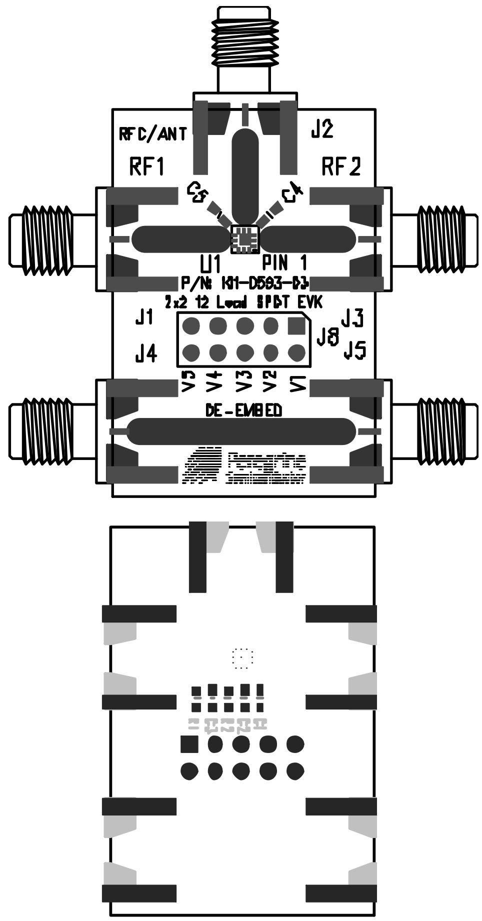
Note: * High frequency performance can be improved by external matching (see *Figure 22* through *Figure 27* and *Figure 30*).

Evaluation Board

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42422. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J2. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J1 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. J8 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top and bottom RF layers are Rogers RO4350 material with a 10 mil RF core. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 22 mils, trace gaps of 7 mils, and metal thickness of 2.1 mils.

Figure 28. Evaluation Board Layout



PRT-29005

Figure 29. Evaluation Board Schematic

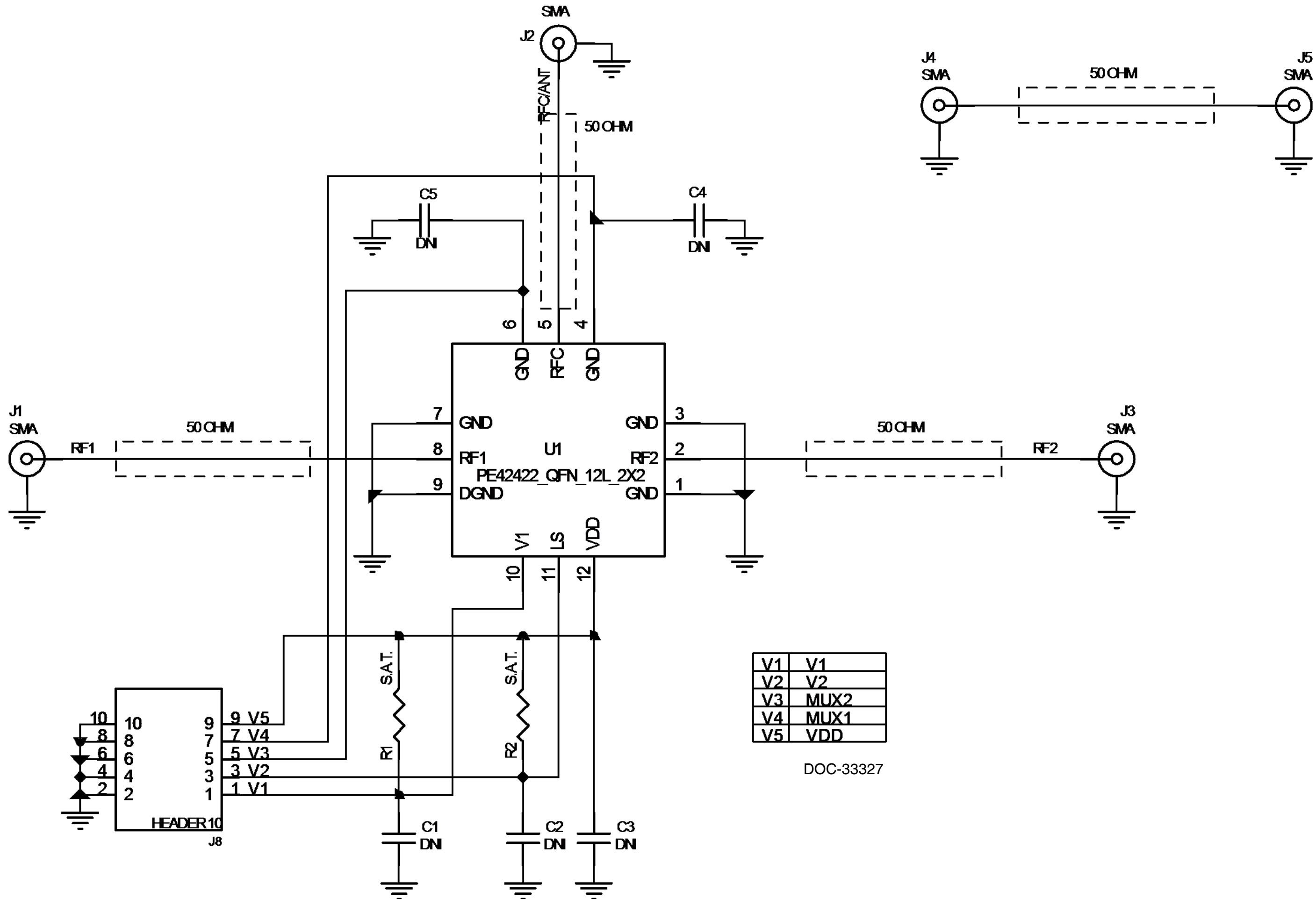
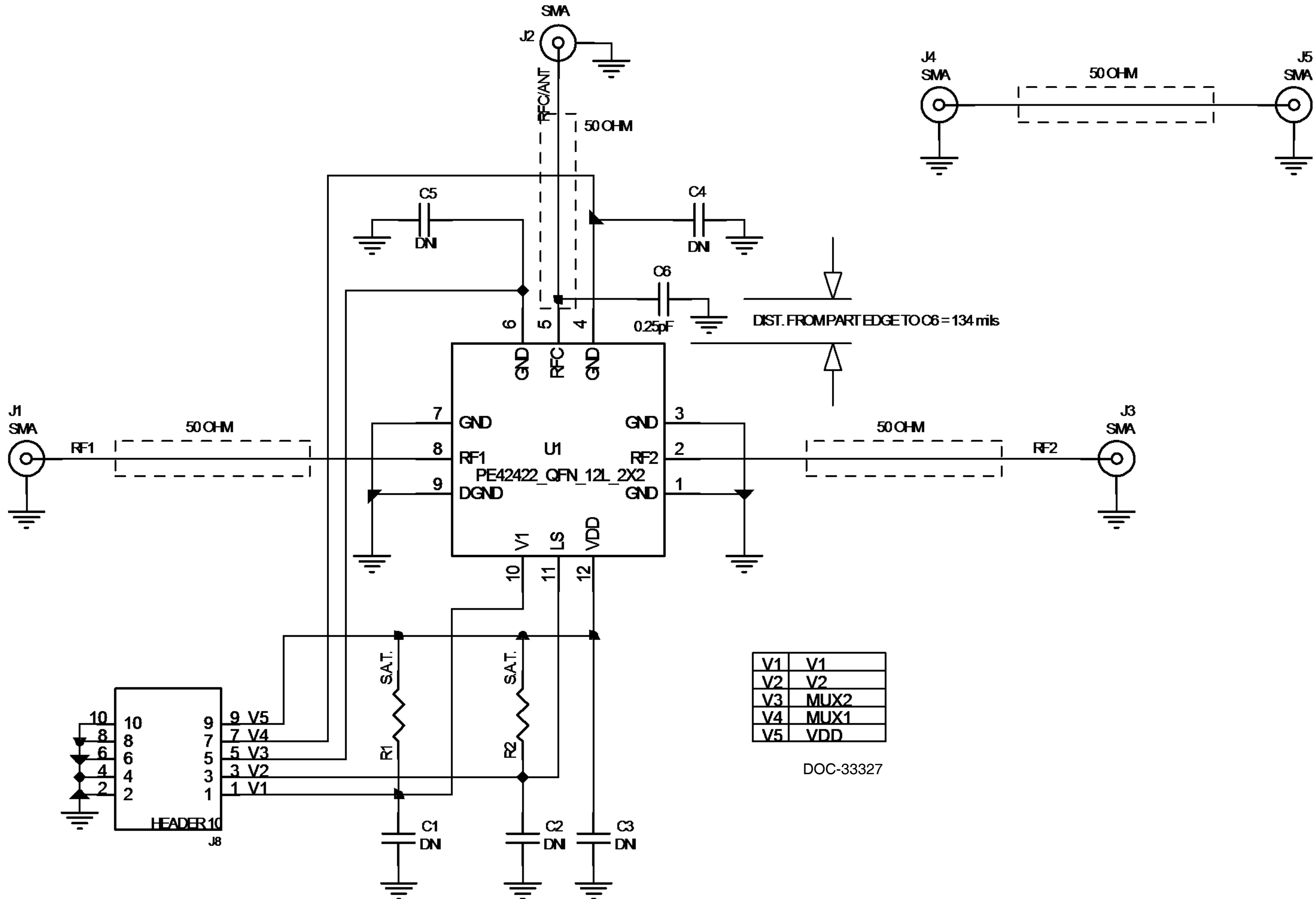


Figure 30. Evaluation Board Schematic with Matching



V1	V1
V2	V2
V3	MUX2
V4	MUX1
V5	VDD

DOC-33327

Figure 31. Package Drawing
12-lead 2 × 2 × 0.55 mm QFN

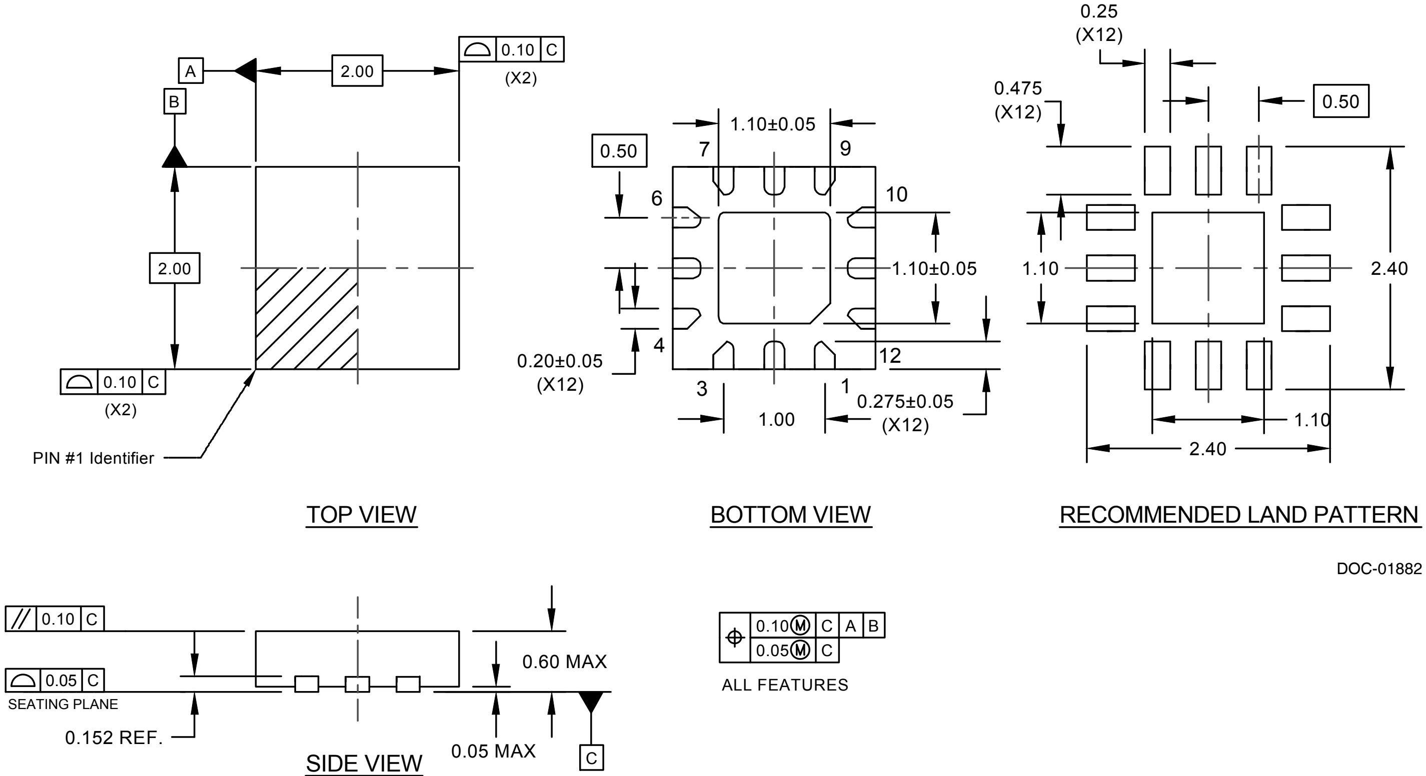
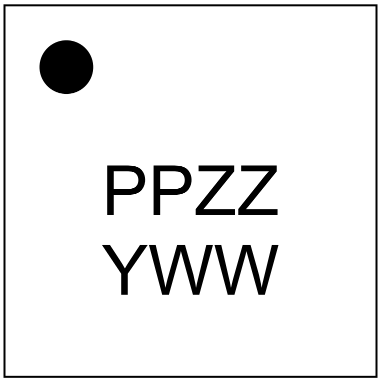
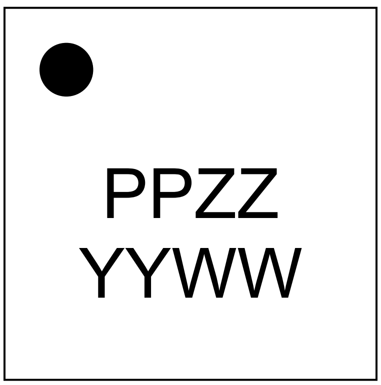


Figure 32. Top Marking Specifications



17-0112

Marking Spec Symbol	Package Marking	Definition
PP	DE	Part number marking for PE42422
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week



DOC-66046

Marking Spec Symbol	Package Marking	Definition
PP	DE	Part number marking for PE42422
ZZ	00-99	Last two digits of lot code
YY	00-99	Last two digits of assembly year (Ex: 15 for 2015)
WW	01-53	Work week

