PE42722

Document Category: Product Specification

UltraCMOS® SPDT RF Switch, 5–1794 MHz

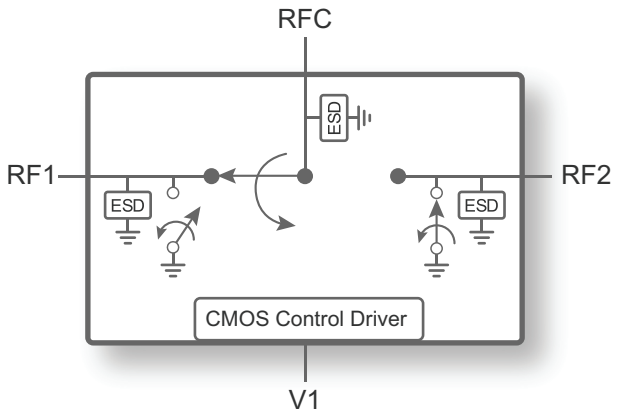
Features

- Supports DOCSIS 3.0/1 requirements
- Exceptional harmonics performance
  - 2fo of –117 dBc @ 170 MHz
  - 3fo of –134 dBc @ 170 MHz
- Best in class linearity across frequency band
- Low insertion loss and high isolation performance
  - Insertion loss of 0.3 dB @ 1218 MHz
  - Isolation of 50 dB @ 204 MHz
- High ESD performance of 1.5 kV HBM
- Packaging – 32-lead 5 × 5 mm QFN

Applications

- Broadband market (DOCSIS 3.0/1)
  - Cable modem
  - Set-top box
- Filter bank switching
- Relay replacement to switch between DOCSIS 3.0 and DOCSIS 3.1 configurations

Figure 1 • *PE42722 Functional Diagram*



Product Description

The PE42722 is a HaRP™ technology-enhanced reflective SPDT RF switch designed for use in cable applications including DOCSIS 3.0/1 cable modem and set-top box. It delivers high linearity and excellent harmonics performance in the 5–1794 MHz band. It also features low insertion loss and high isolation performance that makes the PE42722 ideal for DOCSIS 3.1 applications.

The PE42722 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE42722*

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage, V1	–0.3	3.6	V
Maximum input power[1]		87.5	dBmV
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins[2]		1500	V
ESD voltage MM, all pins[3]		200	V
ESD voltage CDM, all pins[4]		250	V

Notes:
1) 100% duty cycle, all bands, 75Ω.
2) Human body model (MIL-STD 883 Method 3015).
3) Machine model (JEDEC JESD22-A115).
4) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for PE42722. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Condition for PE42722*

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.3	3.3	5.5	V
Supply current, I_{DD}		130	200	µA
Digital input high, V1	1.17		3.6(1)	V
Digital input low, V1	–0.3		0.6	V
RF input power, CW(2)			80	dBmV
RF input power, peak(3)			85	dBmV
Operating temperature range	–40	+25	+85	°C

Notes:
1) Maximum digital input voltage is limited to V_{DD} and cannot exceed 3.6V.
2) 100% duty cycle, 75Ω.
3) OFDMA DOCSIS 3.1, single channel, 75Ω.

Electrical Specifications

The following section provides the PE42722 key electrical specifications at +25 °C, V_{DD} = 3.3V, Z_S = Z_L = 75Ω.

Table 3 • *PE42722 Electrical Specifications*

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			5		1794	MHz
Insertion loss[1]	RFC–RFX	5–204 MHz 204–1218 MHz 1218–1700 MHz 1700–1794 MHz		0.20 0.30 0.70 0.85	0.35 0.50 1.00 1.25	dB
Isolation[1]	All paths	5–204 MHz 204–612 MHz 612–1218 MHz 1218–1794 MHz	45 36 30 26	50 40 33 29		dB
Return loss[1]	RFC–RFX	5–1218 MHz 1218–1794 MHz		25 13		dB
2nd harmonic, 2fo	RFX	170 MHz Average P_{CW} = 65 dBmV 800 MHz Average P_{CW} = 65 dBmV		–117 –119		dBc
3rd harmonic, 3fo	RFX	170 MHz Average P_{CW} = 65 dBmV 800 MHz Average P_{CW} = 65 dBmV		–134 –138		dBc
Input 0.1dB compression point[2]	RFC–RFX	5–1218 MHz		88		dBmV
Switching time		50% CTRL to 90% or 10% RF		15		µs

Notes:

1) Performance specified with external matching. Refer to the evaluation board schematic for details.
2) The input 0.1dB compression point is a linearity figure of merit. Refer to **Table 2** for the operating RF input power (75Ω).

Switching Frequency

The PE42722 has a maximum 25 kHz switching rate. Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious Performance

The typical spurious performance of the PE42722 is –137 dBm.

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$$\Psi_{JT} = (T_J - T_T)/P$$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 4 • *Thermal Data for PE42722*

Parameter	Typ	Unit
Ψ_{JT}	73	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	76	°C/W

Control Logic

Table 5 provides the control logic truth table for the PE42722.

Table 5 • *Truth Table for PE42722*

State	V1
RFC–RF1	H
RFC–RF2	L

Typical Performance Data

Figure 2–Figure 12 show the typical performance data @ +25 °C and V_{DD} = 3.3V (Z_S = Z_L = 75Ω), unless otherwise specified.

Figure 2 • *Insertion Loss vs Temperature (RFC–RFX)*

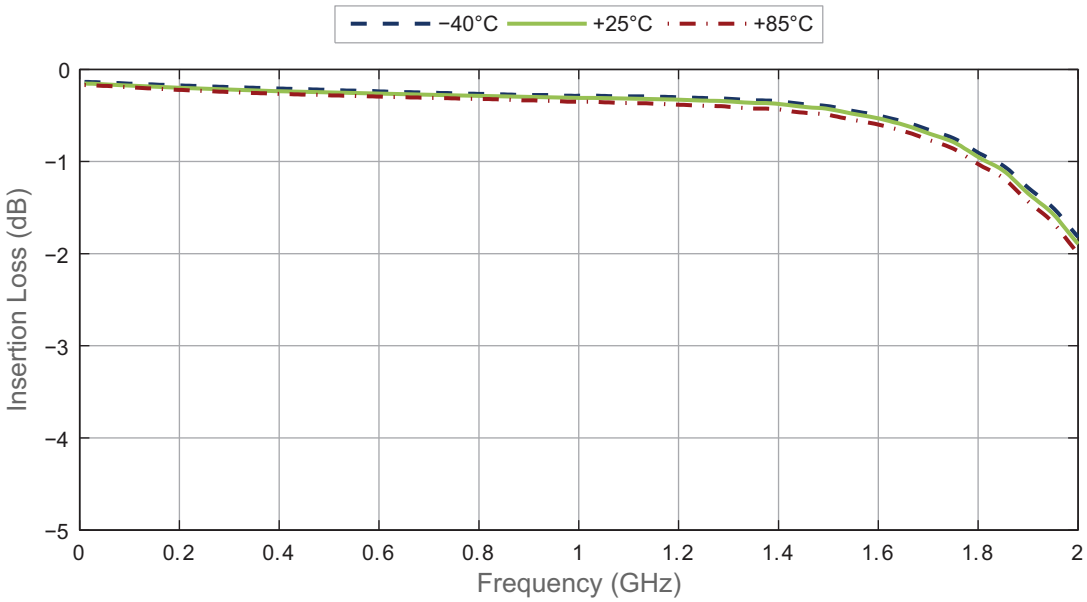


Figure 3 • *Insertion Loss vs V_{DD} (RFC–RFX)*

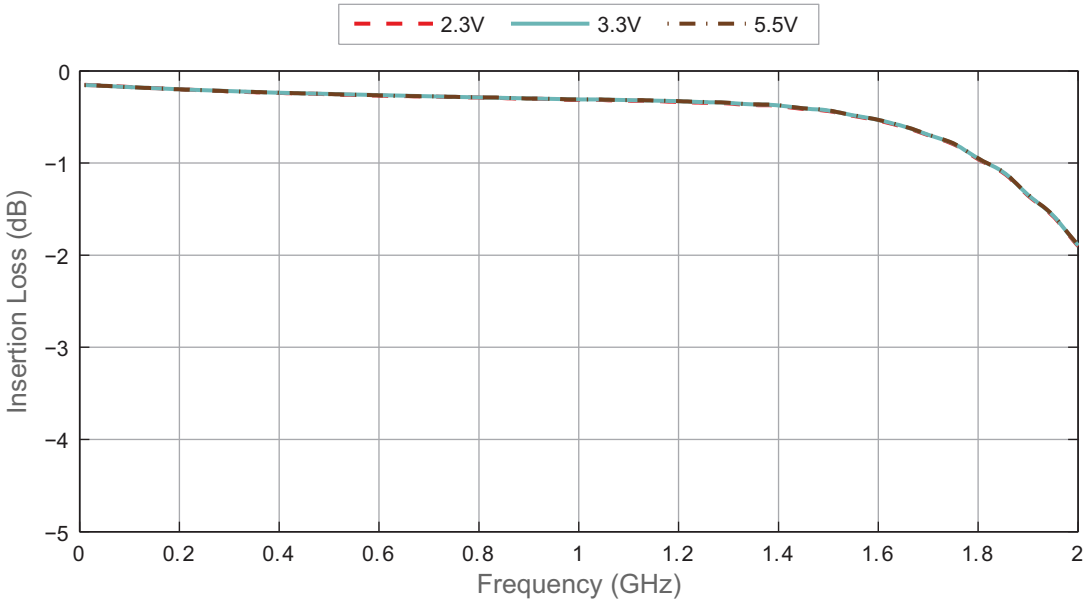


Figure 4 • *RFC Port Return Loss vs. Temperature*

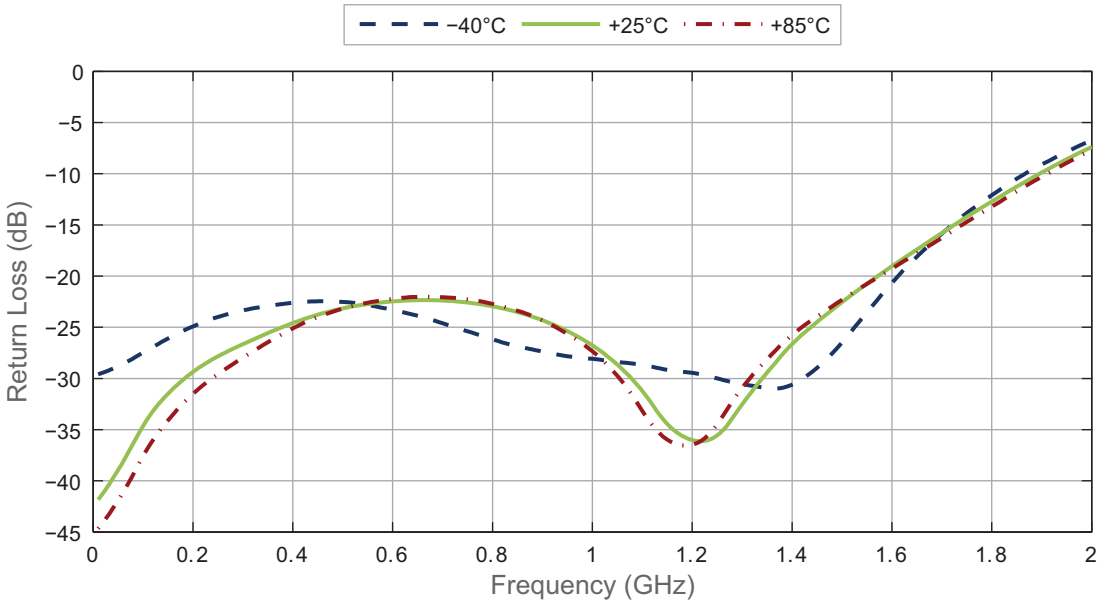


Figure 5 • *RFC Port Return Loss vs. V_{DD}*

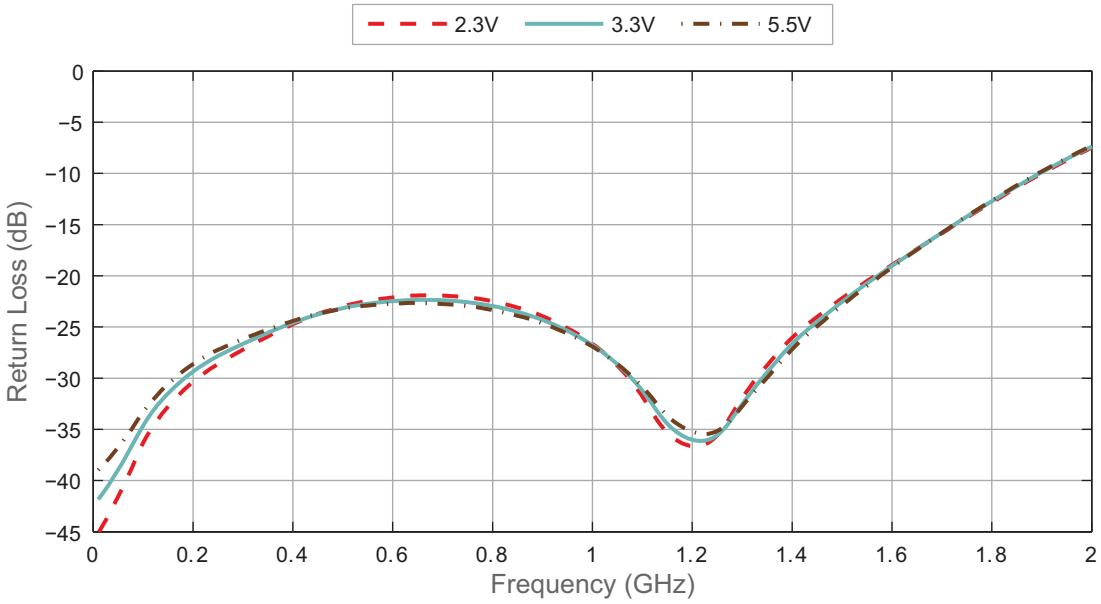


Figure 6 • *Active Port Return Loss vs. Temperature*

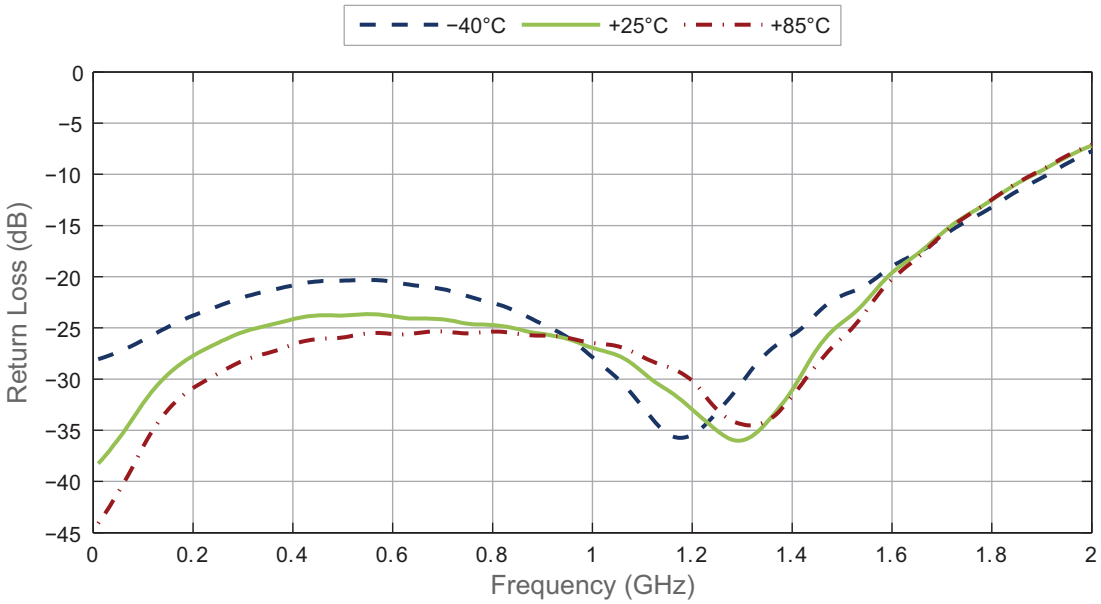


Figure 7 • *Active Port Return Loss vs. V_{DD}*

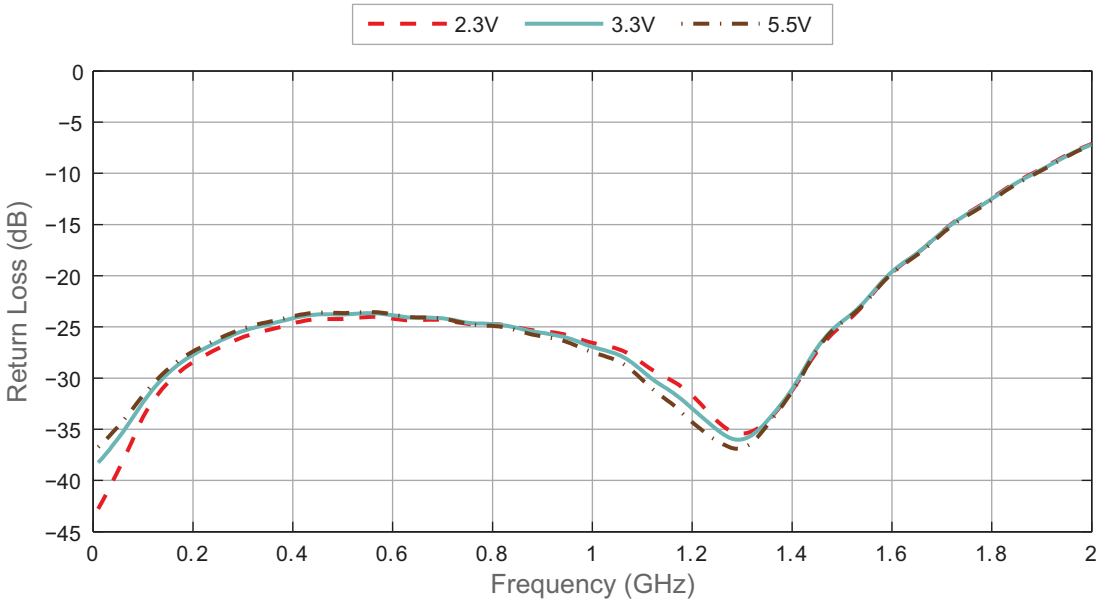


Figure 8 • *Isolation vs. Temperature (RFX–RFX)*

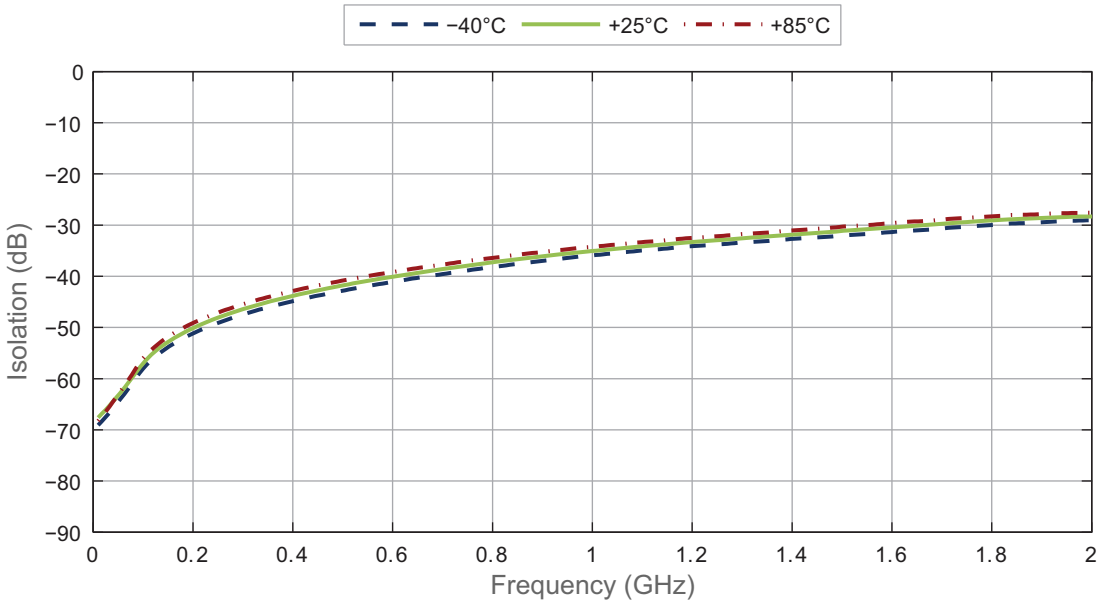


Figure 9 • *Isolation vs. V_{DD} (RFX–RFX)*

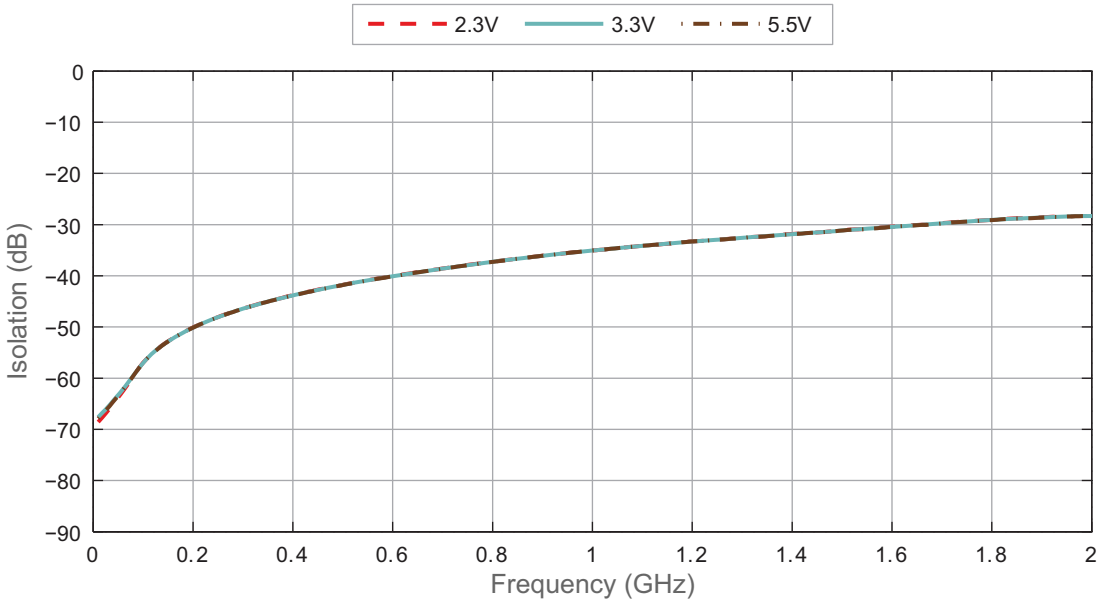


Figure 10 • *Isolation vs Temperature (RFC–RFX)*

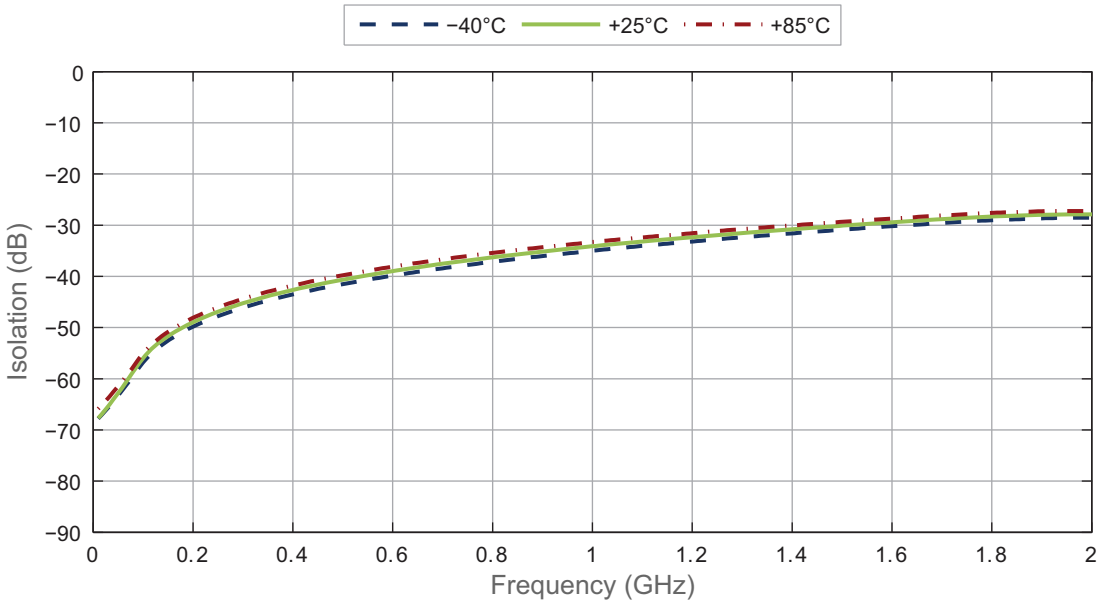


Figure 11 • *Isolation vs. V_{DD} (RFC–RFX)*

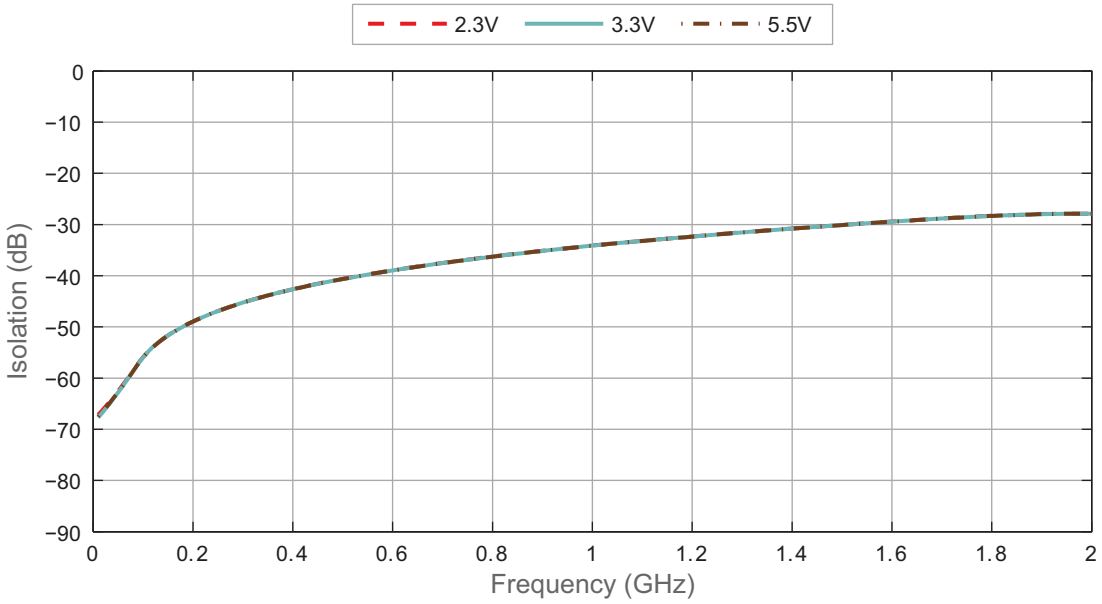
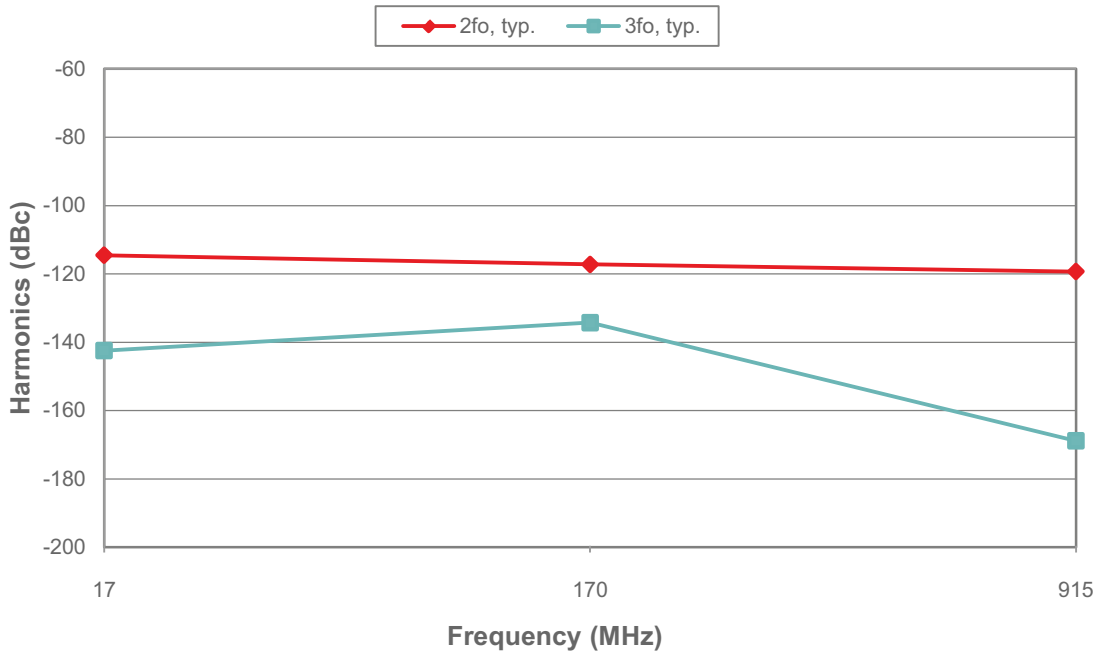


Figure 12 • *Second and Third Harmonics (P_{IN} = 65 dBmV)*

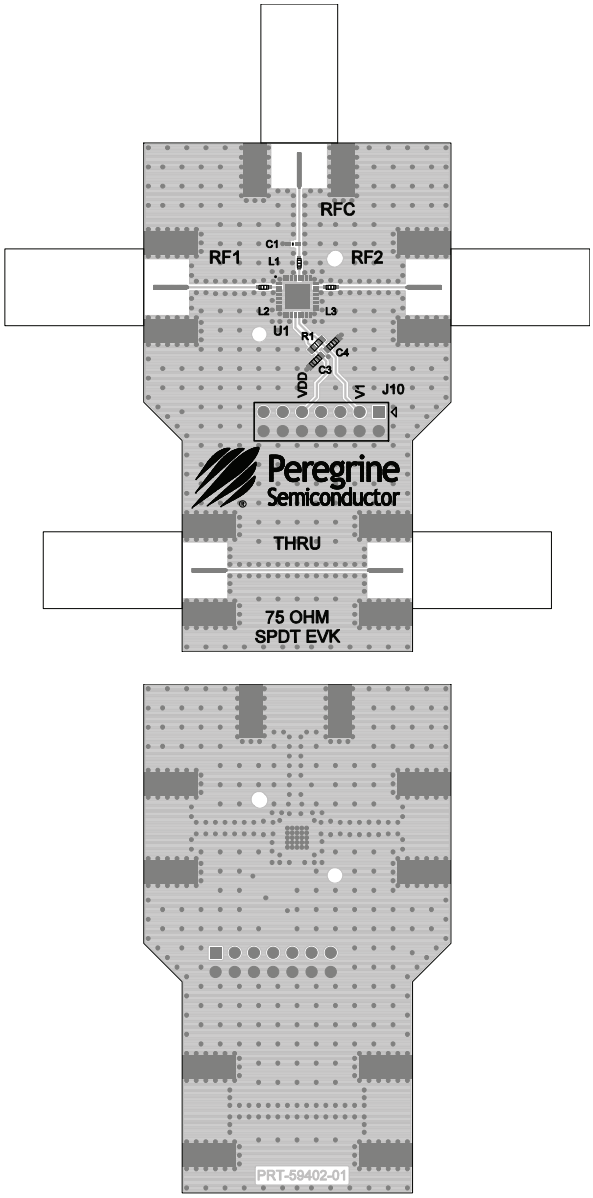


Evaluation Kit

The PE42722 evaluation board was designed to ease customer evaluation of the PE42722 RF switch. The RF common port is connected through a 75Ω transmission line via the F-Type connector, J1. RF1 and RF2 ports are connected through 75Ω transmission lines via F-Type connectors J2 and J3, respectively. A 75Ω through transmission line is available via F-Type connectors J5 (THRU left) and J6 (THRU right), which can be used to de-embed the loss of the PCB. DC power is supplied through J10, with V_{DD} on pin 9, and GND on the entire lower row of even numbered pins. To evaluate a switch path, add or remove jumpers on V1 (pin 3) using **Table 5**.

Series 6.2 nH inductors are used on the three RF ports to provide impedance matching.

Figure 13 • ***Evaluation Kit Layout for PE42722***



Pin Information

This section provides pinout information for the PE42722. **Figure 14** shows the pin map of this device for the available package. **Table 6** provides a description for each pin.

Figure 14 • *Pin Configuration (Top View)*

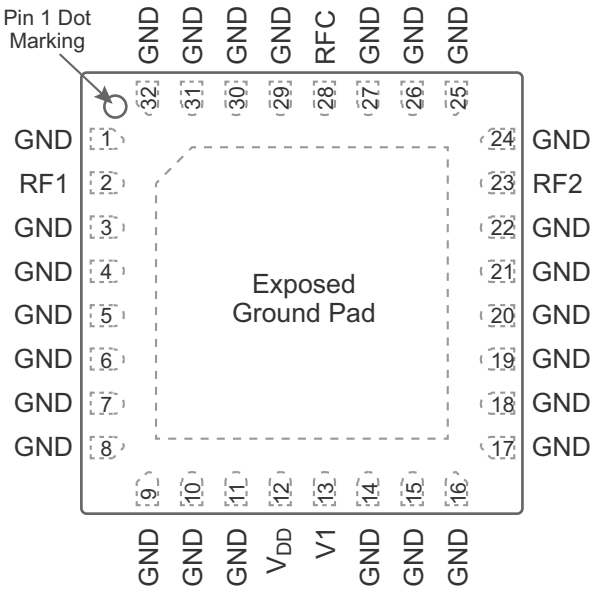


Table 6 • *Pin Descriptions for PE42722*

Pin No.	Pin Name	Description
1, 3–11, 14–22, 24–27, 29–32	GND	Ground
2	RF1(*)	RF port 1
12	V_{DD}	Supply voltage (nominal 3.3V)
13	V1	Digital control logic input 1
23	RF2(*)	RF port 2
28	RFC(*)	RF common
Pad	GND	Exposed pad: ground for proper operation

Note: * RF pins 2, 23 and 28 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging Information

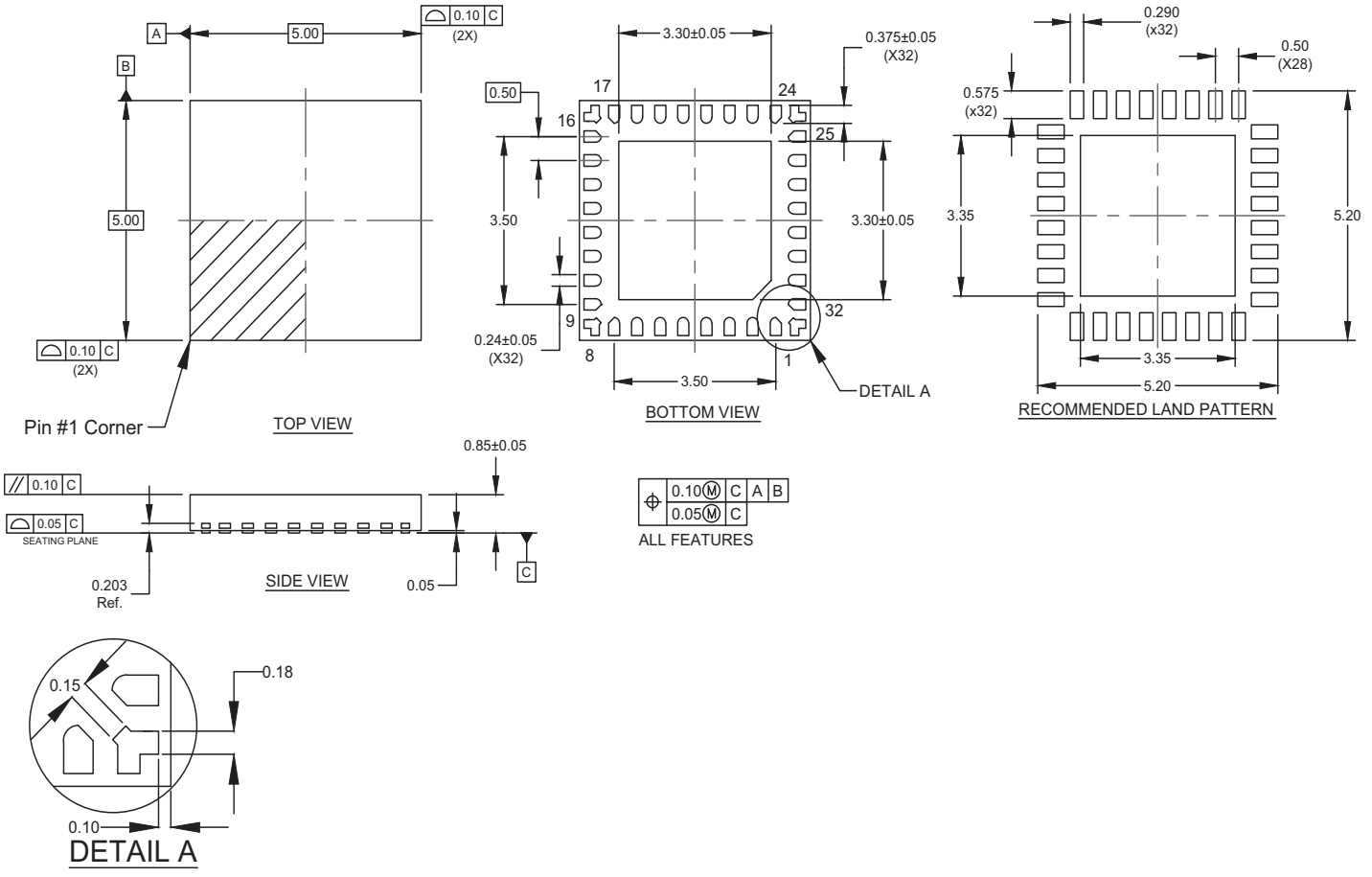
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42722 in the 32-lead 5 × 5 × 0.85 mm QFN QFN package is MSL3.

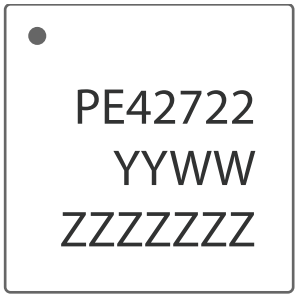
Package Drawing

Figure 15 • *Package Mechanical Drawing for PE42722*



Top-Marking Specification

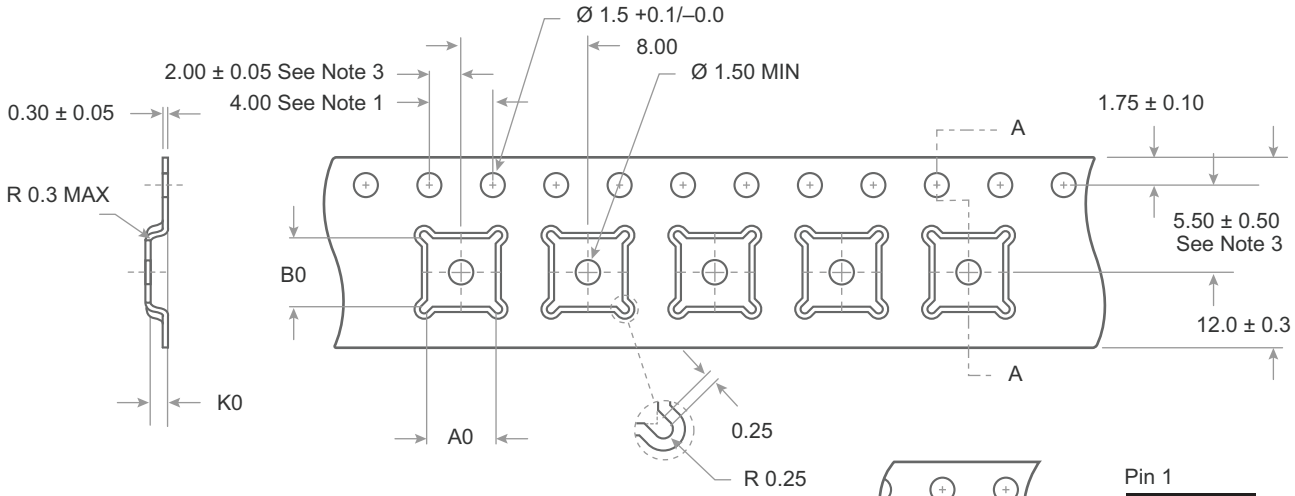
Figure 16 • *Package Marking Specifications for PE42722*



● = Pin 1 indicator
YY = Last 2 digits of assembly year
WW = Work Week of assembly lot molding
ZZZZZZZ = Maximum 7 characters of the assembly lot code

Tape and Reel Specification

Figure 17 • *Tape and Reel Specifications for 32-lead 5 × 5 × 0.85 mm QFN*



Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

A0 = 5.25 ± 0.01 mm
B0 = 5.25 ± 0.01 mm
K0 = 1.10 ± 0.01 mm

Device Orientation in Tape