

PE42822

Document Category: Product Specification

UltraCMOS® SPDT RF Switch, 700 MHz–3.8 GHz



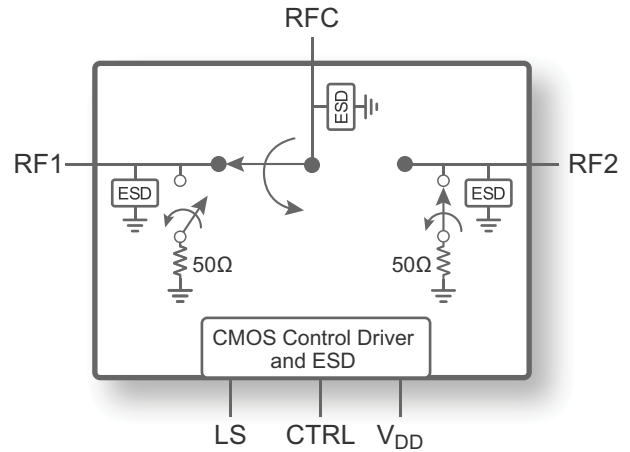
Features

- Excellent single-event peak power handling of 46.1 dBm LTE
- Exceptional linearity performance across all frequencies
 - Input IP3: 65 dBm
 - Input IP2: 120 dBm
- Extended operating temperature of 105 °C
- 1.8V/3.3V TTL compatible control
- High ESD performance of 3 kV HBM on RF pins to ground
- Packaging – 16-lead 3 × 3 × 0.85 mm QFN

Applications

- Wireless infrastructure
- Receiver protection switch

Figure 1 • PE42822 Functional Diagram



Product Description

The PE42822 is a HaRP™ technology-enhanced absorptive 50Ω SPDT RF protection switch designed for use in high power and high performance wireless infrastructure applications such as a mid-power microcell products, supporting frequencies up to 3.8 GHz.

This switch features high linearity, which remains invariant across the full supply range. The PE42822 also features exceptional isolation, fast switching time and is offered in a 16-lead 3 × 3 mm QFN package. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE42822 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • Absolute Maximum Ratings for PE42822

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	-0.3	5.5	V
Digital input voltage, V_{CTRL}	-0.3	3.6	V
LS input voltage	-0.3	3.6	V
Maximum input power, $P_{PK}^{(1)}$ 700–3800 MHz		46.1	dBm
Storage temperature range	-65	+150	°C
ESD voltage HBM ⁽²⁾ RF pins to GND All pins		3000 1500	V V
ESD voltage MM ⁽³⁾ , all pins		200	V
ESD voltage, CDM ⁽⁴⁾ , all pins		1000	V
Notes:			
1) Max 5 cycles at 10 seconds duration each cycle, $P_{PK} = 46.1$ dBm, $P_{AV} = 38.1$ dBm, 8 dB PAR LTE signal. All other parameters within recommended operating conditions. No power applied to off-terminated port. No hot switching.			
2) Human body model (MIL STD 883 Method 3015).			
3) Machine model (JEDEC JESD22 A115).			
4) Charged device model (JEDEC JESD22-C101).			

Recommended Operating Conditions

Table 2 lists the recommending operating conditions for the PE42822. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • Recommended Operating Conditions for PE42822

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.3		5.5	V
Supply current, I_{DD}		120	200	μ A
Digital input high	1.17		3.6	V
Digital input low	-0.3		0.6	V
RF input power, single event ⁽¹⁾ 700–3800 MHz, peak 700–3800 MHz, average			46.1 38.1	dBm dBm
RF input power 700–3800 MHz, pulsed, +25 °C ⁽²⁾ 700–3800 MHz, pulsed, +105 °C ⁽²⁾ 700–3800 MHz, CW, -40 °C to +105 °C			38.5 38 32	dBm dBm dBm
RF input power into terminated ports, CW			24	dBm
Operating temperature range	-40	+25	+105	°C
Notes:				
1) Single event: 10-second duration with 8 dB PAR LTE signal. No power applied to off-terminated port. No hot switching.				
2) 2.5% duty cycle of 4620 μ s period. No power applied to off-terminated port. No hot switching.				

Electrical Specifications

Table 3 provides the PE42822 key electrical specifications @ +25 °C, $V_{DD} = 2.3\text{--}5.5\text{V}$, unless otherwise specified.

Table 3 • PE42822 Electrical Specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operational frequency			700		3800	MHz
Insertion loss	RFC–RFX	700–3800 MHz		0.8	1.05	dB
Isolation	RFX–RFX	700–3800 MHz	44	47		dB
Isolation	RFC–RFX	700–3800 MHz	39	41		dB
Return loss (common and active port)	RFX	700–3800 MHz		20		dB
Input 0.1dB compression point ^(*)	RFC–RFX	700–3800 MHz		39.5		dBm
Input IP3	RFC–RFX	700–3800 MHz		65		dBm
Input IP2	RFC–RFX	700–3800 MHz		120		dBm
Switching time		50% CTRL to 90% or 10% of final value		500	700	ns
Settling time		50% CTRL to 0.05 dB final value, rising and falling edge		2	4	μs

Note: * The input P0.1dB compression point is a linearity figure of merit. Refer to Table 2 for the operating RF input power (50Ω).

Control Logic

Table 4 provides the control logic truth table for the PE42822.

Table 4 • Truth Table for PE42822

LS	CTRL	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

Typical Performance Data

Figure 2–Figure 25 show the typical performance data @ +25 °C, $V_{DD} = 2.3\text{--}5.5\text{V}$, unless otherwise specified.

Figure 2 • Insertion Loss vs Temp (RF1)

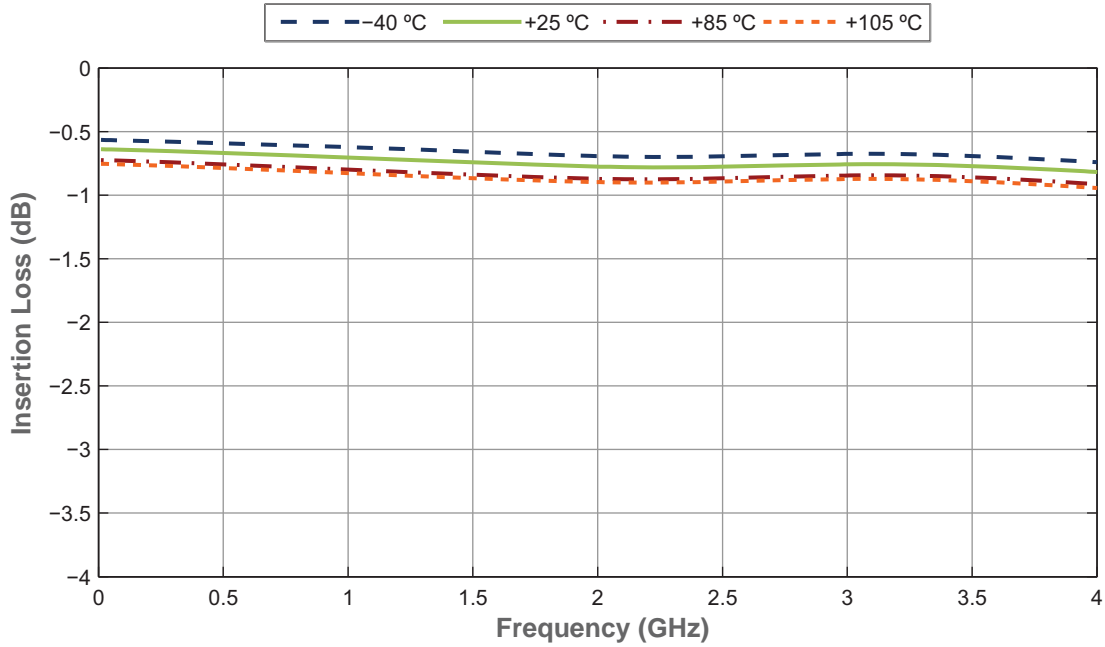


Figure 3 • Insertion Loss vs V_{DD} (RF1)

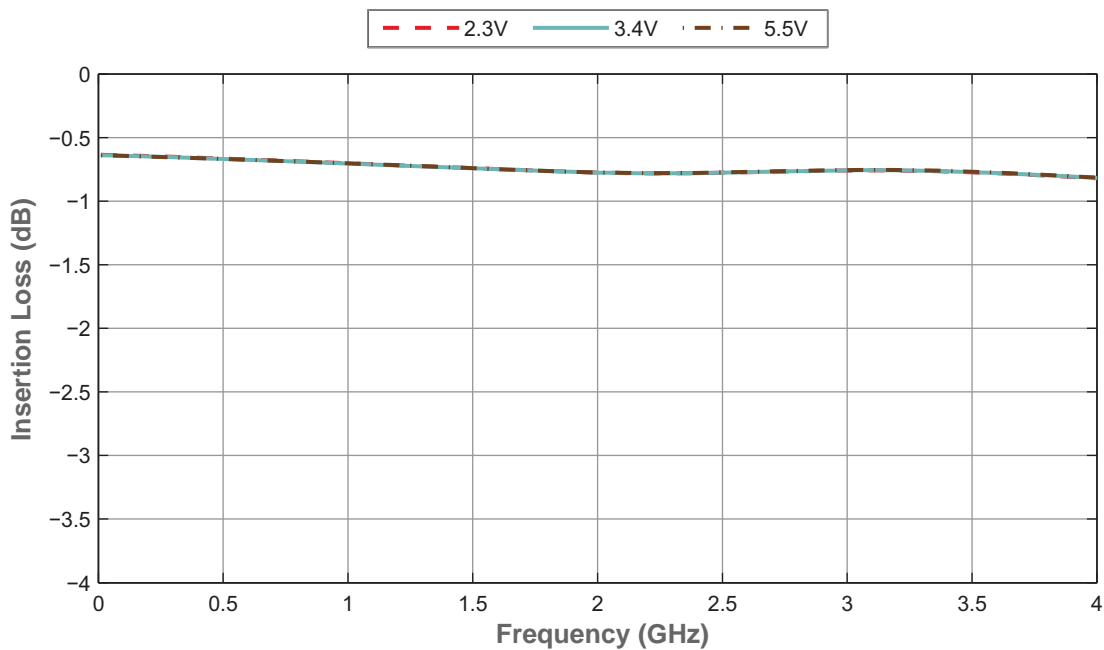


Figure 4 • Insertion Loss vs Temp (RF2)

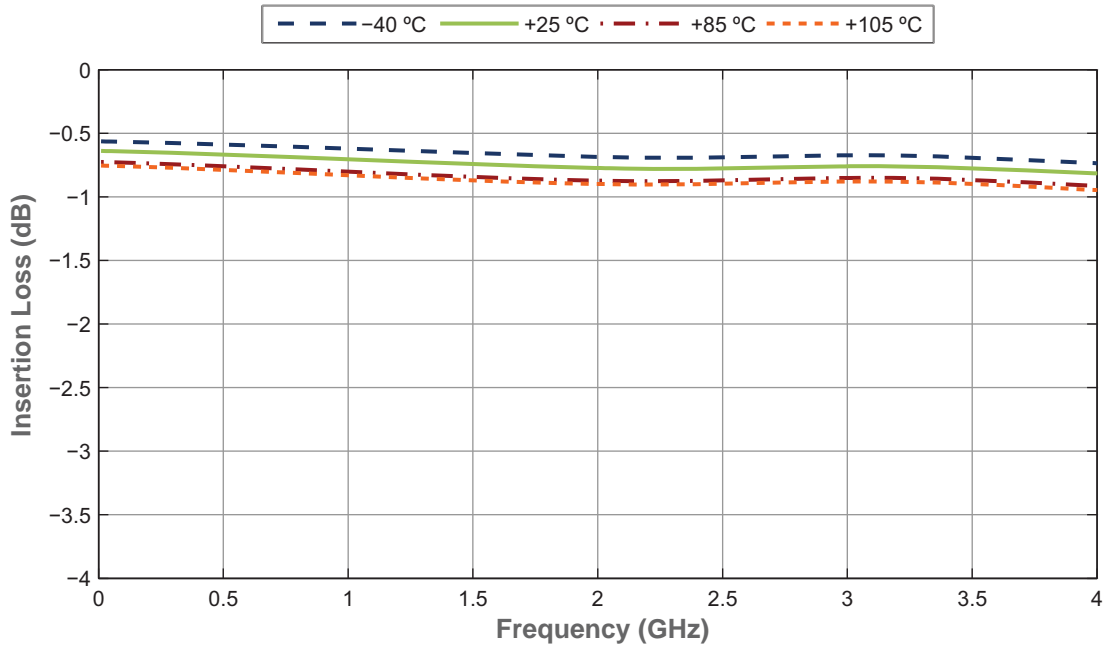


Figure 5 • Insertion Loss vs V_{DD} (RF2)

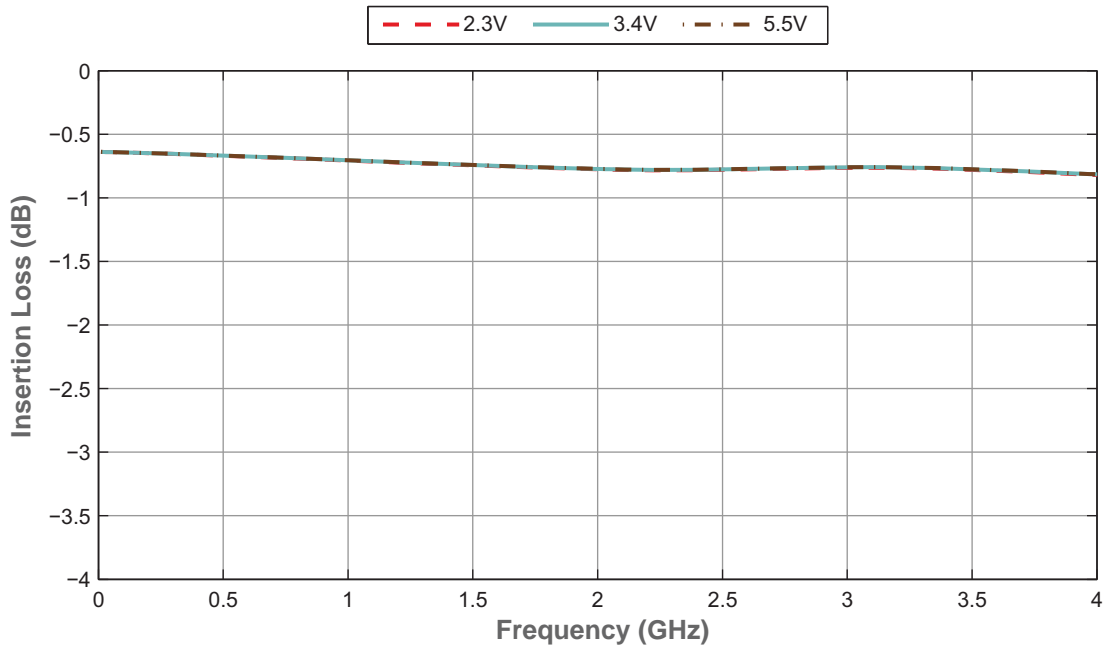


Figure 6 • RFC Port Return Loss vs Temp (RF1)

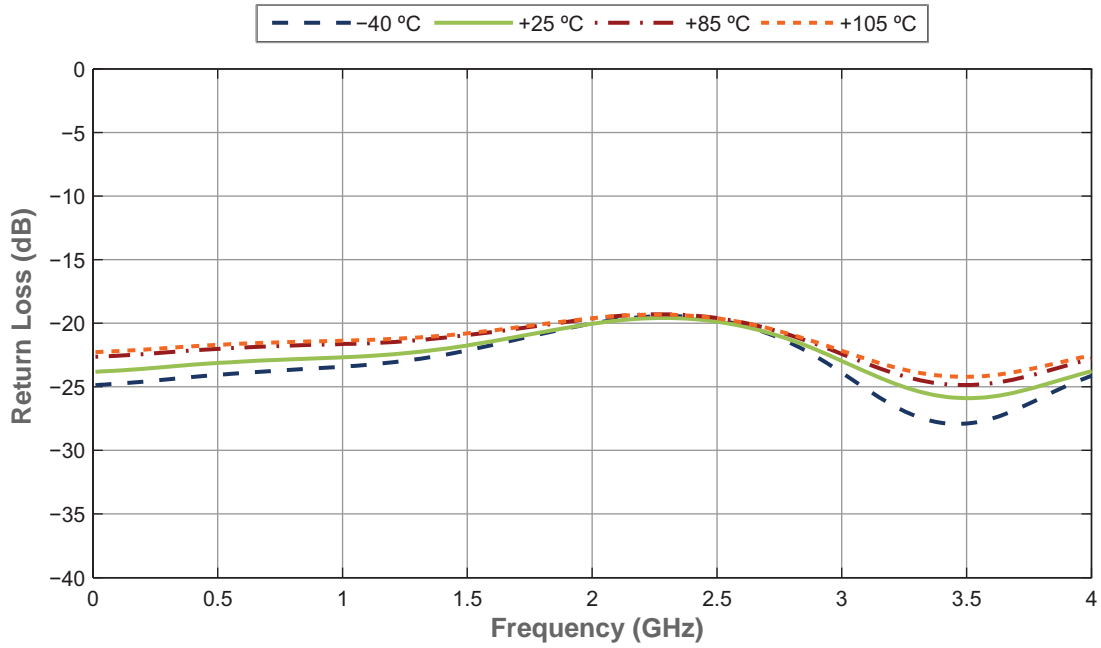


Figure 7 • RFC Port Return Loss vs V_{DD} (RF1)

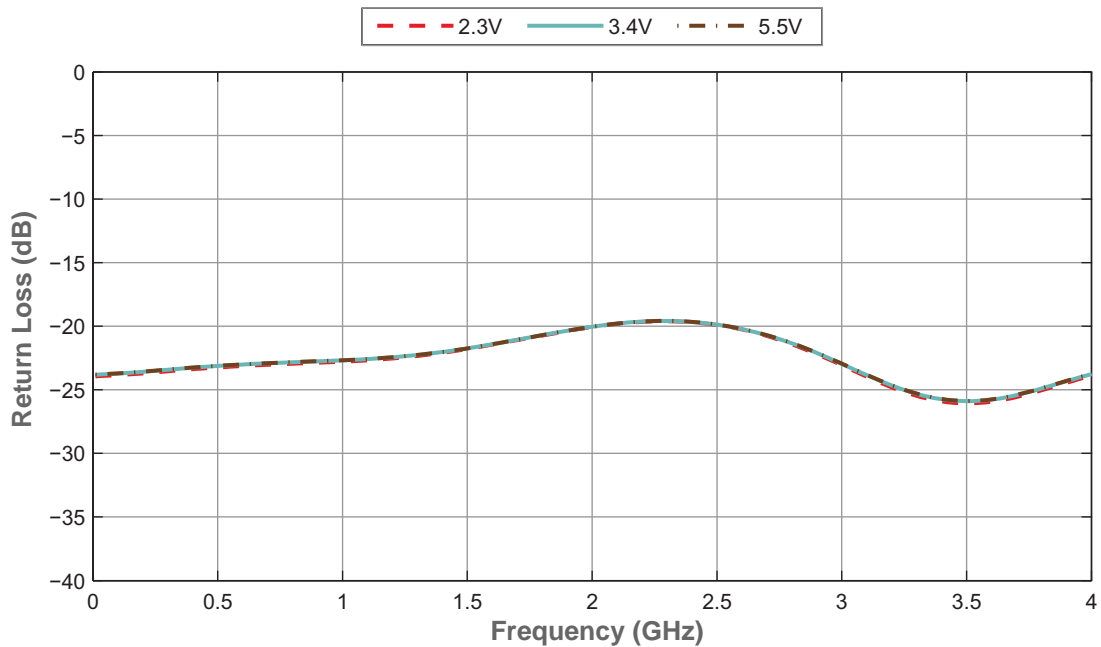


Figure 8 • RFC Port Return Loss vs Temp (RF2)

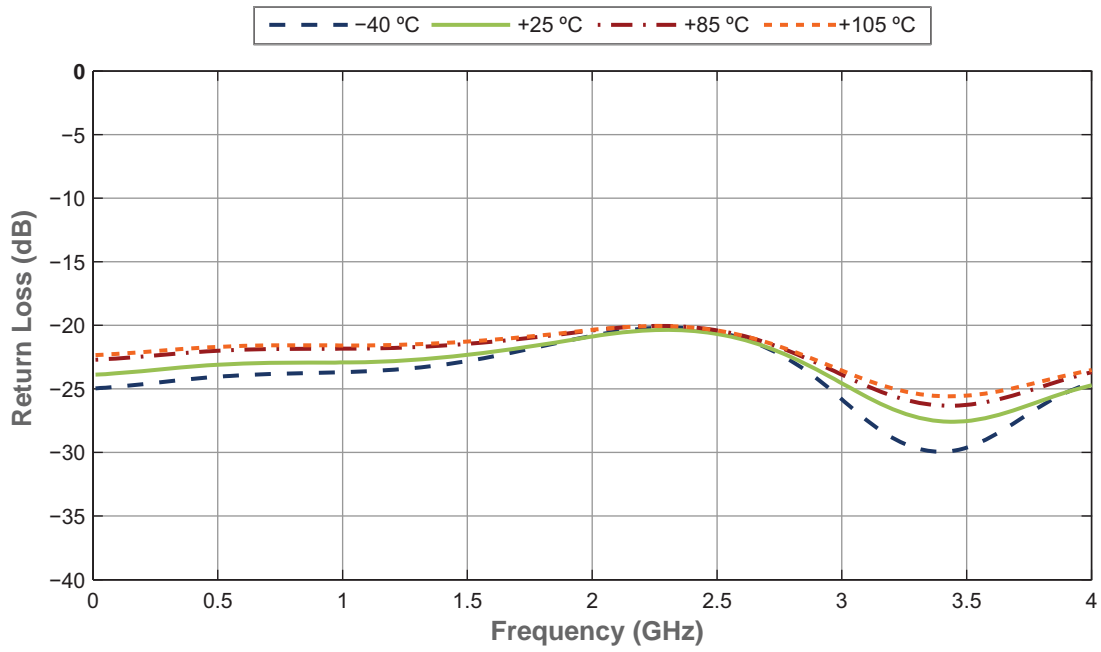


Figure 9 • RFC Port Return Loss vs V_{DD} (RF2)

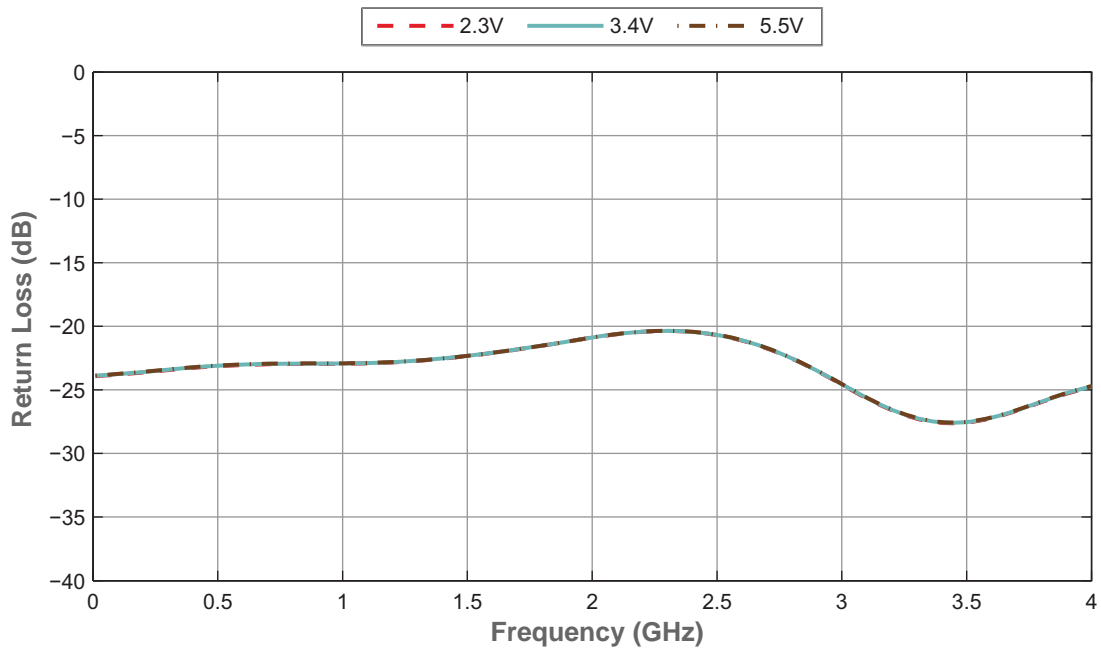


Figure 10 • Active Port Return Loss vs Temp (RF1)

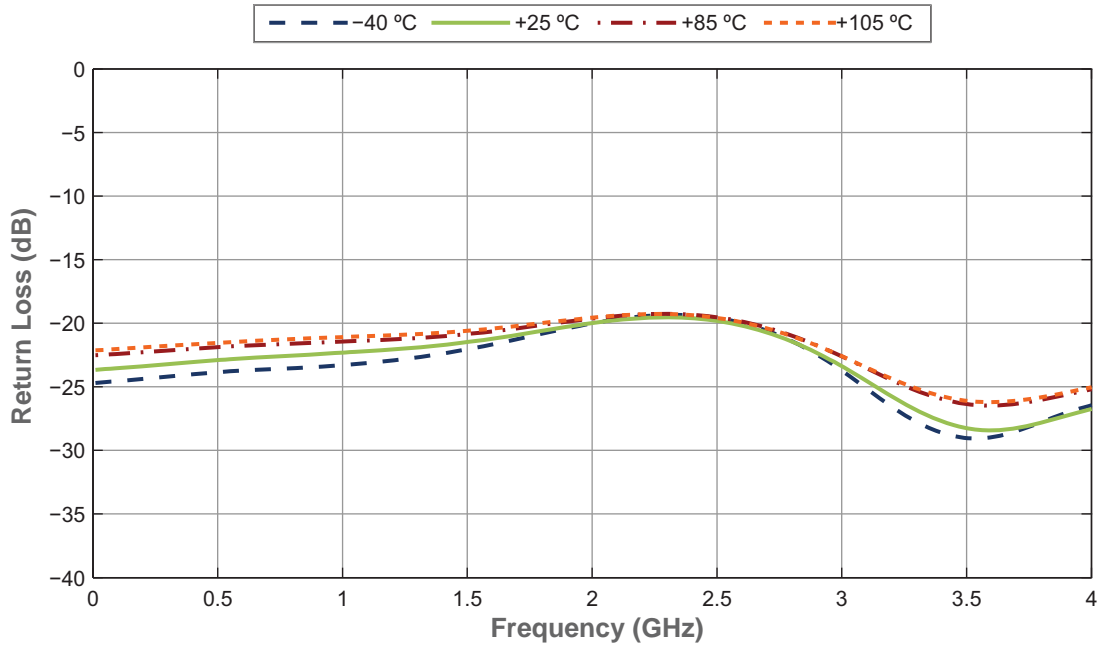


Figure 11 • Active Port Return Loss vs V_{DD} (RF1)

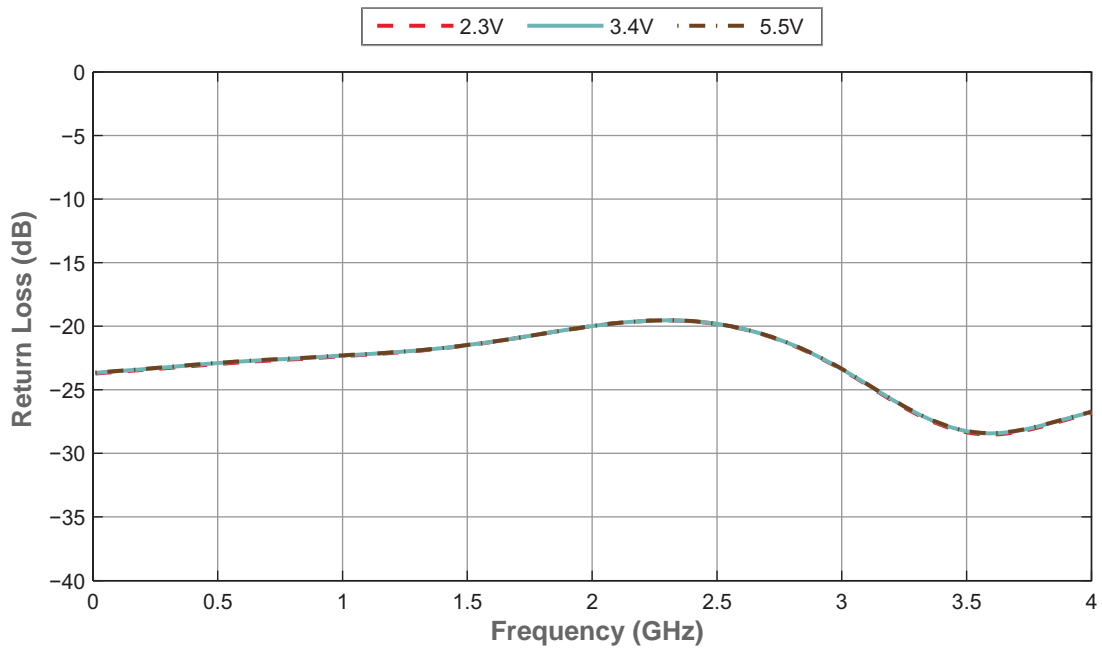


Figure 12 • RFC Port Return Loss vs Temp (RF2)

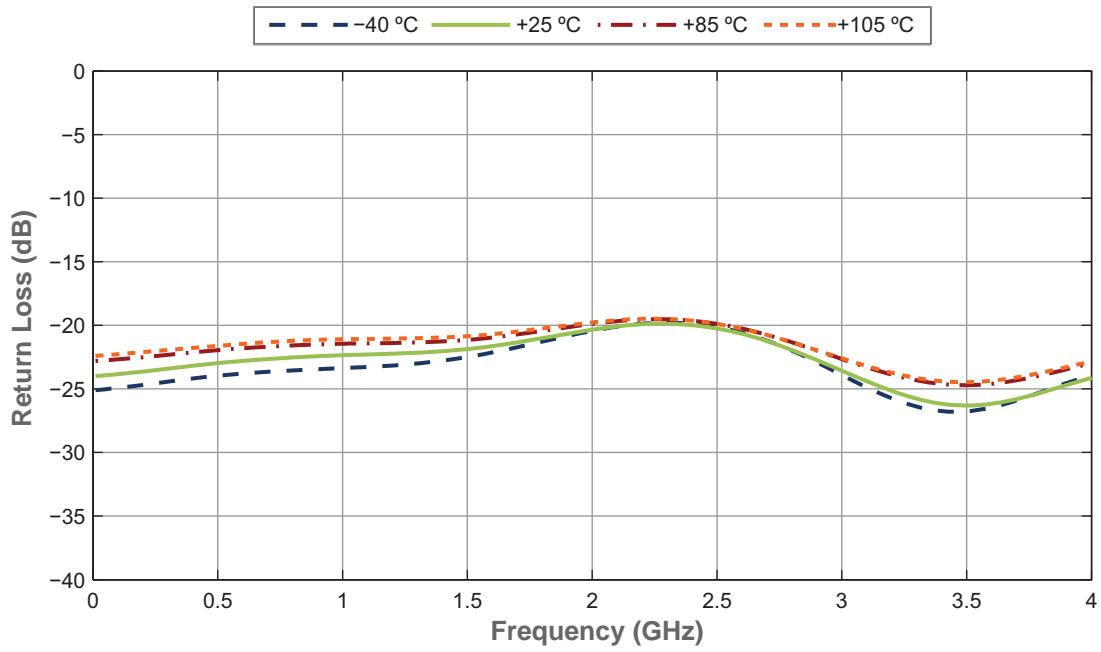


Figure 13 • RFC Port Return Loss vs V_{DD} (RF2)

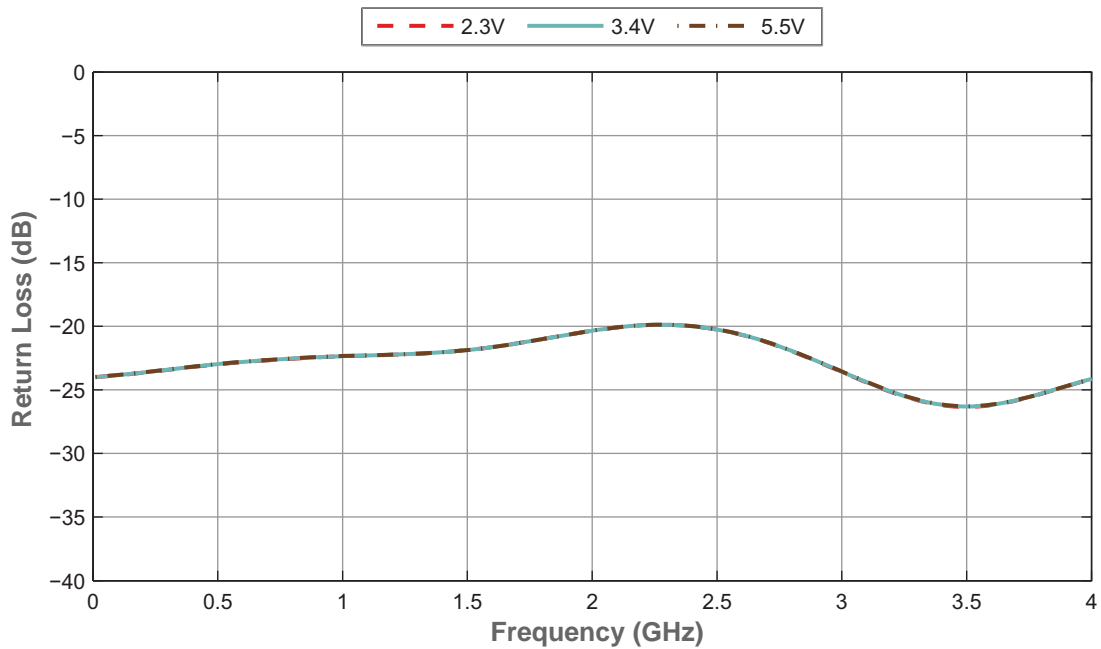


Figure 14 • Terminated Port Return Loss vs Temp (RF1)

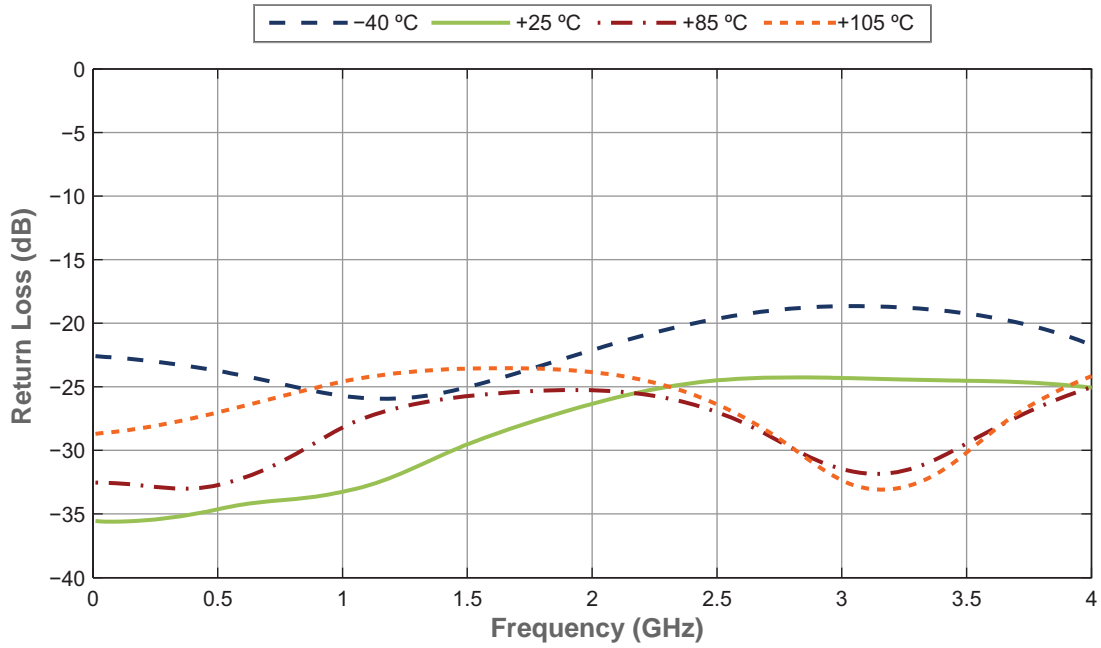


Figure 15 • Terminated Port Return Loss vs V_{DD} (RF1)

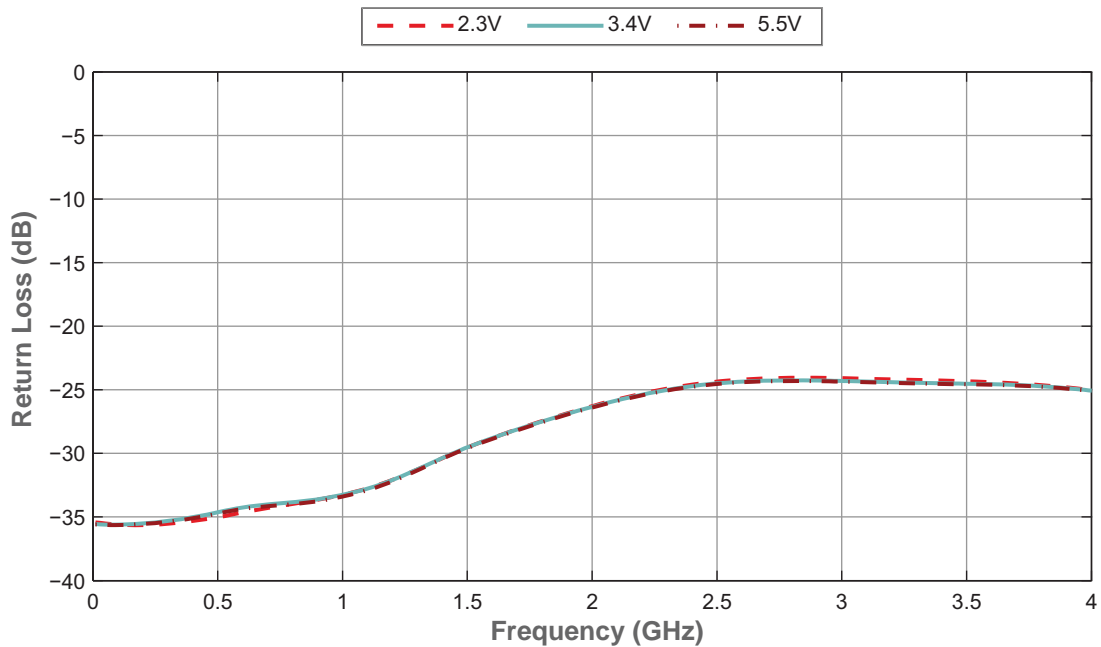


Figure 16 • Terminated Port Return Loss vs Temp (RF2)

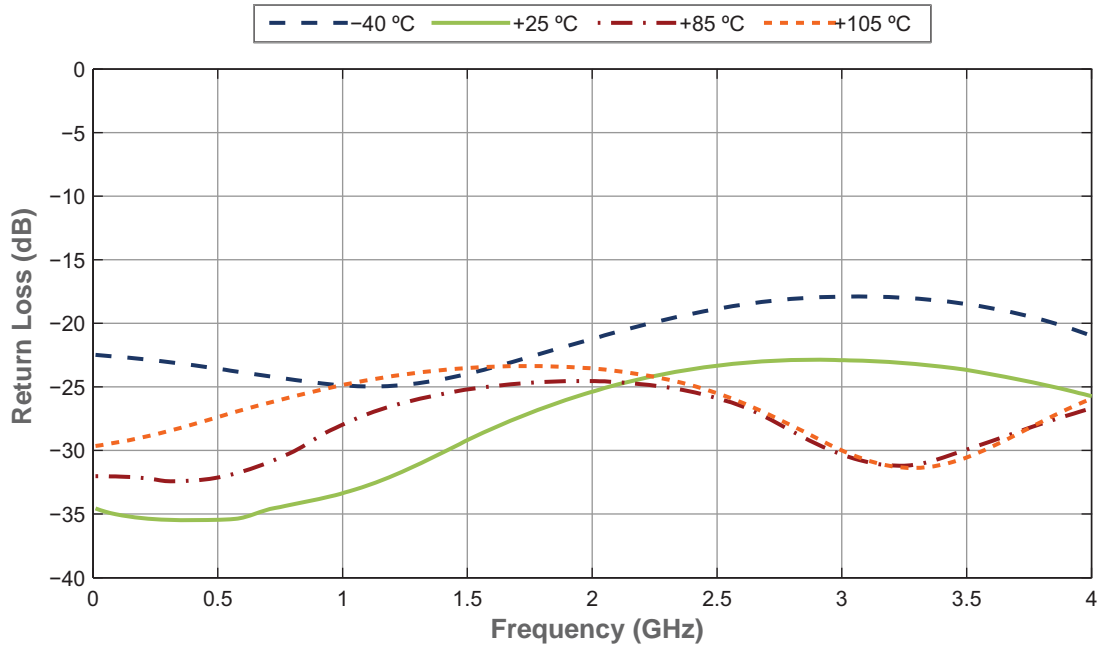


Figure 17 • Terminated Port Return Loss vs V_{DD} (RF2)

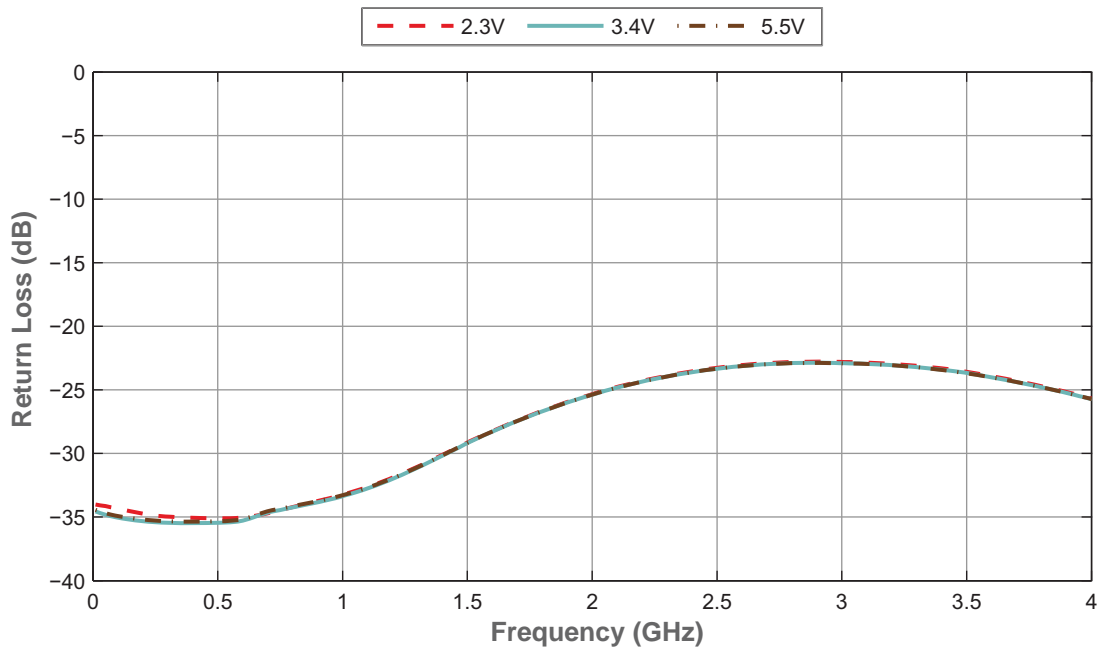


Figure 18 • Isolation vs Temp (RF1–RF2, RF1 Active)

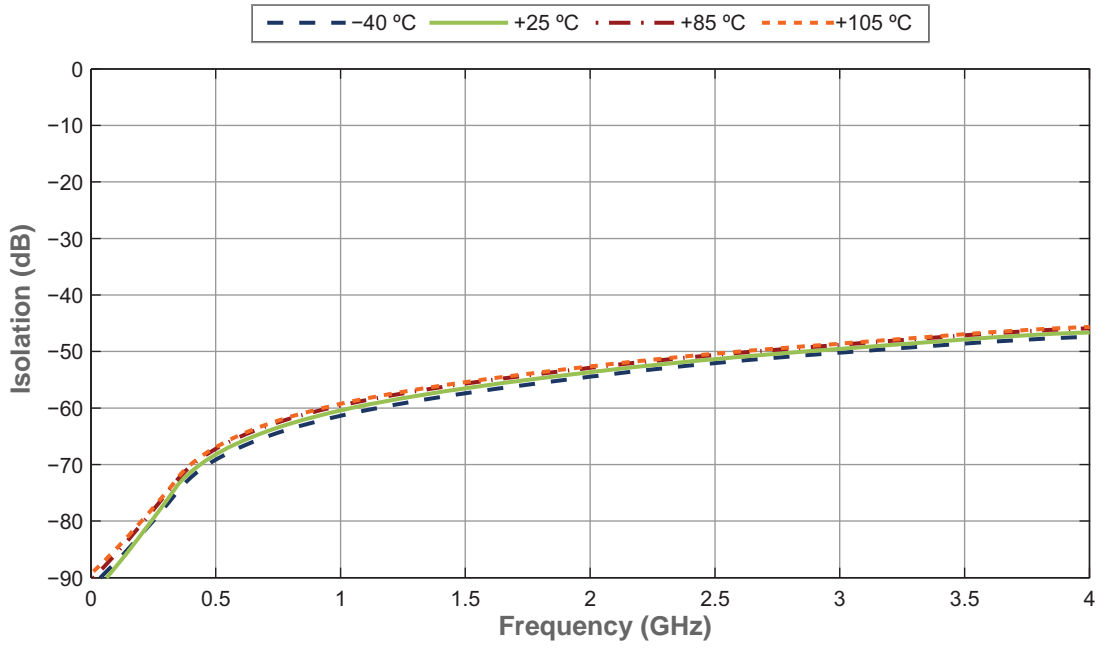


Figure 19 • Isolation vs V_{DD} (RF1–RF2, RF1 Active)

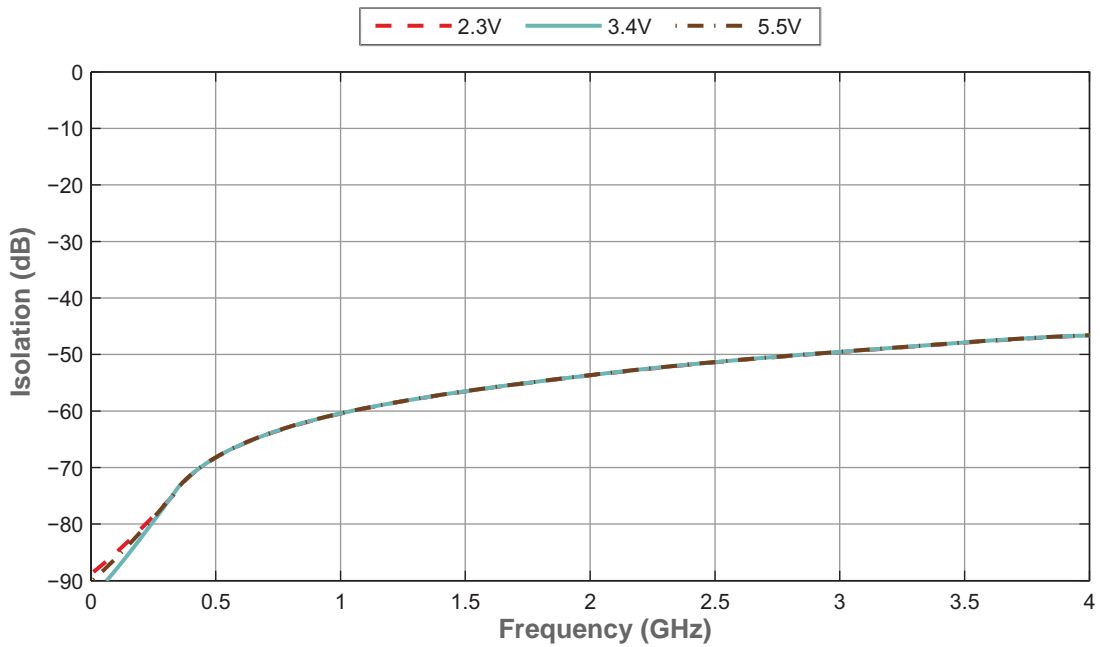


Figure 20 • Isolation vs Temp (RF2–RF1, RF2 Active)

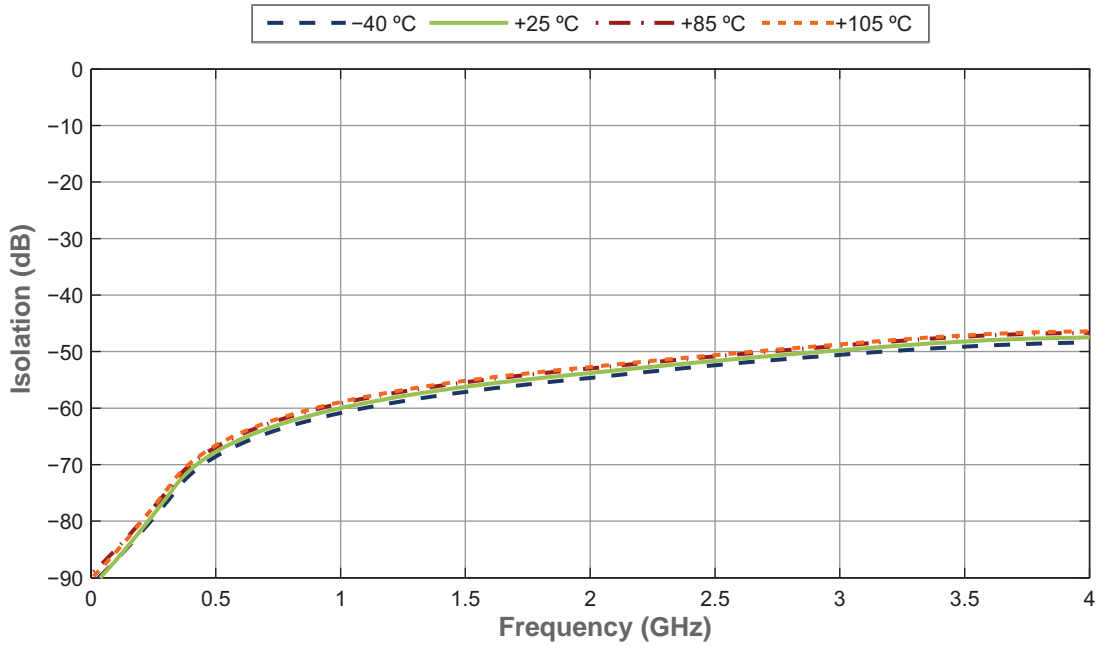


Figure 21 • Isolation vs V_{DD} (RF2–RF1, RF2 Active)

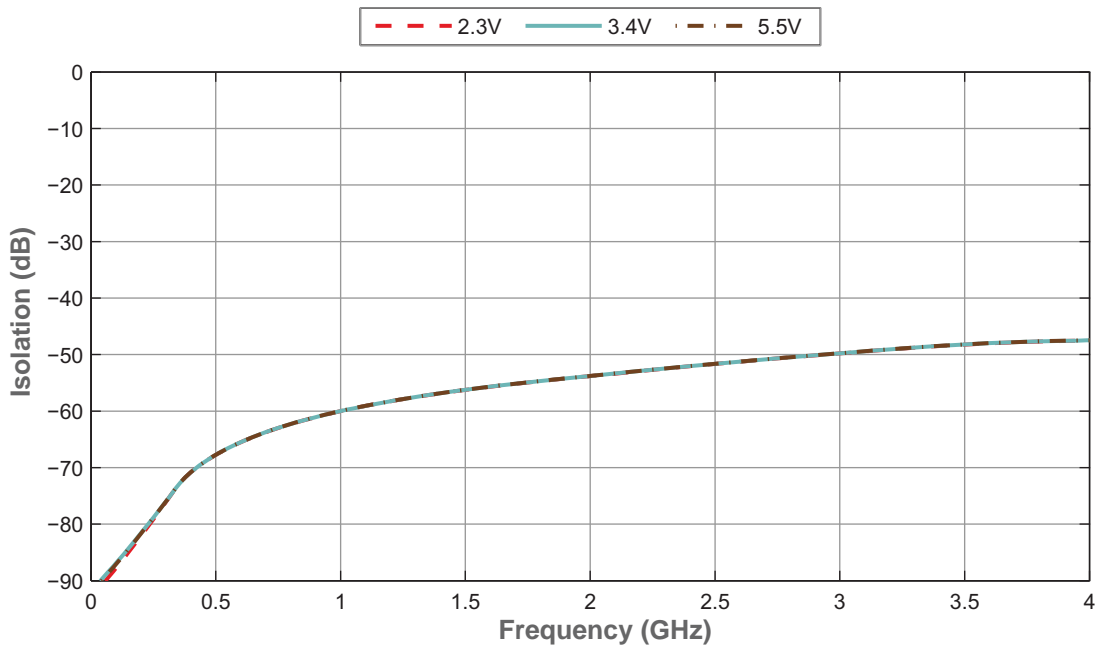


Figure 22 • Isolation vs Temp (RFC–RF1, RF2 Active)

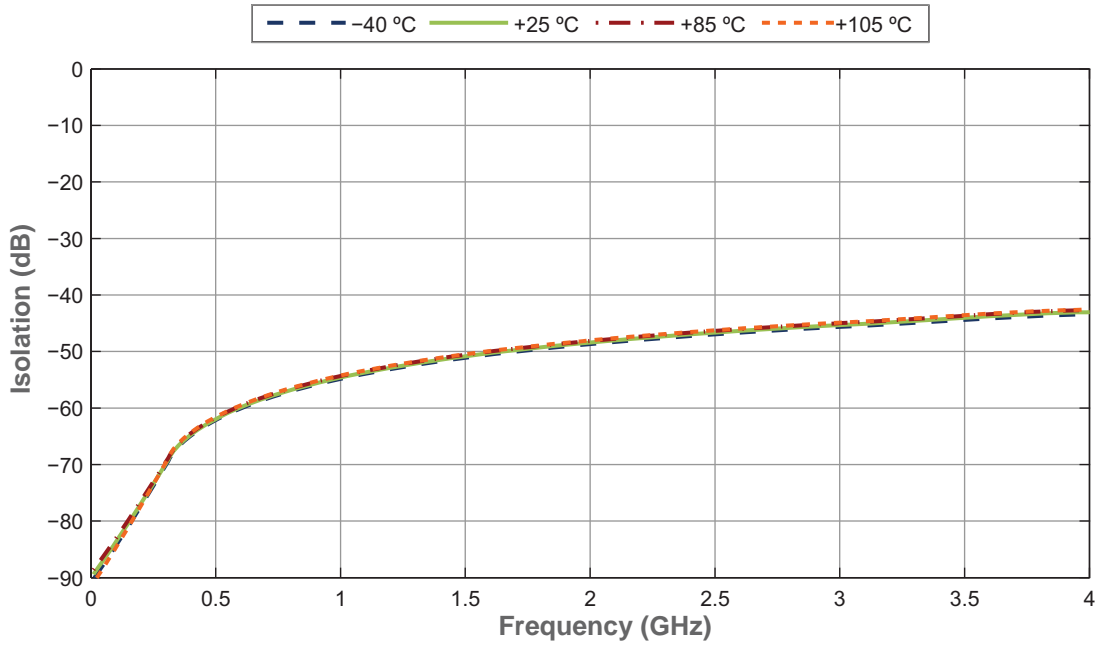


Figure 23 • Isolation vs V_{DD} (RFC–RF1, RF2 Active)

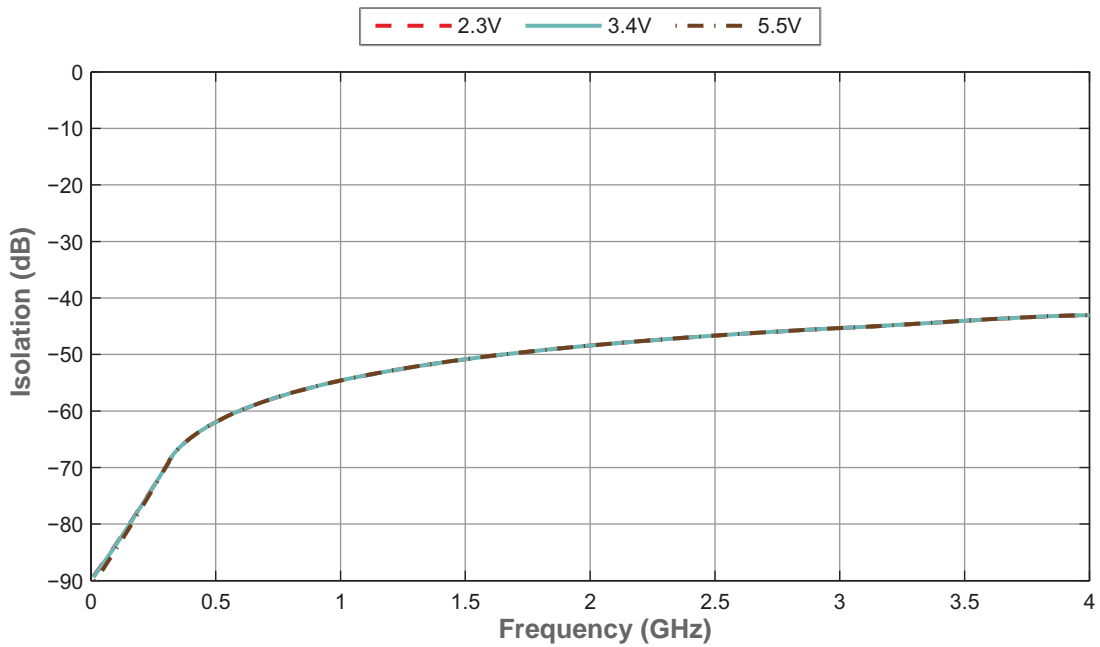


Figure 24 • Isolation vs Temp (RFC–RF2, RF1 Active)

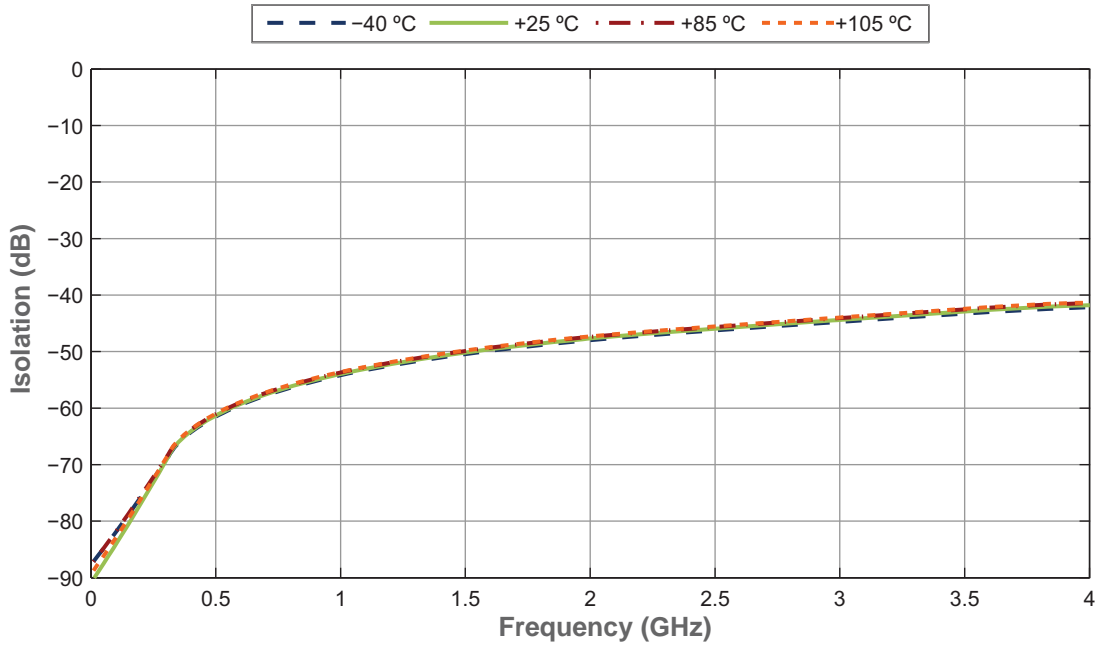
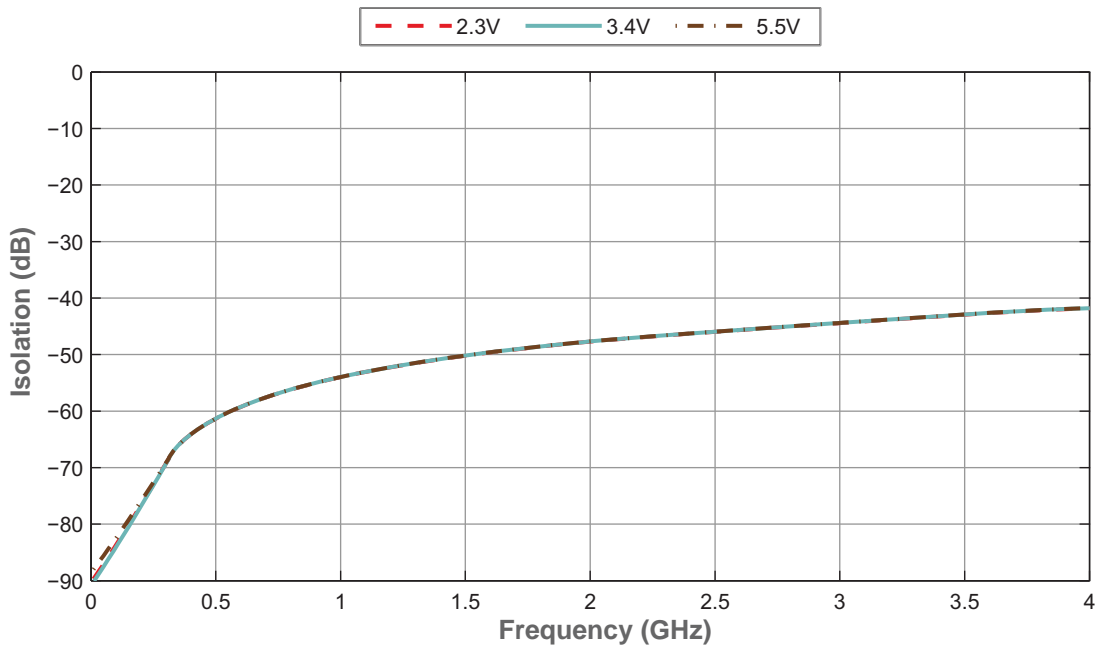


Figure 25 • Isolation vs V_{DD} (RFC–RF2, RF1 Active)

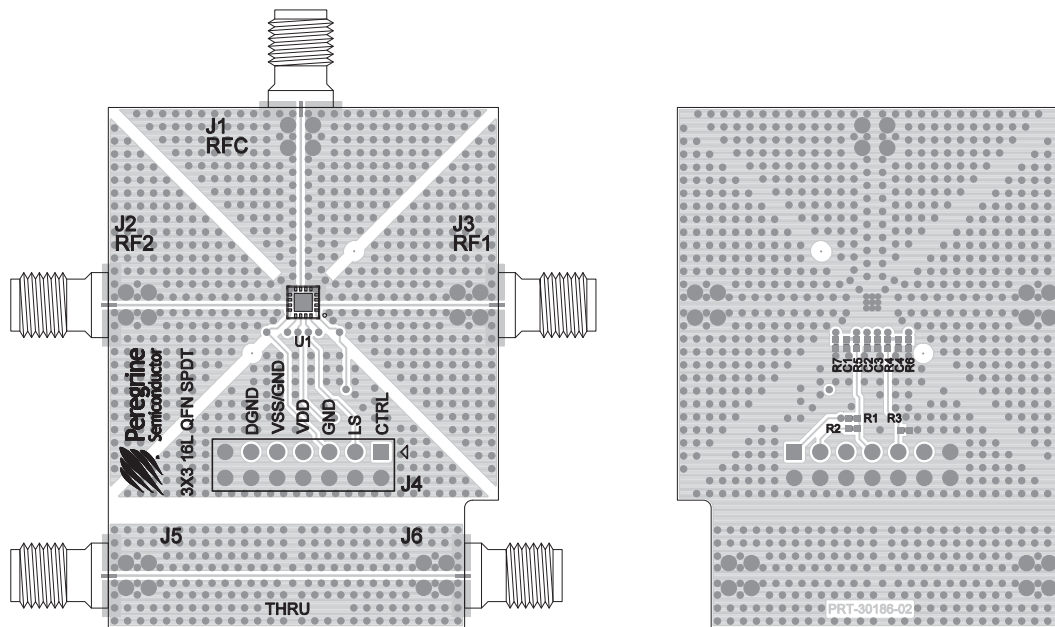


Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42822. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which can be used to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

For the true performance of the PE42822 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

Figure 26 • Evaluation Kit Layout for PE42822



Pin Information

This section provides pinout information for the PE42822. **Figure 27** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

Figure 27 • Pin Configuration (Top View)

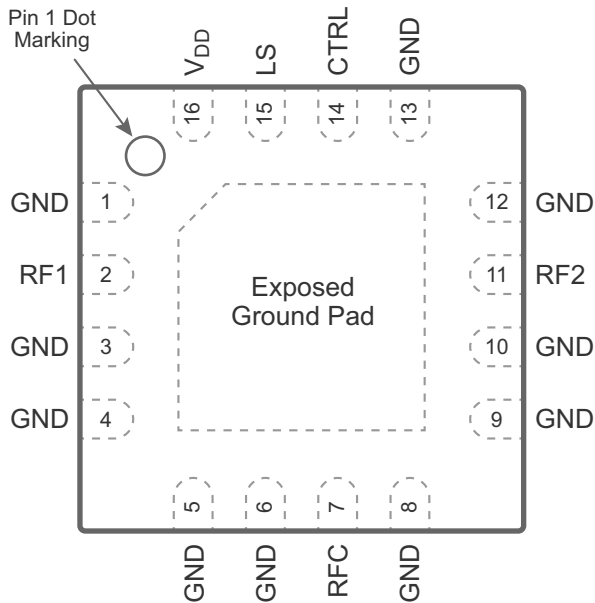


Table 5 • Pin Descriptions for PE42822

Pin No.	Pin Name	Description
1, 3–6, 8–10, 12 13	GND	Ground
2	RF1 ^(*)	RF port 1
7	RFC ^(*)	RF common port
11	RF2 ^(*)	RF port 2
14	CTRL	Digital control logic input
15	LS	Logic select—used to determine the definition for the CTRL pin (see Table 4)
16	V _{DD}	Supply voltage (nominal 3.3V)
Pad	GND	Exposed pad: ground for proper operation

Note: * RF pins 2, 7 and 11 must be 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging Information

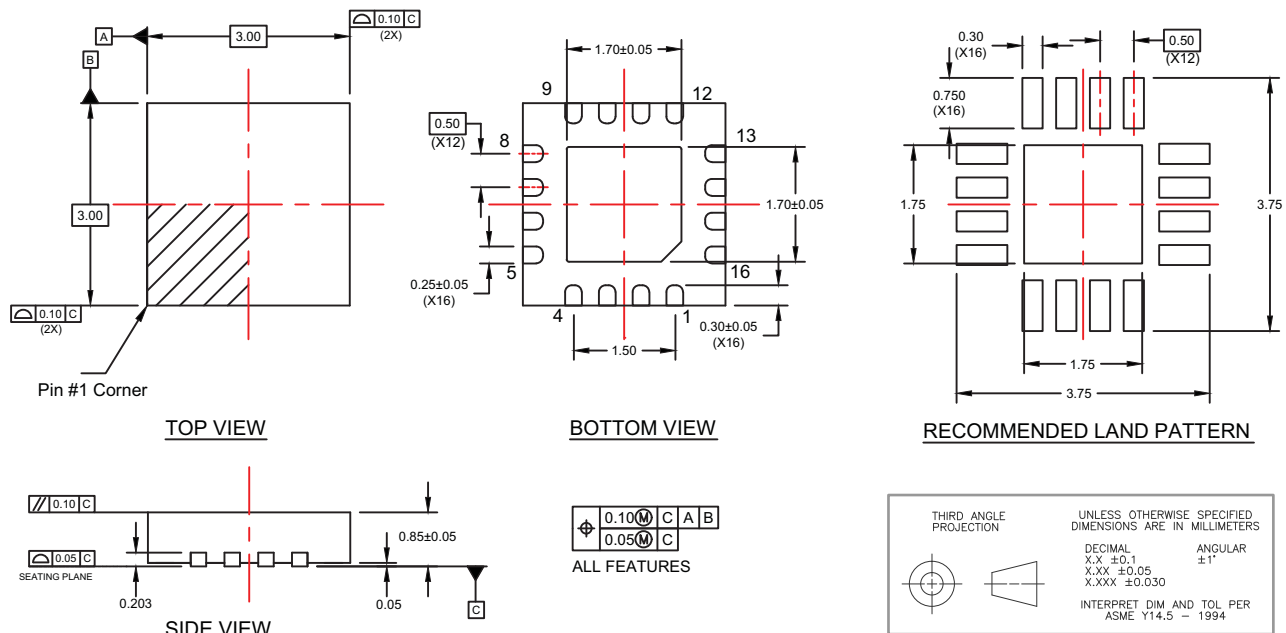
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape and reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42822 in the 16-lead 3 × 3 × 0.85 mm QFN package is MSL3.

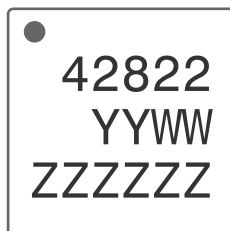
Package Drawing

Figure 28 • Package Mechanical Drawing for 16-lead 3 × 3 × 0.85 mm QFN



Top-Marking Specification

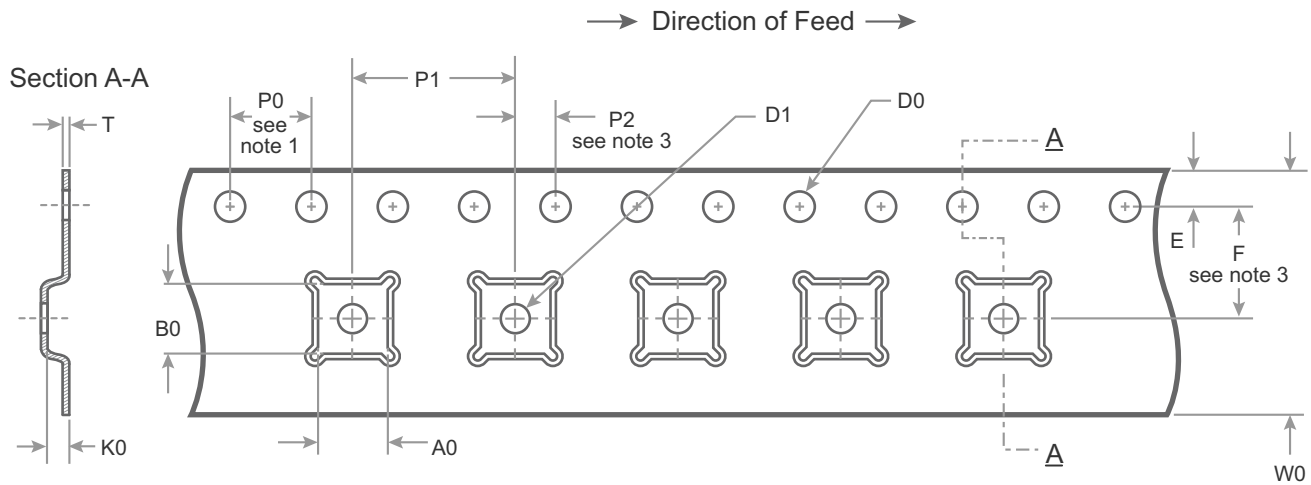
Figure 29 • Package Marking Specifications for PE42822



- = Pin 1 indicator
- YY = Last two digits of assembly year
- WW = Assembly work week
- ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

Figure 30 • Tape and Reel Specifications for 16-lead 3 × 3 × 0.85 mm QFN

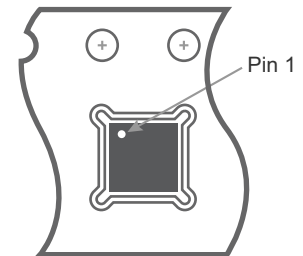


A0	3.3
B0	3.3
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ± 0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape