Product Specification

PE42920

UltraCMOS® Passive DDSPDT High-Isolation RF Switch 10 kHz–6 GHz

Features

- Dual differential single pole double throw switch
- Broadband: 10 kHz to 6 GHz
- Low frequency insertion loss: 0.7 dB typical
- High isolation between same channels at 6 GHz: 26 dB typical
- High isolation between opposite active channels at 6 GHz: 30 dB typical
- Low phase mismatch between matched paths at 6 GHz: 15 degrees typical
- High ESD performance: 2 kV HBM

Product Description

The PE42920 is a dual differential single pole double throw (DDSPDT) RF switch developed on Peregrine's UltraCMOS® process technology. It is a broadband and low loss device enabling the switching of two independent differential signals. This device consumes less power than active differential switches and offers 2 kV HBM ESD protection. It has high isolation between same channel inputs as well as opposite active channels. It has been designed for low phase mismatch between matched paths.

The PE42920 is manufactured on Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 2. Package Type
16-lead 3 × 3 mm QFN

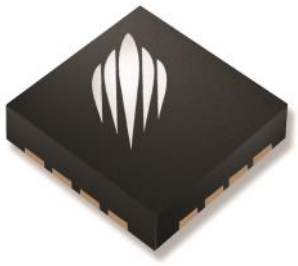
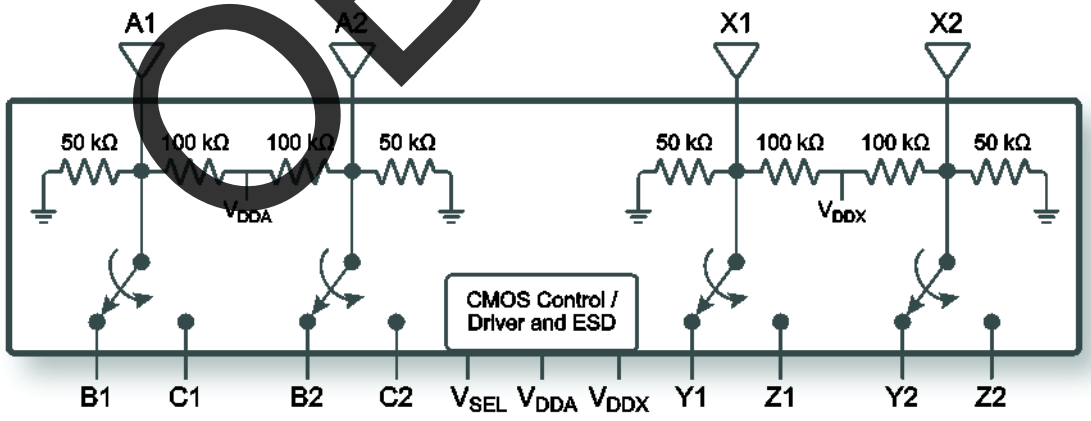


Figure 1. Functional Diagram



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Note: Differential pairs B1/B2 and Y1/Y2 must be switched simultaneously to pairs C1/C2 and Z1/Z2. See *Table 5*, Truth Table.

Table 1. Typical Specifications V_{DD} = 3.3V, Temp = +25 °C (Z_S = Z_L = 100Ω differential) Min/Max Specifications V_{DD} = 3.3V ±10%, –40 °C ≤ Temp ≤ +85 °C, (Z_S = Z_L = 100Ω differential)

AC coupled – external DC blocking caps

Electrical Parameter	Condition/Notes			Min	Typ	Max	Unit
Operating frequency	Frequency range			10 kHz		6 GHz	As shown
	Differential 3 dB bandwidth			5.6	6		GHz
Insertion loss at 10 kHz	V_{CM} = 1.1V				0.7	1.25	dB
Insertion loss at 1 GHz	V_{CM} = 1.1V				1.0	1.4	dB
Isolation between same channel inputs at 6 GHz	A to C when B is ON. A to B when C is ON X to Z when Y ON. X to Y when Z is ON			24	26		dB
Isolation between opposite (active) channels at 6 GHz	Channels A ↔ X. V_{CM} = 1.1V			25	30		dB
Input 1dB compression* (P_{1dB})	VCM = 1.1V, differential			10	13		dBm
Return loss common ports A and X	Differential	50–1250 MHz 1250–2500 MHz 2500–4000 MHz		12.5 8 5.5	14 9 8		dB dB dB
	Single ended	50–1250 MHz 1250–2500 MHz 2500–4000 MHz		14.5 12 10.5	17.5 14 13		dB dB
Return loss active ports B, C, Y, Z	Differential	50–1250 MHz 1250–2500 MHz 2500–4000 MHz		12.5 8.5 8	15.5 9.5 9.5		dB dB dB
	Single ended	50–1250 MHz 1250–2500 MHz 2500–4000 MHz		16 13 10.5	18.5 16 14.5		dB dB dB
Switching time	50% control to 10/90% RF				270	450	ns
Phase mismatch on matched paths at 6 GHz	V_{SEL} = 1 matched paths (A1 ↔ B1 & A2 ↔ B2) (X1 ↔ Y1 & X2 ↔ Y2)	V_{SEL} = 0 matched paths (A1 ↔ C1 & A2 ↔ C2) (X1 ↔ Z1 & X2 ↔ Z2)	V_{CM} = 1.1V		15	30	degrees
Phase mismatch on un-matched paths at 6 GHz	Unmatched: average of A1,A2 delay to average of X1,X2		V_{CM} = 1.1V		22	50	degrees
Phase delta stability	Across voltage and temperature					2	degrees
Common mode voltage	Common port self biased V_{CM} (V_{cm} ≈ V_{DD}/3)				1.1		V
Common mode impedance	Common port bias resistances	Z_{CM} to V_{DD} Z_{CM} to GND			100 50		kΩ kΩ
Input IP3	Single ended (see *Figure 19*)						dBm

Note: * P1dB is an indication of device linearity, max operating power is restricted to limits in *Table 3.*

Figure 3. Pin Configuration (Top View)

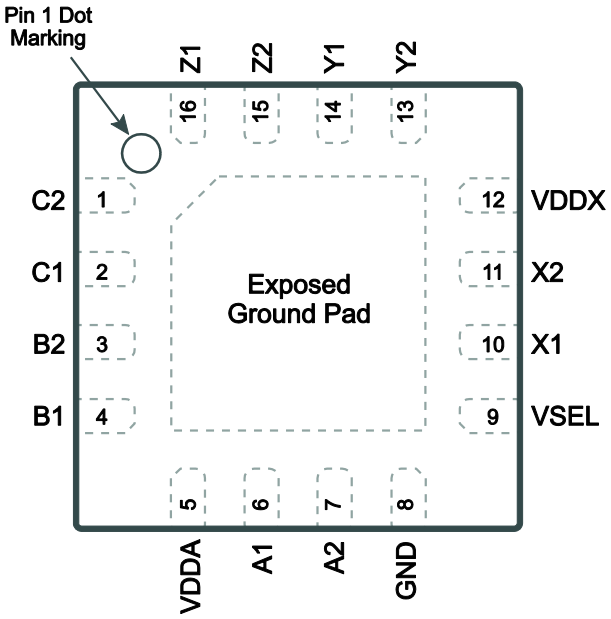


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	C2	C-channel [Logic Low] RF Port –
2	C1	C-channel [Logic Low] RF Port +
3	B2	B-channel [Logic High] RF Port –
4	B1	B-channel [Logic High] RF Port +
5	VDDA	A-channel Supply
6	A1	A-channel RF Common Port +
7	A2	A-channel RF Common Port –
8	GND	Ground
9	VSEL	Simultaneous Logic Select
10	X1	X-channel RF Common Port +
11	X2	X-channel RF Common Port –
12	VDDX	X-channel Supply
13	Y2	Y-channel [Logic High] RF Port –
14	Y1	Y-channel [Logic High] RF Port +
15	Z2	Z-channel [Logic Low] RF Port –
16	Z1	Z-channel [Logic Low] RF Port +
Paddle	GND	Exposed solder pad: Ground for proper operation

Table 3. Operating Ranges[2]

Parameter	Min	Typ	Max	Unit
V_{DD}[1] Power Supply Voltage	2.97	3.3	3.63	V
I_{DD} Supply Current		100	500	µA
T_{OP} Operating Temperature	–40		85	°C
P_{DC} DC Power Consumption			2	mW
V_{IH} V_{SEL} Control Voltage High	0.7xV_{DD}		V_{DD}	V
V_{IL} V_{SEL} Control Voltage Low	0		0.3xV_{DD}	V
I_{IH}/I_{IL} I_{SEL} Control Current – Input High/Low			1	µA
P_{MAX} Max. Input Power (100Ω Differential, Active Port)			10	dBm
P_{MAX} Max. Input Power (50Ω Single Ended, Active Port)			7	dBm
$V_{PEAK-TO-PEAK}$ Max. Input Differential (100Ω) Single Ended (50Ω)			2.8 1.4	V_{PP} V_{PP}

Notes: 1. Operating below min. V_{DD} results in degraded performance.
2. Operation should be restricted to the limits in the Operating Ranges table.

Table 4. Absolute Maximum Ratings

Parameter/Condition	Min	Max	Unit
P_{MAX} Max. Input Power (100Ω Differential, Active Port)		10	dBm
P_{MAX} Max. Input Power (50Ω Single Ended, Active Port)		7	dBm
V_{SEL} Control Voltage		4	V
I_{SW} DC Current on RF Path		5	mA
T_{ST} Storage Temperature	–65	+150	°C
V_{ESD} HBM ESD Voltage[1]		2000	V
V_{ESD} MM ESD Voltage[2]		100	V
$V_{PEAK-TO-PEAK}$ Max Input Differential (100Ω) Single Ended (50Ω)		2.8 1.4	V_{PP} V_{PP}

Notes: 1. HBM ESD Voltage (HBM, MIL_STD 883, Method 3015.7).
2. MM ESD Voltage (JESD22-A115-A).

Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42920 in the 16-lead 3 × 3 mm QFN package is MSL1.

Table 5. Truth Table: Signal-Path Control Logic

Path	Channel A		Channel X	
V_{SEL}	A→B	A→C	X→Y	X→Z
Low	OFF	ON	OFF	ON
High	ON	OFF	ON	OFF

A = Differential pair A1/A2 B = Differential pair B1/B2
C = Differential pair C1/C2 X = Differential pair X1/X2
Y = Differential pair Y1/Y2 Z = Differential pair Z1/Z2

Typical Performance Data @ 3.3V and +25 °C, unless otherwise specified

Figure 4. Differential Insertion Loss over V_{DD}

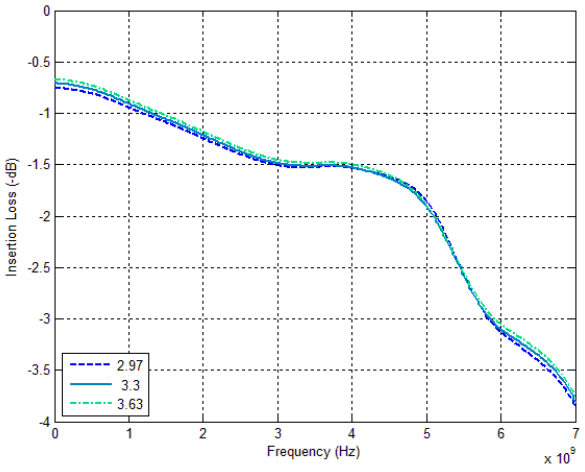


Figure 5. Differential Insertion Loss over Temp

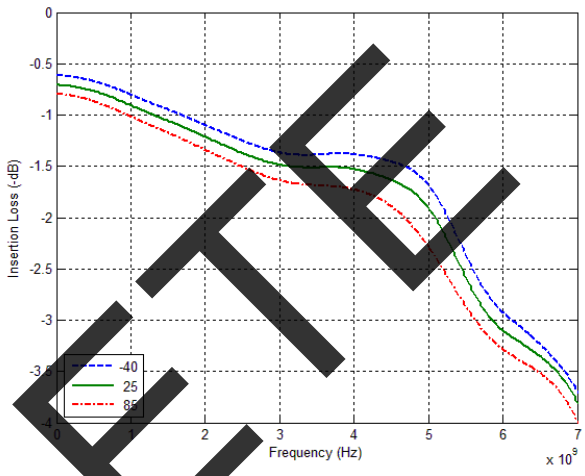


Figure 6. Differential Active Port (B, C, Y, or Z) Return Loss over V_{DD}

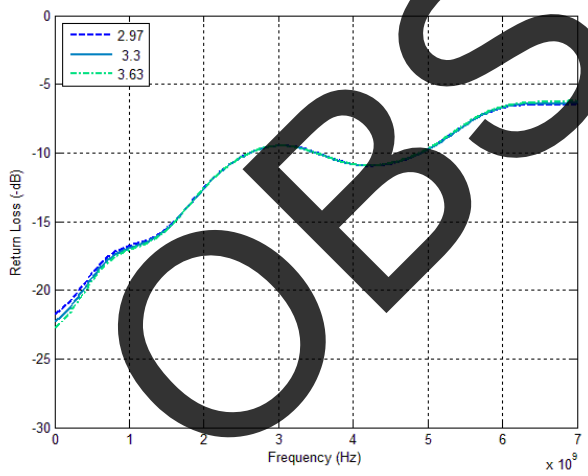
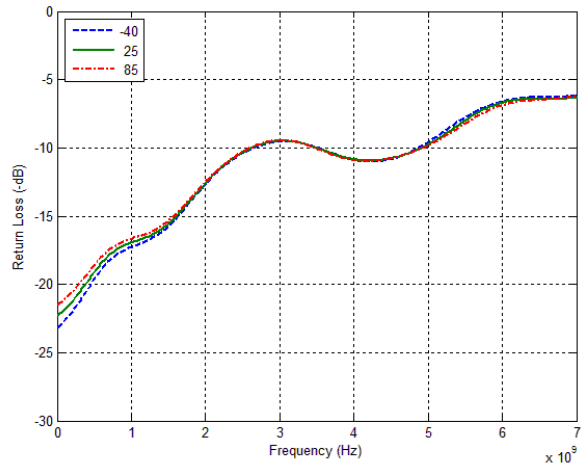


Figure 7. Differential Active Port (B, C, Y, or Z) Return Loss over Temp



Typical Performance Data @ 3.3V and +25 °C, unless otherwise specified

Figure 8. Differential Common Port (A or X) Return Loss over V_{DD}

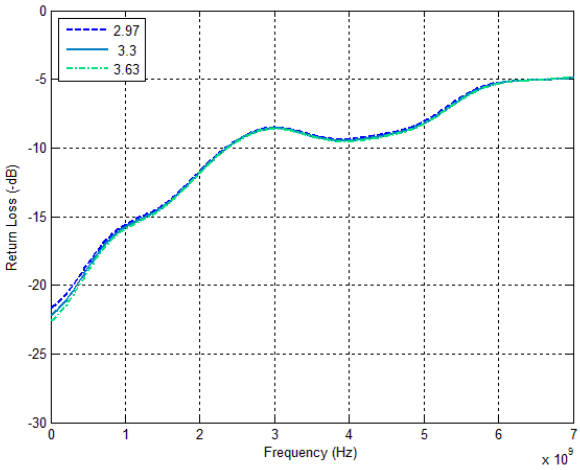


Figure 9. Differential Common Port (A or X) Return Loss over Temp

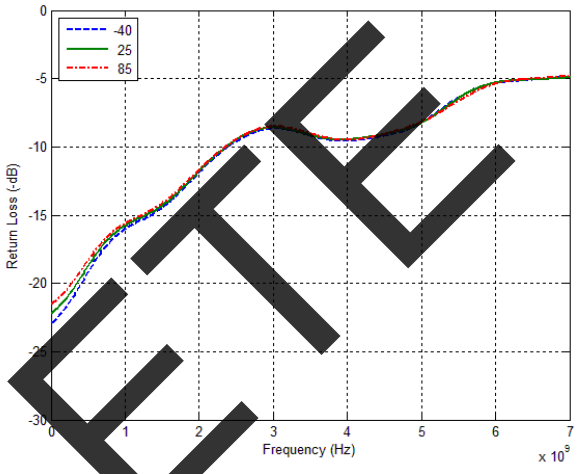


Figure 10. Single-Ended Active Port (B1, B2, C1, C2, Y1, Y2) Return Loss over V_{DD}

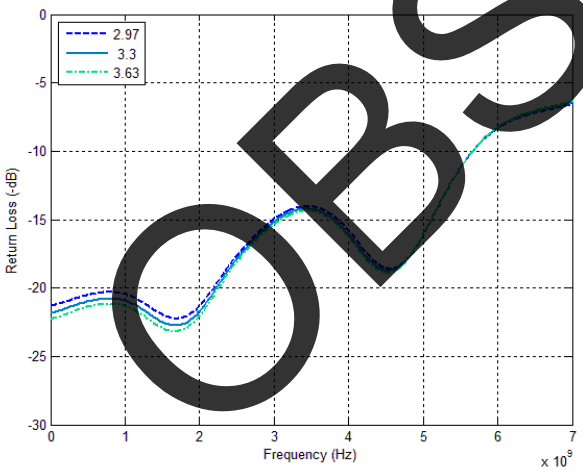
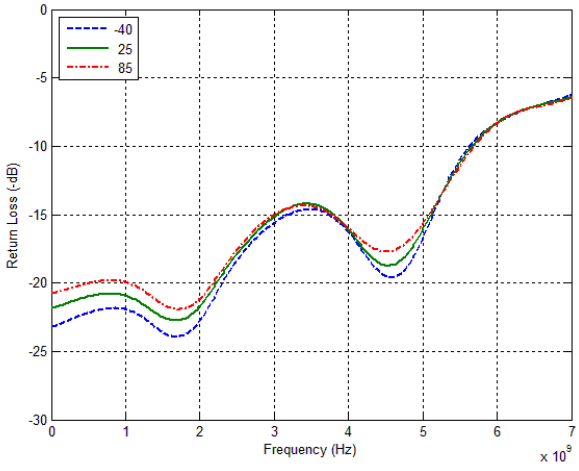


Figure 11. Single-Ended Active Port (B1, B2, C1, C2, Y1, Y2) Return Loss over Temp



Typical Performance Data @ 3.3V and +25 °C, unless otherwise specified (cont.)

Figure 12. Single-Ended Common Port (A1, A2, X1, X2) Return Loss over V_{DD}

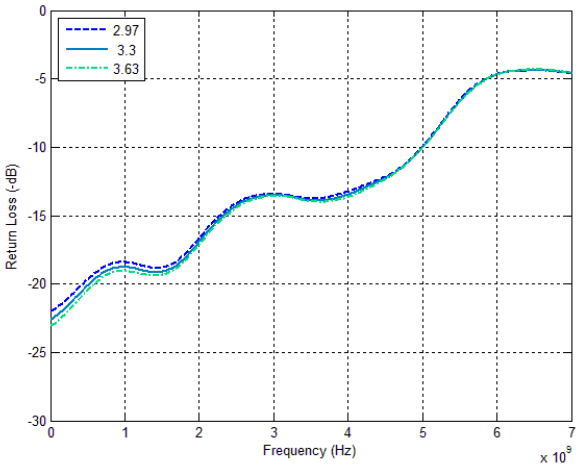


Figure 13. Single-Ended Common Port (A1, A2, X1, X2) Return Loss over Temp

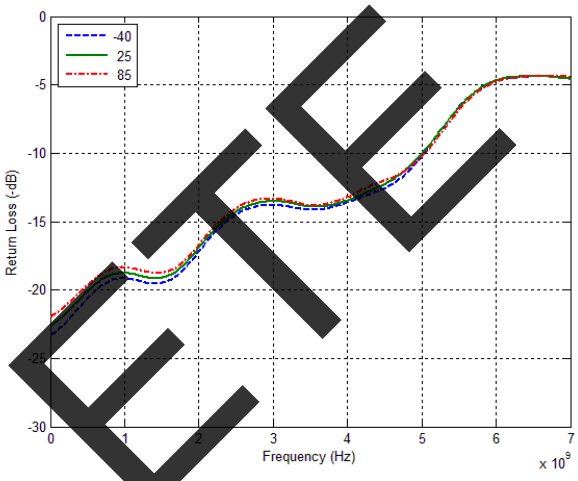


Figure 14. Opposite Channel (A to X) Isolation over V_{DD}

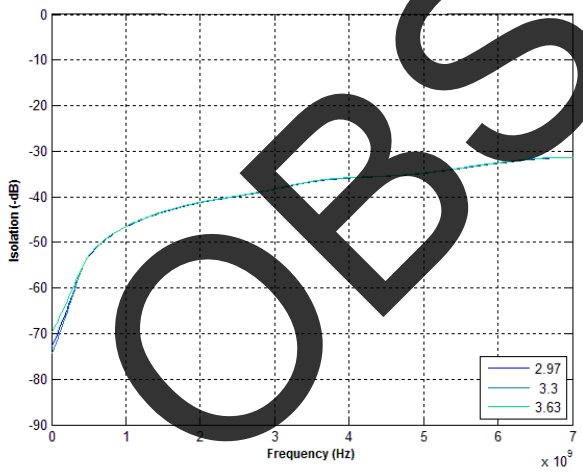
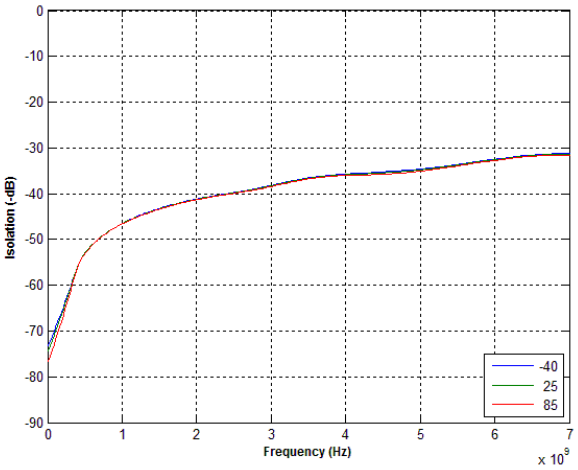


Figure 15. Opposite Channel (A to X) Isolation over Temp



Typical Performance Data @ 3.3V and +25 °C, unless otherwise specified (cont.)

Figure 16. Same Channel (A to B/C and X to Y/Z) Isolation over V_{DD}

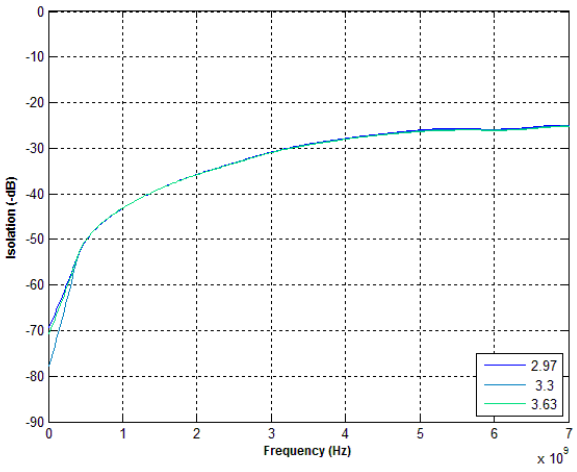


Figure 17. Same Channel (A to B/C and X to Y/Z) Isolation over Temp

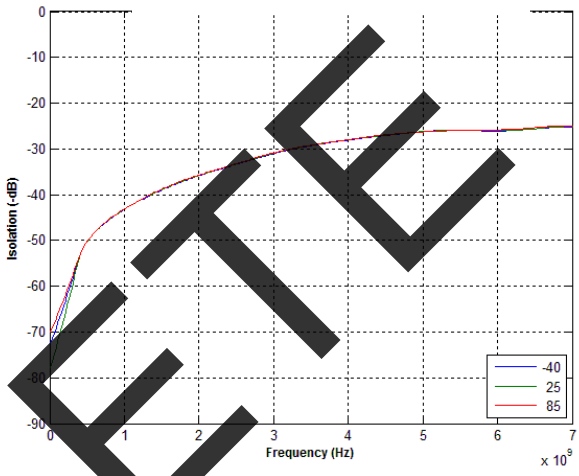


Figure 18. Switching Time (10/90% RF)

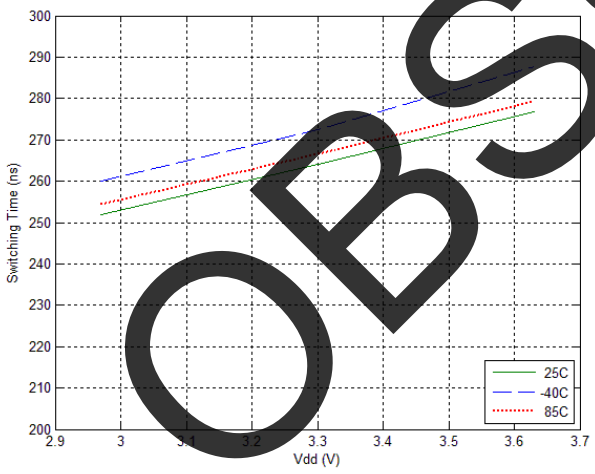


Figure 19. IIP3 (Single Ended)

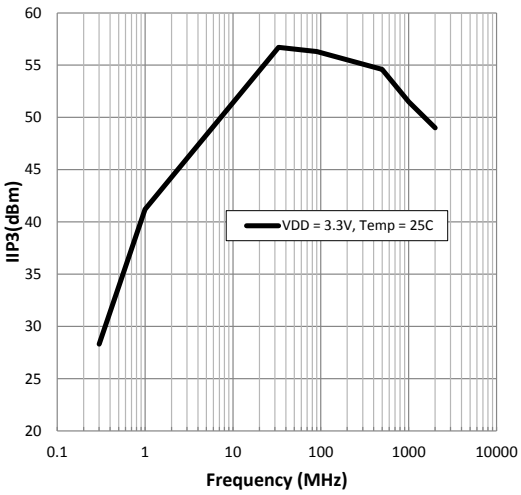


Figure 20. Phase Delta Matched Paths (6 GHz and +25 °C) Stability Across V_{DD}

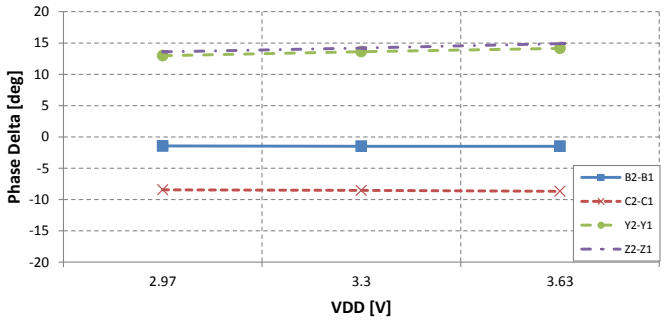


Figure 21. Phase Delta Matched Paths (6 GHz and 3.3V) Stability Across Temp

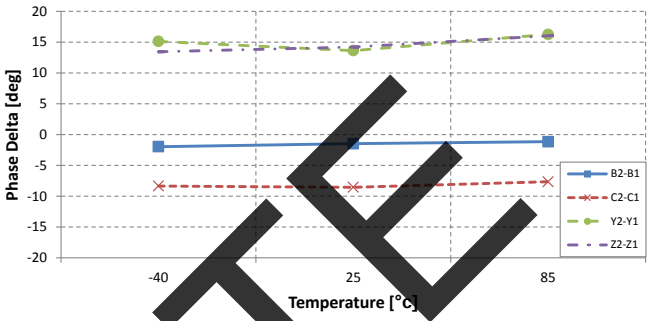


Figure 22. Phase Delta Un-matched Paths (6 GHz and +25 °C) Stability Across V_{DD}

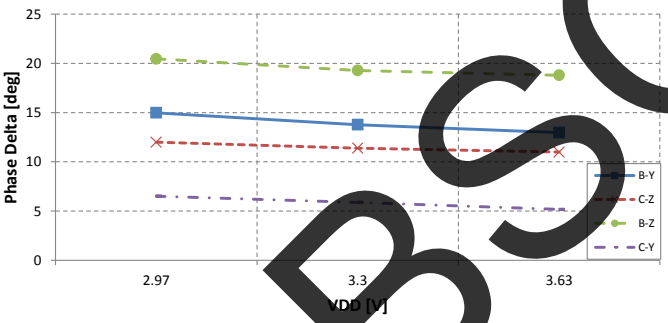
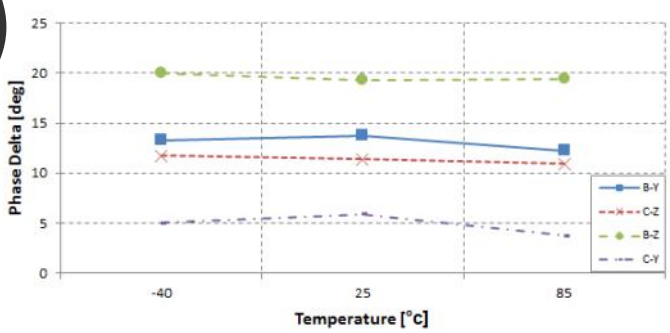


Figure 23. Phase Delta Un-matched Paths (6 GHz and 3.3V) Stability Across Temp



Evaluation board

The DDSPDT switch evaluation kit board was designed to ease customer evaluation of the PE42920 DDSPDT switch.

Calibration structures are available on the bottom side of the PCB. As an alternate connector option, a through transmission line connects connectors J14 and J13. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

J20 provides a means for applying V_{DD} and controlling the logic of the device. A jumper can be used to set AUX = V_{DD} or AUX = GND,* to toggle the logic state.

Proper PCB design is essential for full isolation performance. This evaluation board demonstrates good trace and ground management for minimum coupling and radiation.

DC blocking capacitors (external or on board) are required to prevent interaction with external test equipment. They can be used as external broadband DC blocks or replace 0Ω resistors on board with the desired capacitance value on operation frequency.

Note: * Silkscreen Error – AUX and V_{SEL} labels are swapped. AUX jumper pin on J20 header is equivalent to the V_{SEL} control in the block diagram. V_{SEL} jumper pin on J20 header is a no connect.

Figure 24. Evaluation Board Layouts

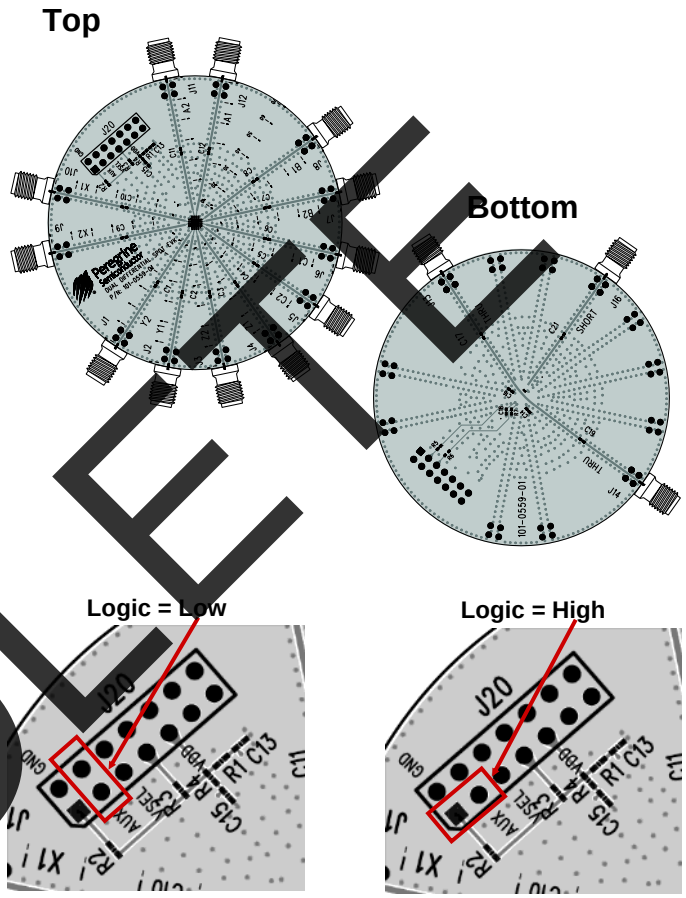


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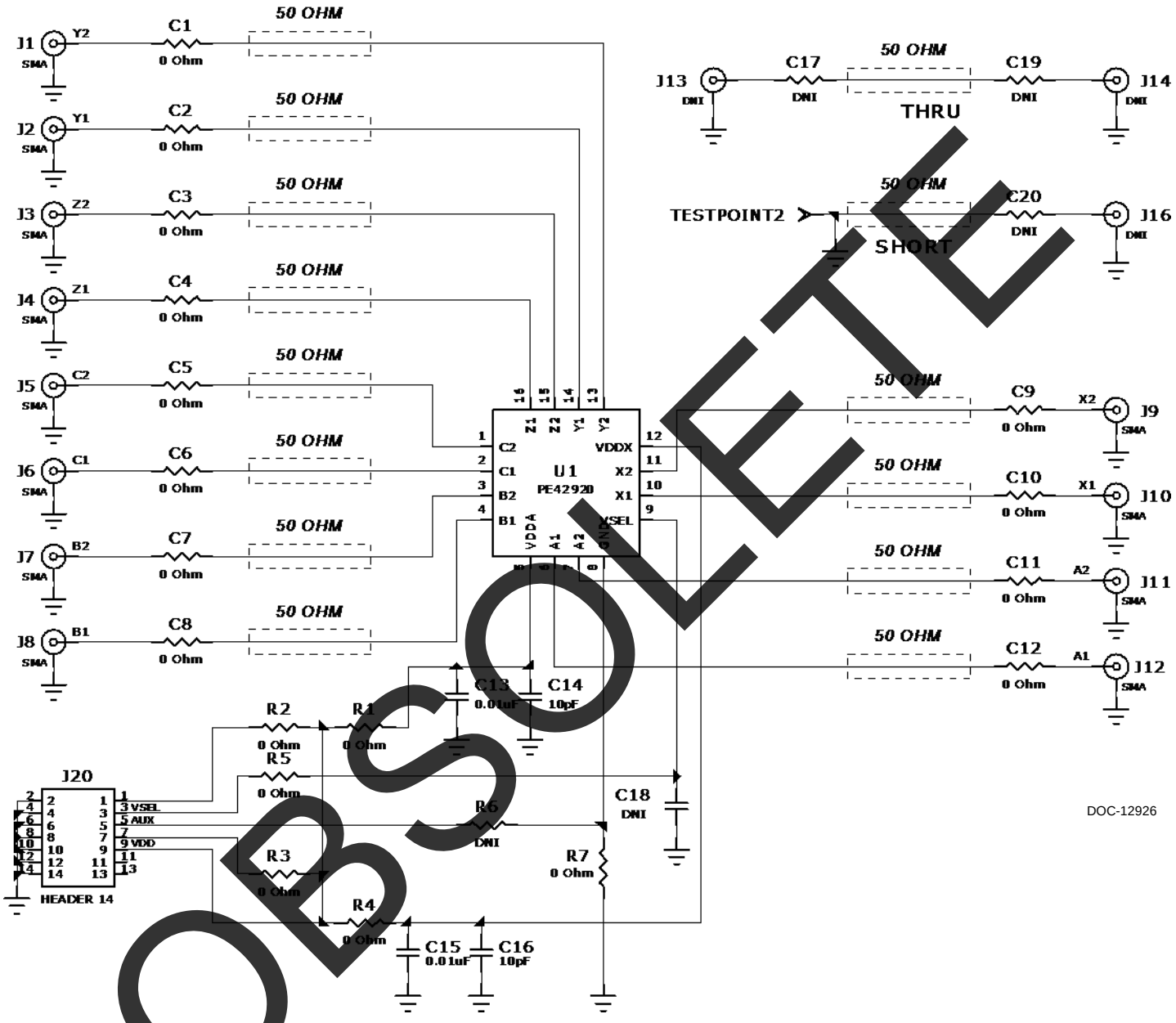
Figure 25. Evaluation Board Schematic[1,2,3]



Notes: 1. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).
2. Silkscreen error: AUX and VSEL labels are swapped on PCB at J20 location.
3. Pin 8 is grounded in PE42920.

Figure 26. Package Drawing
16-lead 3 × 3 mm QFN

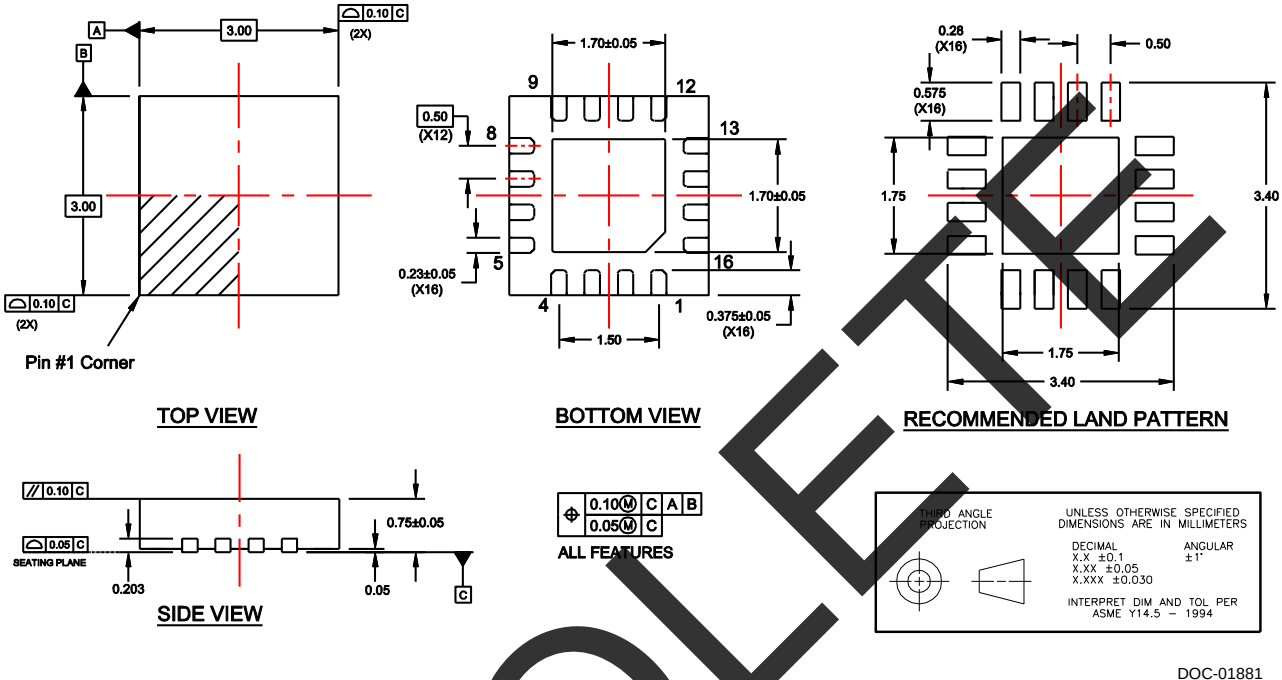


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Figure 27. Top Marking Specification

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZ = Assembly lot code (maximum five characters)

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