PE45361

Document Category: Product Specification

UltraCMOS® Power Limiter, 10 MHz–8 GHz

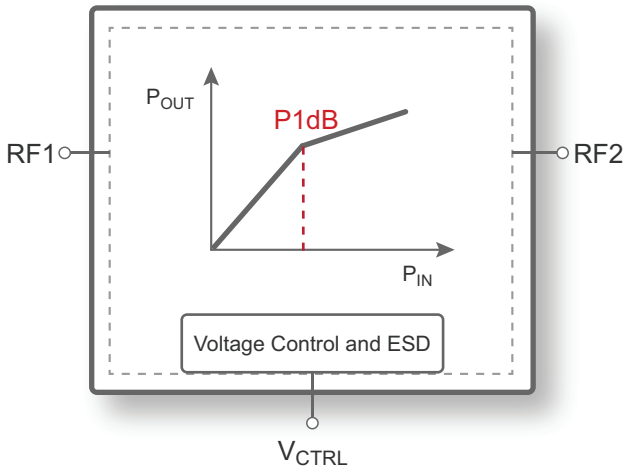
Features

- Monolithic drop-in solution with no external bias components
- Adjustable low power limiting threshold from +7 dBm to +13 dBm
- High maximum power handling of 50 dBm, 100W pulsed
- Positive threshold control from +0V to +0.3V
- Fast response time of less than 1 ns
- Packaging – 12-lead 3 × 3 × 0.5 mm QFN

Applications

- Wireless infrastructure transceivers and antennas
- Test and measurement (T&M)

Figure 1 ▪ PE45361 Functional Diagram



Product Description

The PE45361 is a HaRP™ technology-enhanced power limiter designed for use in high performance power limiting applications in test and measurement equipment and wireless infrastructure transceivers and antennas.

Unlike traditional PIN diode solutions, the PE45361 achieves an adjustable input 1dB compression point or limiting threshold via a low current control voltage (V_{CTRL}), eliminating the need for external bias components such as DC blocking capacitors, RF choke inductors and bias resistors.

It delivers low insertion loss and high linearity under non-limiting power levels and extremely fast response time in a limiting event, ensuring protection of sensitive circuitry. It also offers excellent ESD rating and ESD protection.

The PE45361 is manufactured on pSemi's UltraCMOS® process, a patented advanced form of silicon-on-insulator (SOI) technology, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ▪ Absolute Maximum Ratings for PE45361

Parameter/Condition	Min	Max	Unit
Control voltage, V_{CTRL} Power limiting mode	0	3.6	V
RF input power, Pulsed[1]		50	dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins[2]		7000	V
ESD voltage CDM, all pins[3]		2000	V

Notes:
1) Pulsed, 1.0% duty cycle of 10 µs pulse width in 1 ms period, 50Ω at +25 °C.
2) Human body model (MIL-STD 883 Method 3015).
3) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE45361. Devices should not be operated outside the operating conditions listed below.

Table 2 ▪ Recommended Operating Conditions for PE45361

Parameter	Min	Typ	Max	Unit
Control voltage, V_{CTRL}				
Power limiting mode	0		+0.3	V
Power reflecting mode	0		+3.0	V
RF input power, CW(*)			**Fig. 2**	dBm
Operating temperature range	–55	+25	+105	°C
Operating max junction temperature			+150	°C

Note: * See **Fig. 2**.

Electrical Specifications

Table 3 provides the PE45361 key electrical specifications at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3 ▪ PE45361 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency		10 MHz		8 GHz	As shown
Power Limiting Mode					
Insertion loss	10 MHz–3000 MHz 3001–6000 MHz 6001–8000 MHz		0.40 0.95 1.32	0.50 1.20 1.70	dB dB dB
Return loss	10 MHz–3000 MHz 3001–6000 MHz 6001–8000 MHz		22 12 9.5		dB dB dB
P1dB/limiting threshold	V_{CTRL} = 0V @ 915 MHz V_{CTRL} = +0.15V @ 915 MHz V_{CTRL} = +0.3V @ 915 MHz		13 10 7		dBm dBm dBm
	V_{CTRL} = 0V @ 8 GHz V_{CTRL} = +0.15V @ 8 GHz V_{CTRL} = +0.3V @ 8 GHz		9 8 7		dBm dBm dBm
Leakage power(1)	V_{CTRL} = 0V @ 915 MHz, P_{CW} = 30 dBm V_{CTRL} = +0.15V @ 915 MHz, P_{CW} = 30 dBm V_{CTRL} = +0.3V @ 915 MHz, P_{CW} = 30 dBm		16 15 13	16.8 15.9 14.7	dBm dBm dBm
Input IP2	V_{CTRL} = 0V @ 915 MHz V_{CTRL} = 0V @ 6 GHz V_{CTRL} = 0V @ 8 GHz		88 70 70		dBm dBm dBm
Input IP3	V_{CTRL} = 0V @ 915 MHz V_{CTRL} = 0V @ 6 GHz V_{CTRL} = 0V @ 8 GHz		37 31 30		dBm dBm dBm
Response time	1 GHz		1		ns
Recovery time(4)	1 GHz, P_{IN}, pulse = 30 dBm		1		ns
Power Reflecting Mode(2)					
Leakage power(1)	V_{CTRL} = +3.0V @ 915 MHz, P_{CW} = 30 dBm V_{CTRL} = +3.0V @ 8 GHz, P_{CW} = 30 dBm		–41 –20	–39 –19	dBm dBm
Switching time(3)	State change to 10% RF		3		µs

Table 3 ▪ PE45361 Electrical Specifications (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
Notes: 1) Measured with +30 dBm CW applied at input. 2) This mode requires the control voltage to toggle between +3.0V and 0V. At +3.0V, the limiter equivalent circuit is a low impedance to ground, reflecting most of the incident power back to the source. 3) State change is V_{CTRL} toggle from 0V to +3.0V. 4) Pulsed, 1% duty cycle of 10 µs pulse width in 1 ms period, 50Ω @ +25 °C.					

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$\Psi_{JT} = (T_J - T_T)/P$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

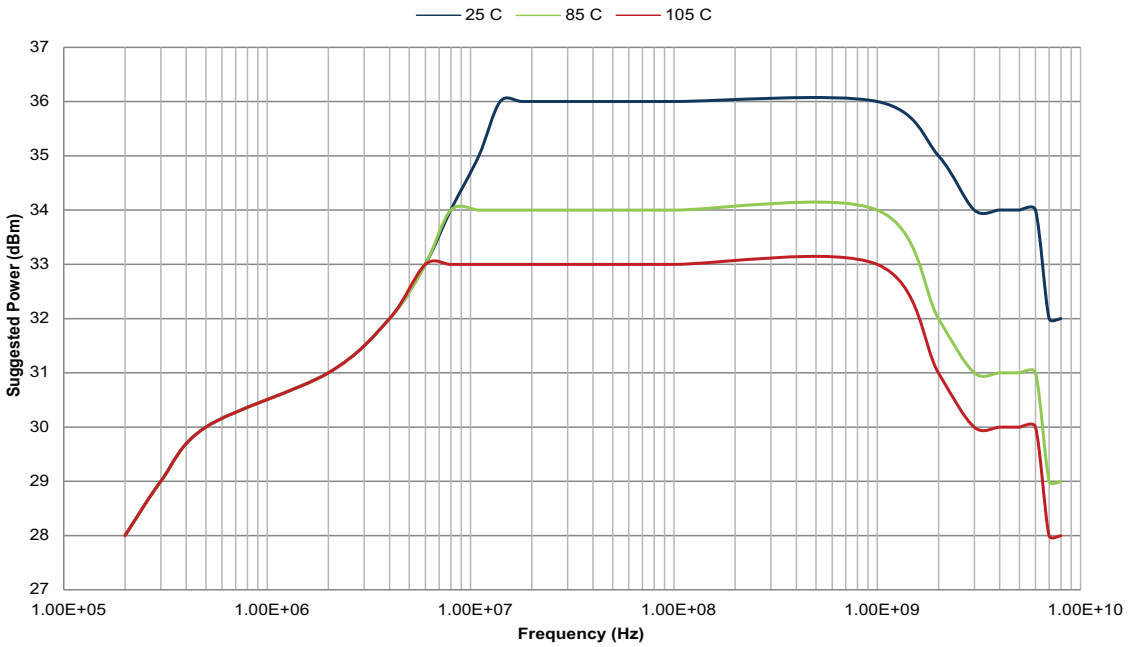
Table 4 ▪ Thermal Data for PE45361

Parameter	Typ	Unit
Ψ_{JT}	35	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	73	°C/W

Power De-rating Curve

Figure 2 shows the power de-rating curve indicating maximum allowable operating RF input power (CW) up to the part's maximum operating ambient temperature of +105 °C. This RF input power maintains the maximum operating junction temperature requirement of +150 °C.

Figure 2 ▪ Power De-rating Curve, 10 MHz–8 GHz, +25 °C to +105 °C Ambient, CW, 50Ω



Dual Mode Operation

Power Limiting Mode

The PE45361 performs as a linear power limiter with adjustable P1dB/limiting threshold. The P1dB/limiting threshold can be adjusted by changing the control voltage between 0V and +0.3V. If unbiased, or if V_{CTRL} = 0V, the PE45361 still offers power limiting protection.

Power Reflecting Mode

Power reflecting mode requires a power detector to sample the RF input power and a microcontroller to toggle the limiter control voltage between +3.0V and 0V based on the system protection requirements. At +3.0V, the limiter impedance to ground is less than 1Ω and most of the incident power will be reflected back to the source. At 0V, the device operates as in power limiting mode.

Typical Performance Data

Fig. 3–Figure 16 show the typical performance data at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified.

Figure 3 ▪ Insertion Loss vs Temp

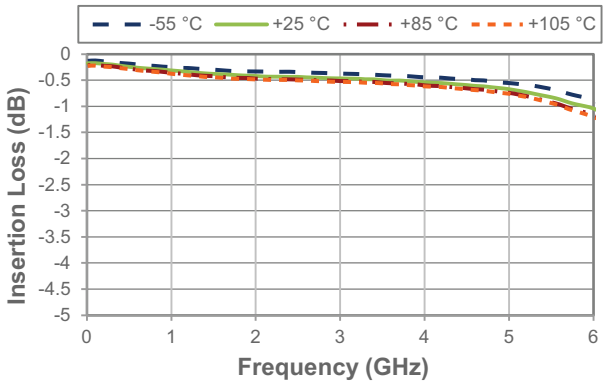


Figure 4 ▪ Input Return Loss vs Temp

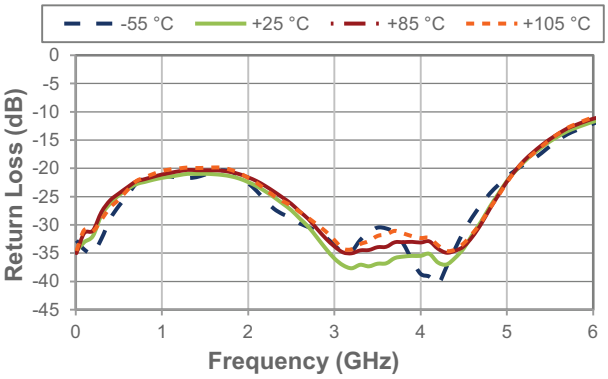


Figure 5 ▪ Output Return Loss vs Temp

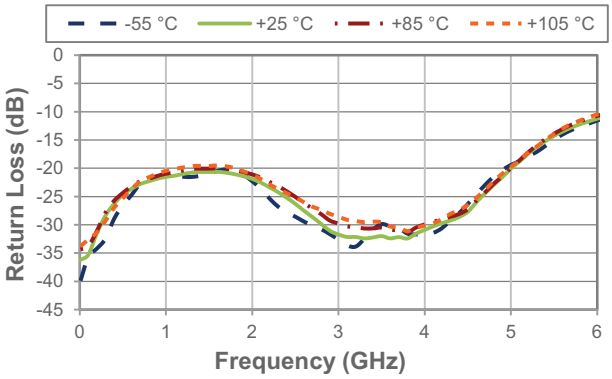


Figure 6 ▪ P_{OUT} vs P_{IN} Over V_{CTRL} (Limiting Mode @ 915 MHz)

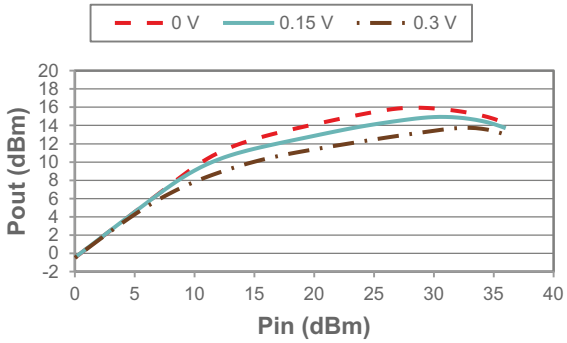


Figure 7 ▪ P_{OUT} vs P_{IN} Over V_{CTRL} (Limiting Mode @ 6 GHz)

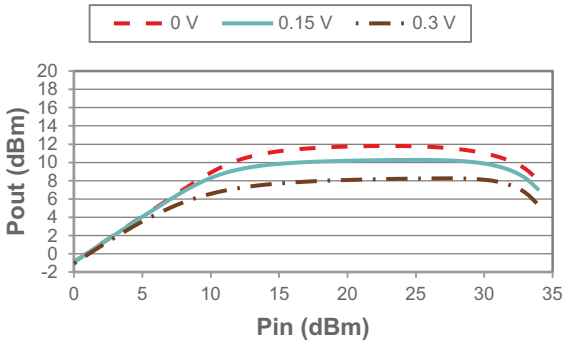


Figure 8 ▪ P1dB vs V_{CTRL} Over Temp @ 915 MHz

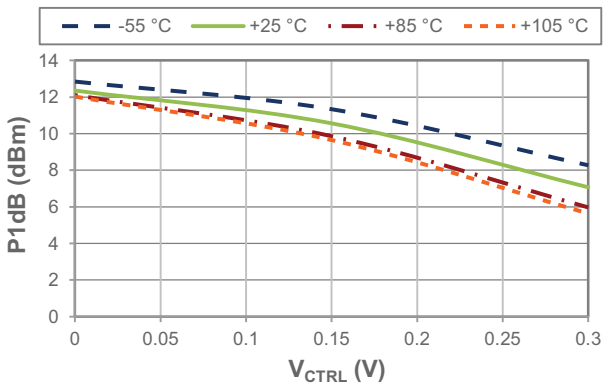


Figure 9 ▪ P_{OUT} vs P_{IN} Over V_{CTRL} (Reflecting Mode @ 915 MHz)

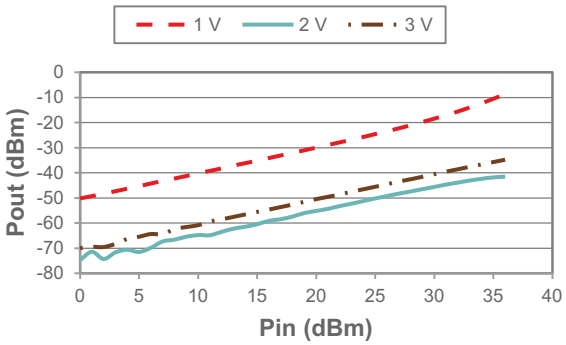


Figure 10 ▪ P_{OUT} vs P_{IN} Over V_{CTRL} (Reflecting Mode @ 6 GHz)

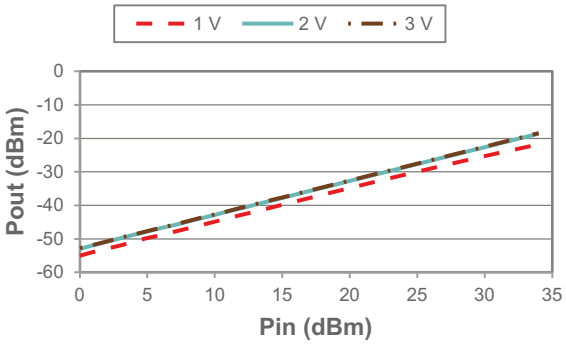


Figure 11 ▪ P1dB vs V_{CTRL} Over Temp @ 6 GHz

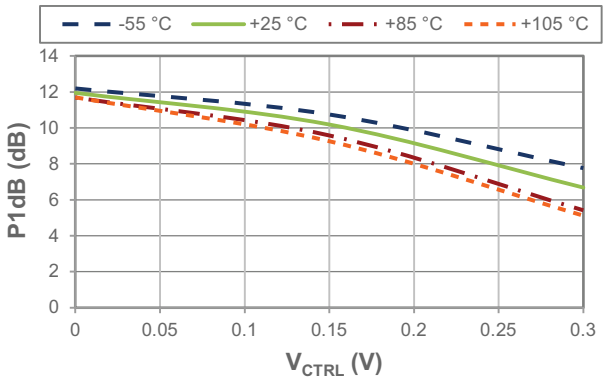


Figure 12 ▪ Leakage Power @ P_{MAX} vs V_{CTRL} Over Temp @ 915 MHz

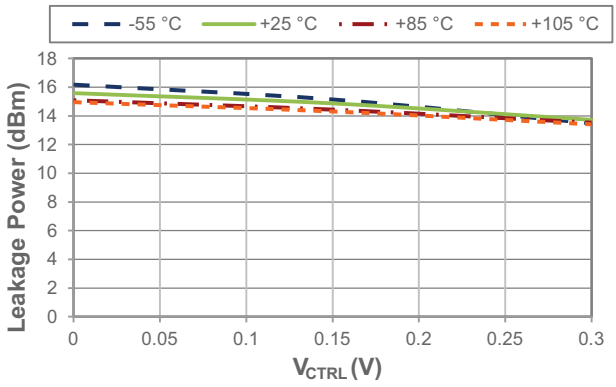


Figure 13 ▪ IIP2/IIP3 vs P_{IN} Over V_{CTRL} @ 915 MHz

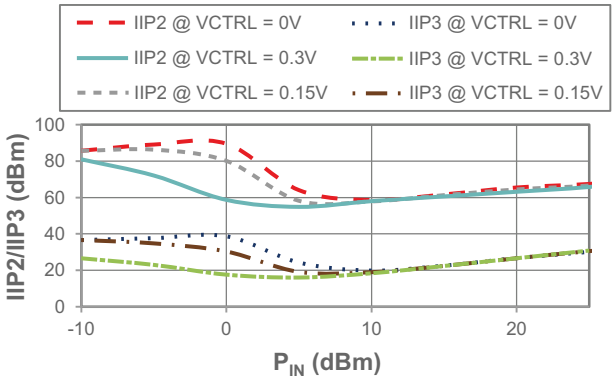


Figure 14 ▪ IIP2/IIP3 vs V_{CTRL} Over P_{IN} @ 915 MHz

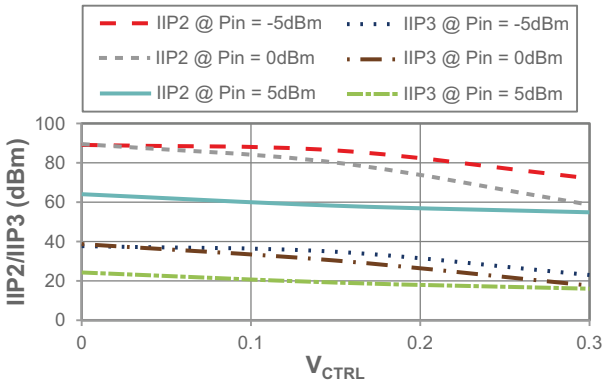


Figure 15 ▪ Leakage Power @ P_{MAX} vs V_{CTRL} Over Temp @ 6 GHz

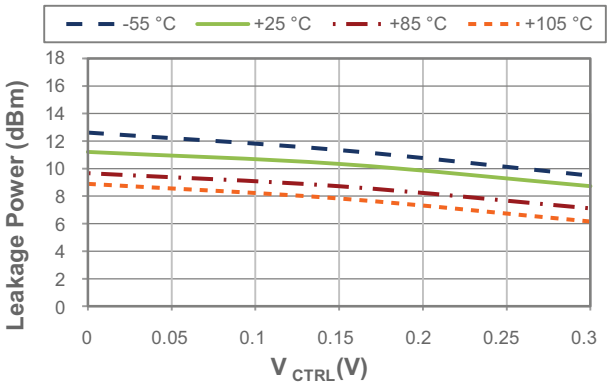


Figure 16 ▪ IIP2/IIP3 vs P_{IN} Over V_{CTRL} @ 6 GHz

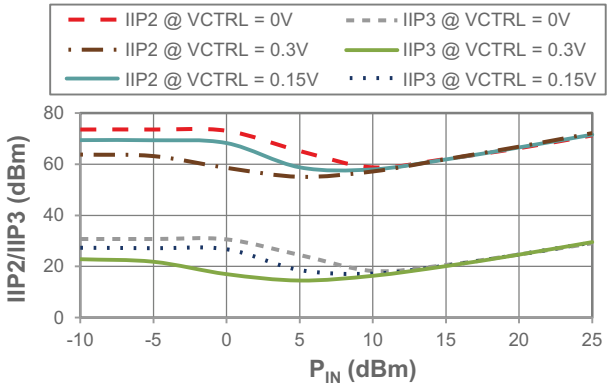
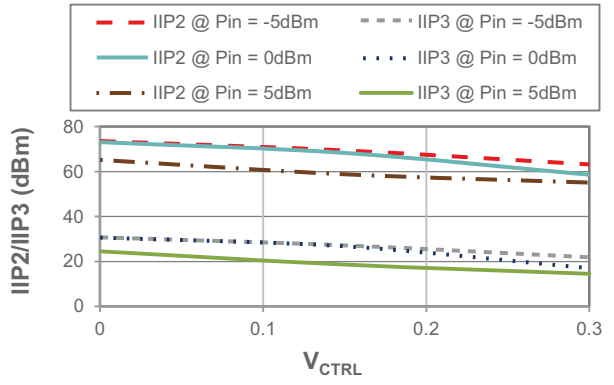


Figure 17 ▪ IIP2/IIP3 vs V_{CTRL} Over P_{IN} @ 6 GHz

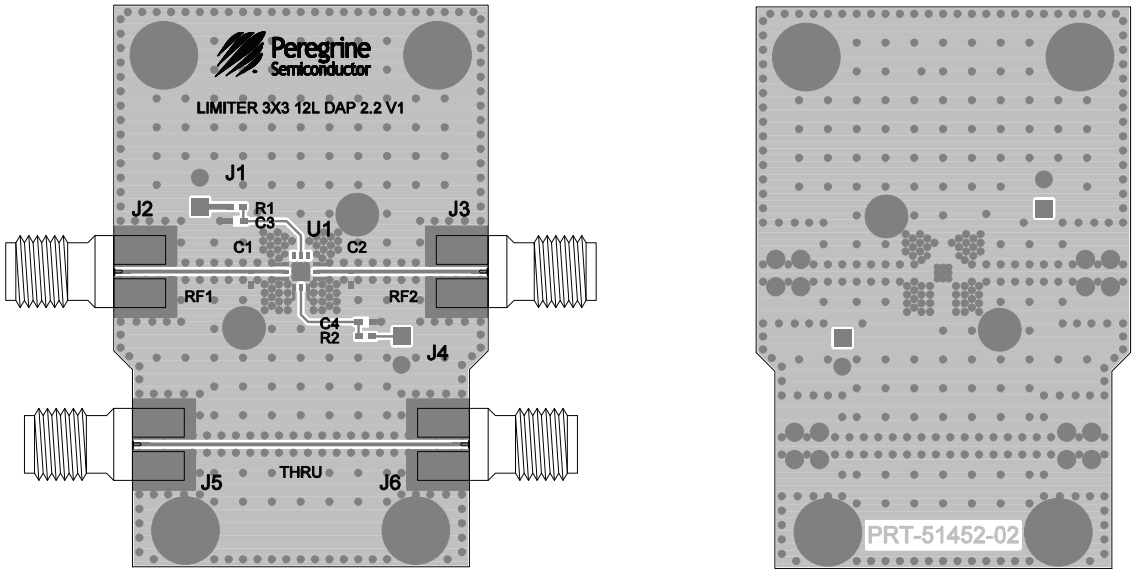


Evaluation Kit

The power limiter evaluation kit board (EVB) was designed to ease customer evaluation of pSemi's PE45361. The uni-directional RF input and output are connected to the RF1 and RF2 port through a 50Ω transmission line via SMA connectors J2 and J3. A through 50Ω transmission line is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. The 2-pin connector J4 is connected to the external bias V_{CTRL}.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers RO4350B material with a 6.6 mil RF core and ε_R = 3.66. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 13.5 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

Figure 18 ▪ Evaluation Kit Layout for PE45361



Pin Information

This section provides pinout information for the PE45361. **Figure 19** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

Figure 19 ▪ Pin Configuration (Top View)

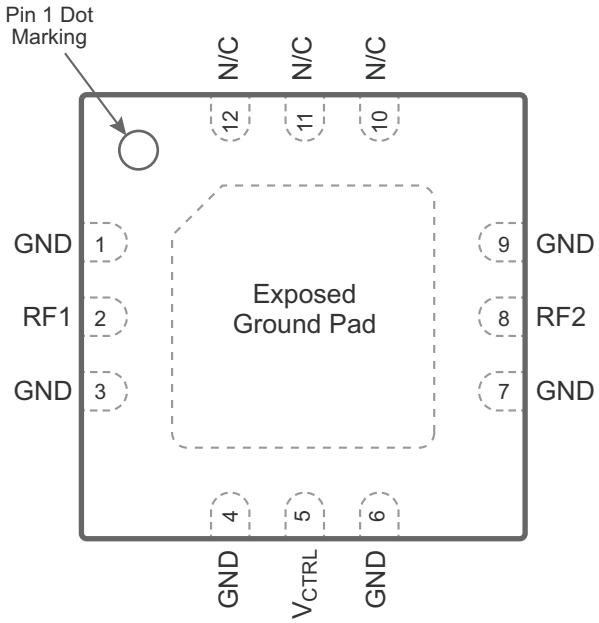


Table 5 ▪ Pin Descriptions for PE45361

Pin No.	Pin Name	Description
1, 3, 4, 6, 7, 9	GND	Ground
2	RF1[(1)(3)]	RF port 1
5	V_{CTRL}	Control voltage
8	RF2[(1)(3)]	RF port 2
10–12	N/C[(2)]	No connect
Pad	GND	Exposed pad: ground for proper operation

Notes:

1) RF pins 2 and 8 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) Pins 10–12 can be grounded if deemed necessary by the customer.
3) The limiter is not bi-directional. RF1 is the RF input and RF2 is the RF output.

Packaging Information

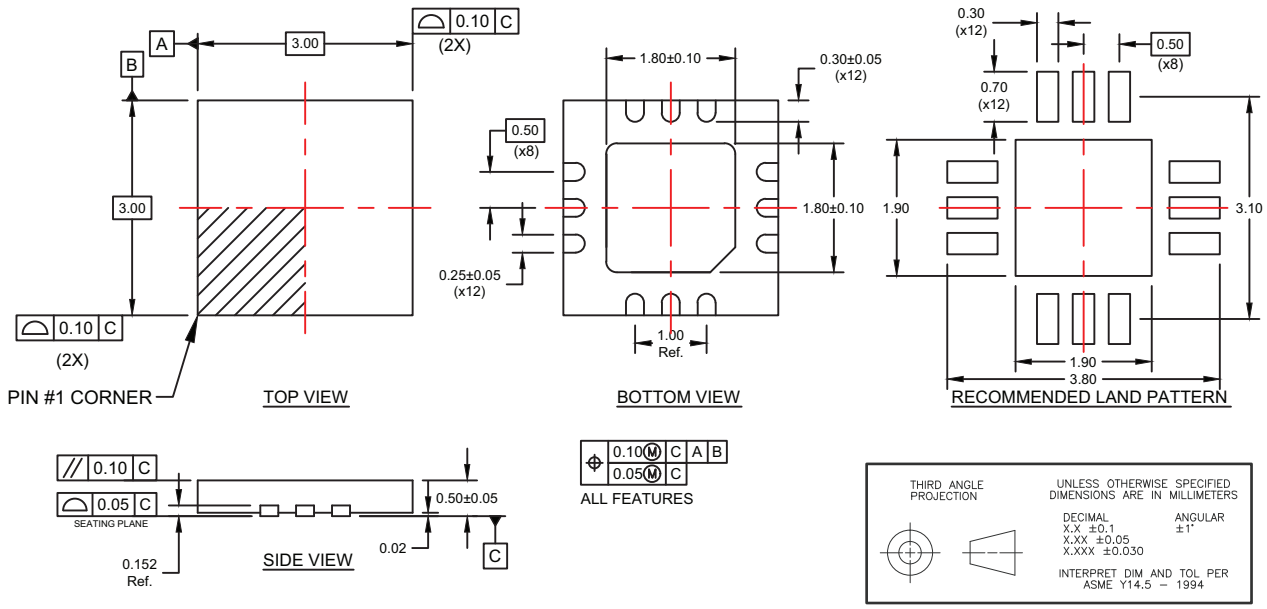
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE45361 in the 12-lead 3 × 3 × 0.5 mm QFN package is MSL1.

Package Drawing

Figure 20 ▪ Package Mechanical Drawing for 12-lead 3 × 3 × 0.5 mm QFN



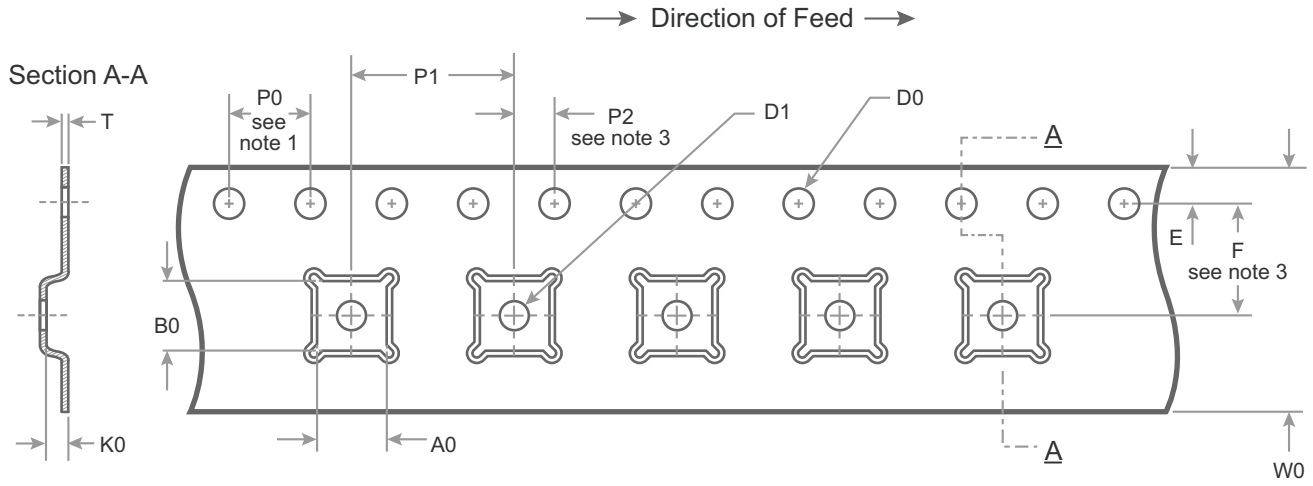
Top-Marking Specification

Figure 21 ▪ Package Marking Specifications for PE45361

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

Figure 22 ▪ Tape and Reel Specifications for 12-lead 3 × 3 × 0.5 mm QFN

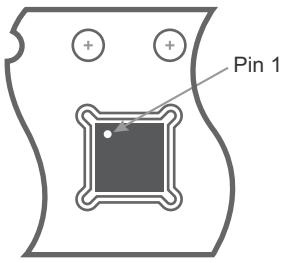


A0	3.3
B0	3.3
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in milimeters unless otherwise specified



Device Orientation in Tape