Product Specification

PE64904

UltraCMOS® Digitally Tunable Capacitor (DTC) 100 - 3000 MHz

Features

- 3-wire (SPI compatible) Serial Interface with built-in bias voltage generation and ESD protection
- DuNE™-enhanced UltraCMOS® device
- 5-bit 32-state Digitally Tunable Capacitor
- Series configuration C = 0.60 - 4.60 pF (7.7:1 tuning ratio) in discrete 129 fF steps
- Shunt configuration C = 1.14 - 5.10 pF (4.6:1 tuning ratio) in discrete 129 fF steps
- High RF Power Handling (up to 38 dBm, 30 V_{pk} RF) and High Linearity
- Wide power supply range (2.3 to 3.6V) and low current consumption (typ. 140 µA at 2.6V)
- Excellent 1.5 kV HBM ESD tolerance on all pins
- 2 x 2 x 0.45 mm QFN package
- Applications include:
  - Tunable Filter Networks
  - Tunable Antennas
  - RFID
  - Tunable Matching Networks
  - Phase Shifters
  - Wireless Communications

Product Description

The PE64904 is a DuNE™-enhanced Digitally Tunable Capacitor (DTC) based on Peregrine's UltraCMOS® technology. DTC products provide a monolithically integrated impedance tuning solution for demanding RF applications.

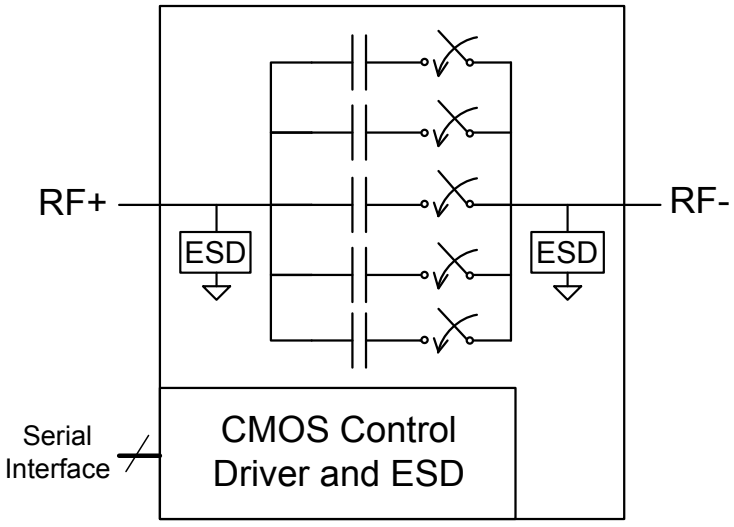
The PE64904 offers high RF power handling and ruggedness, while meeting challenging harmonic and linearity requirements.

This highly versatile product can be used in series or shunt configurations to support a wide variety of tuning circuit topologies.

The device is controlled through the widely supported 3-wire (SPI compatible) interface. All decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

Peregrine's DuNE™ technology enables excellent linearity and exceptional harmonic performance. DuNE devices deliver performance superior to GaAs devices with the economy and integration of conventional CMOS.

Figure 1. Functional Block Diagram



71-0066-01

Figure 2. Package Type

10L 2 x 2 x 0.45 mm QFN package

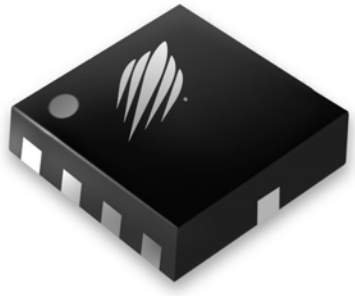


Table 1. Electrical Specifications @ 25°C, V_{DD} = 2.6V

Parameter	Configuration	Condition	Min	Typ	Max	Units
Operating Frequency Range	Both		100		3000	MHz
Minimum Capacitance	Series Shunt	State = 00000, 100 MHz (RF+ to RF-) State = 00000, 100 MHz (RF+ to Grounded RF-)	0.49 0.90	0.60 1.10	0.71 1.30	pF
Maximum Capacitance	Series Shunt	State = 11111, 100 MHz (RF+ to RF-) State = 11111, 100 MHz (RF+ to Grounded RF-)	3.78 4.19	4.60 5.10	5.45 6.00	pF
Parasitic Capacitance	Series	All States, 100 MHz (RF+ to GND, RF- to GND)		0.5		pF
Tuning Ratio	Series Shunt	100 MHz 100 MHz		7.7:1 4.6:1		
Step Size	Both	5 bits (32 states), constant step size (100 MHz)		0.129		pF
Equivalent Series Resistance	Series	State = 00000 State = 11111		1.40 1.33		Ω
Quality Factor (C_{min})[1]	Shunt	100 MHz, with L_s removed 1 GHz, with L_s removed 2 GHz, with L_s removed 3 GHz, with L_s removed		10 35 32 25		
Quality Factor (C_{max})[1]	Shunt	100 MHz, with L_s removed 1 GHz, with L_s removed 2 GHz, with L_s removed 3 GHz, with L_s removed		27 25 11 6		
Self Resonant Frequency	Shunt	State 00000 State 11111		7.5 3.1		GHz
Harmonics (2fo)[2]	Series	100 MHz - 3 GHz			-36	dBm
Harmonics (3fo)[2]		100 MHz - 3 GHz			-36	dBm
Input Intercept Point (2nd Order)	Series	100 MHz - 3 GHz, +18 dBm per tone, 1 MHz Spacing		105		dBm
Input Intercept Point (3rd Order)	Series	100 MHz - 3 GHz, +18 dBm per tone, 1 MHz Spacing		65		dBm
Switching Time[3, 4]	Both	50% CTRL to 10/90% delta capacitance between any two states			12	µs
Start-up Time[3]	Both	Time from V_{DD} within specification to all performances within specification			100	µs
Wake-up Time[3, 4]	Both	State change from standby mode to RF state to all performances within specification			100	µs

Notes: 1. Q for a Shunt DTC based on a Series RLC equivalent circuit.
$Q = X_C/R = (X-X_L)/R$, where $X = X_L+X_C$, $X_L = 2*pi*f*L$, $X_C = -1/(2*pi*f*C)$, which is equal to removing the effect of parasitic inductance L_S.
2. In series or shunt between 50 Ω ports. Pulsed RF input with 4620 µs period, 50% duty cycle, measured per 3GPP TS 45.005.
3. DC path to ground at RF+ and RF- must be provided to achieve specified performance.
4. State change activated on falling edge of SEN following data word.

Figure 3. Pin Configuration (Top View)

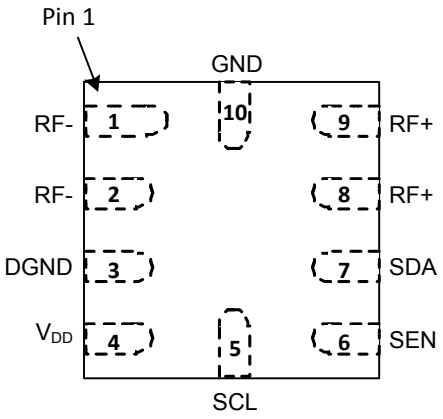


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	RF-	Negative RF Port[1]
2	RF-	Negative RF Port[1]
3	DGND	Ground
4	V_{DD}	Power supply pin
5	SCL	Serial interface Clock input
6	SEN	Serial Interface Latch Enable Input
7	SDA	Serial interface Data input
8	RF+	Positive RF Port[1]
9	RF+	Positive RF Port[1]
10	GND	RF Ground

Note 1: Pins 1-2 and 8-9 must be tied together on PCB for optimal performance.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Supply Voltage	2.3	2.6	3.6	V
I_{DD} Power Supply Current (V_{DD} = 2.6V)		140	200	µA
I_{DD} Standby Current (V_{DD} = 2.6V)		25		µA
V_{IH} Control Voltage High	1.2	1.8	3.6	V
V_{IL} Control Voltage Low	0	0	0.57	V
RF Input Power (50Ω)[1]				
698 - 915 MHz			+34	dBm
1710 -1910 MHz			+32	dBm
Peak Operating RF Voltage[2]				
V_P to V_M			30	Vpk
V_P to RFGND			30	Vpk
V_M to RFGND			30	Vpk
T_{OP} Operating Temperature Range	-40		+85	°C
T_{ST} Storage Temperature Range	-65		+150	°C

Notes: 1. Maximum Power Available from 50Ω Source. Pulsed RF input with 4620 µS period, 50% duty cycle, measured per 3GPP TS 45.005.
2. Node voltages defined per Equivalent Circuit Model Schematic (*Figure 18*). When DTC is used as a part of reactive network, impedance transformation may cause the internal RF voltages (V_P, V_M) to exceed Peak Operating RF Voltage even with specified RF Input Power Levels. For operation above about +20 dBm (100 mW), the complete RF circuit must be simulated using actual input power and load conditions, and internal node voltages (V_P, V_M in *Figure 18*) monitored to not exceed 30 Vpk.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	4.0	V
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE64904 in the 10-lead 2 x 2 x 0.45 mm QFN package is MSL1.

Performance Plots @ 25°C and 2.6V unless otherwise specified

Figure 4. Measured Shunt C (@ 100 MHz) vs. State (temperature)

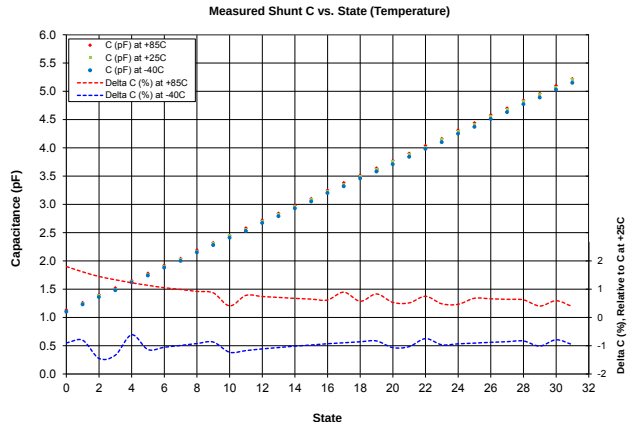


Figure 5. Measured Shunt S_{11} (major states)

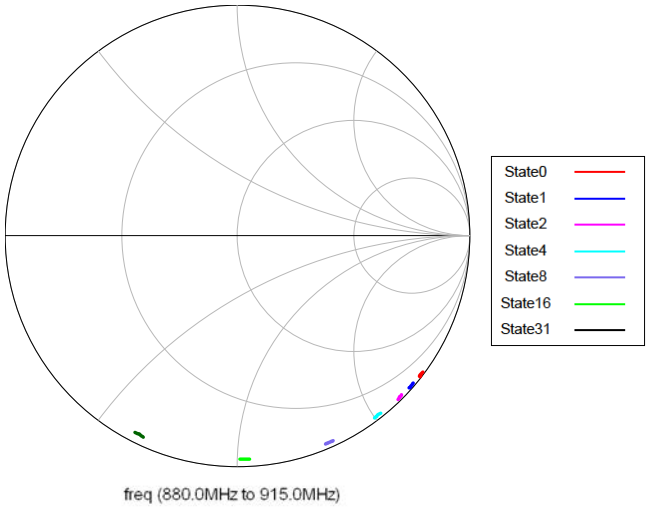


Figure 6. Measured Step Size vs State (frequency)

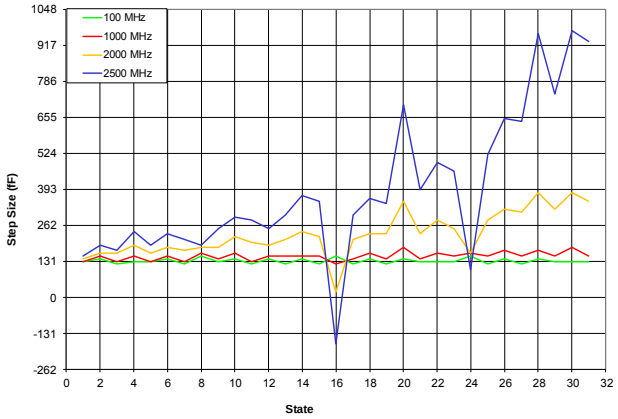


Figure 7. Measured Series S_{11}/S_{22} (major states)

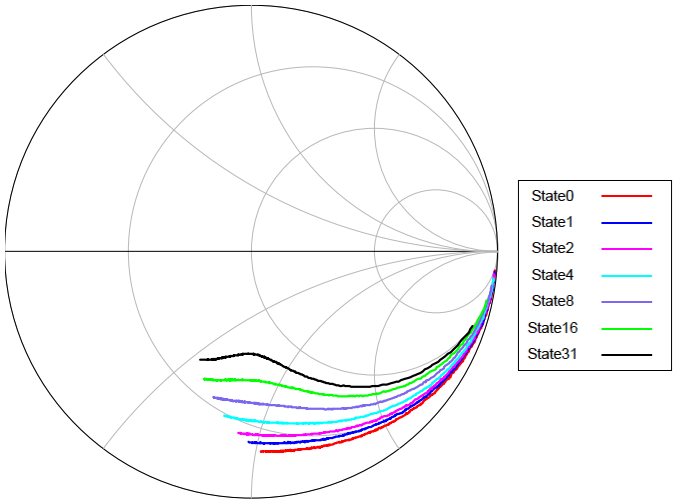


Figure 8. Measured Shunt C vs. Frequency (major states)

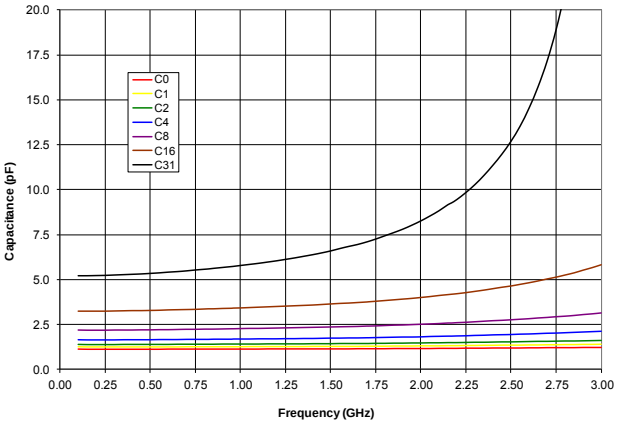


Figure 9. Measured Series S_{21} vs. Frequency (major states)

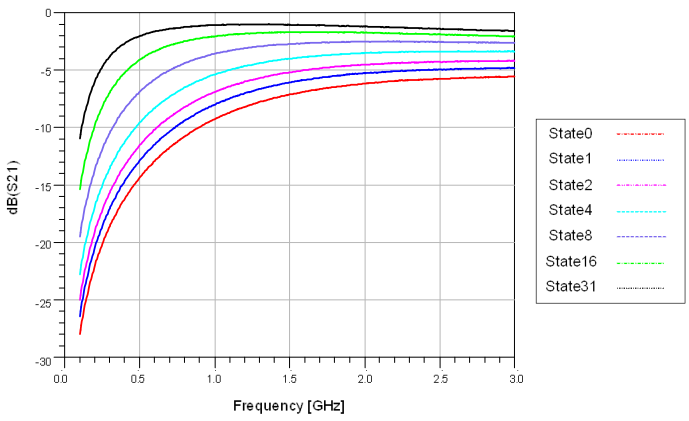


Figure 10. Measured Shunt Q vs. Frequency (major states)

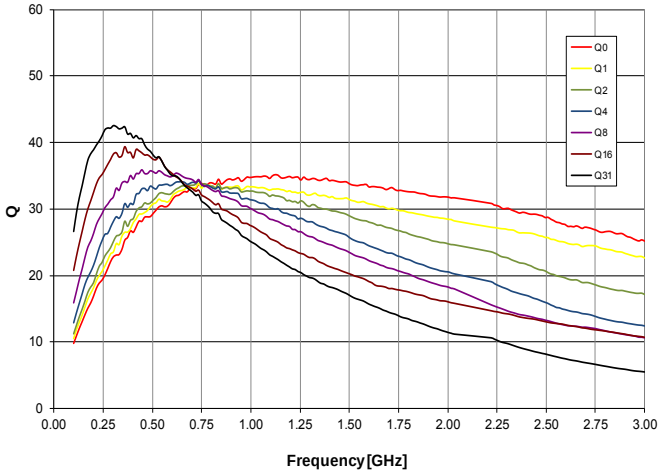


Figure 11. Measured Shunt Q (state 0) vs. Frequency (temperature)

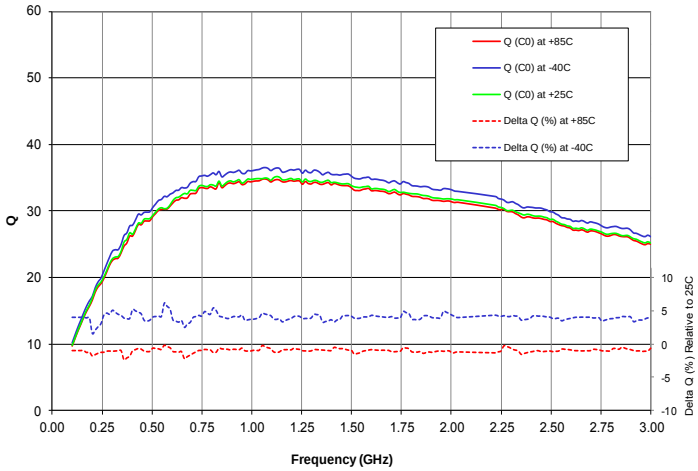
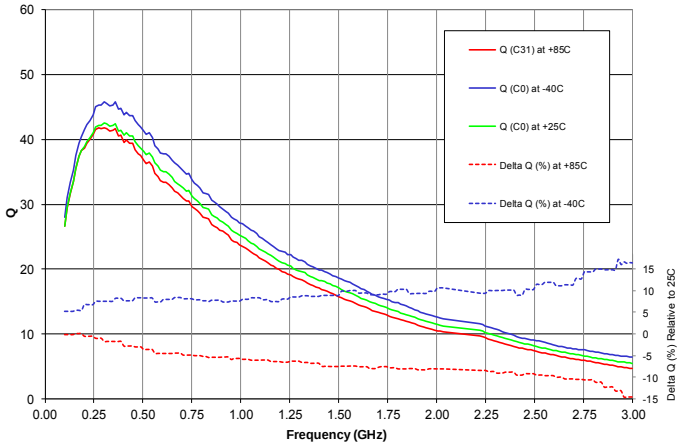


Figure 12. Measured Shunt Q (state 31) vs. Frequency (temperature)



Operation at Frequencies Below 100 MHz

The PE64904 may be operated below the 100 MHz specified minimum operating frequency. The total capacitance and peak operating RF voltage are de-rated down to 1 MHz. *Figure 13* shows the total shunt capacitance from 1 MHz through 100 MHz. As seen in *Figure 14*, the maximum RF voltage that can be placed across the RF terminals or across either RF terminal to Ground is de-rated as a function of frequency.

Note: *Table 1* performance specifications are not guaranteed below 100 MHz. *Figures 13*, *14*, and *15* reflect performance of a typical PE64904.

Figure 13. Measured Shunt C vs. Frequency (major states, 1 MHz - 100 MHz)

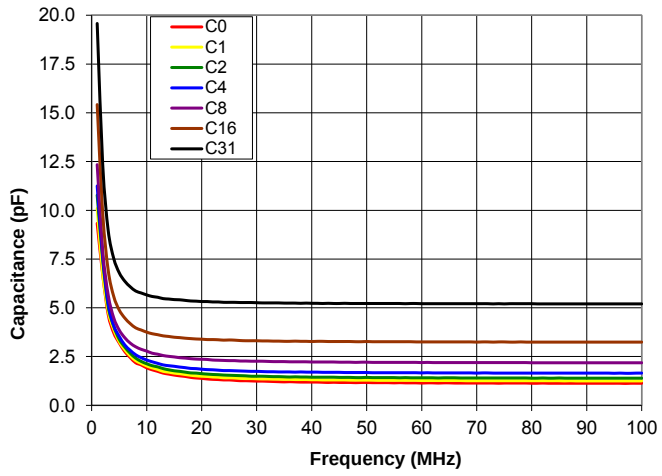


Figure 14. Voltage Derating vs. Frequency (1 MHz - 100 MHz)

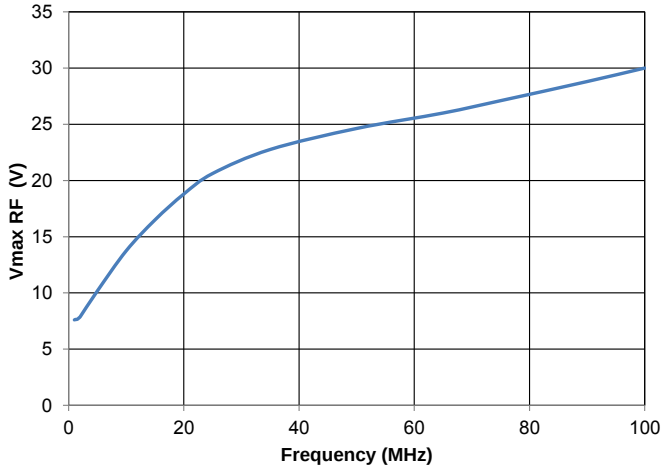
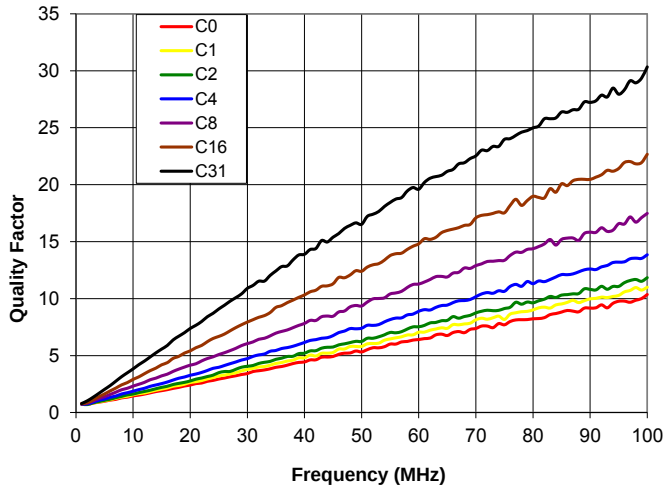


Figure 15. Measured Shunt Q vs. Frequency (major states, 1 MHz - 100 MHz)



Serial Interface Operation and Sharing

The PE64904 is controlled by a three wire SPI-compatible interface. As shown in *Figure 16*, the serial master initiates the start of a telegram by driving the SEN (Serial Enable) line high. Each bit of the 8-bit telegram is clocked in on the rising edge of the SCL (Serial Clock) line. SDA bits are clocked by most significant bit (MSB) first, as shown in *Table 5* and *Figure 16*. Transactions on SDA (Serial Data) are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last 8 bits it received.

More than 1 DTC can be controlled by one interface by utilizing a dedicated enable (SEN) line for each DTC. SDA, SCL, and V_{DD} lines may be shared as shown in *Figure 17*. Dedicated SEN lines act as a chip select such that each DTC will only respond to serial transactions intended for them. This makes each DTC change states sequentially as they are programmed.

Alternatively, a dedicated SDA line with common SEN can be used. This allows all DTCs to change states simultaneously, but requires all DTCs to be programmed even if the state is not changed.

Figure 16. Serial Interface Timing Diagram (oscilloscope view)

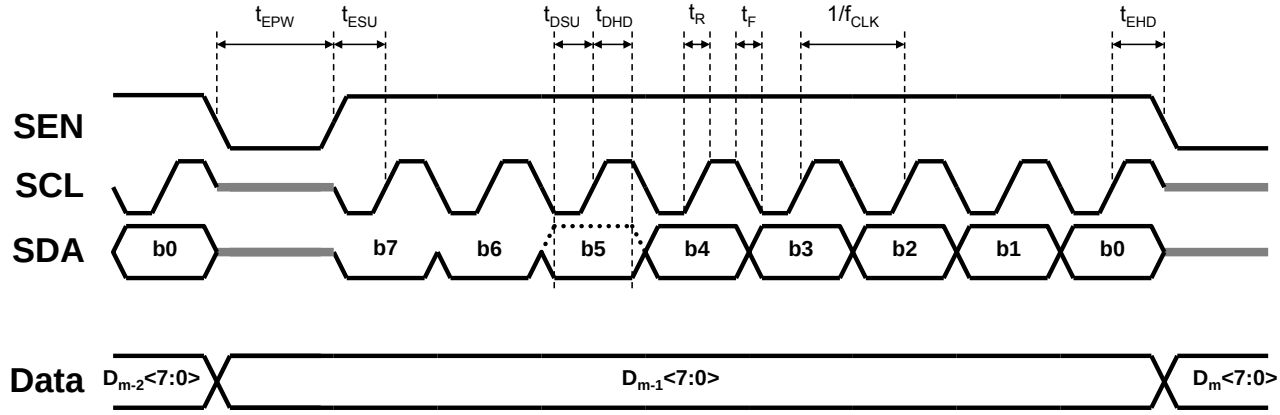


Table 5. Register Map

b7	b6	b5	b4	b3	b2	b1	b0
0	0	STB[1]	d4	d3	d2	d1	d0

MSB (first in) — LSB (last in)

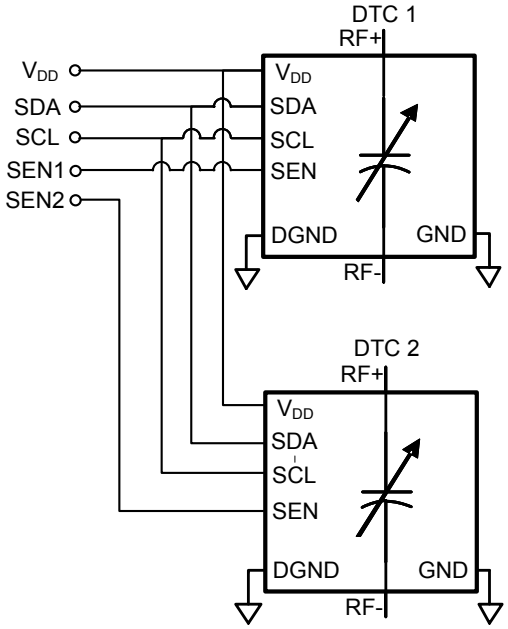
Note 1: The DTC is active when low (set to 0) and in low-current stand-by mode when high (set to 1)

Table 6. Serial Interface Timing Characteristics

V_{DD} = 2.6V, -40°C < T_A < +85°C, unless otherwise specified

Symbol	Parameter	Min	Max	Units
f_{CLK}	Serial Clock Frequency		26	MHz
t_R	SCL, SDA, SEN Rise Time		6.5	ns
t_F	SCL, SDA, SEN Fall Time		6.5	ns
t_{ESU}	SEN rising edge to SCL rising edge	19.2		ns
t_{EHD}	SCL rising edge to SEN falling edge	19.2		ns
t_{DSU}	SDA valid to SCL rising edge	13.2		ns
t_{DHD}	SDA valid after SCL rising edge	13.2		ns
t_{EOW}	SEN falling edge to SEN rising edge	38.4		ns

Figure 17. Recommended Bus Sharing



Equivalent Circuit Model Description

The DTC Equivalent Circuit Model includes all parasitic elements and is accurate in both Series and Shunt configurations, reflecting physical circuit behavior accurately and providing very close correlation to measured data. It can easily be used in circuit simulation programs. Most parameters are state independent, and simple equations are provided for the state dependent parameters. The Tuning Core capacitance C_S represents capacitance between RF+ and RF- ports. It is linearly proportional to state (0 to 31 in decimal) in a discrete fashion. The Series Tuning Ratio is defined as C_{Smax}/C_{Smin}.

C_P represents the circuit and package parasitics from RF ports to GND. In Shunt configuration the total capacitance of the DTC is higher due to parallel combination of C_P and C_S. In Series configuration, C_S and C_P do not add in parallel and the DTC appears as an impedance transformation network.

Parasitic inductance due to circuit and package is modeled as L_S and causes the apparent capacitance of the DTC to increase with frequency until it reaches Self Resonant Frequency (SRF). The value of SRF depends on state and is approximately inversely proportional to the square root of capacitance.

The overall dissipative losses of the DTC are modeled by R_S, R_{P1} and R_{P2} resistors. The parameter R_S represents the Equivalent Series Resistance (ESR) of the tuning core and is dependent on state. R_{P1} and R_{P2} represent losses due to the parasitic and biasing networks, and are state-independent.

Table 7. Maximum Operating RF Voltage

Condition	Limit
V_P to V_M	30 Vpk
V_P to RFGND	30 Vpk
V_M to RFGND	30 Vpk

Figure 18. Equivalent Circuit Model Schematic

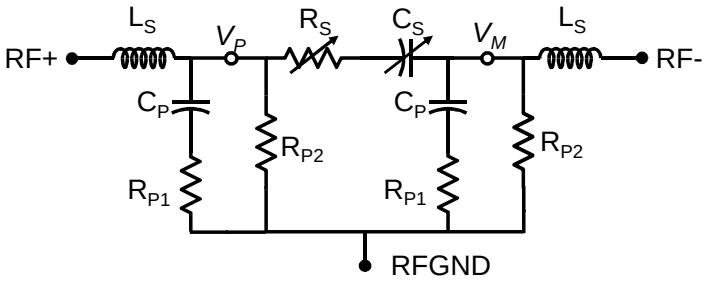


Table 8. Equivalent Circuit Model Parameters

Variable	**Equation** (state = 0, 1, 2…31)	Units
C_S	0.129*state + 0.600	pF
R_S	20/(state+20/(state+0.7)) + 0.7	Ω
R_{P1}	7	Ω
R_{P2}	10	kΩ
C_P	0.5	pF
L_S	0.27	nH

Table 9. Equivalent Circuit Data

State		DTC Core	
Binary	Decimal	C_s [pF]	R_s [Ω]
00000	**0**	0.60	1.40
00001	**1**	0.73	2.27
00010	**2**	0.86	2.83
00011	**3**	0.99	3.08
00100	**4**	1.12	3.12
00101	**5**	1.25	3.05
00110	**6**	1.37	2.93
00111	**7**	1.50	2.78
01000	**8**	1.63	2.64
01001	**9**	1.76	2.51
01010	**10**	1.89	2.39
01011	**11**	2.02	2.27
01100	**12**	2.15	2.17
01101	**13**	2.28	2.08
01110	**14**	2.41	2.00
01111	**15**	2.54	1.93
10000	**16**	2.66	1.86
10001	**17**	2.79	1.80
10010	**18**	2.92	1.75
10011	**19**	3.05	1.70
10100	**20**	3.18	1.65
10101	**21**	3.31	1.61
10110	**22**	3.44	1.57
10111	**23**	3.57	1.54
11000	**24**	3.70	1.51
11001	**25**	3.83	1.48
11010	**26**	3.95	1.45
11011	**27**	4.08	1.42
11100	**28**	4.21	1.40
11101	**29**	4.34	1.37
11110	**30**	4.47	1.35
11111	**31**	4.60	1.33

Layout Recommendations

For optimal results, place a ground fill directly under the DTC package on the PCB. Layout isolation is desired between all control and RF lines. When using the DTC in a shunt configuration, it is important to make sure the RF-pin is solidly grounded to a filled ground plane. Ground traces should be as short as possible to minimize inductance. A continuous ground plane is preferred on the top layer of the PCB. When multiple DTCs are used together, the physical distance between them should be minimized and the connection should be as wide as possible to minimize series parasitic inductance.

Figure 19. Recommended Schematic of Multiple DTCs

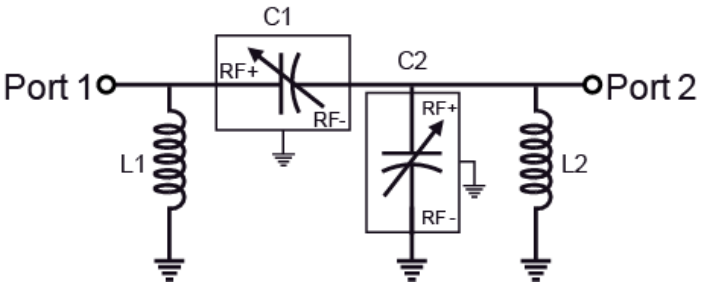
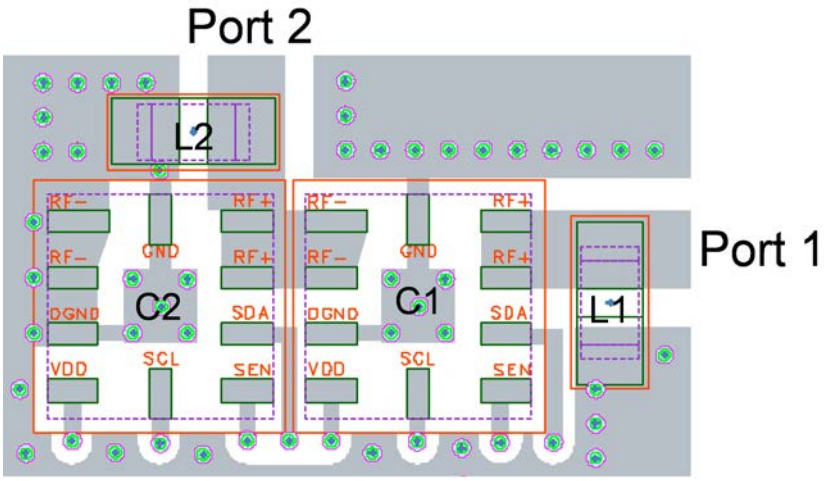


Figure 20. Recommended Layout of Multiple DTCs



Evaluation Board

The 101-0597 Evaluation Board (EVB) was designed for accurate measurement of the DTC impedance and loss. Two configurations are available: 1 Port Shunt (J3) and 2 Port Series (J4, J5). Three calibration standards are provided. The open (J2) and short (J1) standards (104 ps delay) are used for performing port extensions and accounting for electrical length and transmission line loss. The Thru (J9, J10) standard can be used to estimate PCB transmission line losses for scalar de-embedding of the 2 Port Series configuration (J4, J5).

The board consists of a 4 layer stack with 2 outer layers made of Rogers 4350B (ε_r = 3.48) and 2 inner layers of FR4 (ε_r = 4.80). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

Figure 21. Evaluation Board Layout

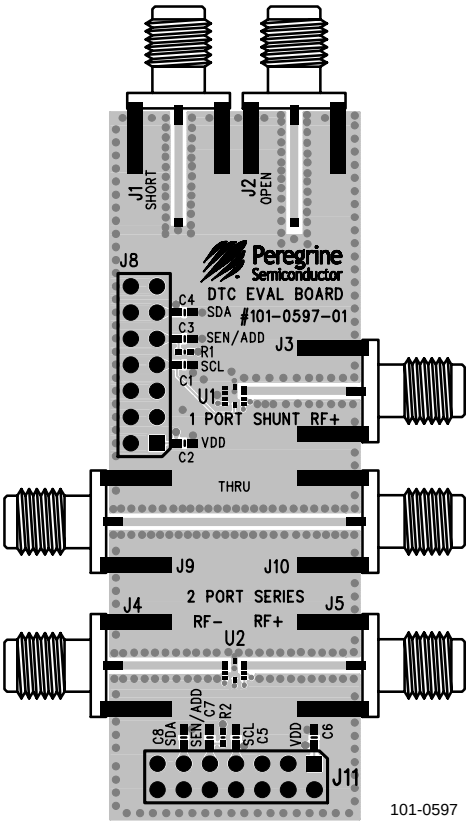
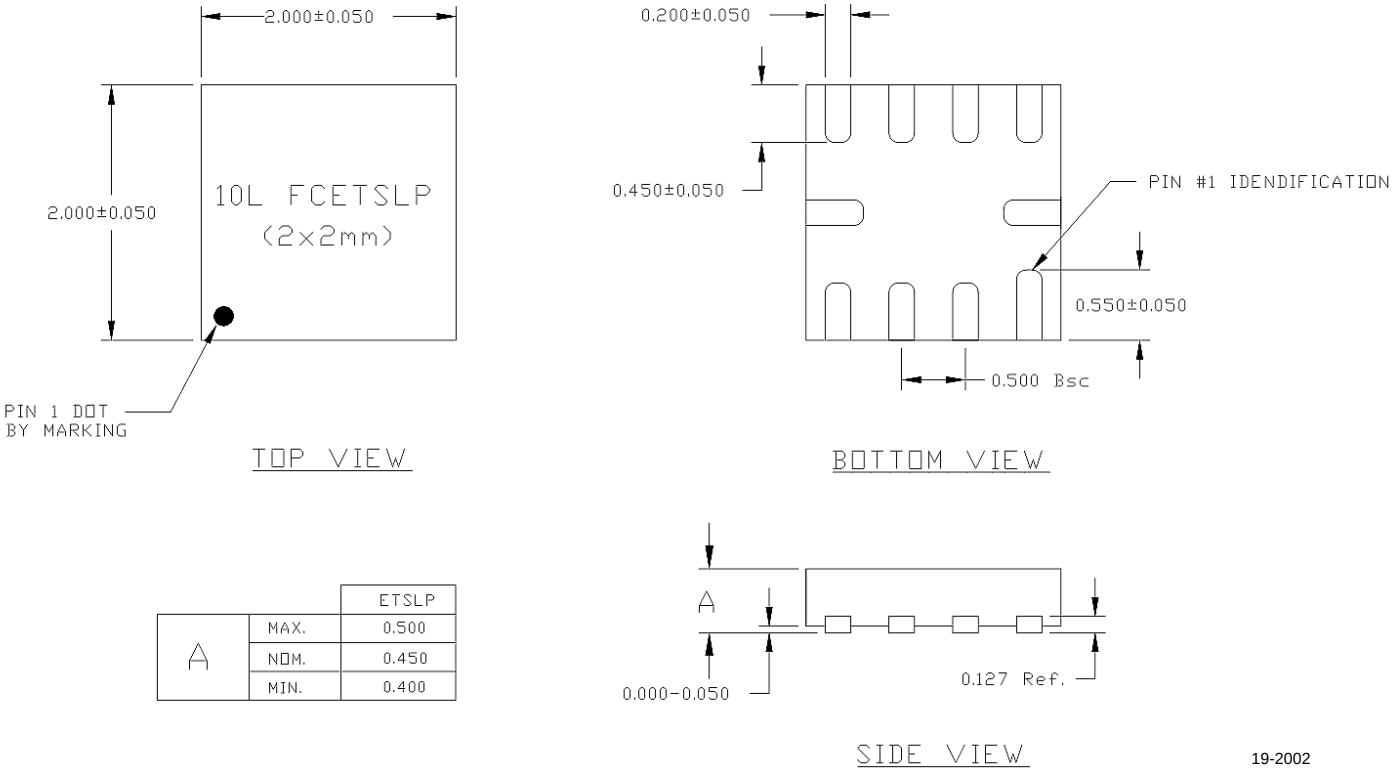
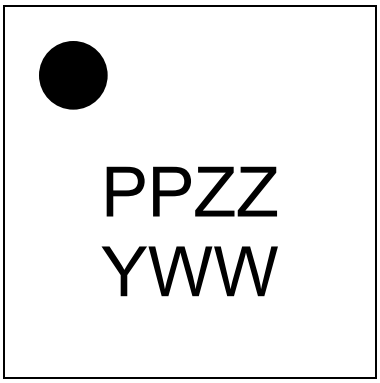


Figure 22. Package Drawing
10-lead 2 x 2 x 0.45 mm



		ETSLP
A	MAX.	0.500
	NOM.	0.450
	MIN.	0.400

Figure 23. Marking Specifications



17-0112

Marking Spec Symbol	Package Marking	Definition
PP	CG	Part number marking for PE64904
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week