Product Specification

PE64909

UltraCMOS® Digitally Tunable Capacitor (DTC)
100-3000 MHz

Product Description

PE64909 is a DuNE™ technology-enhanced Digitally Tunable Capacitor (DTC) based on Peregrine's UltraCMOS® technology. This highly versatile product supports a wide variety of tuning circuit topologies with emphasis on impedance matching and aperture tuning applications.

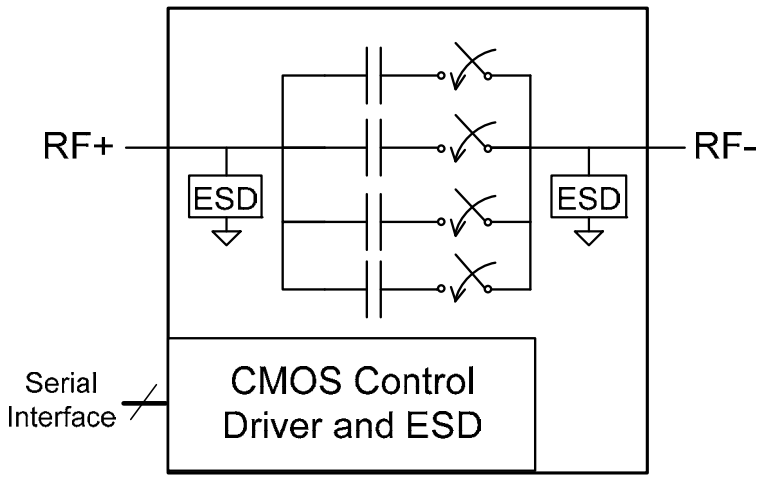
PE64909 offers high RF power handling and ruggedness while meeting challenging harmonic and linearity requirements enabled by Peregrine's HaRP™ technology. The device is controlled through the widely supported 3-wire (SPI compatible) interface. All decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

DuNE™ devices feature ease of use while delivering superior RF performance in the form of tuning accuracy, monotonicity, tuning ratio, power handling, size, and quality factor. With built-in bias voltage generation and ESD protection, DTC products provide a monolithically integrated tuning solution for demanding RF applications.

Features

- 3-wire (SPI compatible) serial interface with built-in bias voltage generation and ESD protection
- DuNE™ technology enhanced
- 4-bit 16-state Digitally Tunable Capacitor
- Shunt configuration C = 0.6 pF to 2.35 pF (3.9:1 tuning ratio) in discrete 117 fF steps
- High RF power handling (30 V_{pk} RF) and linearity
- Wide power supply range (2.3 to 4.8V) and low current consumption (typ. 140 µA at 2.75V)
- High ESD tolerance of 2kV HBM on all pins
- Applications include:
  - Tunable antennas
  - Tunable matching networks
  - Tunable filter networks
  - Phase shifters

Figure 1. Functional Diagram



71-0090-01

Figure 2. Package Type

10-lead 2 x 2 x 0.55 mm QFN

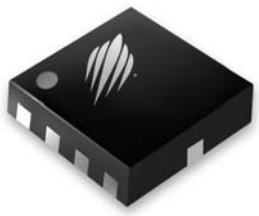


Table 1. Electrical Specifications @ 25 °C, V_{DD} = 2.75V (In shunt configuration, RF- connected to GND)

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency		100		3000	MHz
Minimum capacitance (C_{min})	State 0000, 100 MHz	0.54	0.60	0.66	pF
Maximum capacitance (C_{max})	State 1111, 100 MHz	1.88	2.35	2.82	pF
Tuning ratio	C_{max}/C_{min}, 100 MHz		3.9:1		
Step size	4 bits (16 states), 100 MHz		0.117		pF
Quality factor at C_{min}[1]	698 to 960 MHz, with L_S removed 1710 to 2170 MHz, with L_S removed		40 40		
Quality factor at C_{max}[1]	698 to 960 MHz, with L_S removed 1710 to 2170 MHz, with L_S removed		29 13		
Self resonant frequency	State 0000 State 1111		9.1 3.7		GHz
Harmonics[2]	2fo, 3fo: 698 to 915 MHz; P_{IN} = +34 dBm, 50**Ω** 2fo, 3fo: 1710 to 1910 MHz; P_{IN} = +32 dBm, 50**Ω**			-36 -36	dBm dBm
IMD3	Bands I,II,V/VIII, +20 dBm CW @ TX freq, -15 dBm CW @ 2TX-RX freq, 50**Ω**			-105	dBm
Third order intercept point (IP3)	Shunt configuration derived from IMD3 spec IP3 = ($2P_{TX}$ + P_{block} - IMD3) / 2		65		dBm
Switching time[3,4]	State change to 10/90% delta capacitance between any two states			12	µs
Start-up time[3]	Time from V_{DD} within specification to all performances within specification			70	µs
Wake-up time[3,4]	State change from Standby mode to RF state to all performances within specification			70	µs

Notes: 1. Q for a Shunt DTC based on a Series RLC equivalent circuit
Q = X_C/R = $(X-X_L)/R$, where X = X_L+X_C , X_L = 2*pi*f*L, X_C = -1/(2*pi*f*C), which is equal to removing the effect of parasitic inductance L_S
2. In Shunt between 50 **Ω** ports. Pulsed RF input with 4620 µS period, 50% duty cycle, measured per 3GPP TS 45.005
3. DC path to ground at RF– must be provided to achieve specified performance
4. State change activated on falling edge of SEN following data word

Figure 3. Pin Configuration (Top View)

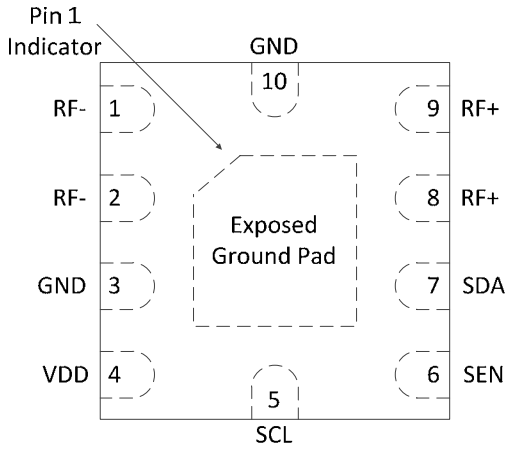


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	RF-	Negative RF port[1]
2	RF-	Negative RF port[1]
3	GND	Ground[2]
4	V_{DD}	Power supply pin
5	SCL	Serial interface clock input
6	SEN	Serial interface latch enable input
7	SDA	Serial interface data input
8	RF+	Positive RF port[1]
9	RF+	Positive RF port[1]
10	GND	Ground[2]
Pad	GND	Exposed pad: ground for proper operation[2]

Notes: 1. For optimal performance, recommend tying pins 1-2 and pins 8-9 together on PCB
2. For optimal performance, recommend tying pins 3, 10, and exposed ground pad together on PCB

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE64909 in the 10-lead 2x2 mm QFN package is MSL1.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.30	2.75	4.80	V
Supply current (V_{DD} = 2.75V)	I_{DD}		140	200	µA
Standby current (V_{DD} = 2.75V)	I_{DD}		25		µA
Digital input high	V_{IH}	1.2	1.8	3.1	V
Digital input low	V_{IL}	0	0	0.57	V
RF input power (50Ω)[1] 698 to 915 MHz 1710 to 1910 MHz				 +34 +32	 dBm dBm
Peak operating RF voltage[2] V_P to V_M V_P to RFGND				 30 30	 Vpk Vpk
Operating temperature range	T_{OP}	-40	+25	+85	°C
Storage temperature range	T_{ST}	-65	+25	+150	°C

Notes: 1. Maximum Power Available from 50Ω Source. Pulsed RF input with 4620 µS period, 50% duty cycle, measured per 3GPP TS 45.005 measured in shunt between 50Ω ports, RF- connected to GND
2. Node voltages defined per Equivalent Circuit Model Schematic (*Figure 13*). When DTC is used as a part of reactive network, impedance transformation may cause the internal RF voltages (V_P, V_M) to exceed Peak Operating RF Voltage even with specified RF Input Power Levels. For operation above about +20 dBm (100 mW), the complete RF circuit must be simulated using actual input power and load conditions, and internal node voltages (V_P, V_M in *Figure 13*) monitored to not exceed 30 V_{pk}

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
ESD Voltage HBM[1], all pins	V_{ESD}		2000	V

Note 1: Human Body Model (MIL-STD-883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Performance Plots @ 25°C and 2.75V unless otherwise specified

Figure 4. Measured Shunt C (@ 100 MHz) vs State

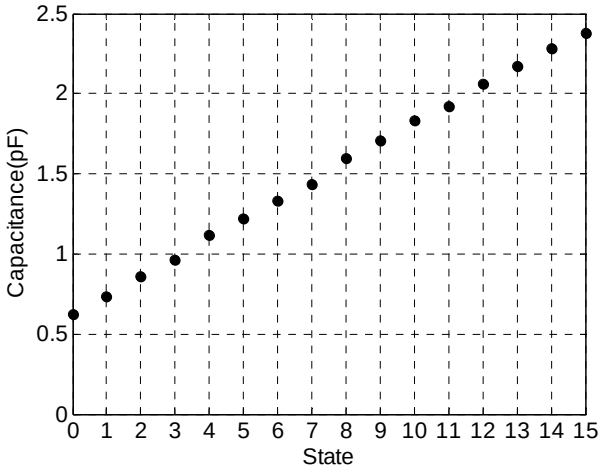


Figure 5. Measured Shunt S_{11} (major states)

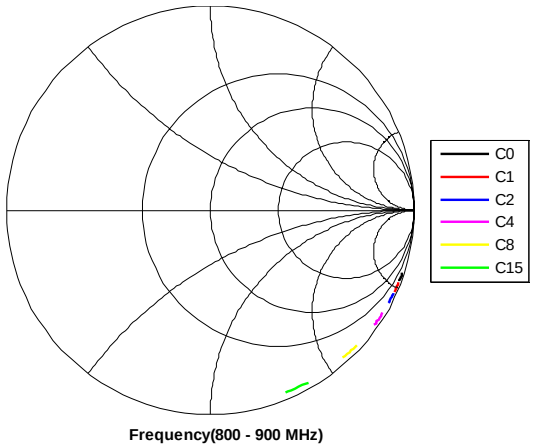


Figure 6. Measured Step Size vs State (frequency)

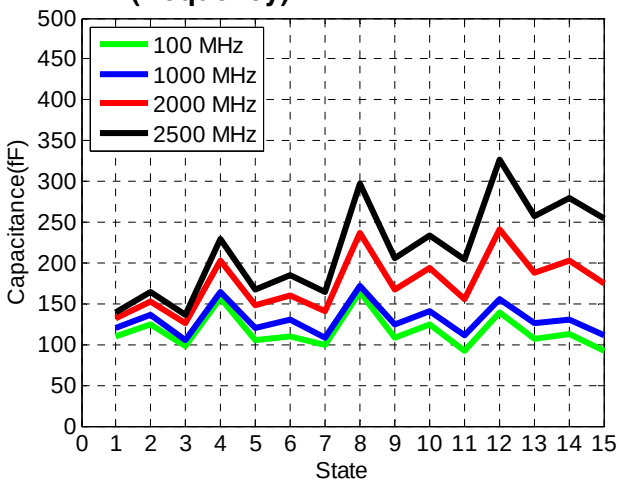


Figure 7. Measured Shunt C vs Frequency (major states)

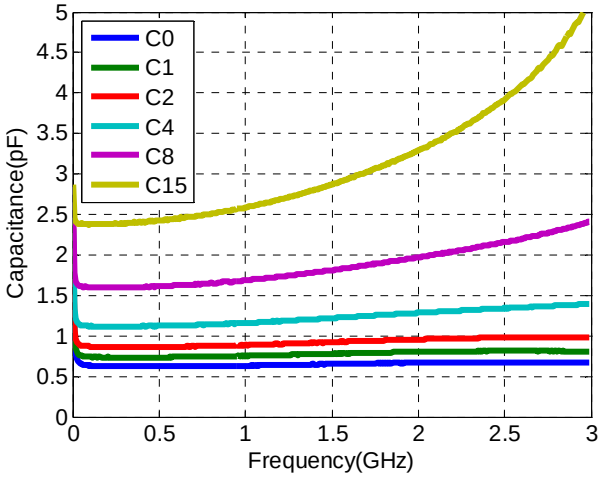


Figure 8. Measured Shunt Q vs Frequency (major states)

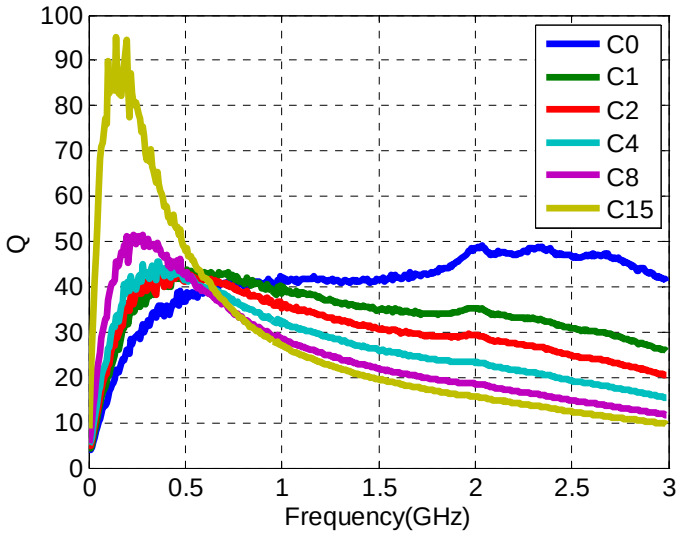


Figure 9. Measured Shunt Q vs State

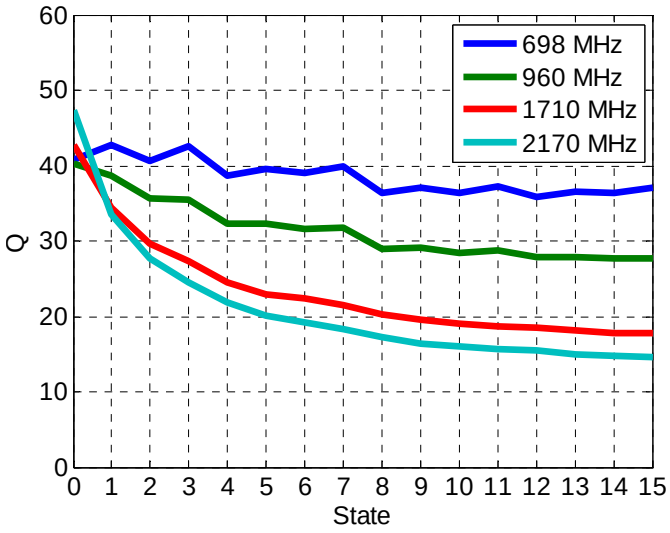
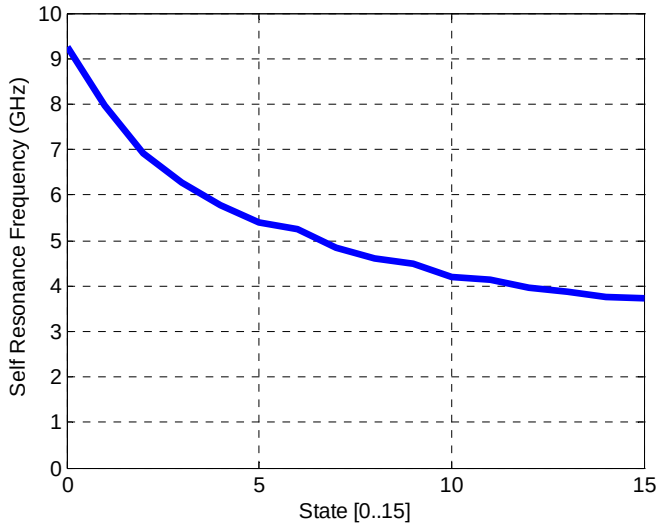


Figure 10. Measured Self Resonance Frequency vs State



Serial Interface Operation and Sharing

The PE64909 is controlled by a three wire SPI-compatible interface with enable active high. As shown in *Figure 11*, the serial master initiates the start of a telegram by driving the SEN (Serial Enable) line high. Each bit of the 8-bit telegram (MSB first in) is clocked in on the rising edge of SCL (Serial Clock), as shown in *Table 5* and *Figure 11*. Transitions on SDA (Serial Data) are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last 8 bits it received.

More than 1 DTC can be controlled by one interface by utilizing a dedicated enable (SEN) line for each DTC. SDA, SCL, and V_{DD} lines may be shared as shown in *Figure 12*. Dedicated SEN lines act as a chip select such that each DTC will only respond to serial transactions intended for them. This makes each DTC change states sequentially as they are programmed.

Alternatively, a dedicated SDA line with common SEN can be used. This allows all DTCs to change states simultaneously, but requires all DTCs to be programmed even if the state is not changed.

Figure 11. Serial Interface Timing Diagram

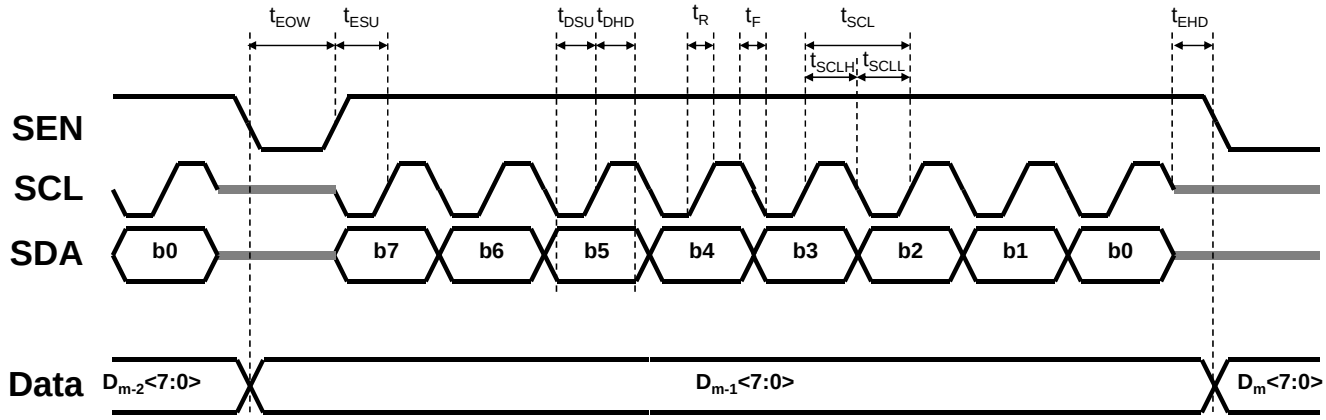


Table 5. 8-Bit Serial Programming Register Map

b7	b6	b5	b4	b3	b2	b1	b0
0[1]	0[1]	STB[2]	0	d3	d2	d1	d0

MSB (first in) LSB (last in)

Notes: 1. These bits are reserved and must be written to 0 for proper operation
2. The DTC is active when low (set to 0) and in low-current stand-by mode when high (set to 1)

Figure 12. Recommended Bus Sharing

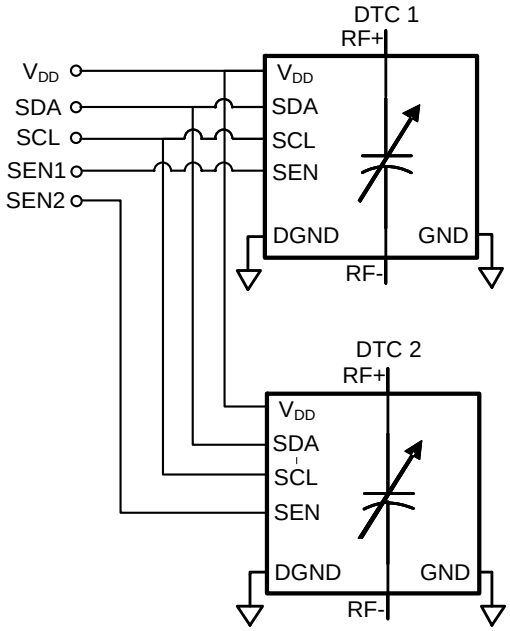


Table 6. Serial Interface Timing Characteristics

V_{DD} = 2.75V, -40°C < T_A < +85°C, unless otherwise specified

Symbol	Parameter	Min	Max	Units
t_{SCL}	Serial clock period	38.4		ns
t_{SCLL}	SCL low time	13.2		ns
t_{SCLH}	SCL high time	13.2		ns
t_R	SCL, SDA, SEN rise time		6.5	ns
t_F	SCL, SDA, SEN fall time		6.5	ns
t_{ESU}	SEN rising edge to SCL rising edge	19.2		ns
t_{EHD}	SCL rising edge to SEN falling edge	19.2		ns
t_{DSU}	SDA valid to SCL rising edge	13.2		ns
t_{DHD}	SDA valid after SCL rising edge	13.2		ns
t_{EOW}	SEN falling edge to SEN rising edge	38.4		ns

Equivalent Circuit Model Description

The DTC Equivalent Circuit Model includes all parasitic elements and is accurate in both Series and Shunt configurations, reflecting physical circuit behavior accurately and providing very close correlation to measured data. It can easily be used in circuit simulation programs.

For V_P and V_M max operating limits, refer to *Table 3*.

Figure 13. Equivalent Circuit Model Schematic

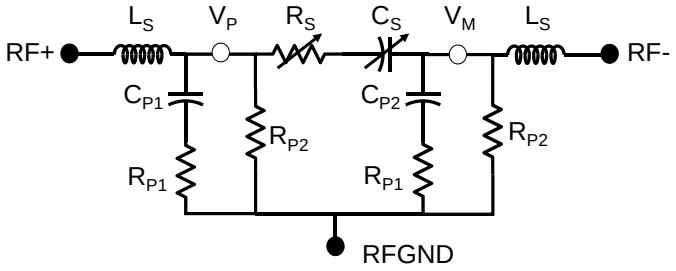


Table 7. Equivalent Circuit Model Parameters

Variable	**Equation** (state = 0, 1, 2…15)	Unit
C_S	0.127*state + 0.20	pF
R_S	20/(state+20/(state+0.7)) + 0.7	Ω
R_{P1}	10+4*state	Ω
R_{P2}	40000+10*state^3	Ω
C_{P1}	-0.01*state + 0.40	pF
C_{P2}	0.0133*state + 0.45	pF
L_S	0.35	nH

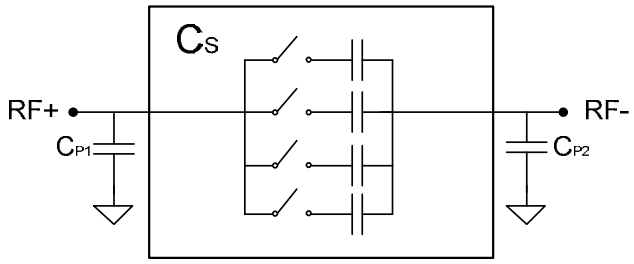
Table 8. Equivalent Circuit Data

State			DTC Core		Parasitic Elements			
Hex	Bin	Dec	C_S [pF]	R_S [Ω]	C_{P1} [pF]	C_{P2} [pF]	R_{P1} [Ω]	R_{P2} [kΩ]
0x00	0000	0	0.20	1.40	0.40	0.45	10.0	40.0
0x01	0001	1	0.33	2.27	0.39	0.46	14.0	40.0
0x02	0010	2	0.45	2.83	0.38	0.48	18.0	40.1
0x03	0011	3	0.58	3.08	0.37	0.49	22.0	40.3
0x04	0100	4	0.71	3.12	0.36	0.50	26.0	40.6
0x05	0101	5	0.83	3.05	0.35	0.52	30.0	41.3
0x06	0110	6	0.96	2.93	0.34	0.53	34.0	42.2
0x07	0111	7	1.09	2.78	0.33	0.54	38.0	43.4
0x08	1000	8	1.21	2.64	0.32	0.56	42.0	45.1
0x09	1001	9	1.34	2.51	0.31	0.57	46.0	47.3
0x0A	1010	10	1.47	2.39	0.30	0.58	50.0	50.0
0x0B	1011	11	1.59	2.27	0.29	0.60	54.0	53.3
0x0C	1100	12	1.72	2.17	0.28	0.61	58.0	57.3
0x0D	1101	13	1.84	2.08	0.27	0.62	62.0	62.0
0x0E	1110	14	1.97	2.00	0.26	0.64	66.0	67.4
0x0F	1111	15	2.10	1.93	0.25	0.65	70.0	73.8

Series Operation

In Series configuration, the effective capacitance between RF+ and RF- ports is represented by C_s and tuning ratio as C_{Smax}/C_{Smin}.

Figure 14. Effective Capacitance Diagram



Shunt Configuration (looking into RF+ when RF- is grounded) will have higher total capacitance at RF+ due to parallel combination of Cs with parasitic capacitance C_{P1} (C_S + C_{P1}), as demonstrated in *Figure 15* and *Table 9.*

Figure 15. Typical Capacitance vs. State

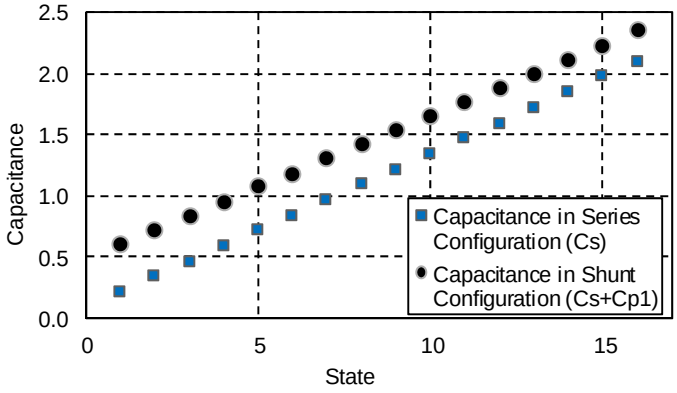


Table 9. Effective Capacitance Summary

Configuration	Effective Capacitance	C_{min} (state 0)	C_{max} (state 31)	Tuning Ratio
Series (RF+ to RF-)	C_S	0.20	2.10	10.5:1
Shunt (RF+ to GND)	C_S + C_{P1}	0.60	2.35	3.9:1

S_{11} and S_{21} for series configuration is illustrated in *Figures 16* and *17*. S_{21} includes mismatch and dissipative losses and is not indicative of tuning network loss. Equivalent Circuit Model can be used for simulation of tuning network loss.

Figure 16. Measured Series S_{11}/S_{22} (major states)

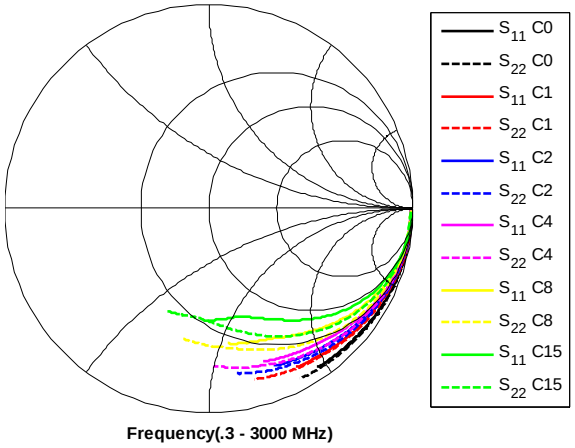
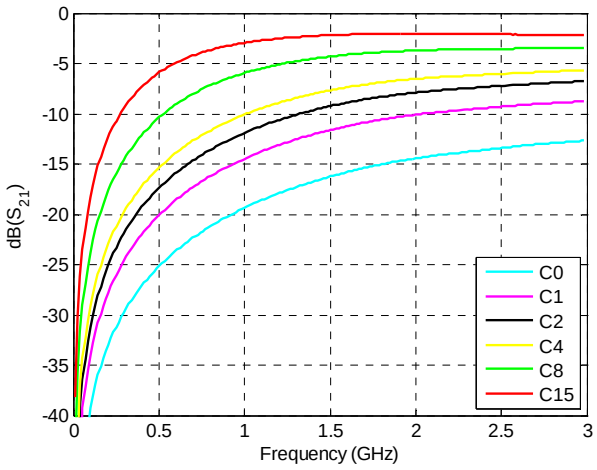


Figure 17. Measured Series S_{21} vs. Frequency (major states)



When the DTC is used as a part of a reactive network, impedance transformation may cause the internal RF voltages (V_P and V_M in *Figure 13*) to exceed peak operating RF voltage. The complete RF circuit must be simulated using actual input power and load conditions to ensure neither V_P nor V_M exceeds 30 Vpk.

Layout Recommendations

For optimal results, place a ground fill directly under the DTC package on the PCB. Layout isolation is desired between all control and RF lines. When using the DTC in a shunt configuration, it is important to make sure the RF-pin is solidly grounded to a filled ground plane. Ground traces should be as short as possible to minimize inductance. A continuous ground plane is preferred on the top layer of the PCB. When multiple DTCs are used together, the physical distance between them should be minimized and the connection should be as wide as possible to minimize series parasitic inductance.

Figure 18. Recommended Schematic of Multiple DTCs

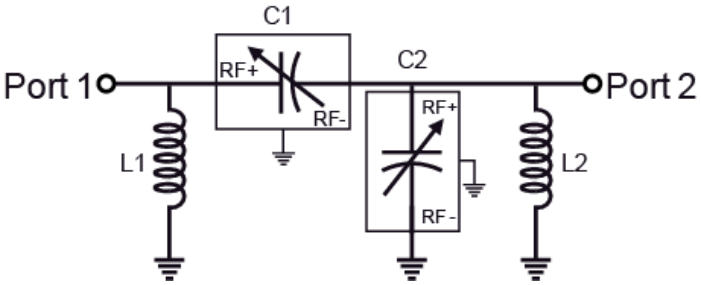
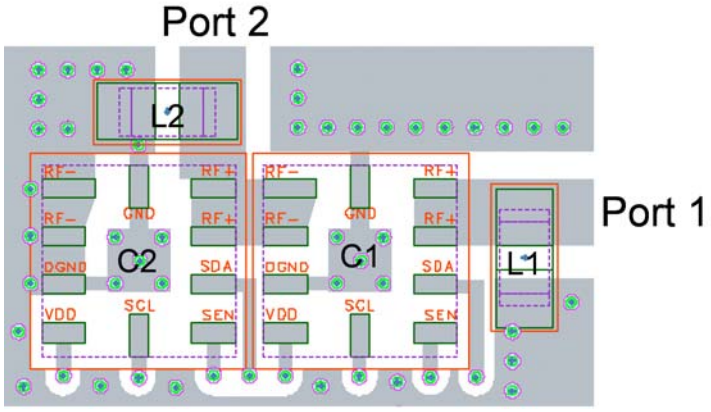


Figure 19. Recommended Layout of Multiple DTCs



Evaluation Board

The 101-0675 Evaluation Board (EVB) was designed for accurate measurement of the DTC impedance and loss. Two configurations are available: 1 Port Shunt (J3) and 2 Port Shunt (J4, J5). Three calibration standards are provided. The open (J2) and short (J1) standards (104 ps delay) are used for performing port extensions and accounting for electrical length and transmission line loss. The Thru (J9, J10) standard can be used to estimate PCB transmission line losses for scalar de-embedding of the 2 Port Series configuration (J4, J5).

The board consists of a 4 layer stack with 2 outer layers made of Rogers 4350B (ε_r = 3.48) and 2 inner layers of FR4 (ε_r = 4.80). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

Figure 20. Evaluation Board Layout

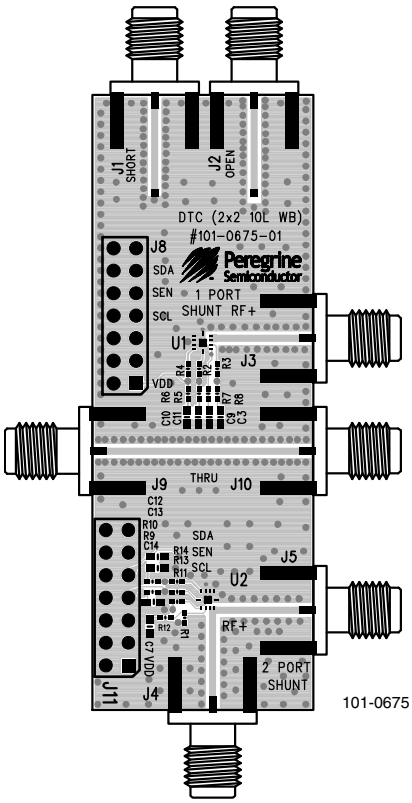
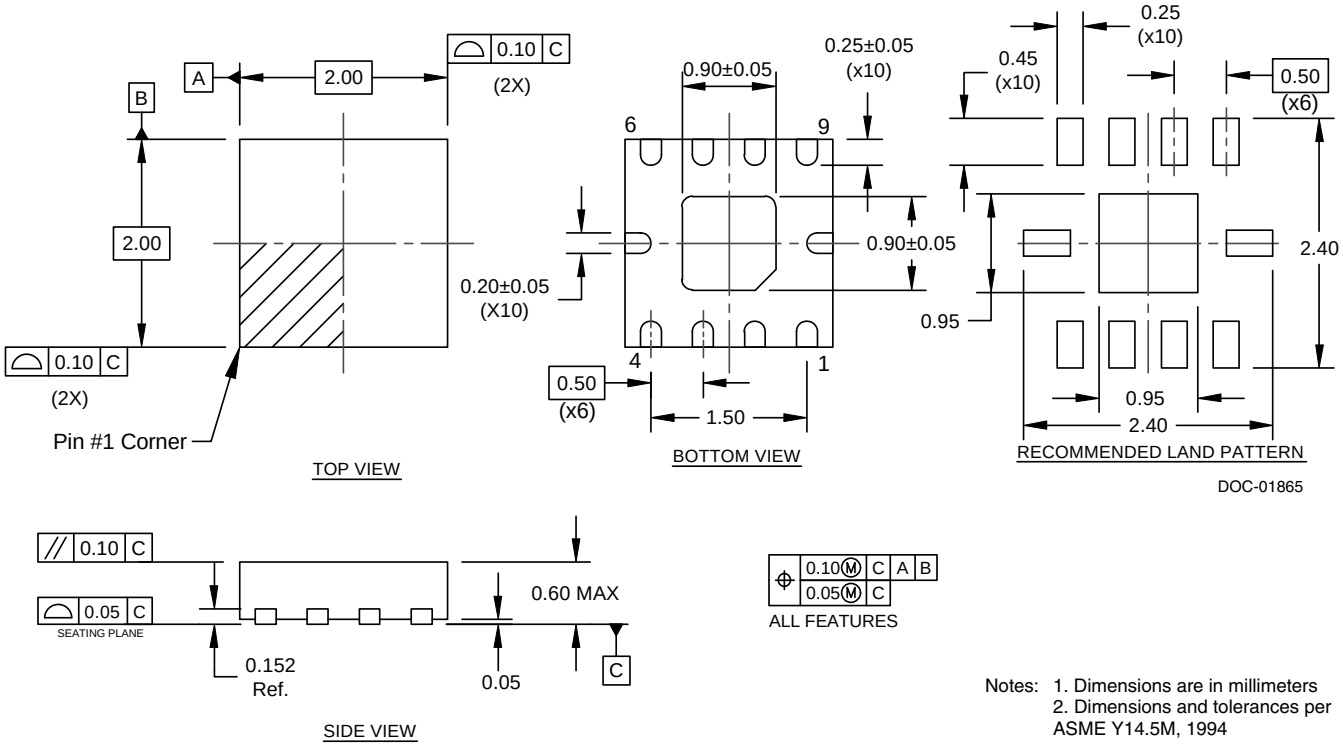
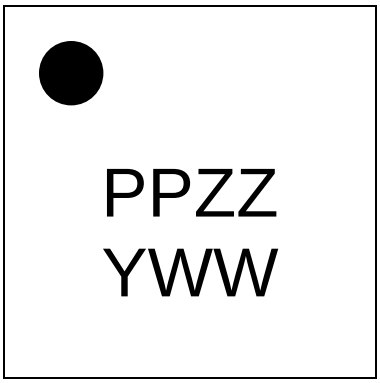


Figure 21. Package Drawing
10-lead 2 x 2 x 0.55 mm QFN



Notes: 1. Dimensions are in millimeters
2. Dimensions and tolerances per ASME Y14.5M, 1994

Figure 22. Top Marking Specifications



17-0112

Marking Spec Symbol	Package Marking	Definition
PP	DL*	Part number marking for PE64909
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week

Note: (PP), the package marking specific to the PE64909, is shown in the figure instead of the standard Peregrine package marking symbol (P).