EL7532EVAL1Z

Evaluation Board

TB445
Rev.1.00
Feb 22, 2005

Using the Evaluation Board

EL7532 is a high efficiency 2A synchronous step-down PWM regulator in a tiny MSOP10 package. The internal compensation makes it possible for the full-featured 2A converter to occupy less than 0.18in^2 of PCB area with all components on one side.

1. Output Adjustment

Use R_1 and R_2 to adjust output voltage according to the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_2}{R_1}\right)$$

The evaluation board is set to V_O = 1.8V.

2. Chip Enable

When EN pin is pulled to Ground, the regulator is disabled. It consumes less than 1µA of current. R_5 can be connected to V_{IN} directly if this function is not needed, reducing the component counts.

3. RSI/POR Function

When powering up, the open-collector Power-On-Reset output holds low for 100ms after V_O reaches the preset voltage. When a reset signal RSI is issued, POR goes to low for the same period of time while the output power is still on (Please refer to the datasheet for the timing diagram). When the function is not used, connect RSI to ground and leave R_4 open, further reduce the total components counts and the overall PCB area to less than 0.18in^2.

The POR output also serves as a 100ms delayed Power Good signal when the pull-up resister R_4 is installed. The RSI pin needs to be directly (or indirectly through R_6) connected to Ground for this to function properly.

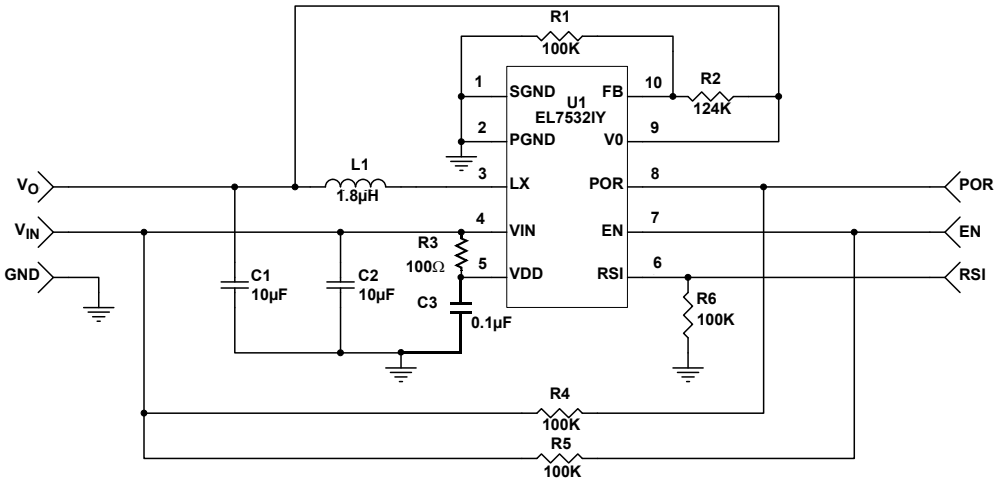

FIGURE 1. DEMO BOARD SCHEMATIC

Evaluation Board Bill of Materials

REFERENCE DESIGNATOR	VALUE	PACKAGE	MANUFACTURER	MANUFACTURER'S PART NUMBER	MANUFACTURER'S PHONE NUMBER
C_1, C_2	10µF/MLCC, X7R	1206	TDK	C3216X7R1A106K	847-803-6100
C_3	0.1µF	0603/0402	Any		
L_1	1.8µH		Coilcraft	1008PS-182M	847-639-6400
R_2	124K, 1%	0603/0402	Any		
R_1, R_4, R_5, R_6	100K, 1%	0603/0402	Any		
R_3	100Ω, 1%	0603/0402	Any		
U_1	EL7532IY	MSOP10	Intersil	EL7532IY	888-INTERSIL

Demo Board Layout (Actual Size - 3” x 2”)

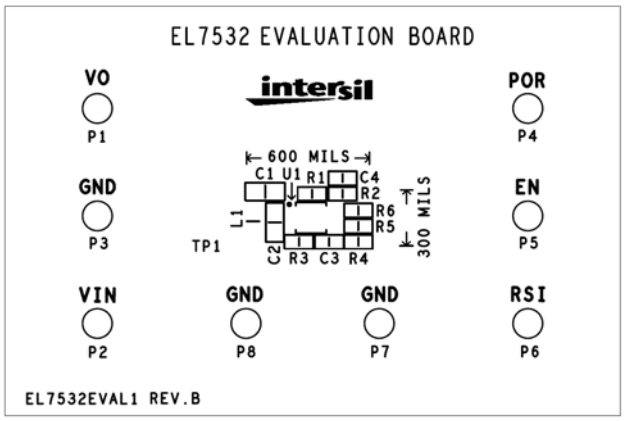

FIGURE 2. SILKSCREEN TOP

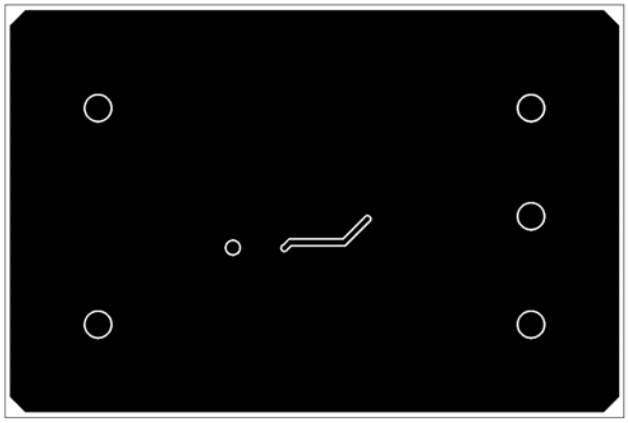

FIGURE 3. TOP LAYER

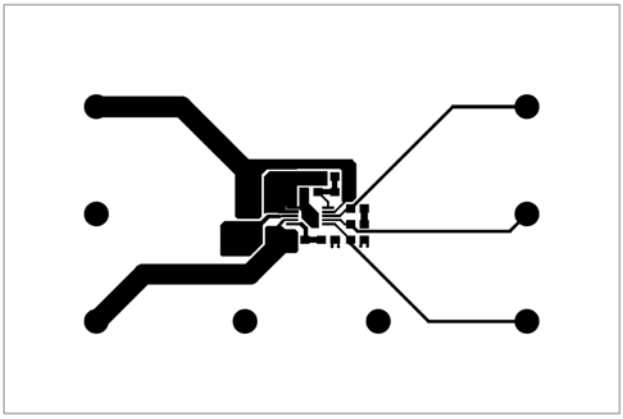

FIGURE 4. BOTTOM LAYER