

EL7554IRE-EVAL

Evaluation Board

TB418
Rev.1.00
Nov 14, 2003**Introduction**

The EL7554 is a high efficiency full-featured synchronous 4A step-down regulator. This document lists the completed schematic diagram and BOM, as well as the layout. With components on one side of the PCB, the complete converter occupies less than 0.58in² of space. Please refer to the

datasheet for the application of features. This demo board is preset to 1.8V for V_O and operates at 600kHz switching frequency. The measured crossover frequencies are around 50kHz with the compensation values.

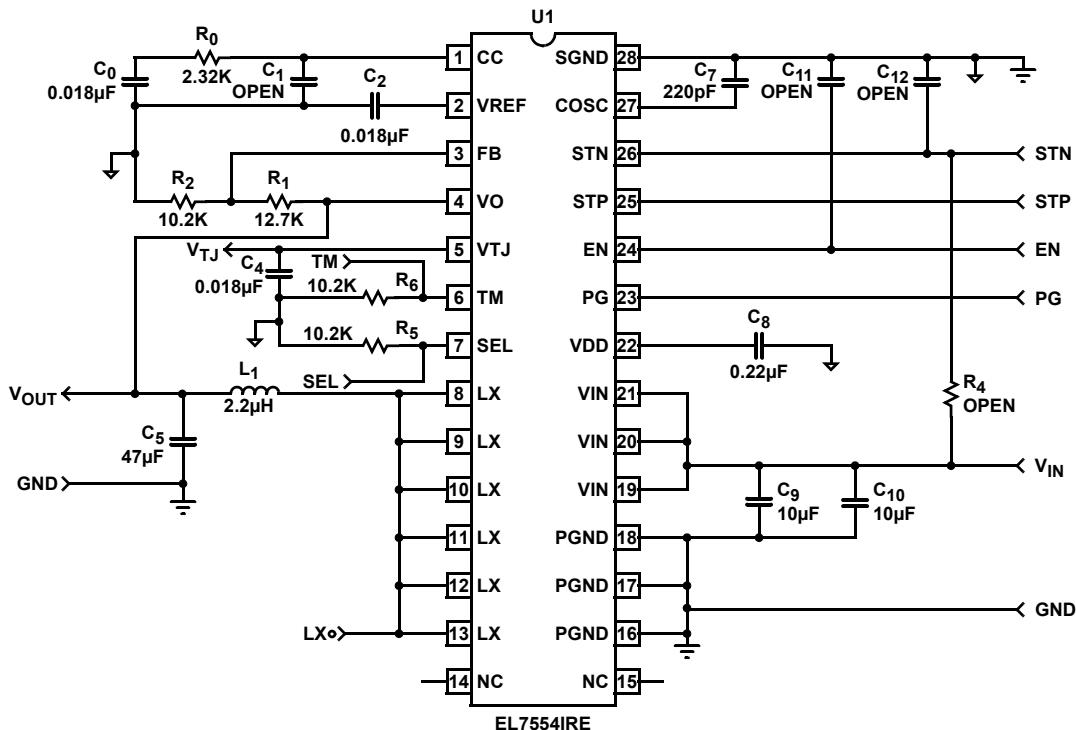
Circuit Diagram

TABLE 1. DEMO BOARD BILL OF MATERIAL

DESIGNATOR	VALUE	PACKAGE	MANUFACTURER	PHONE #	PART NUMBER
C ₀ , C ₂ , C ₄	0.018µF	0603	Any X5R or X7R		
C ₅	47µF	1210	TDK		C3225X5R0J476M
C ₇	220pF 5%	0603	Any 5% MLCC		
C ₈	0.22µF	0603	Any X5R or X7R		
C ₉ , C ₁₀	10µF	1206	Any X5R or X7R		
R ₀	2.32K/1%	0603	Any		
R ₁	12.7K/1%	0603	Any		
R ₂ , R ₅ , R ₆	10.2K/1%	0603	Any		
L ₁	2.2µH		TDK	847-803-6100	RLF7030-2R2M5R4
U1	EL7554IRE	HTSSOP-28	Intersil	888-INTERSIL	EL7554IRE

The output voltage can be as high as the input voltage minus the PMOS and inductor voltage drops. Use R₁ and R₂ to set the output voltage according to the following formula:

$$V_O = V_{FB} \times \left(1 + \frac{R_1}{R_2} \right)$$

Where V_{FB}=0.8V

When the resistors are changed, please change the compensation capacitor C₀ and resister R₀. For the convenience, standard values of R₁ and R₂ are listed in Table 2.

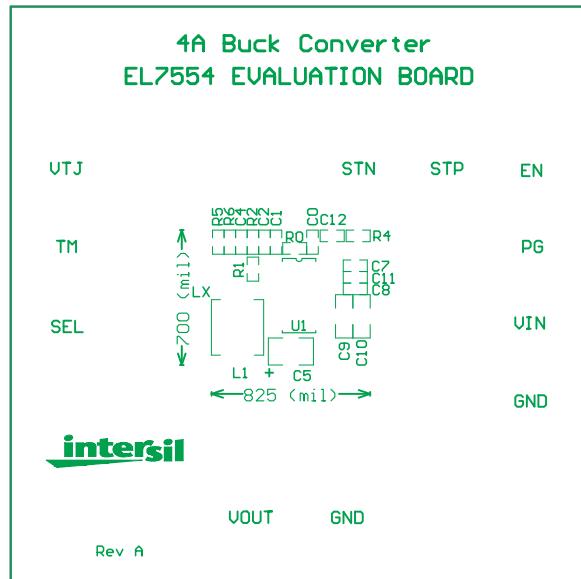
R₅ and R₆ can be eliminated if voltage margin feature is not used. Connect TM and SEL pins directly to ground.

The layout accommodates 1206, 1210, 1812, and D-size package for C5.

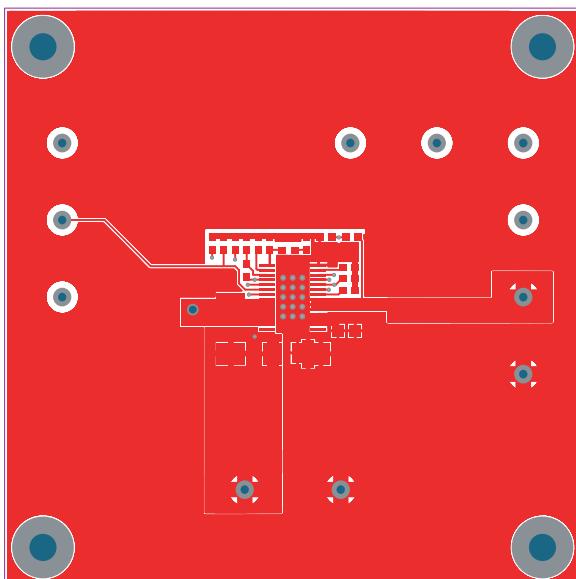
TABLE 2. FEEDBACK RESISTER AND COMPENSATION VALUES

V _O (V)	C ₀ (pF)	R ₀ (kΩ)	R ₁ (kΩ)	R ₂ (kΩ)
0.8	0.018µF	1.02	0	Open
1	0.018µF	1.27	2.49	10
1.2	0.018µF	1.54	4.99	10
1.5	0.018µF	1.91	10	11.5
1.8	0.018µF	2.32	12.7	10.2
2.5	0.018µF	3.24	21.5	10
3.3	0.018µF	4.22	36	11.5

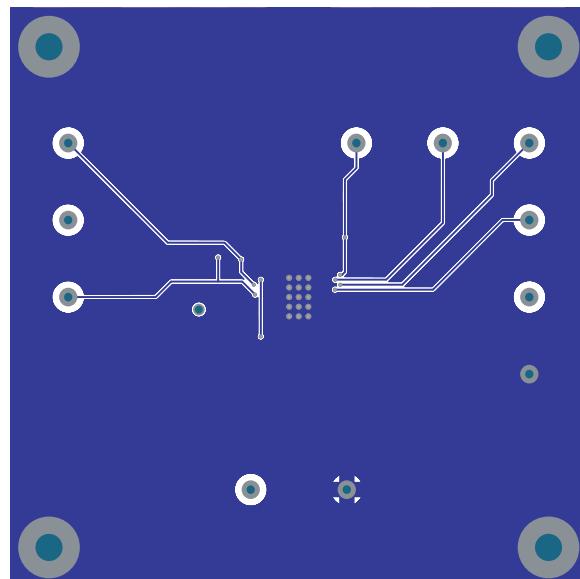
Demo Board Layout



TOP SILKSCREEN



TOP LAYER



BOTTOM LAYER