ESD Protection Diodes

Ultra Low Capacitance ESD Protection Diode for High Speed Data Line

ESD8101, ESD8111

The ESD81x1 Series ESD protection diodes are designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Low Capacitance (0.20 pF Typ, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.0/3.1
- MHL 2.0
- eSATA

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

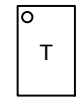
Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
ESD8101: IEC 61000−4−2 Contact IEC 61000−4−2 Air ESD8111: IEC 61000−4−2 Contact IEC 61000−4−2 Air	ESD	 ±23 ±23 ±30 ±30	 kV kV kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

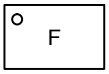
See Application Note AND8308/D for further description of survivability specs.

MARKING DIAGRAMS

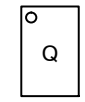
ESD8101 (01005)
DSN2
CASE 152AK



ESD8111 (0201)
WLCSP2
CASE 567AV

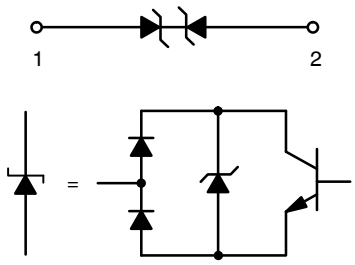


ESD8111P (0201)
X4DFN2
CASE 152AX



T, F, Q = Device Code

PIN CONFIGURATION AND SCHEMATIC



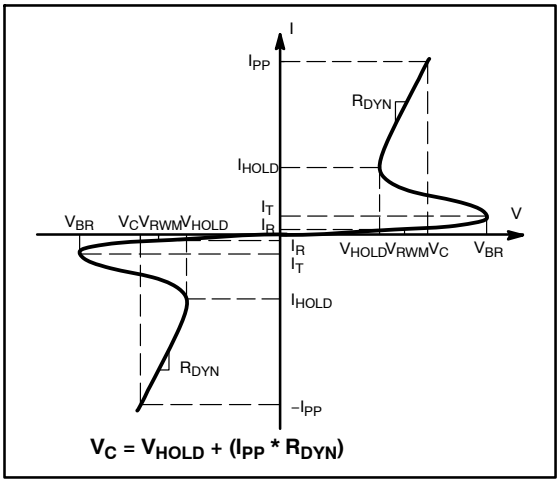
ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.5	7.9	8.6	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND			1.0	μA
Reverse Holding Voltage	V_{HOLD}	I/O Pin to GND		2.1		V
Holding Reverse Current	I_{HOLD}	I/O Pin to GND		17		mA
ESD8111 Clamping Voltage	V_C	I_{PP} = 7.1 A, (8/20 μs pulse)			8.0	V
ESD8101, ESD8111 Clamping Voltage TLP (Note 1)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		6.5		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)		10		
Dynamic Resistance	R_{DYN}	I/O Pin to GND		0.46		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		0.2	0.4	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

ORDERING INFORMATION

Device	Package	Shipping†
ESD8101FCT5G	DSN2 (Pb−Free)	10,000 / Tape & Reel
ESD8111FCT5G	WLCSP2 (Pb−Free)	10,000 / Tape & Reel
ESD8111PFCT5G	WLCSP2 Side wall Isolated 0201 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

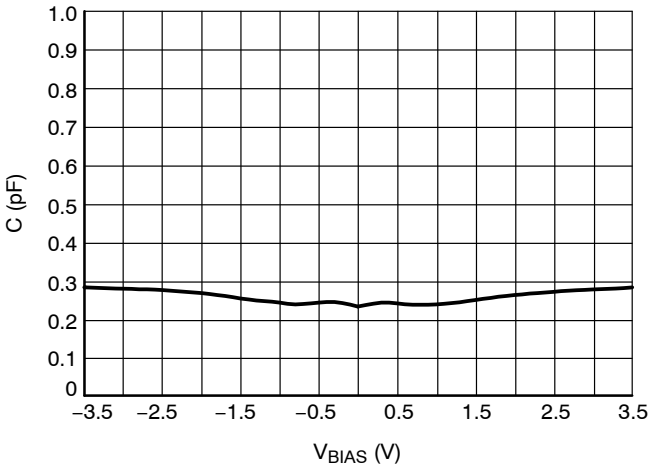


Figure 1. ESD8101 CV Characteristics

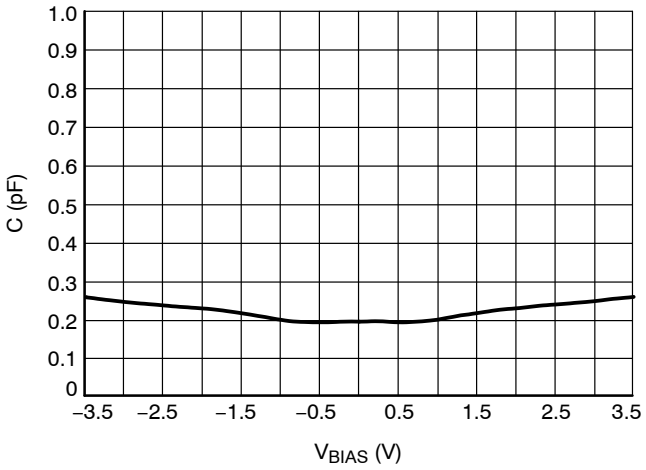


Figure 2. ESD8111 CV Characteristics

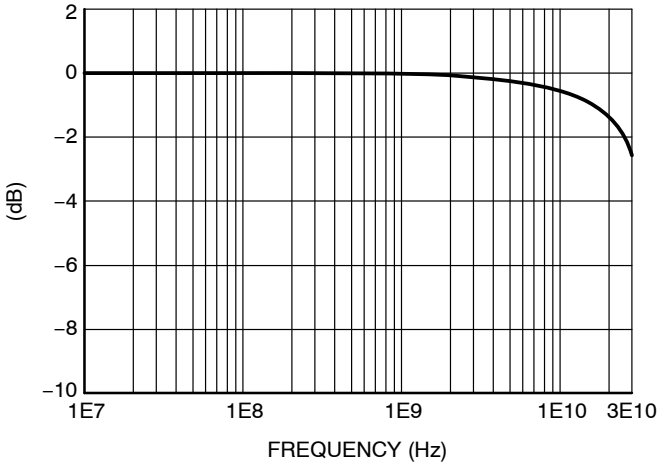


Figure 3. ESD8101 S21 Insertion Loss

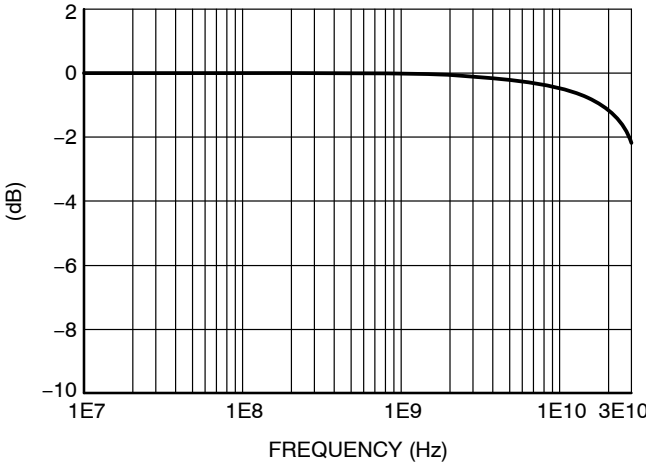


Figure 4. ESD8111 S21 Insertion Loss

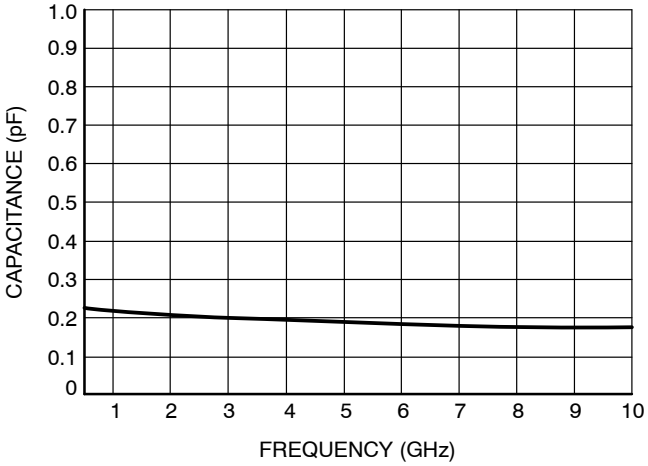


Figure 5. ESD8101 Capacitance over Frequency

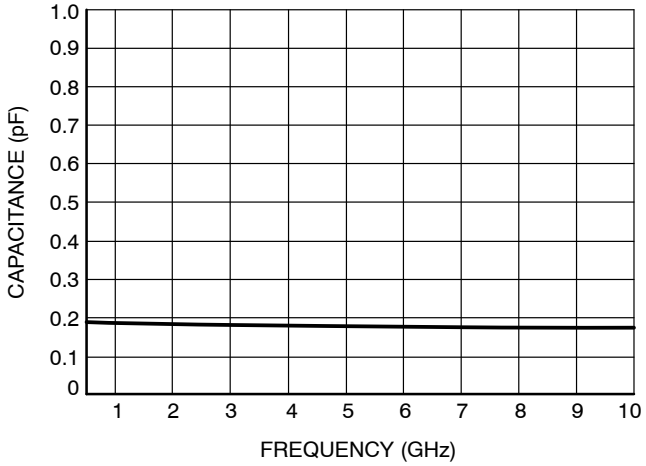


Figure 6. ESD8111 Capacitance over Frequency

TYPICAL CHARACTERISTICS

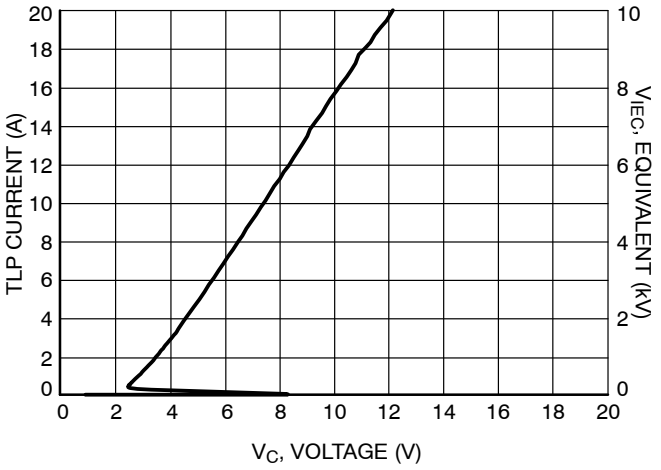


Figure 7. ESD8101 Positive TLP I–V Curve

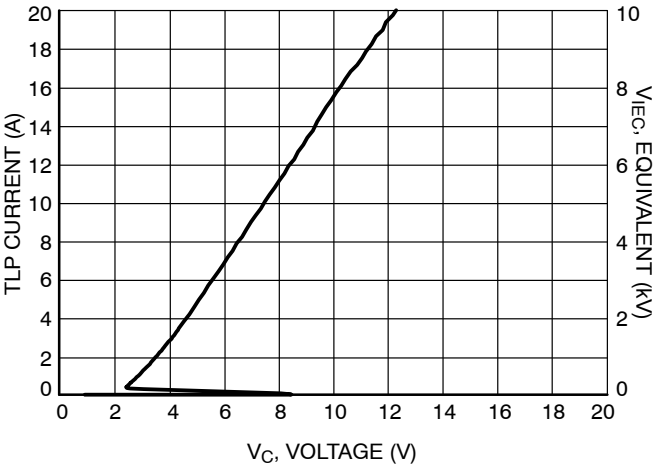


Figure 8. ESD8111 Positive TLP I–V Curve

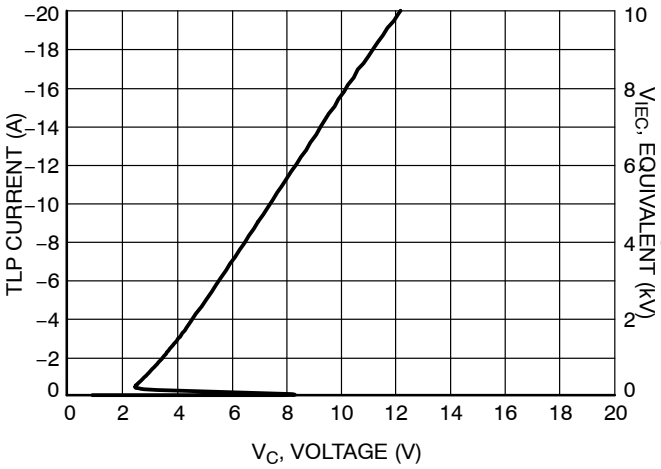


Figure 9. ESD8101 Negative TLP I–V Curve

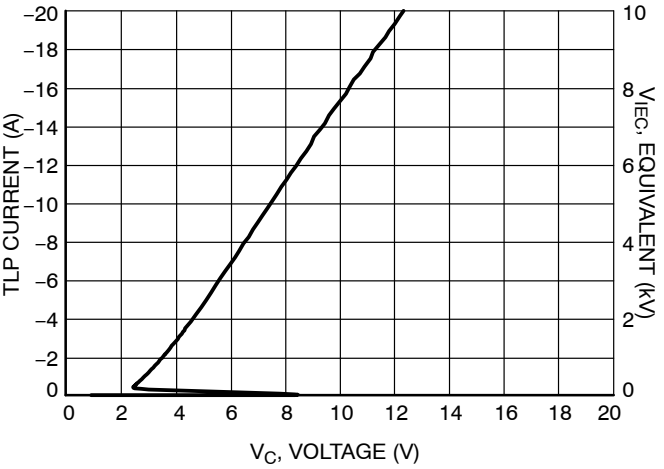


Figure 10. ESD8111 Negative TLP I–V Curve

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

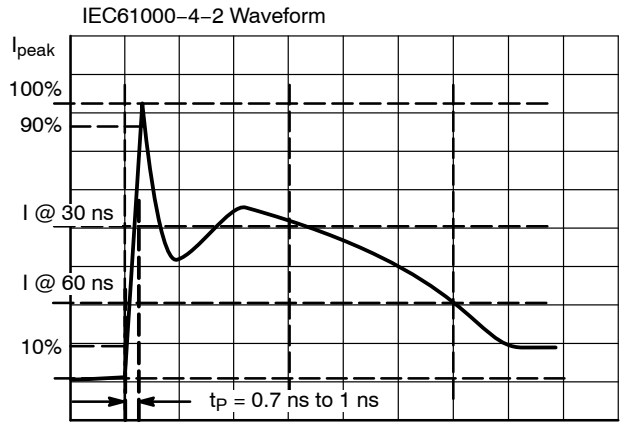


Figure 11. IEC61000−4−2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 12. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 13 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

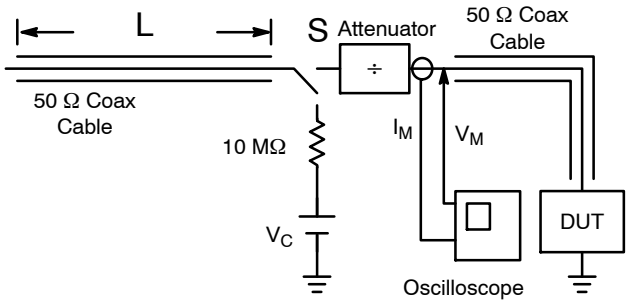


Figure 12. Simplified Schematic of a Typical TLP System

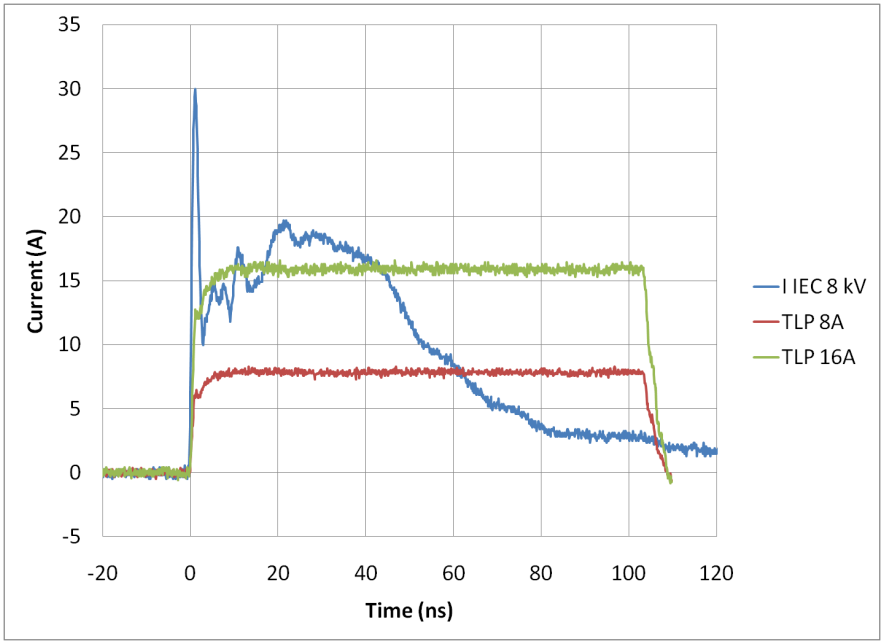
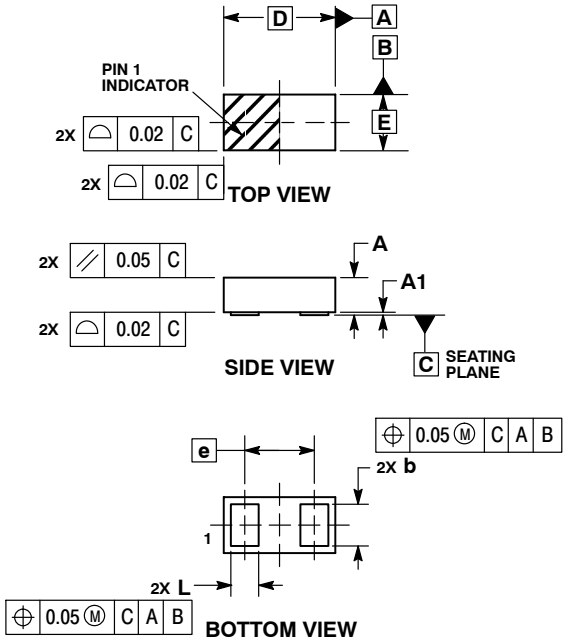


Figure 13. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

DSN2, 0.435x0.23, 0.27P, (01005)
CASE 152AK
ISSUE A

SCALE 16:1

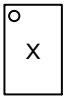
DATE 17 FEB 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.165	0.195
A1	---	0.030
b	0.177	0.193
D	0.435 BSC	
E	0.230 BSC	
e	0.270 BSC	
L	0.112	0.128

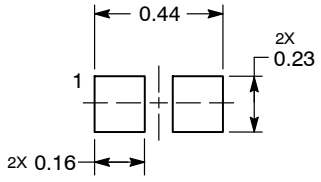
GENERIC MARKING DIAGRAM*



X = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON82198E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DSN2, 0.435X0.23, 0.27P (01005)**	**PAGE 1 OF 1**

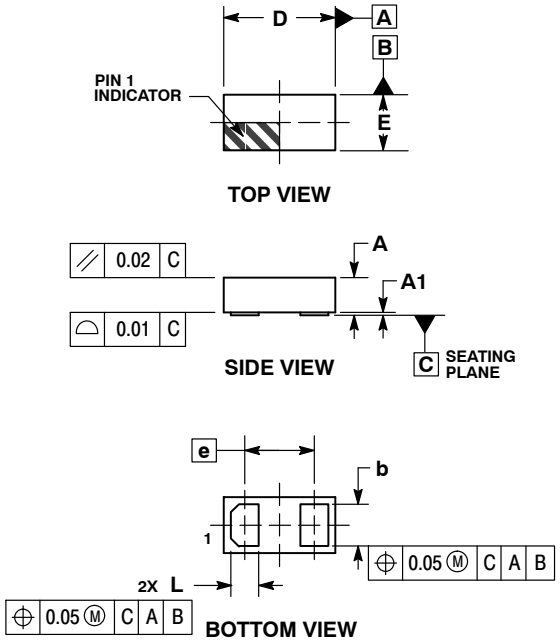
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

X4DFN2, 0.60x0.30, 0.36P
CASE 152AX
ISSUE G

SCALE 8:1

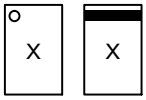
DATE 12 APR 2019



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.175	0.200	0.225
A1		0.018 REF	
b	0.205	0.215	0.225
D	0.575	0.600	0.625
E	0.275	0.300	0.325
e		0.36 BSC	
L	0.145	0.155	0.165

GENERIC MARKING DIAGRAM*



X = Specific Device Code

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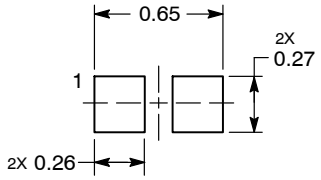
RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**X4DFN2, 0.60x0.30, 0.36P**	**PAGE 1 OF 1**

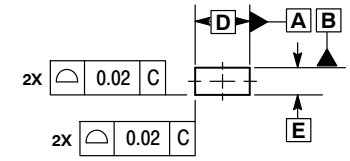
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

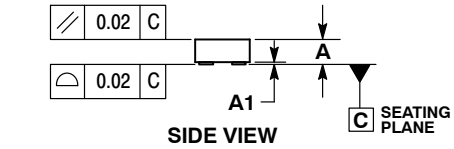
ON Semiconductor®

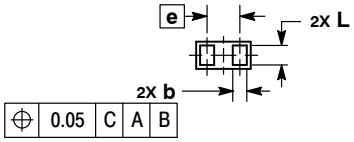
WLCSP2, 0.6x0.3
CASE 567AV
ISSUE C

DATE 22 SEP 2017

SCALE 12:1







NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

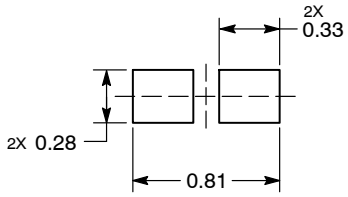
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.250	0.275	0.300
A1	0.000	0.025	0.050
b	0.140	0.155	0.170
D	0.570	0.600	0.630
E	0.270	0.300	0.330
e	0.36 BSC		
L	0.190	0.215	0.240

GENERIC MARKING DIAGRAM*

X = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**WLCSP2, 0.6X0.3**	**PAGE 1 OF 1**