ESDA25B1

Application Specific Discretes
A.S.D.™

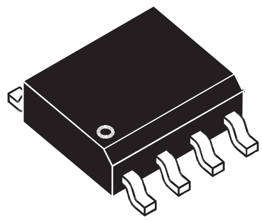
TRANSIL™ ARRAY FOR ESD PROTECTION

APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- COMPUTER
- PRINTERS
- COMMUNICATION SYSTEMS

It is particulary recommended for RS232 I/O port protection where the line interface withstands only 2 kV ESD surges.



SO-8

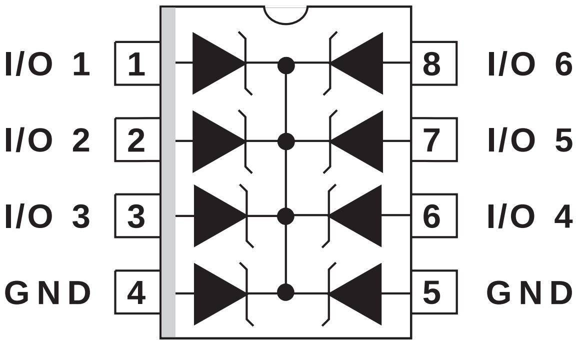
FEATURES

- 6 BIDIRECTIONAL TRANSIL™ FUNCTIONS
- VERY LOW CAPACITANCE : C= 20 pF @ V_{RM}
- 150 W peak pulse power (8/20 µs)

DESCRIPTION

The ESDA25B1 is a monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against EDS.

FUNCTIONAL DIAGRAM



BENEFITS

High ESD protection level : up to 25 kV
High integration
Suitable for high density boards

COMPLIES WITH THE FOLLOWING STANDARDS :

IEC 1000-4-2 : level 4

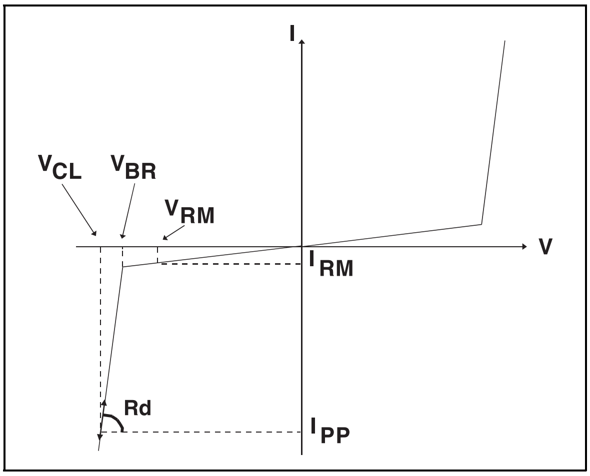
MIL STD 883C-Method 3015-6 : class 3
(human body model)

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
V_{PP}	Electrostatic discharge MIL STD 883C - Method 3015-6	25	kV
P_{PP}	Peak pulse power (8/20µs)	150	W
T_{stg} T_j	Storage temperature range Maximum junction temperature	- 55 to + 150 125	°C °C
T_L	Maximum lead temperature for soldering during 10s	260	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance
Rd	Dynamic resistance



Types	V_{BR} @		I_R	I_{RM} @	V_{RM}	Rd	αT	C
	min.	max.		max.		typ.	max.	typ.
	note 1			note 1		note 2	note 3	0V bias
	V	V	mA	µA	V	Ω	10^{-4}/°C	pF
ESDA25B1	25	30	1	2	24	1.5	9.7	15

note 1 : Between any I/O pin and Groung
note 2 : Square pulse, Ipp = 25A, tp=2.5µs.
note 3 : $\Delta V_{BR} = \alpha T$* (Tamb -25°C) * V_{BR} (25°C)

CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

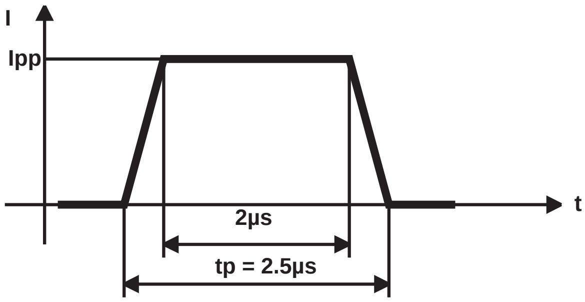
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL}. This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + Rd\ I_{PP}$$

Where Ipp is the peak current through the ESDA cell.

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20µs and 10/1000µs surges.



2.5µs duration measurement wave.

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

Fig. 1 : Peak power dissipation versus initial junction temperature.

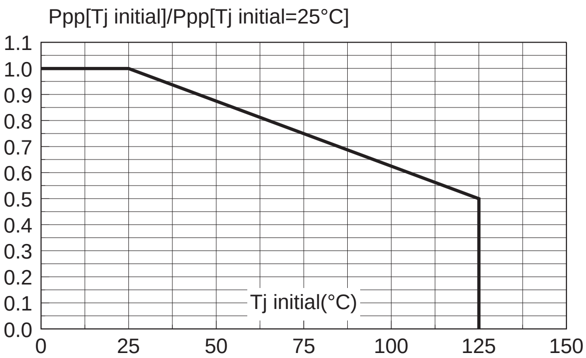


Fig. 2 : Peak pulse power versus exponential pulse duration (Tj initial = 25 °C).

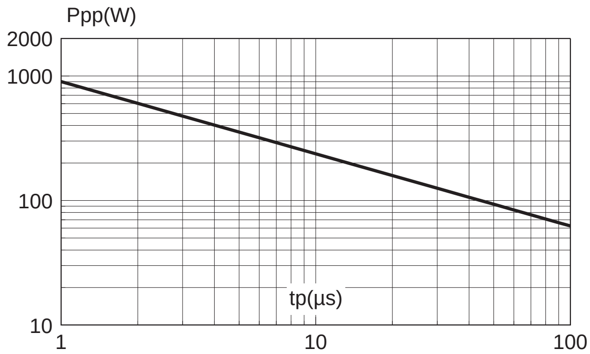


Fig. 3 : Clamping voltage versus peak pulse current (Tj initial = 25 °C).
Rectangular waveform tp = 2.5 µs.

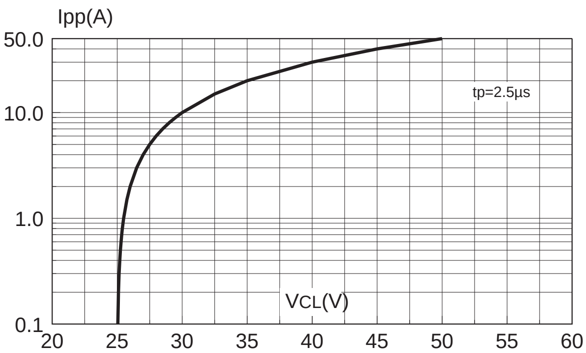


Fig. 4 : Capacitance versus reverse applied voltage (typical values).

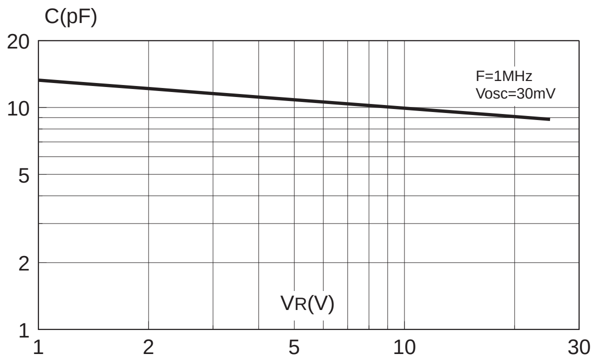


Fig. 5 : Relative variation of leakage current versus junction temperature (typical values).