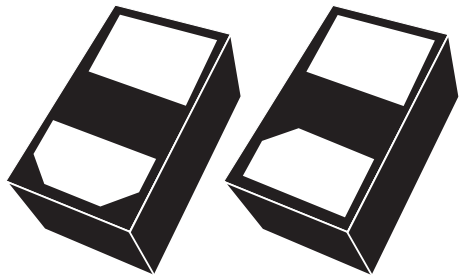
ESDARF02-1BU2CK

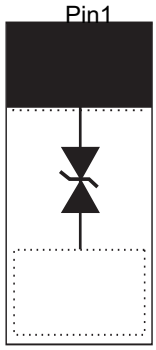
Single-line bidirectional ESD protection for high speed interface

Datasheet – production data



Pin1 available in different shapes
ST0201 package

Figure 1. Functional diagram (top view)



Features

- Bidirectional device
- Extra low diode capacitance: 0.2 pF
- Very high bandwidth: 30 GHz
- Low leakage current
- 0201 SMD package size compatible
- Ultra small PCB area: 0.18 mm^2
- ECOPACK®2 and RoHS compliant component

Complies with the following standards:

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phone and accessories
- Tablet PCs, netbooks and notebooks
- Portable multimedia devices and accessories
- Digital cameras and camcorders
- Communication and highly integrated systems

Description

The ESDARF02-1BU2CK is a bidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	 8 20	kV
P_{PP}	Peak pulse power (8/20 µs)	20	W
I_{PP}	Peak pulse current (8/20 µs)	1.5	A
T_j	Operating junction temperature range	-40 to +150	°C
T_{stg}	Storage temperature range	-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s	260	°C

Note: For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{RM}	=	Stand-off voltage
I_{RM}	=	Leakage current @ V_{RM}
I_{PP}	=	Peak pulse current
R_d	=	Dynamic impedance
αT	=	Voltage temperature coefficient
C	=	Parasite capacitance

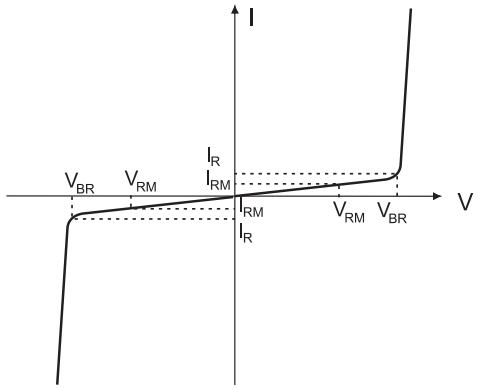


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	5	6.6		V
I_{RM}	V_{RM} = 3.6 V		5	100	nA
V_{CL}	I_{PP} = 1 A, 8/20 µA		10	12	V
R_d	Dynamic resistance, pulse duration 100 ns		1.3		Ω
C_{line}	F = (200 MHz- 3000 MHz), V_R = 0 V		0.2	0.3	pF
fc	-3 dB		30		GHz

Figure 3. Leakage current versus junction temperature (typical values)

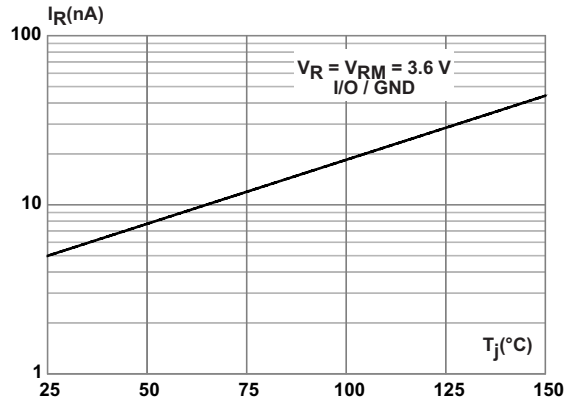


Figure 4. Junction capacitance versus frequency (typical values)

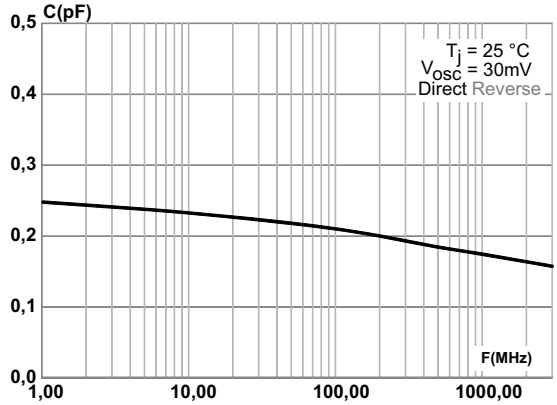


Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

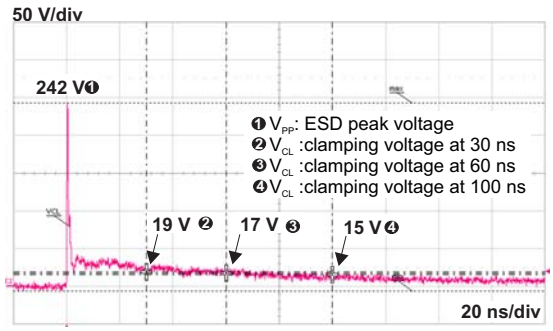


Figure 6. JESD response to IEC 61000-4-2 (-8 kV contact discharge)

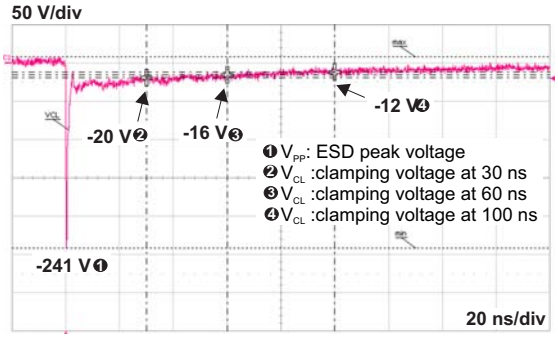


Figure 7. S21 attenuation measurement results

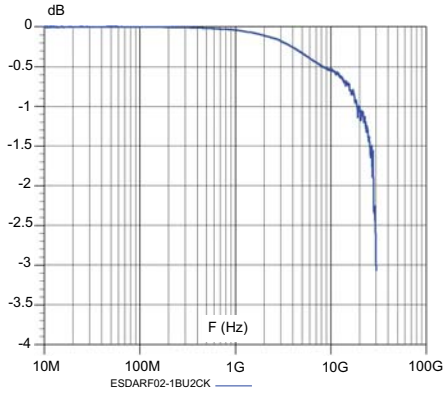
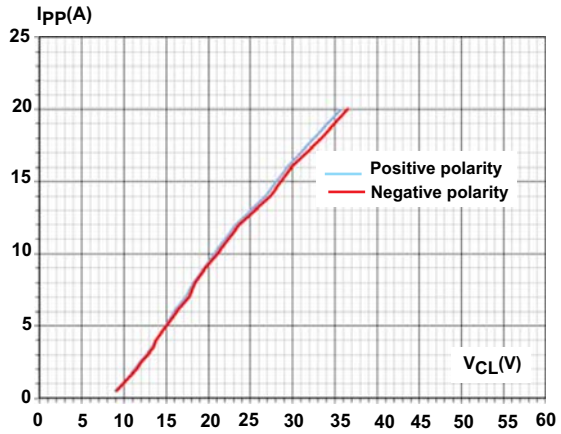


Figure 8. TLP measurements



2 Package information

- Epoxy meets UL94, V0
- Bar indicates pin 1

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

2.1 ST0201 package information

Figure 9. ST0201 package outline

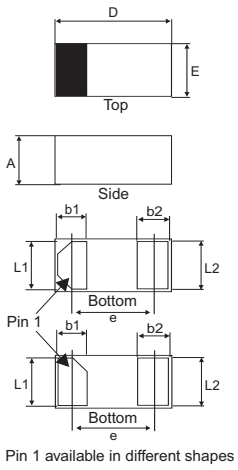


Table 3. 0201 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.23	0.28	0.33	0.0091	0.0110	0.0130
b1	0.20	0.25	0.30	0.0079	0.0098	0.0118
b2	0.20	0.25	0.30	0.0079	0.0098	0.0118
D	0.55	0.60	0.65	0.0217	0.0236	0.0256
E	0.25	0.30	0.35	0.0099	0.0118	0.0138
e		0.35			0.0138	
L1	0.13	0.18	0.23	0.0052	0.0071	0.0091
L2	0.14	0.19	0.24	0.0055	0.0075	0.0095

Figure 10. Footprint, dimensions in mm (inches)

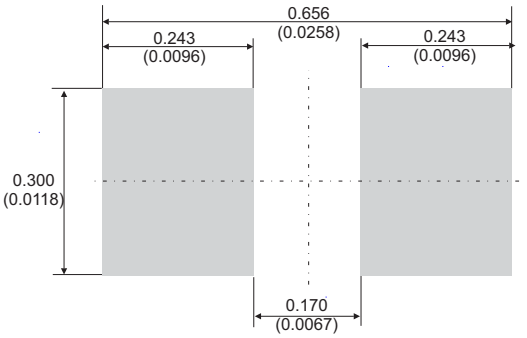
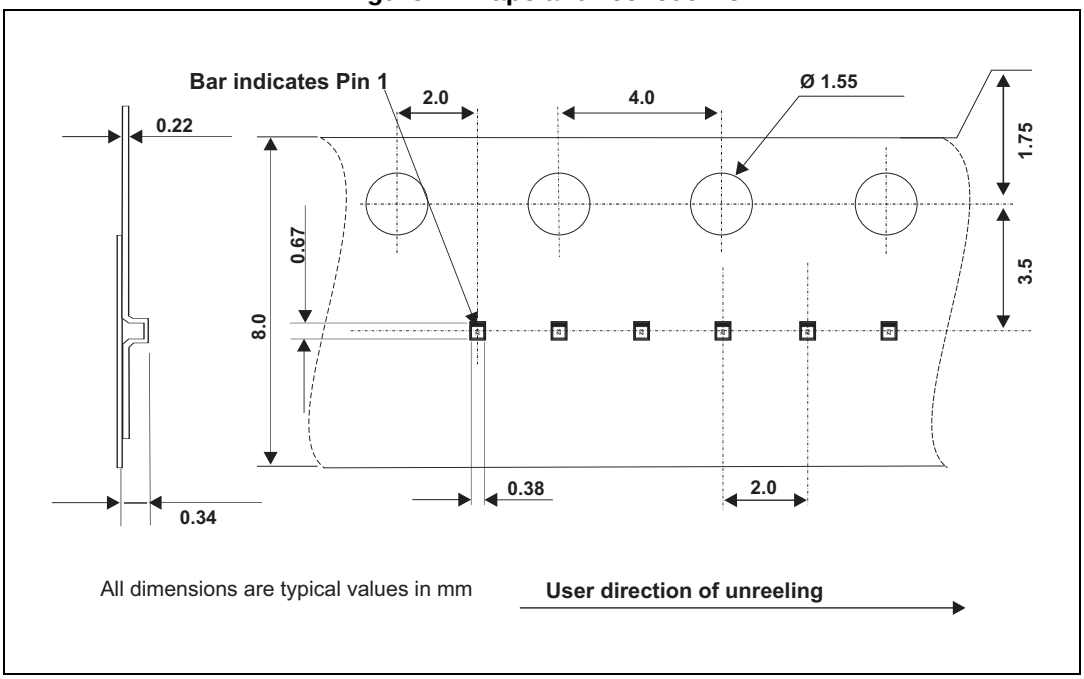


Figure 11. Marking

Note: Product marking may be rotated by 180° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

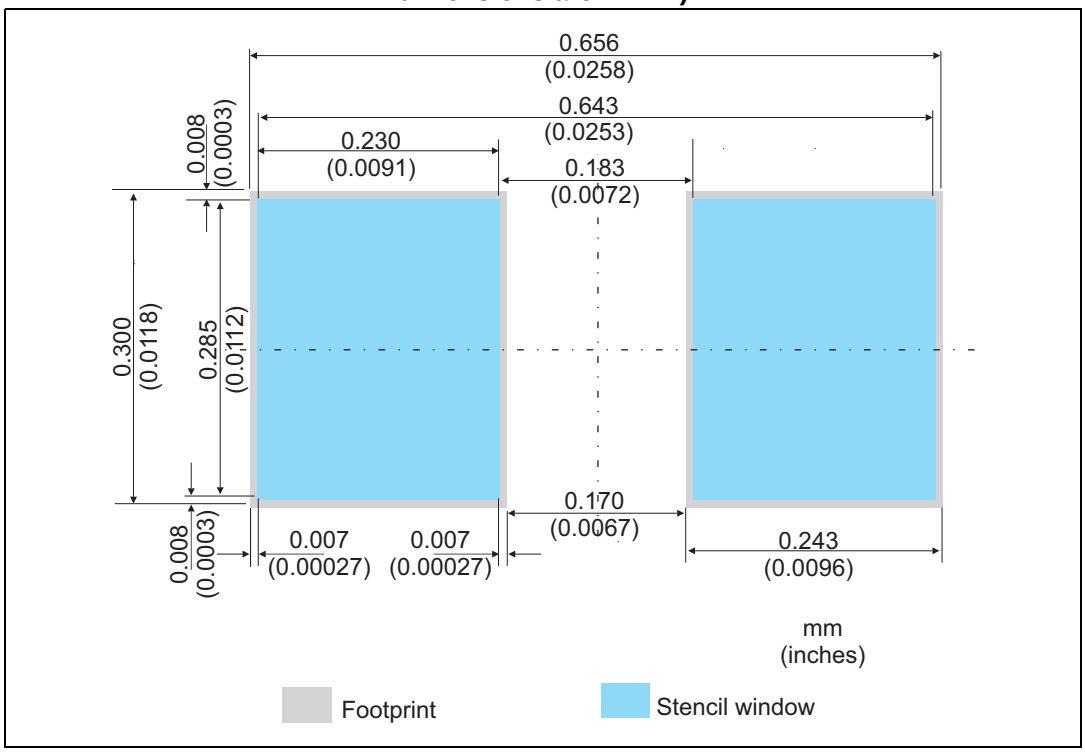
Figure 12. Tape and reel outline



3 Recommendation on PCB assembly

3.1 Stencil opening design

Figure 13. Recommended stencil windows-opening 90%/Thickness 80µm (all dimensions are in mm)



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: Type4 (powder particle size is 20-45 µm).

3.3 Placement

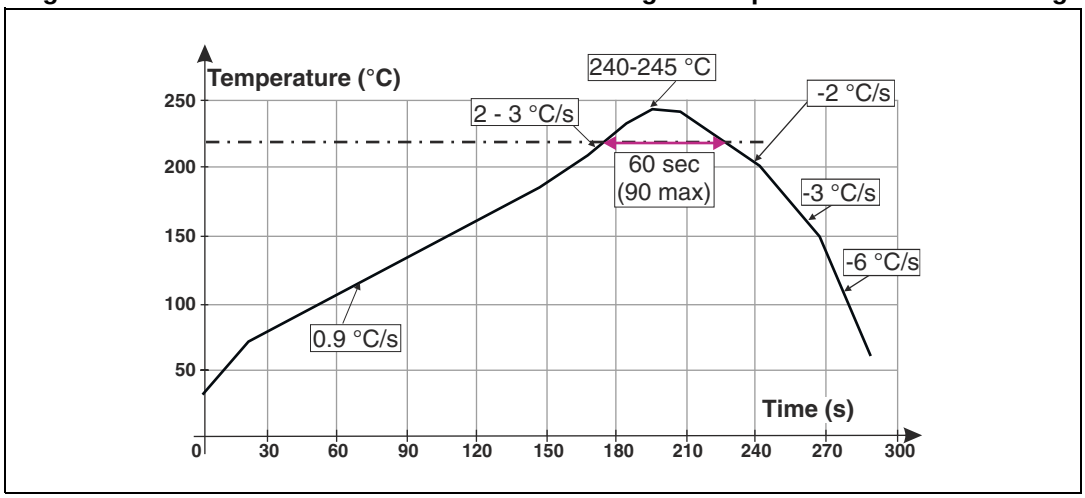
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 15. Ordering information scheme

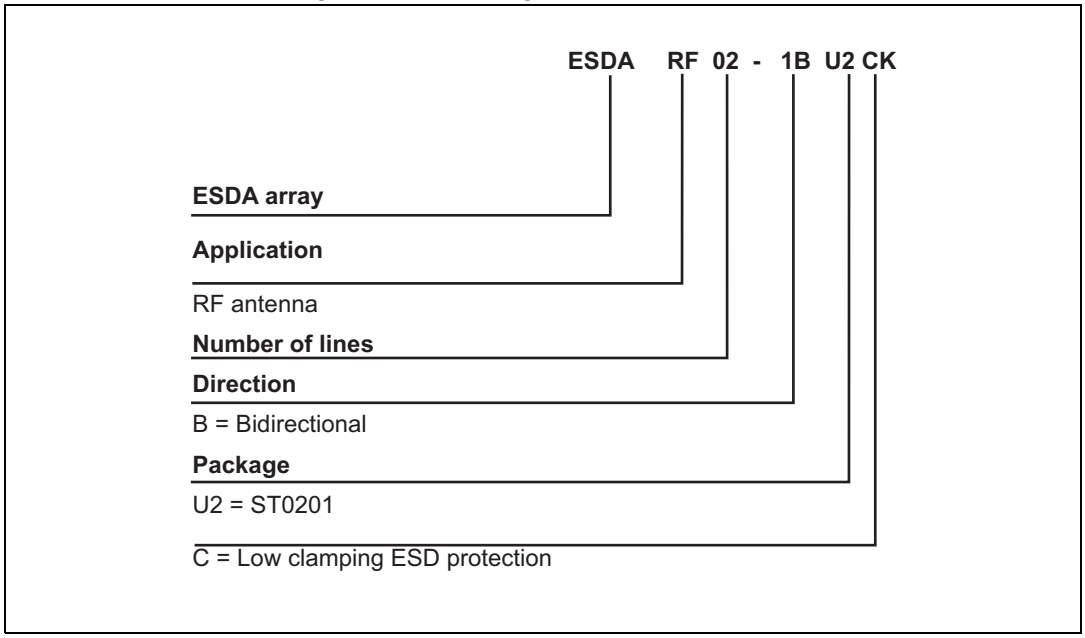


Table 4. Ordering information

Order code	Marking	Weight	Base qty.	Delivery mode
ESDARF02-1BU2CK	Z3(1)	0.124 mg	15000	Tape and reel

1. The marking can be rotated by 180° to differentiate assembly location

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
25-Feb-2015	1	Initial release.
02-Jun-2016	2	Updated *Features*. Updated *Table 2* and reformatted to current standard.
23-Jan-2017	3	Updated *Table 3*.