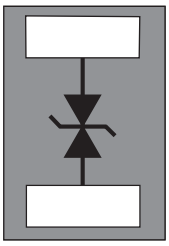
# ESDAULC5-1BF4

Datasheet

## Low clamping and ultra low capacitance single line bidirectional ESD protection


ST0201 package



| Product status link |
| --- |
| ESDAULC5-1BF4 |

## Features

- Low clamping voltage:
- Bidirectional diode
- Dynamic resistance Rd = 0.3 Ω typ.
- Low leakage current
- ST0201 package size compatible
- Ultra small PCB area: 0.18 mm²
- ECOPACK2 compliant component
- Complies with the following standards: IEC 61000-4-2 level 4
  - ±30 kV (air discharge)
  - ±30 kV (contact discharge)

## Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablet, PC, netbooks and notebooks
- Portable multimedia devices and accessories
- Digital cameras and camcorders
- Communication and highly integrated systems

## Description

The ESDAULC5-1BF4 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

# 1 Characteristics

**Table 1. Absolute maximum ratings ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{pp}$ (1) | Peak pulse voltage | IEC 61000-4-2 contact discharge<br>IEC 61000-4-2 air discharge | ±30<br>±30 | kV |
| $P_{pp}$ (1) | Peak pulse power (8/20 µs) | | 140 | W |
| $I_{pp}$ (1) | Peak pulse current (8/20 µs) | | 10 | A |
| $T_j$ | Operating junction temperature range | | -40 to 150 | °C |
| $T_{stg}$ | Storage junction temperature range | | -65 to 150 | |
| $T_L$ | Maximum lead temperature for soldering during 10 s | | 260 | |

1. *For a surge greater than the maximum values, the diode will fail in short-circuit.*

**Figure 1. Electrical characteristics (definitions)**

| Symbol | | Parameter |
|---|---|---|
| $V_{BR}$ | = | Breakdown voltage |
| $V_{CL}$ | = | Clamping voltage |
| $I_{RM}$ | = | Leakage current at $V_{RM}$ |
| $V_{RM}$ | = | Stand-off voltage |
| $I_{PP}$ | = | Peak pulse current |
| $R_d$ | = | Dynamic resistance |
| $\alpha T$ | = | Voltage temperature |
| $C_{LINE}$ | = | Line capacitance |

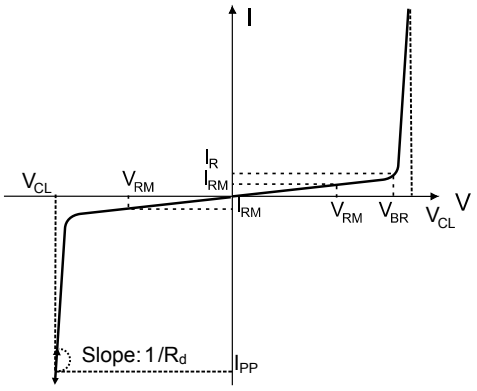



**Table 2. Electrical characteristics (values) ($T_{amb}$ = 25° C)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{BR}$ | Breakdown voltage | $I_R$ = 1 mA | 5.8 | | 8.5 | V |
| $I_{RM}$ | Leakage current | $V_{RM}$ = 3 V | | | 70 | nA |
| $V_{CL}$ | Clamping voltage | IEC 61000-4-2, 8 kV<br>contact measured at 30 ns | | 13.5 | | V |
| $R_D$ | Dynamic resistance, pulse duration 100 ns, I/O to GND | | | 0.3 | | Ω |
| $C_{LINE}$ | Line capacitance | $V_{LINE}$ = 0 V, F = 1 MHz, $V_{OSC}$ = 30 mV | | 1.5 | 3 | pF |

## 1.1 Characteristics (curves)

**Figure 2. Leakage current versus junction temperature (typical values)**

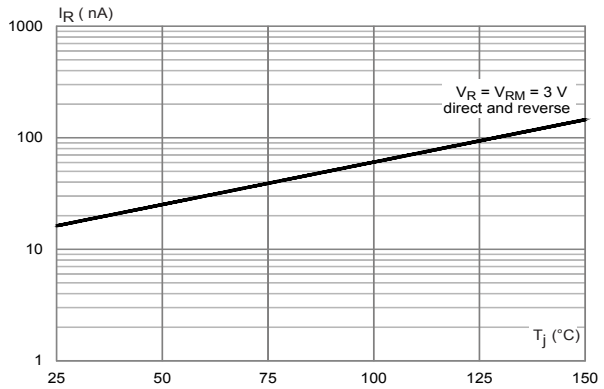



**Figure 3. S21 attenuation measurement result**

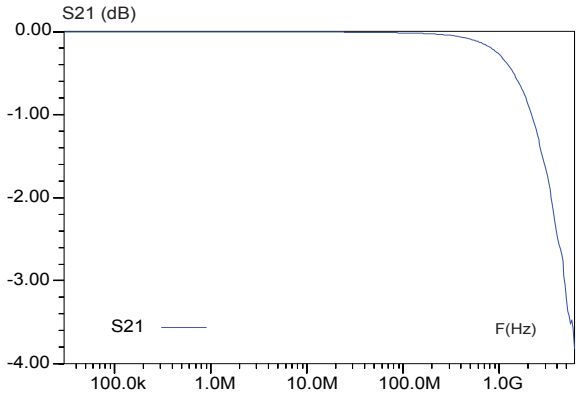



**Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)**

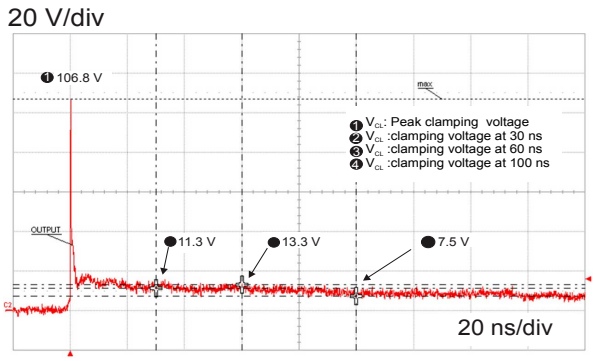



**Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)**

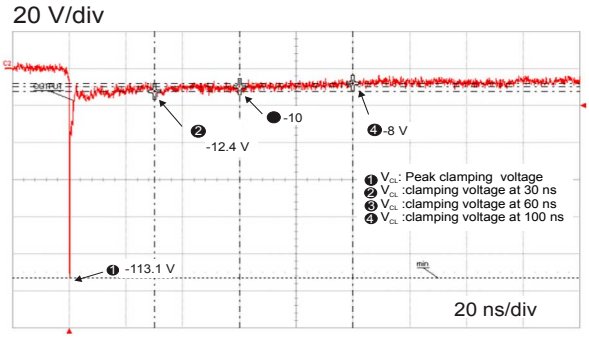
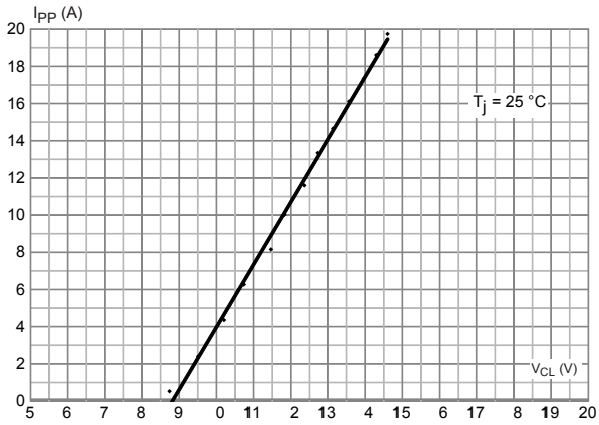



**Figure 6. TLP measurements**



# 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 2.1 ST0201 package information

**Figure 7. ST0201 package outline**

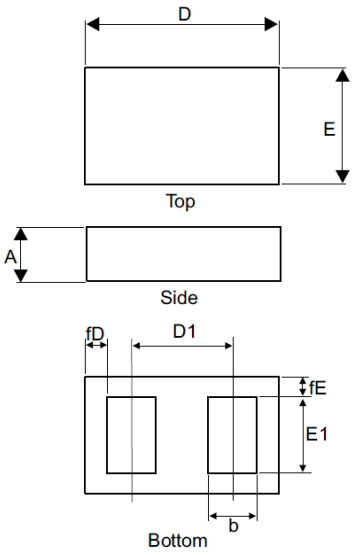



**Table 3. ST0201 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.280 | 0.300 | 0.320 | 0.0110 | 0.0118 | 0.0126 |
| b | 0.125 | 0.140 | 0.155 | 0.0049 | 0.0055 | 0.0061 |
| D | 0.570 | 0.600 | 0.630 | 0.0224 | 0.0236 | 0.0248 |
| D1 | | 0.350 | | | 0.0138 | |
| E | 0.270 | 0.300 | 0.330 | 0.0106 | 0.0118 | 0.0130 |
| E1 | 0.175 | 0.190 | 0.205 | 0.0069 | 0.0075 | 0.0081 |
| fD | 0.065 | 0.08 | 0.095 | 0.0026 | 0.0031 | 0.0037 |
| fE | 0.11 | 0.125 | 0.13 | 0.0043 | 0.0049 | 0.0051 |

**Figure 8. Footprint in mm (inches)**

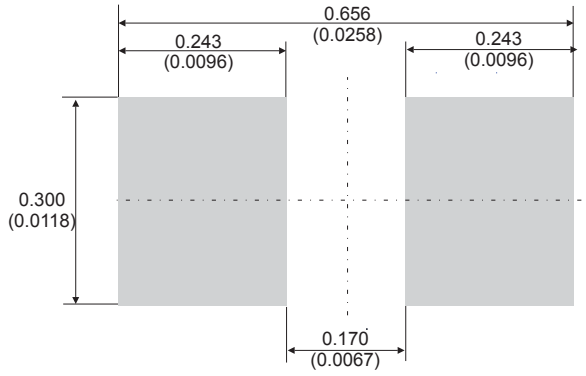
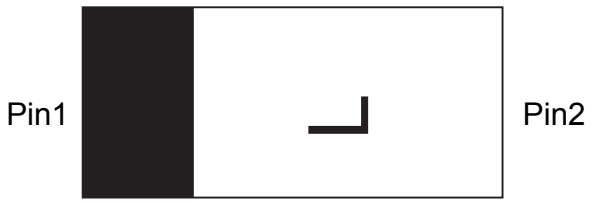
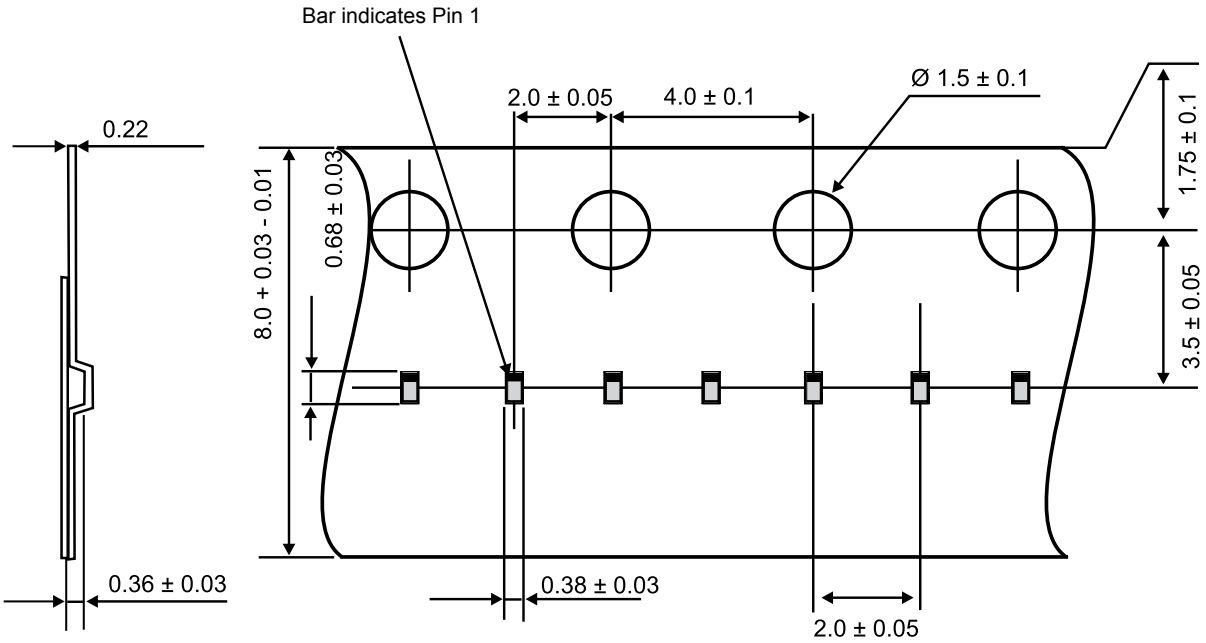



**Figure 9. Marking**




*Note: Marking can be rotated by 90° or 180° to differentiate assembly location.*

**Figure 10. Tape and reel specification**

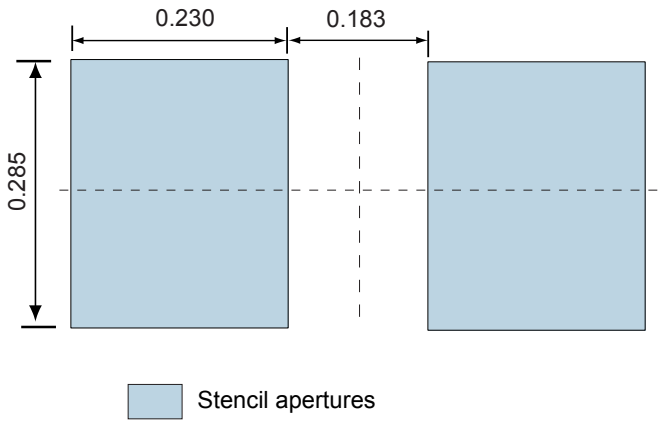


# 3 Recommendation on PCB assembly

## 3.1 Stencil opening design

1. Recommended design reference
   a. Stencil opening dimensions: 75 µm

**Figure 11. Stencil opening recommendations**



## 3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-48 µm.

## 3.3 Placement

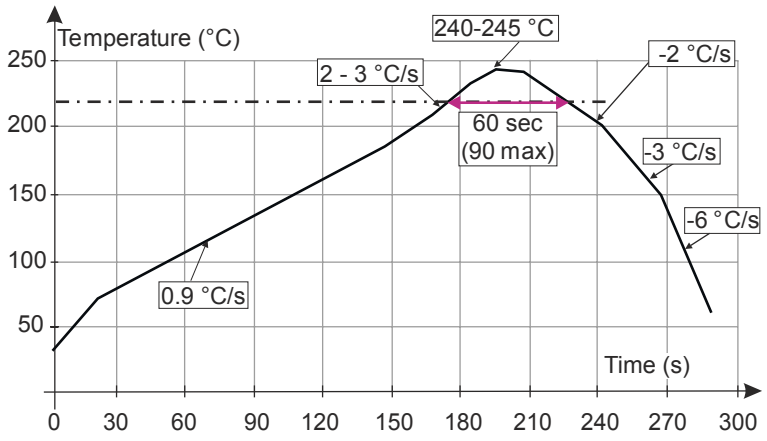
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

## 3.5 Reflow profile

**Figure 12. ST ECOPACK recommended soldering reflow profile for PCB mounting**




*Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.*

# 4 Ordering information

Figure 13. **Ordering information scheme**

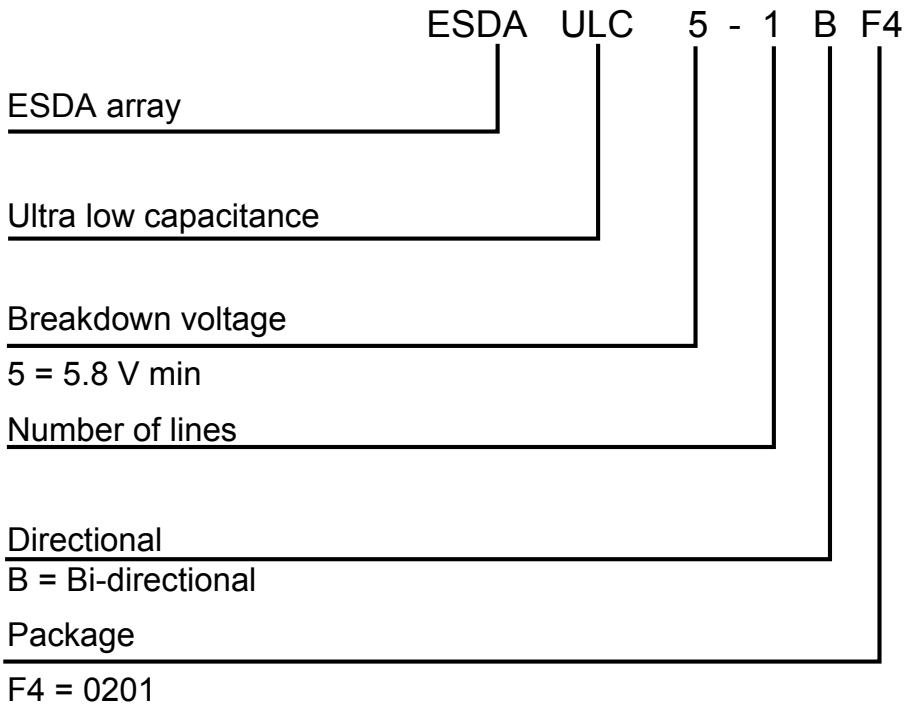



Table 4. **Ordering information**

| Order code | Marking | Package | Weight | Base qty. | Delivery mode |
|---|---|---|---|---|---|
| ESDAULC5-1F4 | L | ST0201 | 0.12 mg | 15000 | Tape and reel |

1. *The marking codes can be rotated by 90° or 180° to differentiate assembly location.*

## Revision history

Table 5. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 03-Jun-2014 | 1 | First issue. |
| 20-May-2021 | 2 | Removed all eye diagram figures. Minor text changes. |