24 GHz, ISM Band, Multichannel FMCW Radar Transmitter

Data Sheet

ADF5902

FEATURES

- 24 GHz to 24.25 GHz VCO (industrial, scientific, and medical (ISM) radio band)
- 2-channel 24 GHz power amplifier with 8 dBm output
- Single-ended outputs
- 2-channel muxed outputs with mute function
- Programmable output power
- LO output buffer
- RF frequency range: 24 GHz to 24.25 GHz
- Power control detector
- Auxiliary 8-bit ADC
- High and low speed FMCW ramp generation
- 25-bit fixed modulus allows subhertz frequency resolution
- PFD frequencies up to 110 MHz
- Normalized phase noise floor of −222 dBc/Hz
- Programmable charge pump currents
- ±5°C temperature sensor
- 4-wire SPI
- ESD performance
  - HBM: 2000 V
  - CDM: 250 V
- Qualified for automotive applications

APPLICATIONS

- Automotive radars
- Industrial radars
- Microwave radar sensors

GENERAL DESCRIPTION

The ADF5902 is a 24 GHz transmitter (Tx) monolithic microwave integrated circuit (MMIC) with an on-chip, 24 GHz voltage controlled oscillator (VCO). The VCO features a fractional-N frequency synthesizer with waveform generation capability with programmable grid array (PGA) and dual transmitter channels for radar systems. The on-chip, 24 GHz VCO generates the 24 GHz signal for the two transmitter channels and the local oscillator (LO) output. Each transmitter channel contains a power control circuit. There is also an on-chip temperature sensor.

Control of all the on-chip registers is through a simple, 4-wire serial peripheral interface (SPI).

The ADF5902 comes in a compact, 32-lead, 5 mm × 5 mm LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

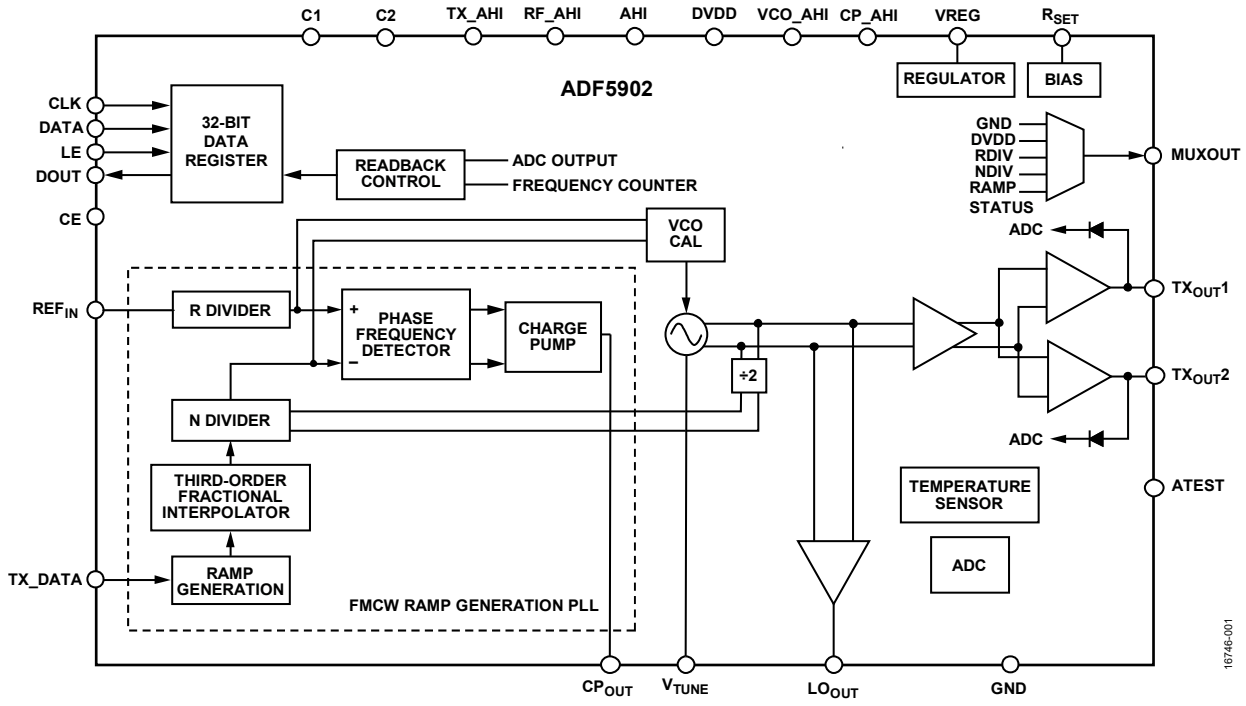

Figure 1.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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REVISION HISTORY

1/2020—Rev. 0 to Rev. A

Changes to Figure 23 ... 15
Changes to Figure 41 ... 30

11/2018—Revision 0: Initial Version

SPECIFICATIONS

AHI = TX_AHI = RF_AHI = VCO_AHI = DVDD = CP_AHI = 3.3 V ± 5%, GND = 0 V, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted. The operating temperature range is −40°C to +105°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING CONDITIONS					
RF Frequency Range	24		24.25	GHz	
VCO CHARACTERISTICS					
V_{TUNE}	0.5		2.5	V	
V_{TUNE} Impedance		100		kΩ	
VCO Phase Noise Performance					Closed-loop, 10 kHz loop filter
At 100 kHz Offset		−88		dBc/Hz	
At 1 MHz Offset		−108		dBc/Hz	
At 10 MHz Offset		−128		dBc/Hz	
Amplitude Noise		−150		dBc/Hz	At 1 MHz offset
Static Pulling VCO Frequency (f_{VCO}) Change vs. Load		±2		MHz	Open-loop into 2:1 voltage standing wave ratio (VSWR) load
Dynamic Pulling Transmitter On or Off Switch Change		±10		MHz	Open-loop
Dynamic Pulling Transmitter to Transmitter Switch Change		±5		MHz	Open-loop
Pushing f_{VCO} Change vs. AHI Change		±5		MHz/V	Open-loop
Spurious Level Harmonics		−30		dBc	
Spurious Level Nonharmonics		<−70		dBc	
POWER SUPPLIES					
AHI, TX_AHI, RF_AHI, VCO_AHI, DVDD, CP_AHI	3.135	3.3	3.465	V	
Total Current (I_{TOTAL})[1]		190		mA	
Software Power-Down Mode		1.2		mA	
Hardware Power-Down Mode		200		µA	
TRANSMITTER OUTPUT					
Output Power	2	8	12	dBm	
Output Impedance		50		Ω	
On to Off Isolation		30		dB	Single transmitter output switched on to off
Transmitter to Transmitter Isolation		25		dB	
Power-Up/Power-Down Time		200		ns	
LO OUTPUT					
Output Power	−7	−1	+5	dBm	
Output Impedance		50		Ω	
On to Off Isolation		35		dB	
PHASE FREQUENCY DETECTOR (PFD)					
Phase Detector Frequency[2]			110	MHz	
CHARGE PUMP					
Charge Pump Current (I_{CP}) Sink and Source Current					Programmable
High Value		4.48		mA	R_{SET} = 5.1 kΩ; R_{SET} is a resistor to ground that sets the maximum charge pump output current
Low Value		280		µA	
Absolute Accuracy		2.5		%	R_{SET} = 5.1 kΩ
R_{SET} Range	5.049	5.1	5.151	kΩ	
I_{CP} Tristate Leakage Current		1		nA	Sink and source current
Sink and Source Matching		2		%	0.5 V < charge pump voltage (V_{CP}) < CP_AHI − 0.6 V
I_{CP} vs. V_{CP}		2		%	0.5 V < V_{CP} < CP_AHI − 0.6 V
I_{CP} vs. Temperature		2		%	V_{CP} = CP_AHI/2

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor, Fractional-N Mode[3]		−222		dBc/Hz	PLL loop bandwidth (BW) = 1 MHz
Normalized 1/f Noise (PN_{1_f})[4]		−120		dBc/Hz	Measured at 10 kHz offset, normalized to 1 GHz
TEMPERATURE SENSOR					
Analog Accuracy		±5		°C	Following one point calibration
Digital Accuracy		±5		°C	Following one point calibration
Sensitivity		6.4		mV/°C	
ANALOG-TO-DIGITAL CONVERTER (ADC)					
Resolution		8		Bits	
Integral Nonlinearity (INL)		±1		LSB	
Differential Nonlinearity (DNL)		±1		LSB	
Least Significant Bit (LSB)		7.4		mV	
REF_{IN} CHARACTERISITICS					
REF_{IN} Input Frequency	10		260	MHz	−5 dBm minimum to +9 dBm maximum biased at AHI/2 (ac coupling ensures 1.8 ÷ 2 bias); for frequencies < 10 MHz, use a dc-coupled, CMOS-compatible square wave with a slew rate > 25 V/µs
REF_{IN} Input Capacitance[2]			1.2	pF	
REF_{IN} Input Current			±100	µA	
LOGIC INPUTS					
Input Voltage					
High (V_{IH})	1.4			V	
Low (V_{IL})			0.6	V	
Input Current (I_{INH}, I_{INL})			±1	µA	
Input Capacitance (C_{IN})[2]			10	pF	
LOGIC OUTPUTS					
Output Voltage					
High (V_{OH})[5]	DVDD − 0.4			V	
Low (V_{OL})			0.4	V	
Output Current					
High (I_{OH})			500	µA	
Low (I_{OL})			500	µA	

[1] Following the initialization sequence described in the Initialization Sequence section, T_A = 25°C, AHI = 3.3 V, f_{REFIN} = 100 MHz, and RF = 24.025 GHz.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] This specification can be used to calculate phase noise for any application. Use the formula ((Normalized Phase Noise Floor) + 10 log(f_{PFD}) + 20 logN) to calculate in-band phase noise performance as seen at the VCO output.
[4] The PLL phase noise is composed of flicker (1/f) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at an offset frequency (f) is given by PN = PN_{1_f} + 10 log(10 kHz/f) + 20 log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[5] DVDD selected from the IO level bit (Bit DB11 in Register 3).

TIMING SPECIFICATIONS

Write Timing Specifications

AHI = TX_AHI = RF_AHI = VCO_AHI = DVDD = CP_AHI = 3.3 V ± 5%, GND = 0 V, dBm referred to 50 Ω, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. The operating temperature range is −40°C to +105°C.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width
t_8	10	ns max	LE setup time to DOUT
t_9	15	ns max	CLK setup time to DOUT

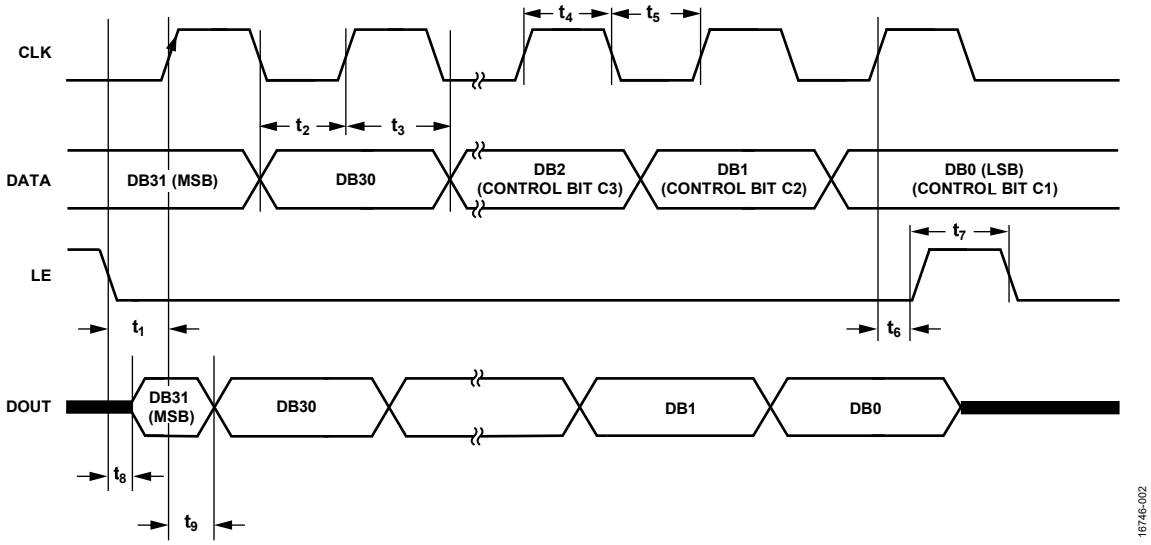

Figure 2. Write Timing Diagram

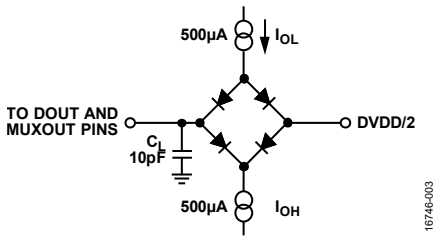

Figure 3. Load Circuit for DOUT/MUXOUT Timing, C_L = 10 pF

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AHI to GND	−0.3 V to +3.9 V
AHI to TX_AHI	−0.3 V to +0.3 V
AHI to RF_AHI	−0.3 V to +0.3 V
AHI to VCO_AHI	−0.3 V to +0.3 V
AHI to DVDD	−0.3 V to +0.3 V
AHI to CP_AHI	−0.3 V to +0.3 V
V_{TUNE} to GND	−0.3 V to +3.6 V
Digital Input/Output Voltage to GND	−0.3 V to DVDD + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Electrostatic Discharge (ESD)	
Charged Device Model (CDM)	250 V
Human Body Model (HBM)	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The ADF5902 is a high performance RF integrated circuit with an ESD rating of 2 kV and is ESD sensitive. Take proper precautions for handling and assembly.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-32-12[3]	48.18	26.86	°C/W

[1] θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.
[2] θ_{JC} is the junction-to-case thermal resistance.
[3] Test Condition 1: thermal impedance simulated values are based on use of a PCB with the thermal impedance pad soldered to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

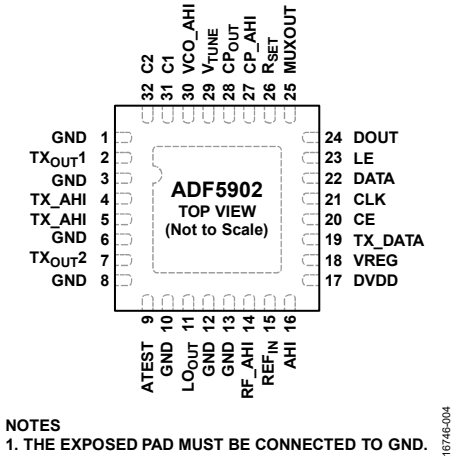

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 6, 8, 10, 12, 13	GND	RF Ground. Tie all GND pins together.
2	$TX_{OUT}1$	24 GHz Transmitter Output 1.
4, 5	TX_AHI	Voltage Supply for the Transmitter Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. TX_AHI must be the same value as AHI.
7	$TX_{OUT}2$	24 GHz Transmitter Output 2.
9	ATEST	Analog Test Output Pin.
11	LO_{OUT}	LO Output.
14	RF_AHI	Voltage Supply for the RF Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. RF_AHI must be the same value as AHI.
15	REF_{IN}	Reference Input. This pin is a CMOS input with a nominal threshold of DVDD/2 and a dc equivalent input resistance of 100 kΩ. See Figure 17. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
16	AHI	Voltage Supply for the Analog Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin.
17	DVDD	Digital Power Supply. This supply may range from 3.135 V to 3.465 V. Place decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. DVDD must be the same value as AHI.
18	VREG	Internal 1.8 V Regulator Output. Connect a 220 nF capacitor to ground as close as possible to this pin.
19	TX_DATA	Transmit Data Pin. This pin controls some of the ramping functionality. Synchronize the rising edge of the TX_DATA signal to the rising edge of REF_{IN}.
20	CE	Chip Enable. A logic low on this pin powers down the device. Taking the pin high powers up the device.
21	CLK	Serial Clock Input. This serial clock input clocks in the serial data to the registers. The data is latched into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
22	DATA	Serial Data Input. The serial data is loaded MSB first with the four LSBs as the control bits. This input is a high impedance CMOS input.
23	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded to one of the 18 latches with the latch selected via the control bits.
24	DOUT	Serial Data Output.
25	MUXOUT	Multiplexer Output. This multiplexer output allows various internal signals to be accessed externally.
26	R_{SET}	Resistor Setting Pin. Connecting a 5.1 kΩ resistor between this pin and GND sets an internal current. The nominal voltage potential at the R_{SET} pin is 0.62 V.
27	CP_AHI	Charge Pump Power Supply. This supply may range from 3.135 V to 3.465 V. Place decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. CP_AHI must be the same value as AHI.
28	CP_{OUT}	Charge Pump Output. When the charge pump is enabled, this output provides $\pm I_{CP}$ to the external loop filter, which, in turn, drives the VCO.

Pin No.	Mnemonic	Description
29	V_{TUNE}	Control Input to the VCO. This voltage determines the output.
30	VCO_AHI	Voltage Supply for the VCO Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. VCO_AHI must be the same value as AHI.
31	C1	Decoupling Capacitor 1. Place a 47 nF capacitor to ground as close as possible to this pin.
32	C2	Decoupling Capacitor 2. Place a 220 nF capacitor to ground as close as possible to this pin.
	EP	Exposed Pad. The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

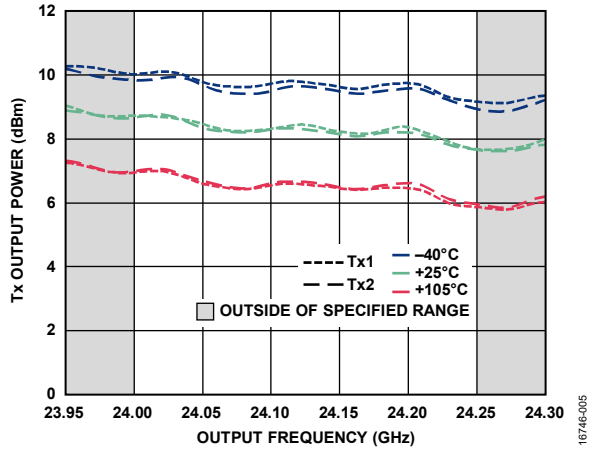

Figure 5. Transmitter (Tx) Output Power vs. Output Frequency

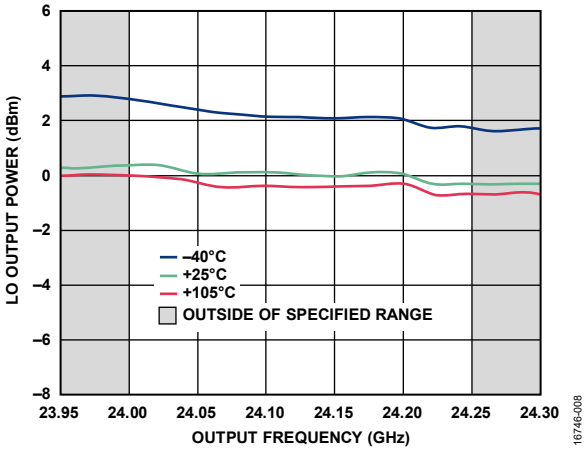

Figure 8. LO Output Power vs. Output Frequency

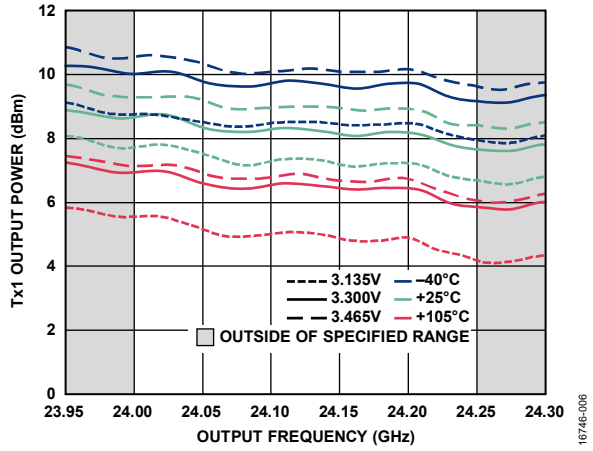

Figure 6. Transmitter 1 (Tx1) Output Power Variation vs. Output Frequency with Temperature and Supply

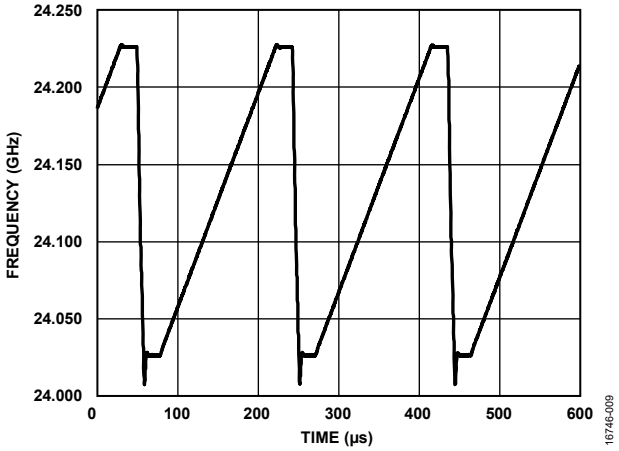

Figure 9. Triangular Ramp with Delay

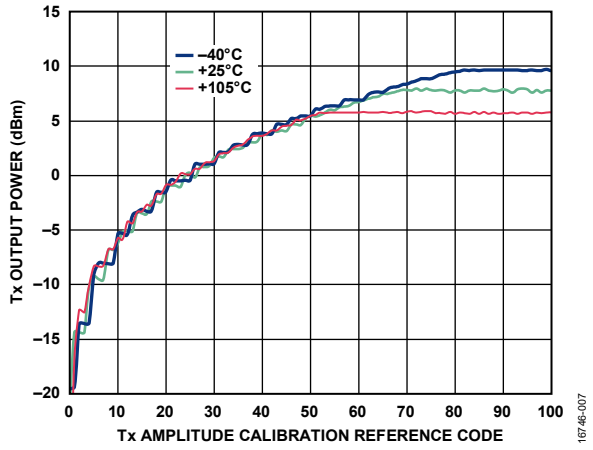

Figure 7. Transmitter (Tx) Output Power vs. Transmitter (Tx) Amplitude Calibration Reference Code

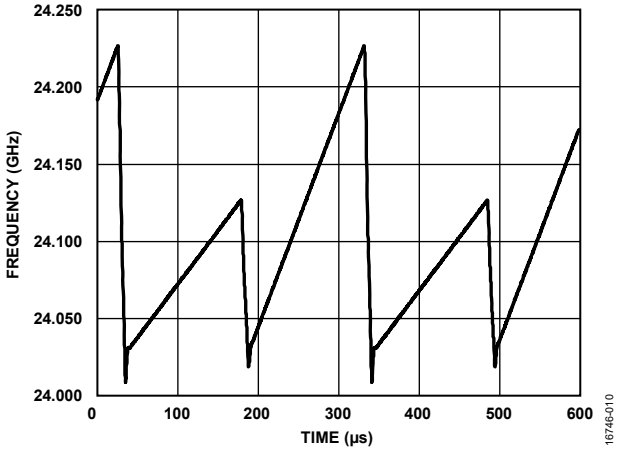

Figure 10. Dual Triangular Ramp

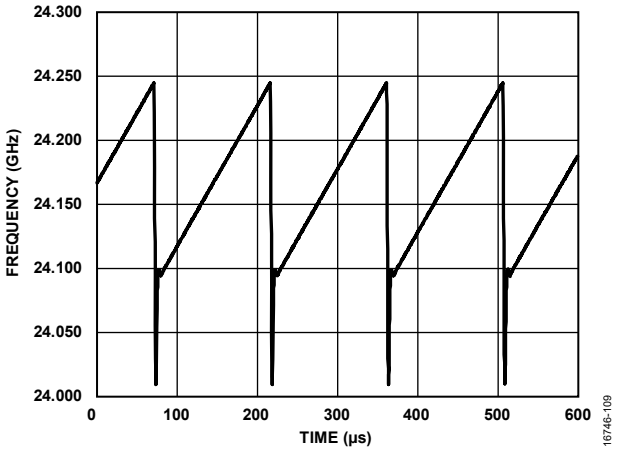

Figure 11. Sawtooth Ramp

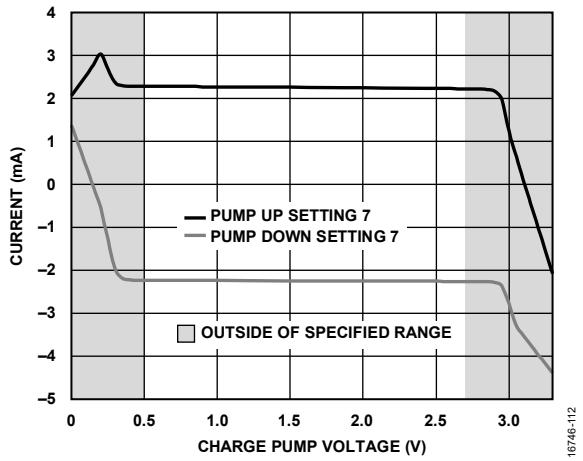

Figure 14. Charge Pump Output Characteristics, CP_AHI = 3.3 V, at 25°C

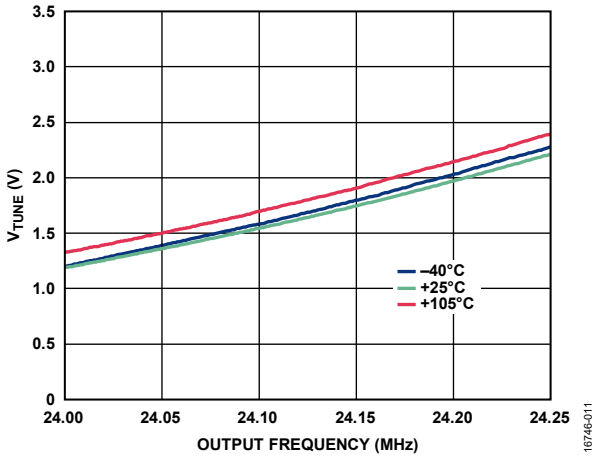

Figure 12. V_{TUNE} Frequency Range

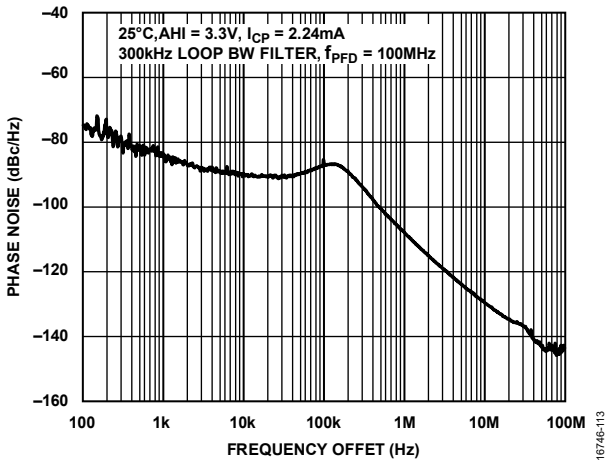

Figure 15. Closed-Loop Phase Noise on Transmitter 1 at 24.125 GHz

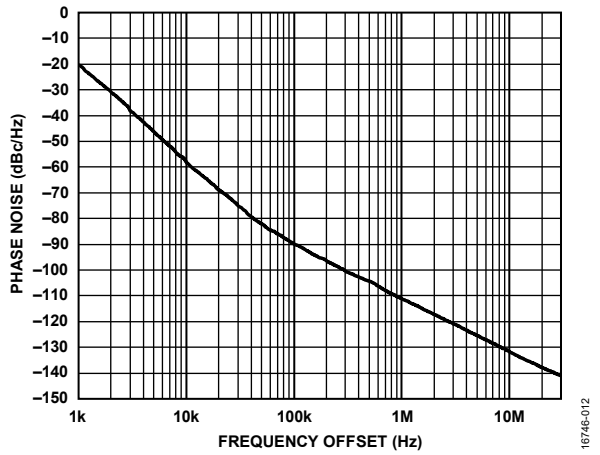

Figure 13. Open-Loop Phase Noise on Transmitter 1 Output at 24.125 GHz

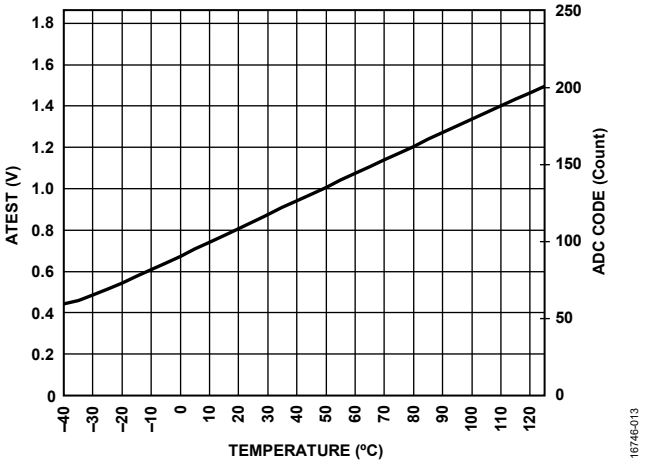

Figure 16. ATEST Voltage and ADC Code vs. Temperature

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 17. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This configuration ensures that there is no loading of the REF_{IN} pin on power-down.

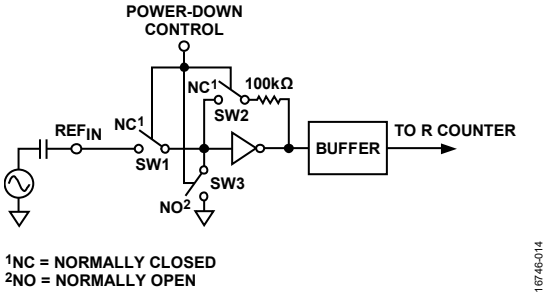

Figure 17. Reference Input Stage

RF INT DIVIDER

The RF INT counter allows a division ratio in the RF feedback counter. Division ratios from 75 to 4095 are allowed.

INT, FRAC, AND R RELATIONSHIP

Generate the RF VCO frequency (RF_{OUT}) using the INT and FRAC values in conjunction with the R counter, as follows:

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/2^{25})) \times 2 \quad (1)$$

where:

RF_{OUT} is the output frequency of the internal VCO.

f_{PFD} is the phase frequency detector (PFD) frequency.

INT is the preset divide ratio of the binary 12-bit counter (75 to 4095).

FRAC is the numerator of the fractional division (0 to $2^{25} - 1$).

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (2)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit (0 or 1).

R is the preset divide ratio of the binary, 5-bit, programmable reference counter (1 to 32).

T is the REF_{IN} divide by 2 bit (0 or 1).

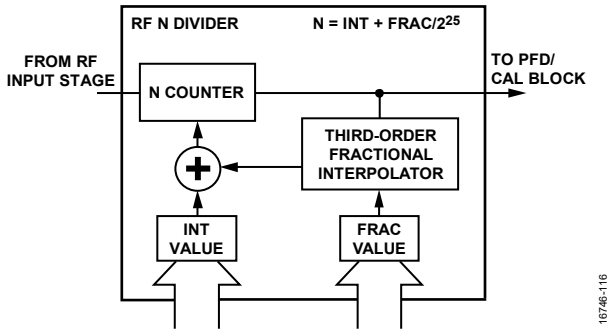

Figure 18. RF N Divider

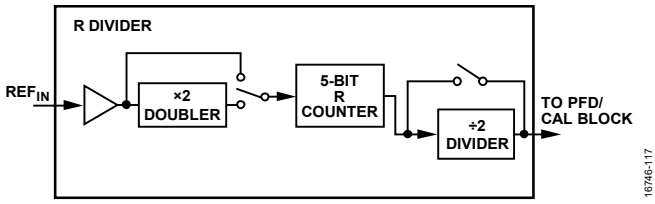

Figure 19. Reference Divider

R COUNTER

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to supply the reference clock to the PFD and VCO calibration block. Division ratios from 1 to 32 are allowed.

PFD AND CHARGE PUMP

The PFD receives inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 20 shows a simplified schematic of the PFD.

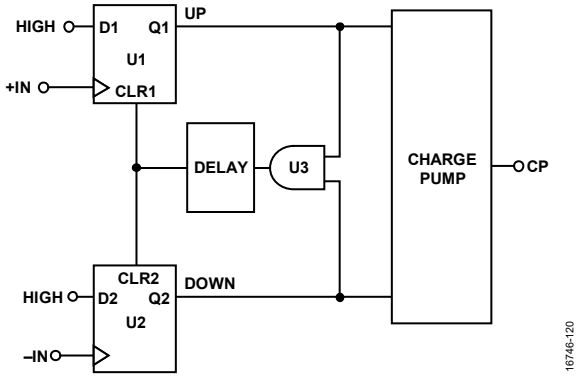

Figure 20. PFD Simplified Schematic

The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 1 ns. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level.

INPUT SHIFT REGISTER

The ADF5902 digital section includes a 5-bit RF R counter, a 12-bit RF N counter, and a 25-bit FRAC counter. Data is clocked to the 32-bit input shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input shift register to one of 18 latches on the rising edge of LE. The destination latch is determined by the state of the five control bits (C5, C4, C3, C2, and C1) in the input shift register. These are the five LSBs (DB4, DB3, DB2, DB1, and DB0, respectively), as shown in Figure 2. Table 6 shows the truth table for these bits. Figure 21 and Figure 22 show a summary of how the latches are programmed.

PROGRAM MODES

Table 6 and Figure 24 through Figure 42 show how to set up the program modes in the ADF5902.

Several settings in the ADF5902 are double buffered. These include the LSB fractional value, R counter value (R divider), reference doubler, clock divider, RDIV2, and MUXOUT. This means that two events must occur before the device uses a new value for any of the double buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R5.

For example, updating the fractional value can involve a write to the 13 LSB bits in Register R6 and the 12 MSB bits in Register R5. Write to Register R6 first, followed by the write to Register R5. The frequency change begins after the write to Register R5. Double buffering ensures that the bits written to in Register R6 do not take effect until after the write to Register R5.

Table 6. C5, C4, C3, C2, and C1 Truth Table

Control Bits					
C5 (DB4)	**C4 (DB3)**	**C3 (DB2)**	**C2 (DB1)**	**C1 (DB0)**	**Register**
0	0	0	0	0	R0
0	0	0	0	1	R1
0	0	0	1	0	R2
0	0	0	1	1	R3
0	0	1	0	0	R4
0	0	1	0	1	R5
0	0	1	1	0	R6
0	0	1	1	1	R7
0	1	0	0	0	R8
0	1	0	0	1	R9
0	1	0	1	0	R10
0	1	0	1	1	R11
0	1	1	0	0	R12
0	1	1	0	1	R13
0	1	1	1	0	R14
0	1	1	1	1	R15
1	0	0	0	0	R16
1	0	0	0	1	R17

REGISTER MAPS

REGISTER 0 (R0)

RESERVED																		Tx2 AMP CAL	Tx1 AMP CAL	PUP VCO	VCO CAL	PUP ADC	PUP Tx2	PUP Tx1	PUP LO	CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	Tx2C	Tx1C	PVCO	VCAL	PADC	PTx2	PTx1	PLO	C5(0)	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1 (R1)

RESERVED																		Tx AMP CAL REF CODE								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	TAR7	TAR6	TAR5	TAR4	TAR3	TAR2	TAR1	TAR0	C5(0)	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2 (R2)

RESERVED																ADC START	ADC AVERAGE		ADC CLOCK DIVIDER								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	AS	AA0	AA0	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	C5(0)	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3 (R3)

RESERVED																MUXOUT DBR[1]			IO LEVEL	READBACK CONTROL							CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	M3	M2	M1	M0	IOL	RC5	RC4	RC3	RC2	RC1	RC0	C5(0)	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4 (R4)

RESERVED												RAMP STATUS/ANALOG TEST BUS														CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	AB14	AB13	AB12	AB11	AB10	AB9	AB8	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0	C5(0)	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5 (R5)

RESERVED		RAMP ON	INTEGER WORD												FRAC MSB WORD												CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	RON	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	C5(0)	C4(0)	C3(1)	C2(0)	C1(1)

REGISTER 6 (R6)

RESERVED														FRAC LSB WORD DBR[1]												CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	C5(0)	C4(0)	C3(1)	C2(1)	C1(0)

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 5.

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Figure 21. Register Summary (Register 0 to Register 6)

REGISTER 7 (R7)

RESERVED						MASTER RESET	RESERVED	CLOCK DIVIDER DBR[1]										RDIV2 DBR[1]	REF DOUBLER DBR[1]	R DIVIDER DBR[1]					CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	MR	1	C1D11	C1D10	C1D9	C1D8	C1D7	C1D6	C1D5	C1D4	C1D3	C1D2	C1D1	C1D0	RD2	RD	R4	R3	R2	R1	R0	C5(0)	C4(0)	C3(1)	C2(1)	C1(1)

REGISTER 8 (R8)

RESERVED																	FREQENCY CAL DIVIDER										CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	C5(0)	C4(1)	C3(0)	C2(0)	C1(0)

REGISTER 9 (R9)

RESERVED																											CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	C5(0)	C4(1)	C3(0)	C2(0)	C1(1)

REGISTER 10 (R10)

RESERVED																											CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0	1	0	C5(0)	C4(1)	C3(0)	C2(1)	C1(0)

REGISTER 11 (R11)

RESERVED																				SD RESET	RESERVED	SING FULL TRI RAMP	RAMP MODE		RESERVED	CNTR RESET	CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SDR	0	SFT	RM1	RM0	0	CR	C5(0)	C4(1)	C3(0)	C2(1)	C1(1)

REGISTER 12 (R12)

RESERVED											DBR[1] CHARGE PUMP CURRENT				RESERVED	CP TRISTATE DBR[1]	RESERVED										CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	0	CC3	CC2	CC1	CC0	1	CTRI	0	0	0	0	0	0	0	0	0	0	C5(0)	C4(1)	C3(1)	C2(0)	C1(0)

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[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 5.

Figure 22. Register Summary (Register 7 to Register 12)

REGISTER 13 (R13)

RESERVED										LE SEL	CLK DIV MODE		CLOCK DIVIDER 2												CLK DIV SEL		CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	LES	CDM1	CDM0	C2D11	C2D10	C2D9	C2D8	C2D7	C2D6	C2D5	C2D4	C2D3	C2D2	C2D1	C2D0	CDS1	CDS0	C5(0)	C4(1)	C3(1)	C2(0)	C1(1)

REGISTER 14 (R14)

Tx_DATA INV	TX RAMP CLK	RESERVED			DEVIATION SEL		DEVIATION OFFSET				DEVIATION WORD																CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TDI	TRC	0	0	0	DS1	DS0	DO3	DO2	DO1	DO0	DW15	DW14	DW13	DW12	DW11	DW10	DW9	DW8	DW7	DW6	DW5	DW4	DW3	DW2	DW1	DW0	C5(0)	C4(1)	C3(1)	C2(1)	C1(0)

REGISTER 15 (R15)

RESERVED					STEP SEL		STEP WORD																				CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	SS1	SS0	SW19	SW18	SW17	SW16	SW15	SW14	SW13	SW12	SW11	SW10	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	C5(0)	C4(1)	C3(1)	C2(1)	C1(1)

REGISTER 16 (R16)

RESERVED							DELAY SELECT		RESERVED		Tx_DATA TRIGGER	RAMP DEL	RESERVED		DELAY START WORD												CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	DSL1	DSL0	0	0	TR1	RD	0	0	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0	C5(1)	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 17 (R17)

RESERVED																											CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C5(1)	C4(0)	C3(0)	C2(0)	C1(1)

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Figure 23. Register Summary (Register 13 to Register 17)

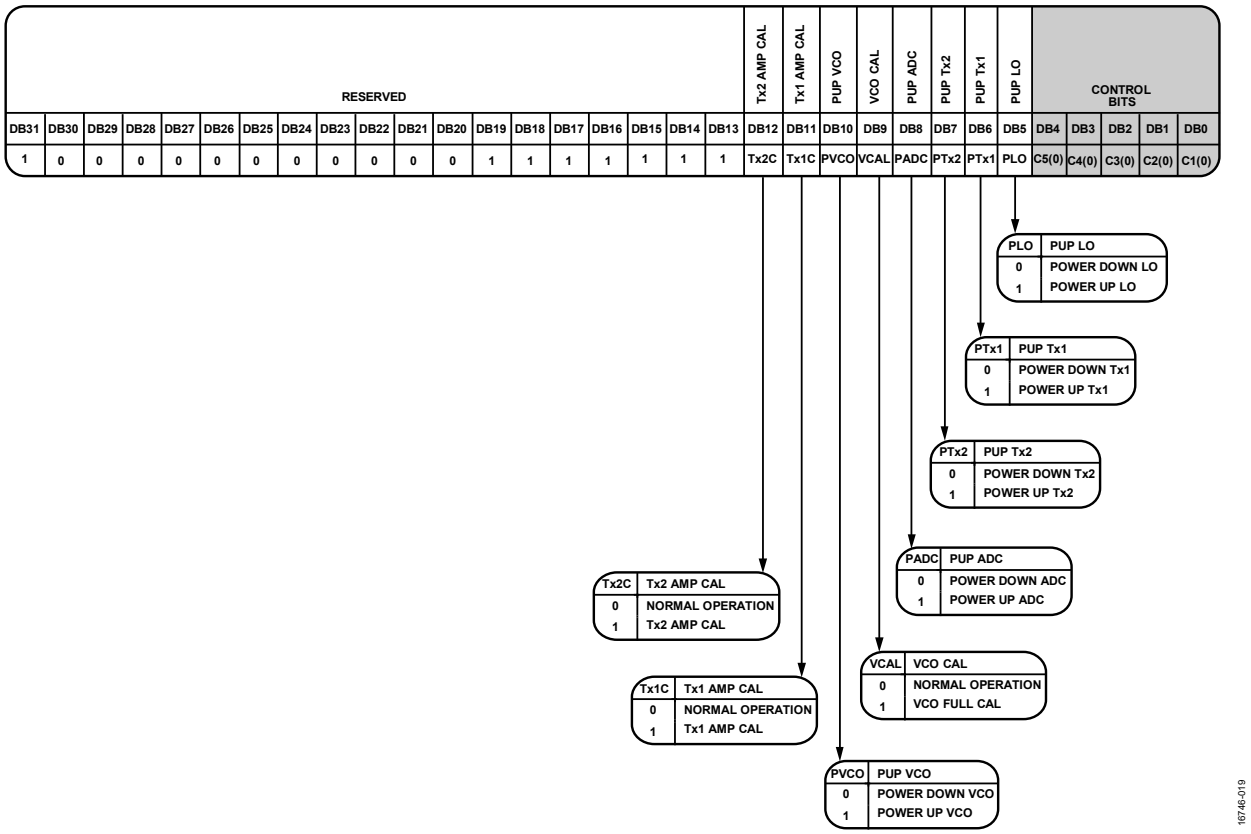

Figure 24. Register 0 (R0)

REGISTER 0

Control Bits

With Bits[C5:C1] set to 00000, Register R0 is programmed. Figure 24 shows the input data format for programming this register.

Reserved

Bits[DB31:DB13] are reserved and must be set as shown in Figure 24.

Transmitter 2 (Tx2) Amplitude Calibration

Bit DB12 provides the control bit for amplitude calibration of the Tx2 output. Set this bit to 0 for normal operation. Setting this bit to 1 performs an amplitude calibration of the Tx2 output. Bit DB12 is shown as Tx2 AMP CAL in Figure 24.

Tx1 Amplitude Calibration

Bit DB11 provides the control bit for amplitude calibration of the Tx1 output. Set this bit to 0 for normal operation. Setting this bit to 1 performs an amplitude calibration of the Tx1 output. Bit DB11 is shown as Tx1 AMP CAL in Figure 24.

Power-Up VCO

Bit DB10 provides the power-up bit for the VCO. Setting this bit to 0 performs a power-down of the VCO. Setting this bit to 1 performs a power-up of the VCO. Bit DB10 is shown as PUP VCO in Figure 24.

VCO Calibration

Bit DB9 provides the control bit for frequency calibration of the VCO. Set this bit to 0 for normal operation. Setting this bit to 1 performs a VCO frequency and amplitude calibration. Bit DB9 is shown as VCO CAL in Figure 24.

Power-Up ADC

Bit DB8 provides the power-up bit for the ADC. Setting this bit to 0 performs a power-down of the ADC. Setting this bit to 1 performs a power-up of the ADC. Bit DB8 is shown as PUP ADC in Figure 24.

Power-Up Tx2 Output

Bit DB7 provides the power-up bit for the Tx2 output. Setting this bit to 0 performs a power-down of the Tx2 output. Setting this bit to 1 performs a power-up of the Tx2 output. Only one transmitter output can be powered up at any time, either Tx1 (DB6) or Tx2 (DB7). Bit DB7 is shown as PUP Tx2 in Figure 24.

Power-Up Tx1 Output

Bit DB6 provides the power-up bit for the Tx1 output. Setting this bit to 0 performs a power-down of the Tx1 output. Setting this bit to 1 performs a power-up of the Tx1 output. Only one Tx output can be powered up at any time, either Tx1 (DB6) or Tx2 (DB7). Bit DB6 is shown as PUP Tx1 in Figure 24.

Power-Up LO Output

Bit DB5 provides the power-up bit for the LO output. Setting this bit to 0 performs a power-down of the LO output. Setting this bit to 1 performs a power-up of the LO output. Bit DB5 is shown as PUP LO in Figure 24.

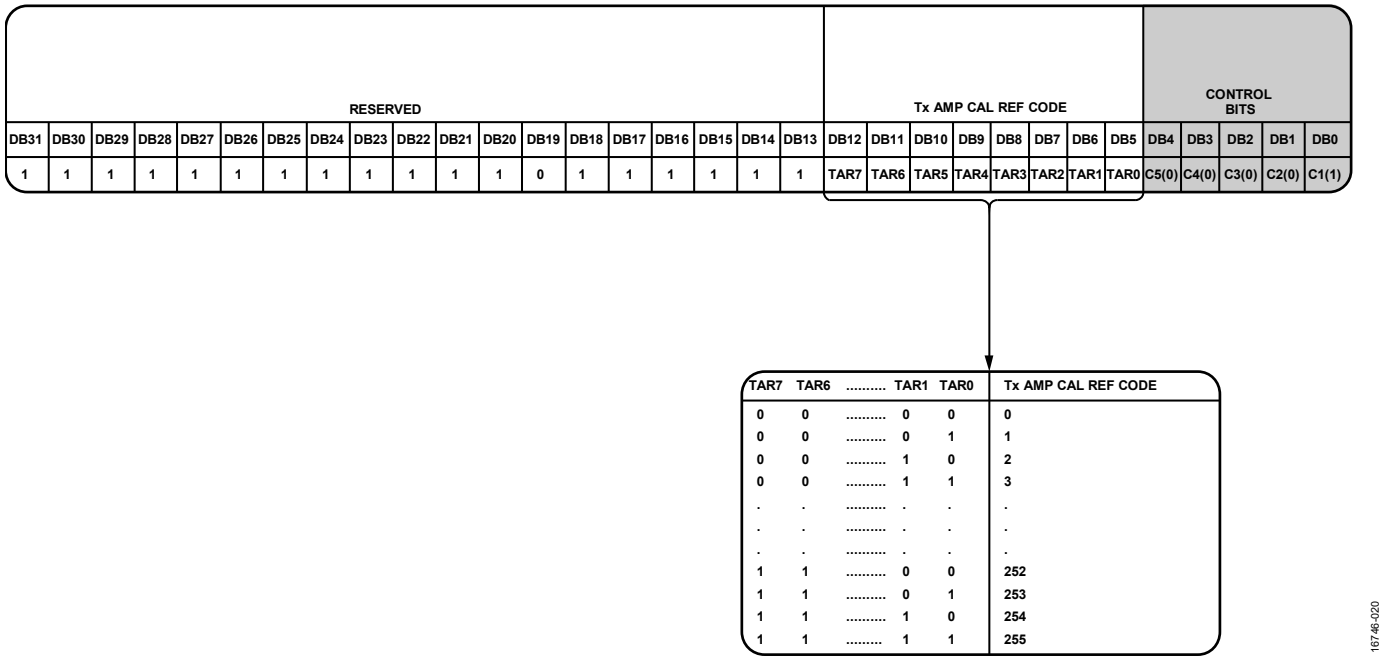

Figure 25. Register 1 (R1)

REGISTER 1

Control Bits

With Bits[C5:C1] set to 00001, Register R1 is programmed. Figure 25 shows the input data format for programming this register.

Reserved

Bits[DB31:DB13] are reserved and must be set as shown in Figure 25.

Transmitter Amplitude Calibration Reference Code

Bits[DB12:DB5] set the transmitter amplitude calibration reference code for the two transmitter outputs during calibration. Calibrate the output power on the transmitter outputs from −20 dBm to 8 dBm by setting the transmitter amplitude calibration reference code (see Figure 7). Bits[DB12:DB5] are shown as Tx AMP CAL REF CODE in Figure 25.

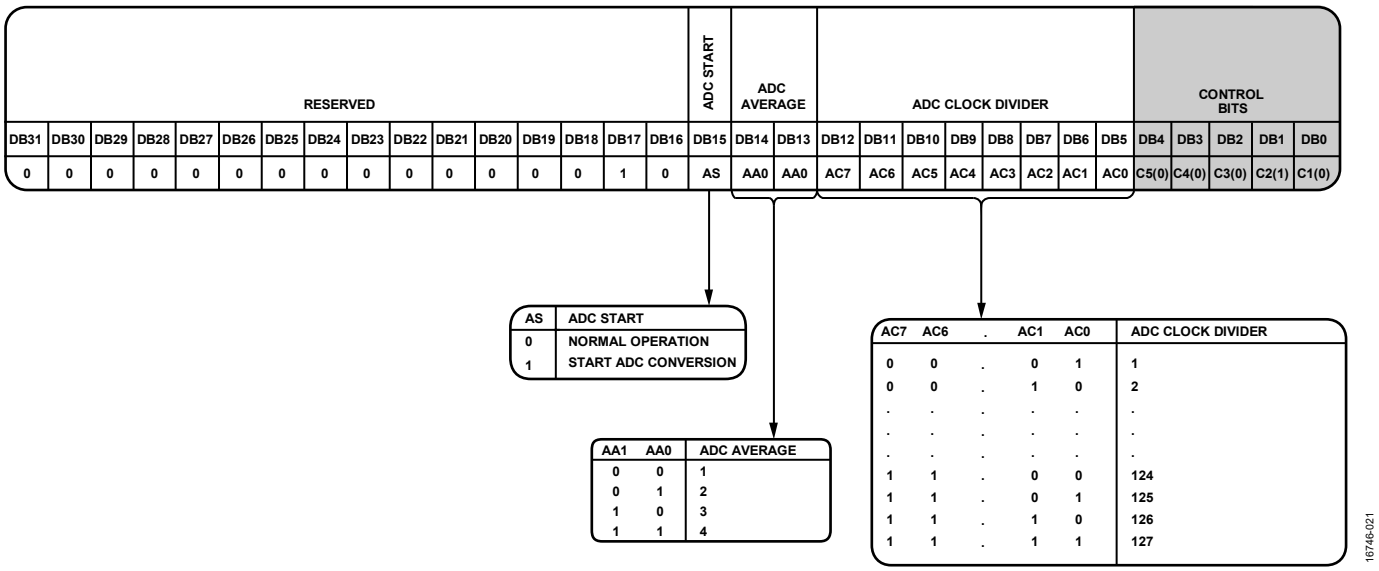

Figure 26. Register 2 (R2)

REGISTER 2

Control Bits

With Bits[C5:C1] set to 00010, Register R2 is programmed. Figure 26 shows the input data format for programming this register.

Reserved

Bits[DB31:DB16] are reserved and must be set as shown in Figure 26.

ADC Start

Bit DB15 starts the ADC conversion. Setting this bit to 1 starts an ADC conversion.

ADC Average

Bits[DB14:DB13] program the ADC average, which is the number of averages of the ADC output (see Figure 26).

ADC Clock Divider

Bits[DB12:DB5] program the clock divider, which is used as the sampling clock for the ADC (see Figure 26). The output of the R divider block clocks the ADC clock divider. Program a divider value to ensure the ADC sampling clock is 1 MHz.

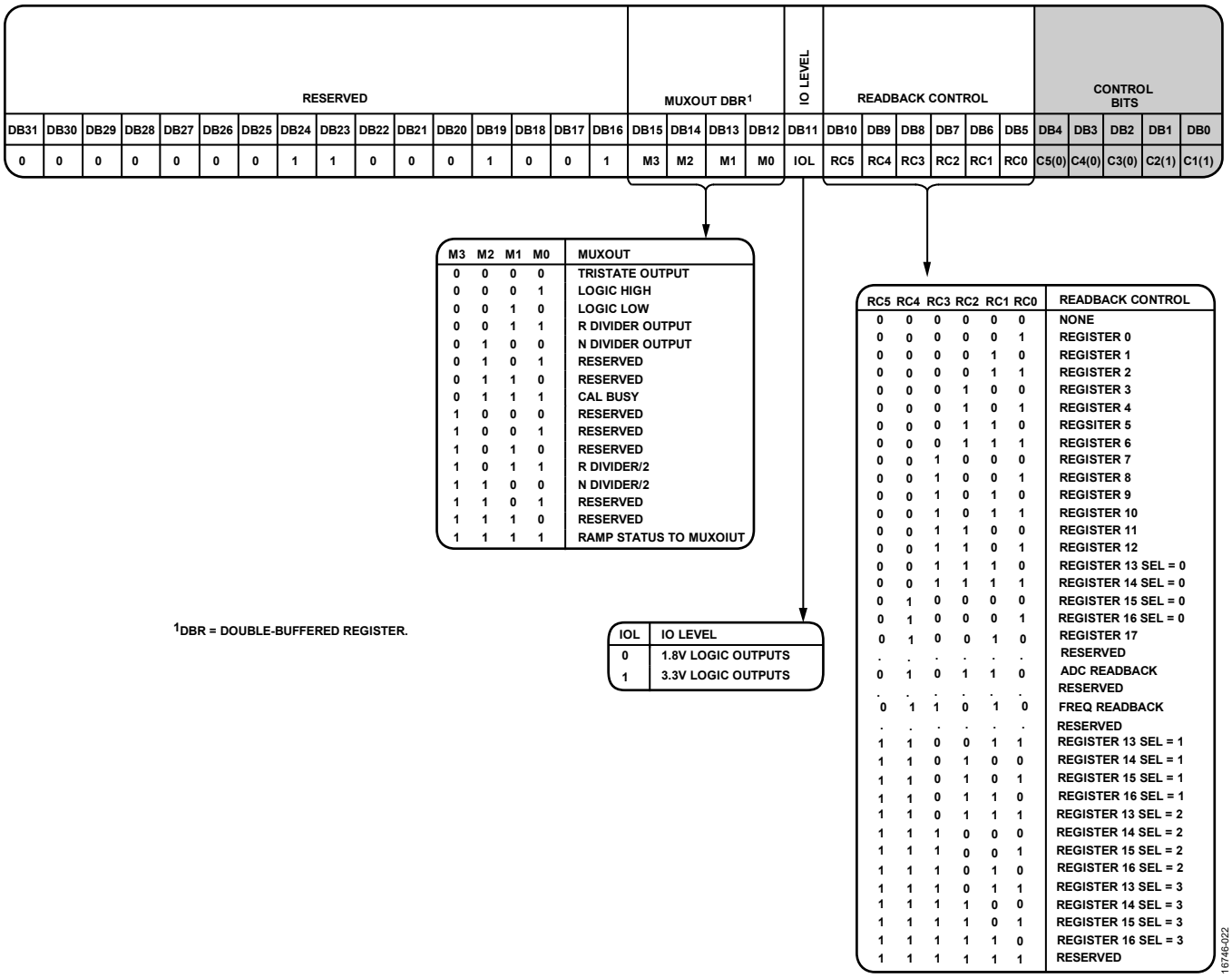

Figure 27. Register 3 (R3)

REGISTER 3

Control Bits

With Bits[C5:C1] set to 00011, Register R3 is programmed. Figure 27 shows the input data format for programming this register.

Reserved

Bits[DB31:DB16] are reserved and must be set as shown in Figure 27.

MUXOUT Control

Bits[DB15:DB12] control the on-chip multiplexer of the ADF5902. See Figure 27 for the truth table.

Input/Output (I/O) Level

Bit DB11 controls the DOUT logic levels. Setting this bit to 0 sets the DOUT logic level to 1.8 V. Setting this bit to 1 sets the DOUT logic level to 3.3 V.

Readback Control

Bits[DB10:DB5] control the readback data to DOUT on the ADF5902. See Figure 27 for the truth table.

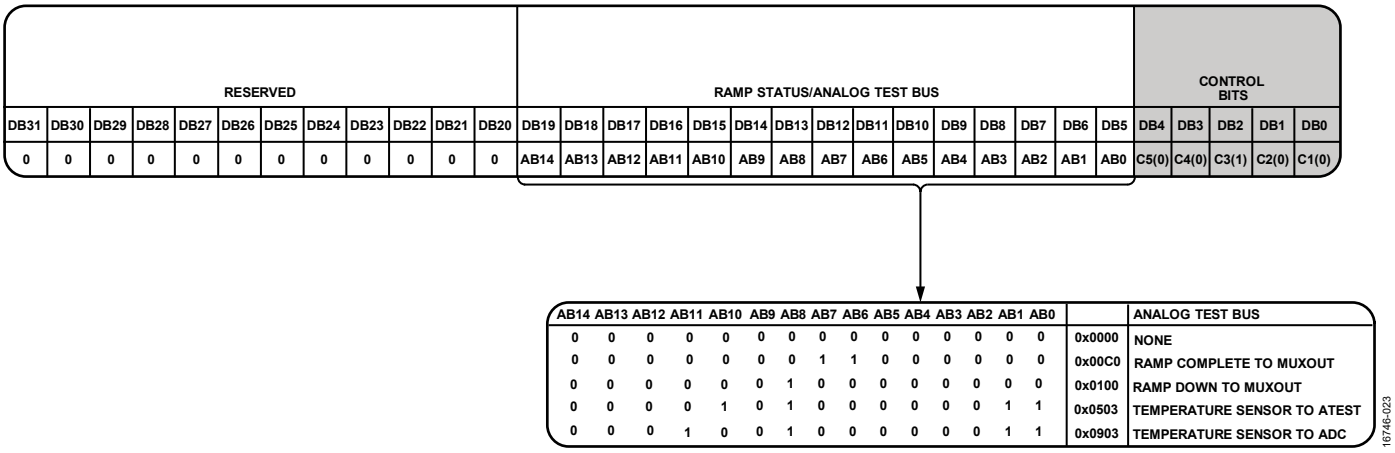

Figure 28. Register 4 (R4)

REGISTER 4

Control Bits

With Bits[C5:C1] set to 00100, Register R4 is programmed. Figure 28 shows the input data format for programming this register.

Reserved

Bits[DB31:DB20] are reserved and must be set as shown in Figure 28.

Ramp Status/Analog Test Bus

Bits[DB19:DB5] control the analog test bus and the ramp status to MUXOUT (see Figure 28).

The analog test bus allows access to internal test signals for the temperature sensor which can be connected to the ATEST pin or the internal ADC.

Setting Bits DB[19:5] to 0 (no value) sets the ATEST pin to high impedance.

For ramp status outputs on MUXOUT, the MUXOUT bits in Register R3 (Bits[DB15:DB12]) must be set to 1111 to access these modes.

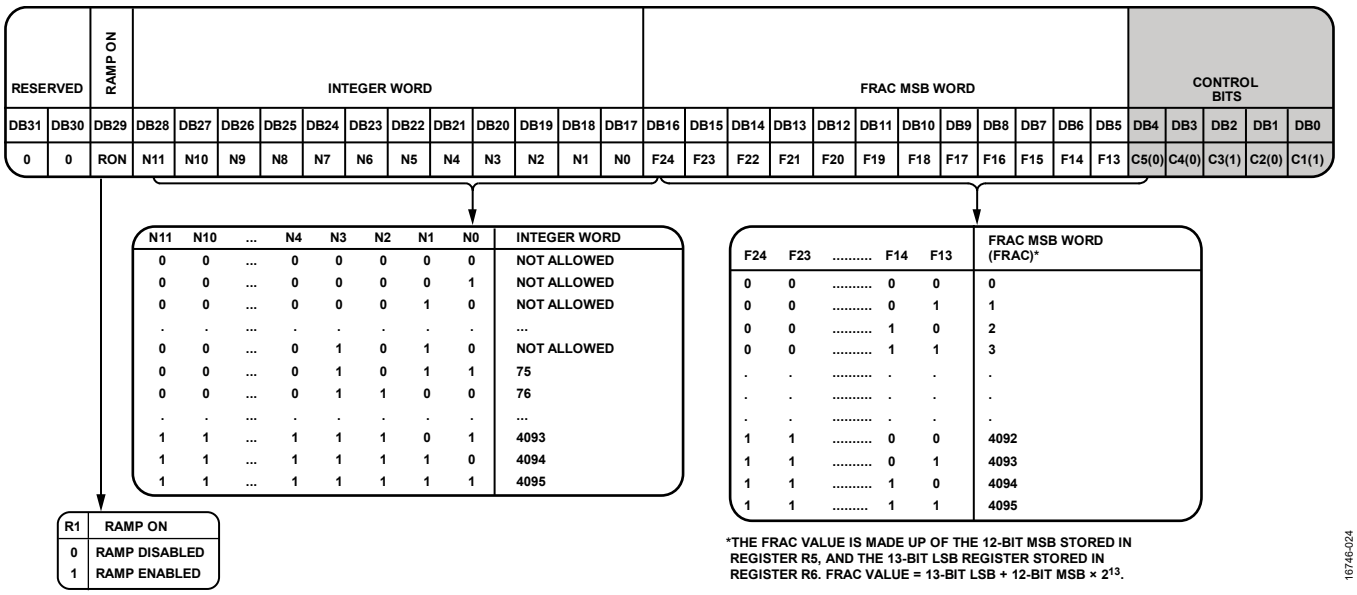

Figure 29. Register 5 (R5)

REGISTER 5

Control Bits

With Bits[C5:C1] set to 00101, Register R5 is programmed. Figure 29 shows the input data format for programming this register.

Reserved

Bits[DB31:DB30] are reserved and must be set as shown in Figure 29.

Ramp On

When Bit DB29 is set to 1, the ramp is started. When Bit DB29 is set to 0, the ramp function is disabled.

In continuous ramp modes, the ramp stops when Bit DB29 is set to 0. For applications that require the ramp to stop at the initial frequency, a write to Register R6 is required prior to disabling the ramp function. In single ramp modes, a write to Register R6 is required prior to repeating the single ramp function.

When using the TX_DATA pin to trigger the ramp off in continuous ramp modes, the ramp stops at the initial frequency, a write to Register R6 is not required. When using the TX_DATA pin in single ramp modes, a write to Register R6 is not required prior to repeating the single ramp function.

12-Bit Integer Value (INT)

These 12 bits (Bits[DB28:DB17]) set the INT value, which determines the integer part of the RF division factor. This INT value is used in Equation 5. See the RF Synthesis: A Worked Example section for more information. All integer values from 75 to 4095 are allowed.

12-Bit MSB Fractional Value (FRAC)

Bits[DB16:DB5], together with Bits[DB17:DB5] (FRAC LSB word) in Register R6, control what is loaded as the FRAC value into the fractional interpolator. This FRAC value partially determines the overall RF division factor. It is also used in Equation 1. These 12 bits are the most significant bits (MSB) of the 25-bit FRAC value, and Bits[DB17:DB5] (FRAC LSB word) in Register R6 are the least significant bits (LSB). See the RF Synthesis: A Worked Example section for more information.

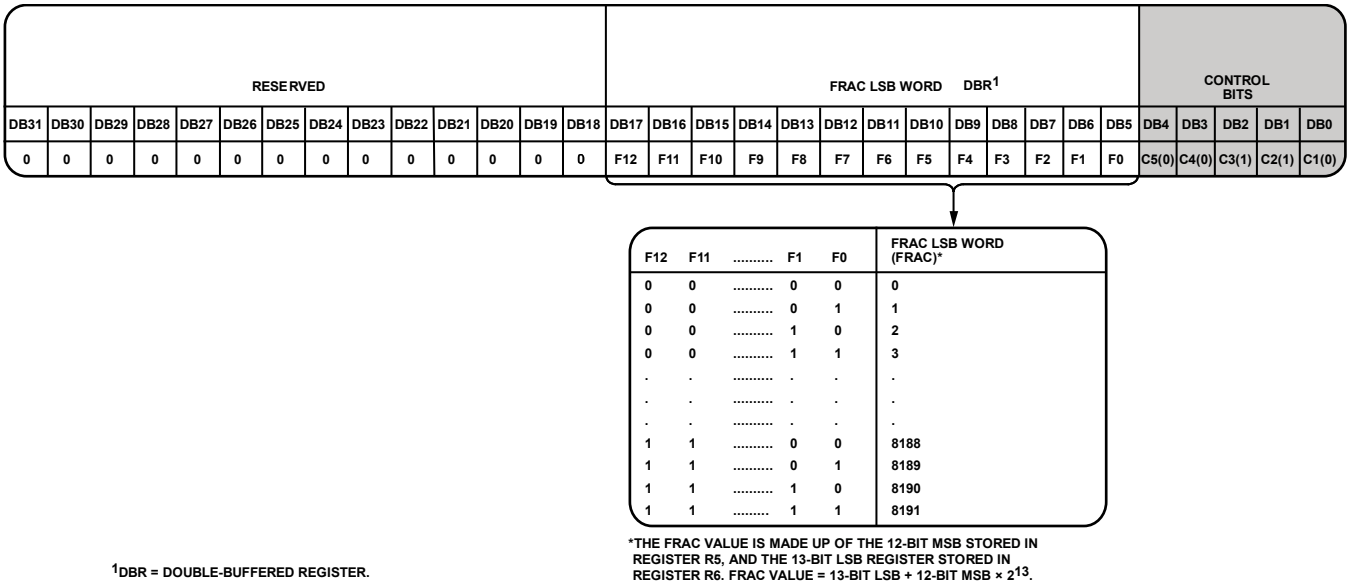

Figure 30. Register 6 (R6)

REGISTER 6

Control Bits

With Bits[C5:C1] set to 00110, Register R6 is programmed. Figure 30 shows the input data format for programming this register.

Reserved

Bits[DB31:DB18] are reserved and must be set as shown in Figure 30.

13-Bit LSB FRAC Value

These 13 bits (Bits[DB17:DB5]), together with Bits[DB16:DB5] (FRAC MSB word) in Register R5, control what is loaded as the FRAC value into the fractional interpolator. This FRAC value partially determines the overall RF division factor. It is also used in Equation 1. These 13 bits are the least significant bits (LSB) of the 25-bit FRAC value, and Bits[DB16:DB5] (FRAC MSB word) in Register R5 are the most significant bits (MSB). See the RF Synthesis: A Worked Example section for more information.

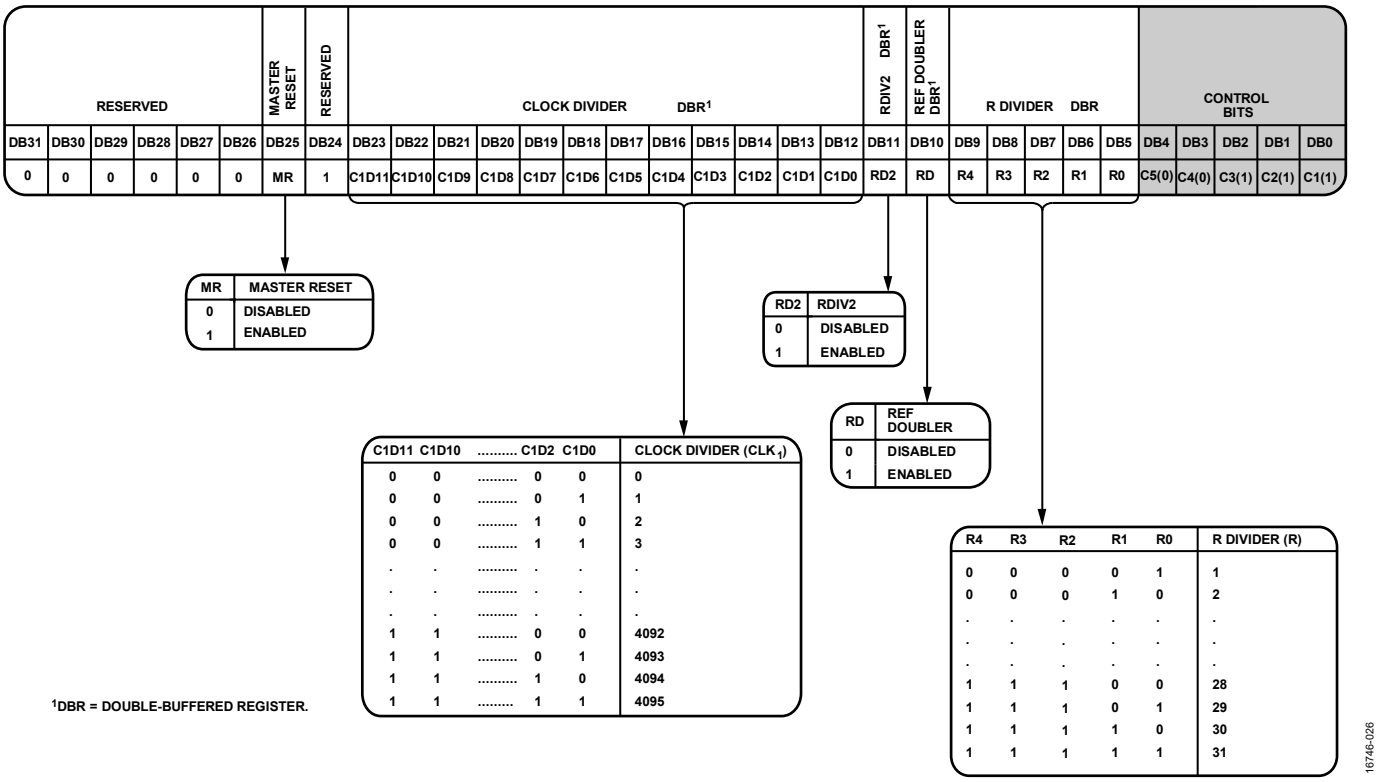

Figure 31. Register 7 (R7)

REGISTER 7

Control Bits

With Bits[C5:C1] set to 00111, Register R7 is programmed. Figure 31 shows the input data format for programming this register.

Reserved

Bits[DB31:DB26] are reserved and must be set as shown in Figure 31.

Master Reset

Bit DB25 provides a master reset bit for the device. Setting this bit to 1 performs a reset of the device and all register maps. Setting this bit to 0 returns the device to normal operation.

Clock Divider

Bits[DB23:DB12] controls the clock divider (CLK_1) value (see Figure 31). The CLK_1 value sets a divider for the VCO frequency calibration. Load the divider such that PFD frequency (f_{PFD})/ CLK_1 is less than or equal to 25 kHz.

For example, for f_{PFD} = 50 MHz, set CLK_1 = 2048 so that f_{PFD}/ CLK_1 < 25 kHz.

The CLK_1 value is also used to determine the duration of the time step in ramp mode. See the Ramp and Modulation section for more information.

Divide by 2 (RDIV2)

Setting the DB11 bit to 1 inserts a divide by 2 toggle flip flop between the R counter and VCO calibration block.

Reference Doubler

Setting DB10 to 0 feeds the REF_{IN} signal directly to the 5-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before the REF_{IN} signal is fed to the 5-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the reference doubler is enabled, for optimum phase noise performance, it is recommended to only use charge pump current settings of 0b0000 to 0b0111, that is, 0.28 mA to 2.24 mA in Register 12. In this case, the best practice is to design the loop filter for a charge pump current of 1.12 mA or 1.4 mA and then use the programmable charge pump current to adjust the frequency response.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 50 MHz.

5-Bit R Divider

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the VCO calibration block. Division ratios from 1 to 31 are allowed.

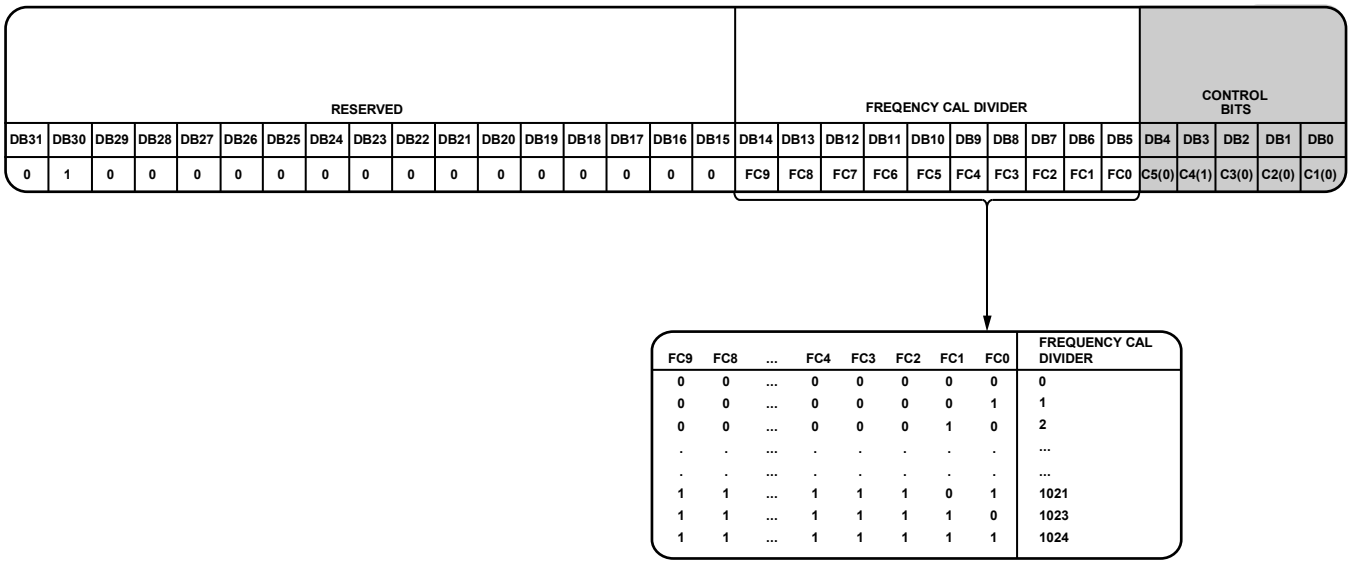

Figure 32. Register 8 (R8)

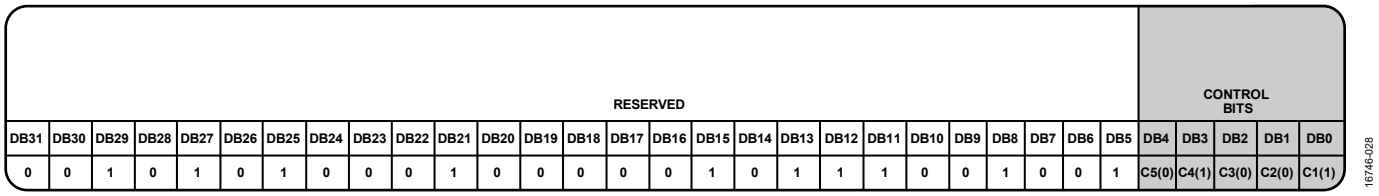

Figure 33. Register 9 (R9 0x2A20B929)

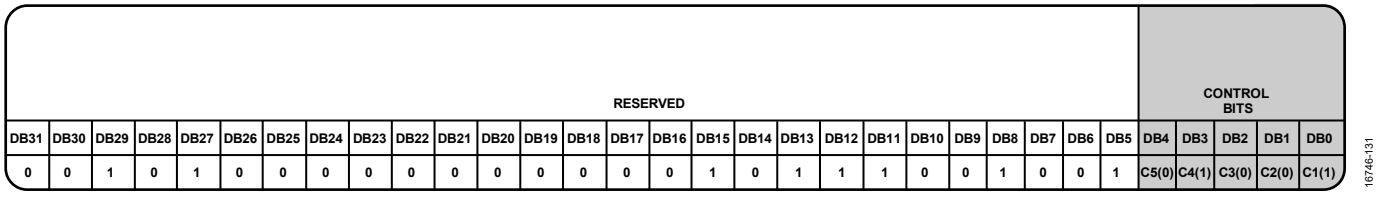

Figure 34. Register 9 (R9 0x2800B929)

REGISTER 8

Control Bits

With Bits[C5:C1] set to 01000, Register R8 is programmed. Figure 32 shows the input data format for programming this register.

Reserved

Bits[DB31:DB15] are reserved and must be set as shown in Figure 32.

Frequency Calibration Divider

Bits[DB14:DB5] set a divider for the VCO frequency calibration clock. Load the divider such that the PFD frequency (f_{PFD})/ frequency calibration divider is less than or equal to 100 kHz (see Figure 32).

REGISTER 9

The bits in Register 9 are reserved and must be programmed as shown in Figure 32 using a hexadecimal word of 0x2A20B929, prior to the VCO calibration.

The bits in Register 9 must be programmed as described in Figure 32, using a hexadecimal word of 0x2800B929 for normal operation.

See the Applications Information section for more information.

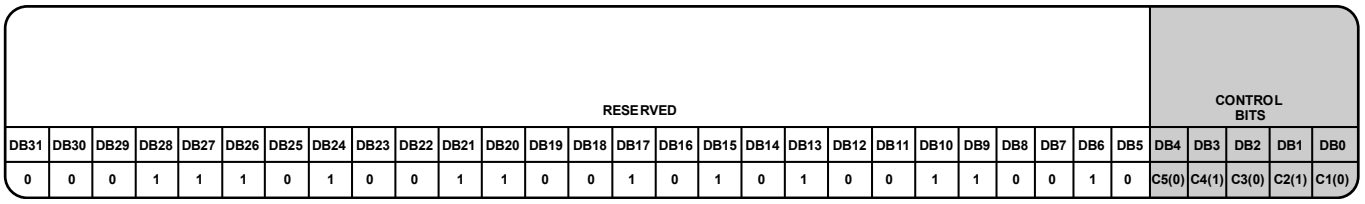

Figure 35. Register 10 (R10 0x1D32A64A)

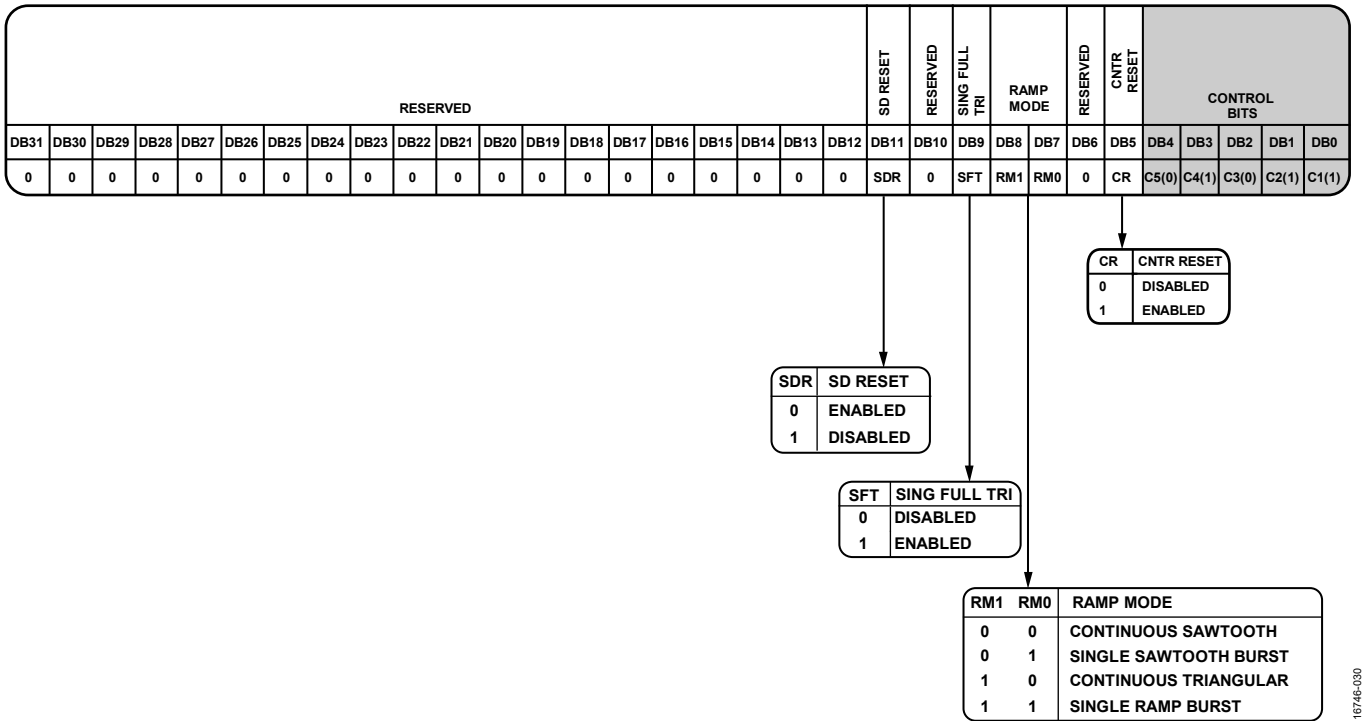

Figure 36. Register 11 (R11)

REGISTER 10

The bits in Register 10 are reserved and must be programmed as shown in Figure 35 using a hexadecimal word of 0x1D32A64A.

REGISTER 11

Control Bits

With Bits[C5:C1] set to 01011, Register R11 is programmed. Figure 36 shows the input data format for programming this register.

Reserved

Bits[DB31:DB12], Bit DB10, and Bit DB6 are reserved and must be set as shown in Figure 36.

SD Reset

For most applications, set Bit DB11 to 0. When this bit is set to 0, the Σ-Δ (SD) modulator is reset on each write to Register R5. If it is not required that the SD modulator be reset on each write to Register R5, set this bit to 1.

Single Full Triangle

When Bit DB9 is set to 1, the single full triangle function is enabled. When Bit DB9 is set to 0, this function is disabled. To use the single full triangle function, ramp mode (Register 11, Bits DB[8:7]) must be set to 0b11, single sawtooth burst. For more information, see the Ramp and Modulation section.

Ramp Mode

Bits[DB8:DB7] determine the type of generated waveform (see Figure 36). For more information, see the Ramp and Modulation section.

Counter Reset

Bit DB5 provides a counter reset bit for the counters. Setting this bit to 1 performs a counter reset of the device counters. Setting this bit to 0 returns the device to normal operation. Bit DB5 is shown as CNTR RESET in Figure 36.

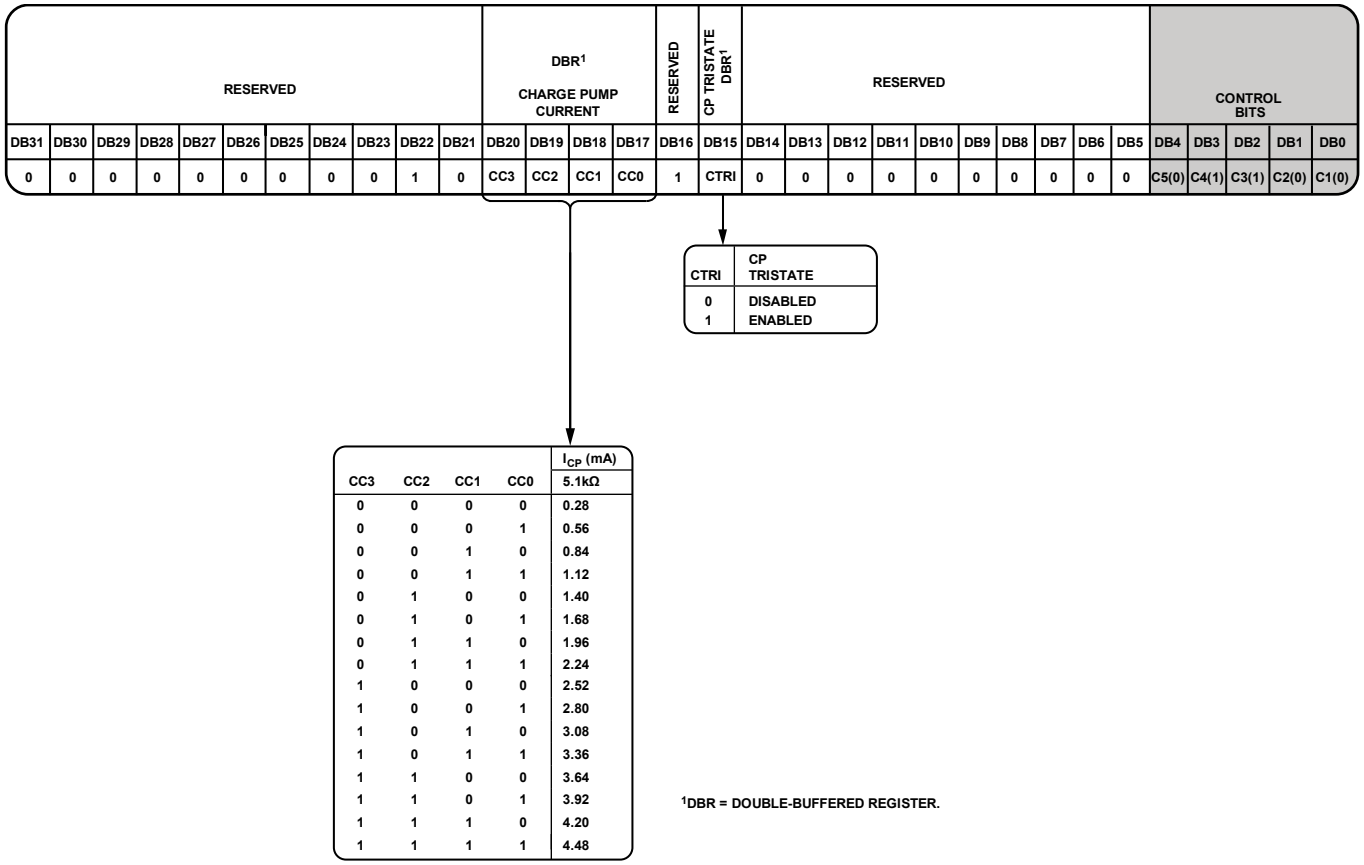

Figure 37. Register 12 (R12)

REGISTER 12

Control Bits

With Bits[C5:C1] set to 01100, Register R12 is programmed. Figure 37 shows the input data format for programming this register.

Reserved

Bits[DB31:DB21] and Bit DB16 are reserved and must be set as shown in Figure 37.

Charge Pump Current Setting

Bits[DB20:DB17] set the charge pump current (see Figure 37). Set these bits to the charge pump current that the loop filter is designed with. The best practice is to design the loop filter for a charge pump current of 2.24 mA or 2.52 mA and then use the programmable charge pump current to adjust the frequency response. See the Reference Doubler section for information on setting the charge pump current when the doubler is enabled.

Charge Pump Tristate

When Bit DB15 is set to 1, the charge pump is placed in tristate mode. For normal charge pump operation, set this bit to 0.

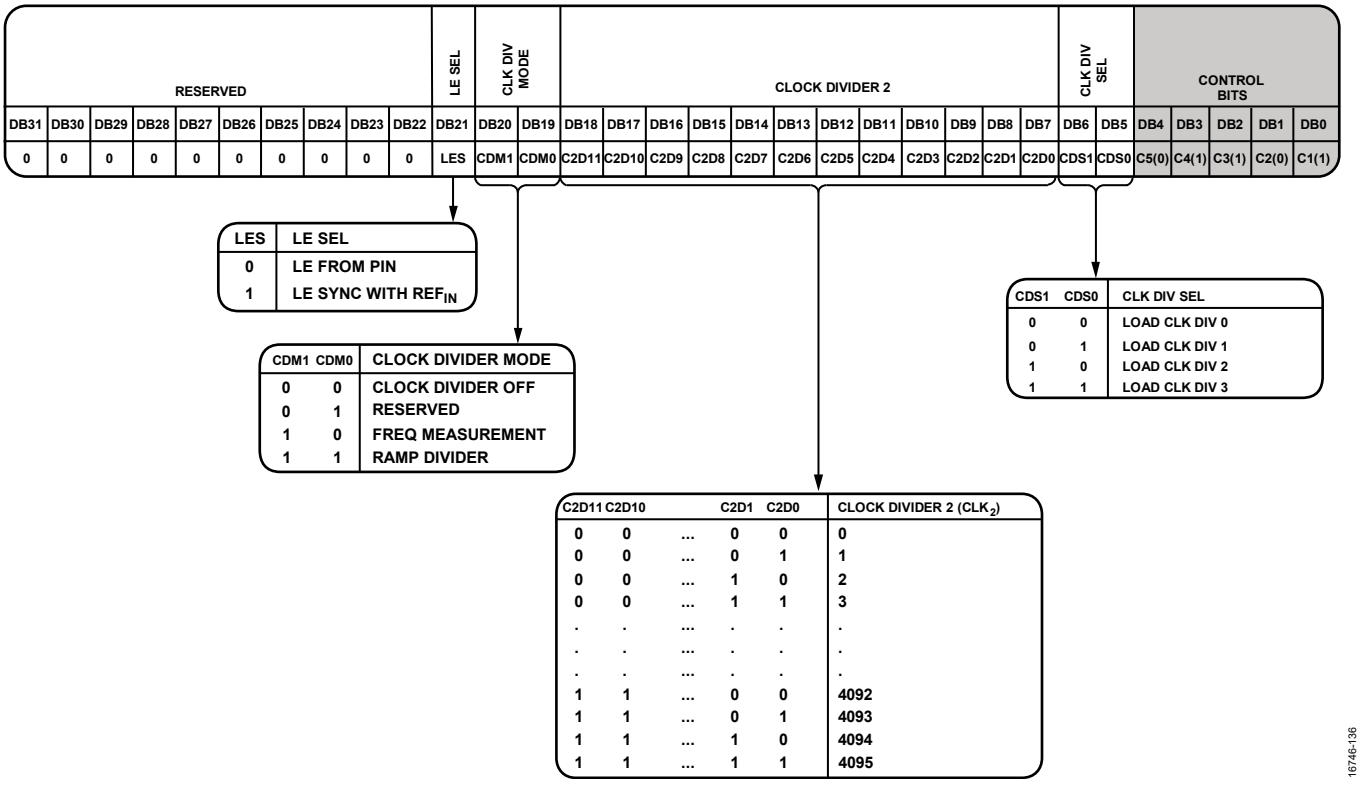

Figure 38. Register 13 (R13)

REGISTER 13

Control Bits

With Bits[C5:C1] set to 01101, Register R13 is programmed. Figure 38 shows the input data format for programming this register.

Reserved

Bits[DB31:DB22] are reserved and must be set as shown in Figure 38.

LE Select

In some applications, it is necessary to synchronize the LE pin with the reference signal. To perform this synchronization, Bit DB21 must be set to 1. Synchronization is performed internally on the device.

Clock Divider Mode

Bits[DB20:DB19] are used to enable ramp divider mode. When using any of the ramp modes, set Bits[CDM1:CDM0] to 11. Otherwise, set these bits to 0b00.

12-Bit Clock Divider (CLK_2) Value

Bits[DB18:DB7] program the clock divider (CLK_2) timer when the device operates in ramp mode (see the Ramp and Modulation section).

Clock Divider Select

Bits[DB6:DB5] select the segment of the ramp CLK_2 is used (see Figure 38). For more information, see the Ramp and Modulation section. Bits[DB6:DB5] are shown as CLK DIV SEL in Figure 38.

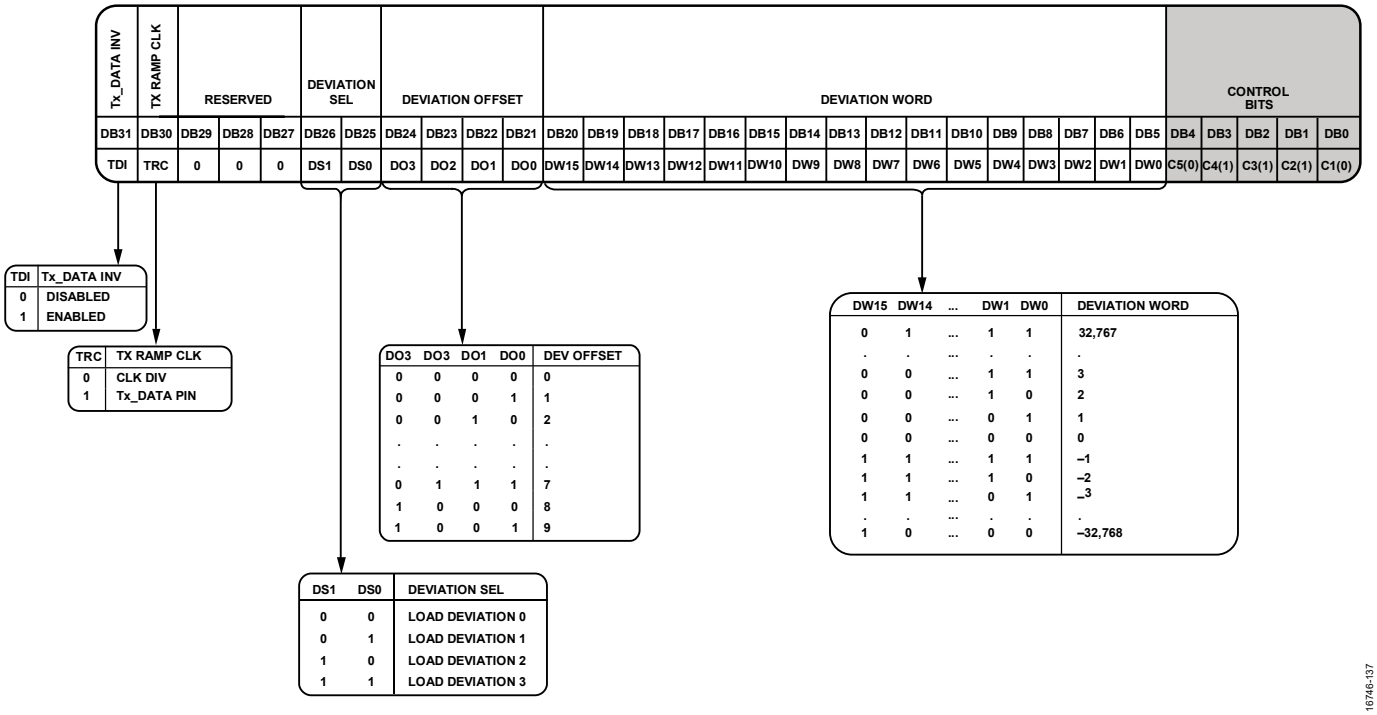

Figure 39. Register 14 (R14)

REGISTER 14

Control Bits

With Bits[C5:C1] set to 01110, Register R14 is programmed. Figure 39 shows the input data format for programming this register.

Reserved

Bits[DB29:DB27] are reserved and must be set as shown in Figure 39.

TX_DATA Invert

When Bit DB31 is set to 0, events triggered by TX_DATA occur on the rising edge of the TX_DATA pulse. When Bit DB31 is set to 1, events triggered by TX_DATA occur on the falling edge of the TX_DATA pulse.

TX_DATA Ramp Clock

When Bit DB30 is set to 0, the clock divider clock is used to clock the ramp. When Bit DB30 is set to 1, the TX_DATA pin is used to clock the ramp.

Deviation Select

Bits[DB26:DB25] select the deviation word to be loaded (see Figure 39).

4-Bit Deviation Offset Word

Bits DB[24:21] determine the deviation offset word. The deviation offset word affects the deviation resolution (see the Ramp and Modulation section).

16-Bit Deviation Word

Bits[DB20:DB5] determine the signed deviation word in twos complement format. The deviation word defines the deviation step (see the Ramp and Modulation section).

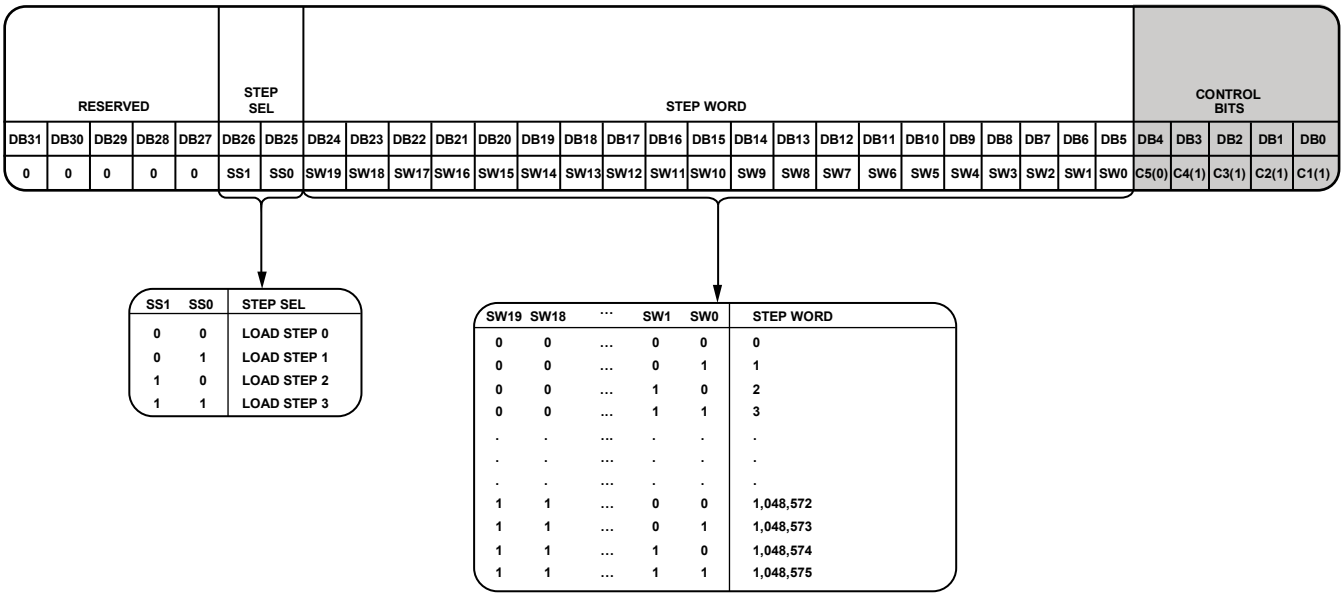

Figure 40. Register 15 (R15)

REGISTER 15

Control Bits

With Bits[C5:C1] set to 01111, Register R15 is programmed. Figure 40 shows the input data format for programming this register.

Reserved

Bits[DB31:DB27] are reserved and must be set as shown in Figure 40.

Step Select

Bits[DB26:DB25] select the step word to be loaded (see Figure 40).

20-Bit Step Word

Bits[DB22:DB3] determine the step word. The step word is the number of steps in the ramp (see the Ramp and Modulation section).

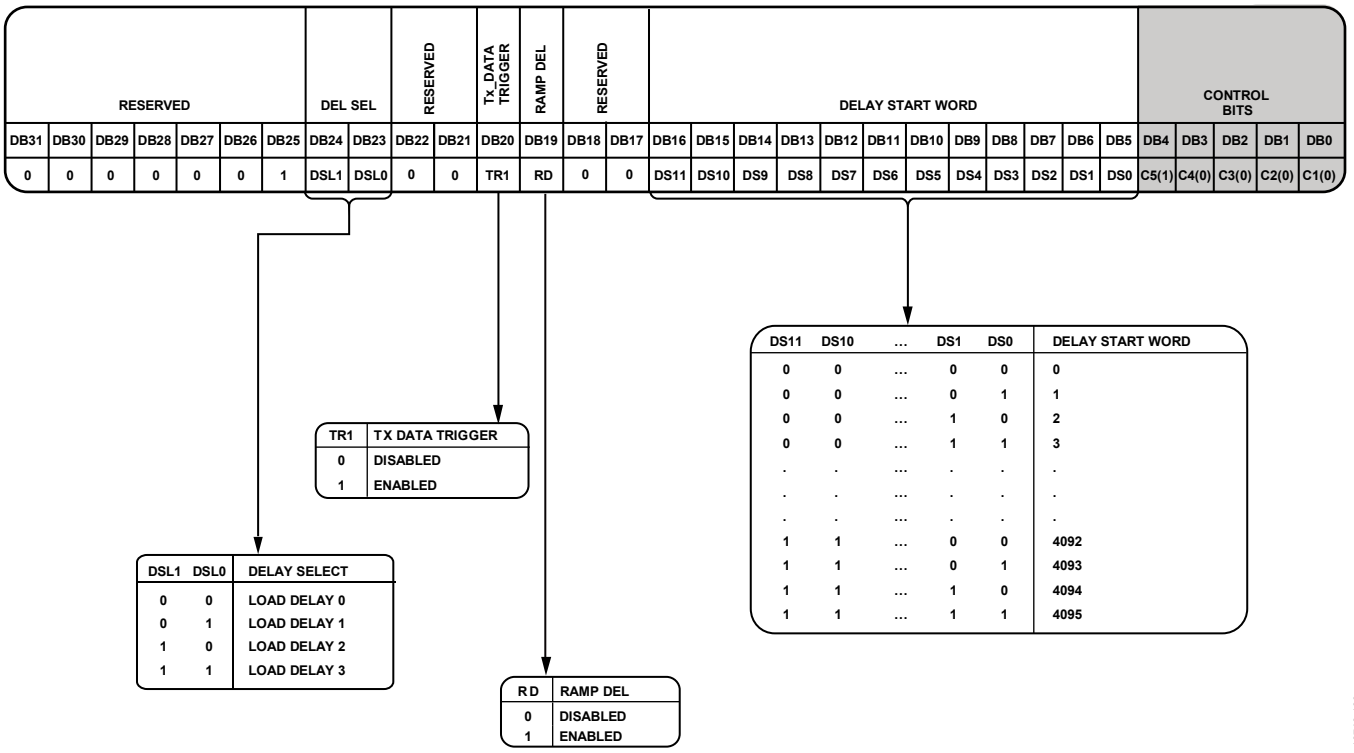

Figure 41. Register 16 (R16)

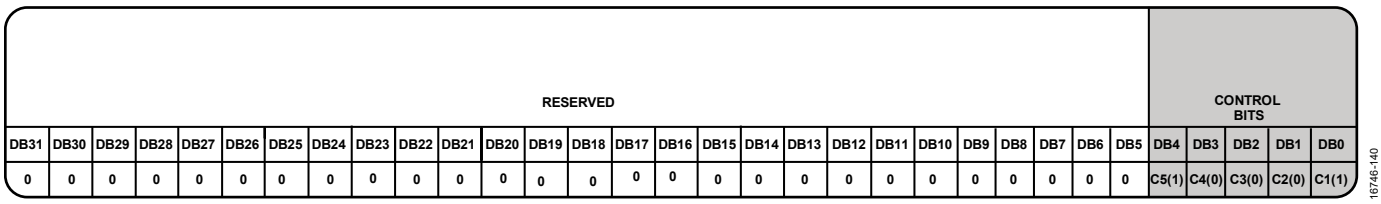

Figure 42. Register 17 (R17)

REGISTER 16

Control Bits

With Bits[C5:C1] set to 10000, Register R16 is programmed. Figure 41 shows the input data format for programming this register.

Reserved

Bits[DB31:DB25], Bits[DB22:DB21], and Bits[DB18:DB17] are reserved and must be set as shown in Figure 41.

Delay Select

Bits[DB24:DB23] select the delay word to be loaded.

TX_DATA Trigger

When Bit DB20 is set to 1, a logic high on the TX_DATA pin activates the ramp in conjunction with Bit DB29 of Register 5. Synchronize the active edge of the pulse applied to the TX_DATA pin to the rising edge of the REF_{IN} reference input.

The pulse duration applied to the TX_DATA pin must be a minimum width of $4 \times 1/f_{PFD}$, where f_{PFD} is the phase frequency detector (PFD) frequency.

When Bit DB20 is set to 0, this function is disabled.

When activating continuous triangular or continuous sawtooth ramps, a pulse applied to the TX_DATA pin is required after Bit DB29 of Register 5 is toggled high. To stop the continuous triangular or sawtooth ramps, a TX_DATA pulse is required after Bit DB29 of Register 5 is toggled low.

When Bit DB20 is set to 0, this function is disabled.

Ramp Delay

When Bit DB19 is set to 1, the delay between ramps function is enabled. When Bit DB19 is set to 0, this function is disabled.

12-Bit Delay Word

Bits[DB16:DB5] determine the delay word. The delay word determines the duration of the ramp start delay.

REGISTER 17

The bits in Register 17 are reserved and must be programmed as described in Figure 42 using a hexadecimal word of 0x00000011.

APPLICATIONS INFORMATION

INITIALIZATION SEQUENCE

After powering up the device, administer the programming sequence shown in Table 7.

This sequence locks the VCO to 24.025 GHz with a 100 MHz reference. The ramp-up rate is 200 MHz at 144 µs. The ramp-down rate is 200 MHz at 9 µs.

Table 7. Initialization Sequence

Step	Register	Hexadecimal Code	Description
1	R7	0x02000007	Master reset
2	R11	0x0000002B	Reset the counters
3	R11	0x0000000B	Enable counters
4	R13	0x0018000D	Enable ramp divider
5	R10	0x1D32A64A	Reserved
6	R9	0x2A20B929	VCO calibration setup
7	R8	0x40003E88	Set the VCO frequency calibration divider clock to 100 kHz
8	R0	0x800FE520	Power up the device and LO
Delay of 10 µs			
9	R7	0x01800827	PFD = 50 MHz, CLK_1 = 2048
10	R6	0x00000006	Set the LSB FRAC = 0
11	R5	0x01E38005	N = 241.175
12	R4	0x00000004	Set the ATEST pin to high impedance
13	R3	0x01897803	Sets the I/O level to 3.3 V, CAL_BUSY to MUXOUT
14	R2	0x00020642	Set ADC clock to 1 MHz
15	R1	0xFFF7FFE1	Set the transmitter amplitude level
16	R0	0x800FE720	Start the VCO frequency calibration
Delay of 1200 µs			
17	R0	0x800FE560	Turn Tx1 on, Tx2 off, and LO on
18	R0	0x800FED60	Tx1 amplitude calibration
Delay of 500 µs			
19	R0	0x800FE5A0	Turn Tx1 off, Tx2 on, and LO on
20	R0	0x800FF5A0	Tx2 amplitude calibration
Delay of 500 µs			
21	R17	0x00000011	Reserved
22	R16	0x00000010	Ramp delay register
23	R15	0x0000120F	Load step register with STEP_SEL = 0, step word is 144
24	R15	0x0200012F	Load step register with STEP_SEL = 1, step word is 9
25	R15	0x0400120F	Load step register with STEP_SEL = 2, step word is 144
26	R15	0x0600012F	Load step register with STEP_SEL = 3, step word is 9
27	R14	0x012038EE	Load deviation register with DEV_SEL = 0, DEV = 455, DEV offset = 9
28	R14	0x033C720E	Load deviation register with DEV_SEL = 1, dev word= −1820, DEV offset = 9
29	R14	0x052038EE	Load deviation register with DEV_SEL = 2, dev word = 455, dev offset = 9
30	R14	0x73C720E	Load deviation register with DEV_SEL = 3, dev word = −1820 dev offset = 9
31	R13	0x0018050D	Load the clock register with CLK DIV SEL = 0, CLK2_0 = 10
32	R13	0x0018052D	Load the clock register with CLK DIV SEL = 1, CLK2_1 = 10
33	R13	0x0018054D	Load the clock register with CLK DIV SEL = 2, CLK2_2 = 10
34	R13	0x0018056D	Load the clock register with CLK DIV SEL = 3, CLK2_3 = 10
35	R12	0x004F000C	Charge pump current = 2.24 mA
36	R9	0x2800B929	Normal Operation
37	R7	0x0100A027	PFD = 100 MHz, CLK_1 = 10
38	R6	0x00000006	Set the LSB FRAC = 0
39	R5	0x00F04005	INT =120, MSB FRAC = 512; lock to 24.025 GHz
40	R4	0x00002004	Ramp down to MUXOUT
41	R3	0x0189F803	I/O voltage level to 3.3 V
Delay of 100 µs			
42	R11	0x0000010B	Select ramp mode

RECALIBRATION SEQUENCE

The ADF5902 can be recalibrated after the initialization sequence is complete and the device is powered up. The recalibration sequence must be run for every 10°C temperature change. The temperature can be monitored using the temperature sensor (see the Temperature Sensor section).

Table 8. Recalibration Sequence

Step Number from Initialization Sequence	Register	Hexadecimal Code	Description
	R0	0x800FE500	Turn Tx1 off, Tx2 off and LO off
6	R9	0x2A20B929	Reserved
9	R7	0x01800827	PFD = 50 MHz, CLK_1 = 2048
10	R6	0x00000006	Set the LSB FRAC = 0
11	R5	0x01E38005	N = 241.175
12	R4	0x00000004	Set the ATEST pin to high impedance
13	R3	0x01897803	I/O level to 3.3 V, CAL_BUSY to MUXOUT
14	R2	0x00020642	Set ADC clock to 1 MHz
15	R1	0xFFF7FFE1	Set the transmitter amplitude level
	R0	0x800FE700	Start the VCO frequency calibration
Delay of 1200 µs			
17	R0	0x800FE560	Turn Tx1 on, Tx2 off, and LO on
18	R0	0x800FED60	Tx1 amplitude calibration
Delay of 500 µs			
19	R0	0x800FE5A0	Turn Tx1 off, Tx2 on, and LO on
20	R0	0x800FF5A0	Tx2 amplitude calibration
Delay of 500 µs			
36	R9	0x2800B929	Reserved
37	R7	0x0100A027	PFD set to 100 MHz, CLK_DIV1 = 10
38	R6	0x00000006	Set the LSB FRAC = 0
39	R5	0x00F04005	Set INT word to 120, set MSB FRAC = 512; lock to 24.025 GHz
40	R4	0x00002004	Ramp down to MUXOUT
41	R3	0x0189F803	I/O voltage level to 3.3 V
Delay of 100 µs			
42	R11	0x0000010B	Select ramp mode

TEMPERATURE SENSOR

The ADF5902 has an on-chip temperature sensor that can be accessed on the ATEST pin or as a digital word on DOUT following an ADC conversion. The temperature sensor operates over the full operating temperature range of −40°C to +105°C. The accuracy can be improved by performing a one-point calibration at room temperature and storing the result in memory.

With the temperature sensor on the analog test bus and test bus connected to the ATEST pin (Register 4 set to 0x0000A064), the ATEST voltage can be converted to temperature with the following equation:

$$Temperature\,(^{\circ}\mathrm{C}) = \frac{(V_{ATEST} - V_{OFF})}{V_{GAIN}} \quad (3)$$

where:
V_{ATEST} is the voltage on the ATEST pin.
V_{OFF} = 0.699 V, the offset voltage.
$V_{GAIN} = 6.4 \times 10^{-3}$, the voltage gain.

The temperature sensor result can be converted to a digital word with the ADC and readback on DOUT with the following sequence:

1. Write 0x00012064 to Register R4 to connect the analog test bus to the ADC and the temperature sensor to the analog test bus.
2. Write 0x0002A802 to Register R2 to start the ADC conversion.
3. Write 0x0189FAC3 to Register R3 to set the ADC output data to DOUT.
4. Read back DOUT.
5. Write 0x00002064 to Register R4 to reset Register R4 to the initial value.
6. Write 0x00020642 to Register R2 to reset Register R2 to the initial value.

Convert the DOUT word to temperature with the following equation:

$$Temperature\,(^{\circ}\mathrm{C}) = \frac{((ADC \times V_{LSB}) - V_{OFF})}{V_{GAIN}} \quad (4)$$

where:
ADC is the ADC code read back on DOUT.
V_{LSB} = 7.33 mV, the ADC LSB voltage.
V_{OFF} = 0.699 V, the offset voltage.
$V_{GAIN} = 6.4 \times 10^{-3}$, the voltage gain.

RF SYNTHESIS: A WORKED EXAMPLE

The following equation governs how to program the ADF5902:

$$RF_{OUT} = (INT + (FRAC/2^{25})) \times f_{REF} \times 2 \quad (5)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC is the fractionality.

$$f_{REF} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (6)$$

where:
REF_{IN} is the reference frequency input.
D is the reference doubler bit, DB10 in Register R7 (0 or 1).
R is the reference division factor.
T is the reference divide by 2 bit, DB11 in Register R7 (0 or 1).

For example, in a system where a 24.125 GHz RF frequency output (RF_{OUT}) is required and a 100 MHz reference frequency input (REF_{IN}) is available, f_{REF} is set to 50 MHz.

From Equation 6,

$$f_{REF} = (100\ \mathrm{MHz} \times (1 + 0)/(1 \times (1 + 1)) = 50\ \mathrm{MHz}$$

From Equation 5,

$$24.125\ \mathrm{GHz} = 50\ \mathrm{MHz} \times (N + FRAC/2^{25}) \times 2$$

Calculating the N and FRAC values,

$$N = \mathrm{int}(RF_{OUT}/(f_{REF} \times 2)) = 241$$
$$FRAC = F_{MSB} \times 2^{13} + F_{LSB}$$
$$F_{MSB} = \mathrm{int}(((RF_{OUT}/(f_{REF} \times 2)) - \mathrm{N}) \times 2^{12}) = 1024$$
$$F_{LSB} = \mathrm{int}(((((RF_{OUT}/(f_{REF} \times 2)) - \mathrm{N}) \times 2^{12}) - F_{MSB}) \times 2^{13}) = 0$$

where:
F_{MSB} is the 12-bit MSB FRAC value in Register R5.
F_{LSB} is the 13-bit LSB FRAC value in Register R6.
int() makes an integer of the argument in parentheses.

REFERENCE DOUBLER

The on-chip reference doubler allows the input reference signal to be doubled. This doubling is useful for increasing the PFD comparison frequency. Doubling the PFD frequency typically improves the noise performance of the system by 3 dB.

FREQUENCY MEASUREMENT PROCEDURE

Use the following procedure to measure the output locked frequency of the ADF5902:

1. In Register R3, set the readback control bits (Bits[DB10:DB5]) to 26.
2. Read back the frequency counter value on DOUT and record this value as Frequency 1 (see Figure 3).
3. In Register R7, set the CLK1 bits (Bits[DB23:DB12]) to 1808.
4. In Register R13, set the CLK2 bits (Bits[DB18:DB7]) to 10.
5. In Register R5, set the ramp on bit (Bit DB29) to 0.
6. In Register R13, Set the clock divider mode bits (Bits[DB20:DB19]) to 2.
7. Allow a minimum delay of 428 µs (CLK_{DIV}/f_{PFD} (sec)).
8. In Register R3, set the readback control bits (Bits[DB10:DB5]) to 26.
9. Read back the frequency counter value on DOUT and record this value as Frequency 2.

   Where Frequency 1 > Frequency 2,

   Frequency Counter Value Delta = (2^{16} − *Frequency 1*) + *Frequency 2*.

   Where Frequency 2 > Frequency 1,

   Frequency Counter Value Delta = *Frequency* 2 − *Frequency* 1.
10. Calculate the output frequency using the following formula:

    Output Frequency = (*Frequency Counter Value Delta*/CLK_{DIV}) × f_{PFD} × N_{DIV} × 2

    where:
    CLK_{DIV} = ((CLK_2 × 2^{12}) + CLK_1).
    f_{PFD} = f_{REF}/R_{DIV}.
    N_{DIV} = INT value + (FRAC value/(2^{25})).
11. Set Register R13 and Register R7 back to the original settings and enable the ramp function in Register R5 if required.

WAVEFORM GENERATION

The ADF5902 is capable of generating five types of waveforms in the frequency domain: single ramp burst, single triangular burst, single sawtooth burst, continuous sawtooth ramp, and continuous triangular ramp. Figure 43 through Figure 47 show the types of waveforms available.

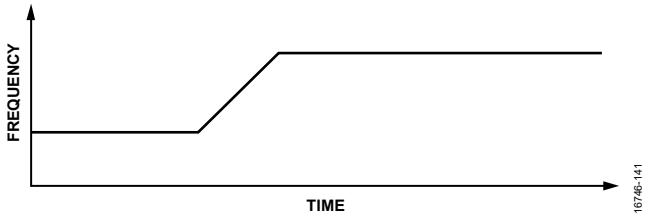

Figure 43. Single Ramp Burst

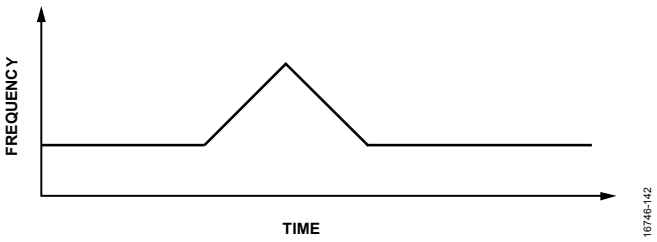

Figure 44. Single Triangular Burst

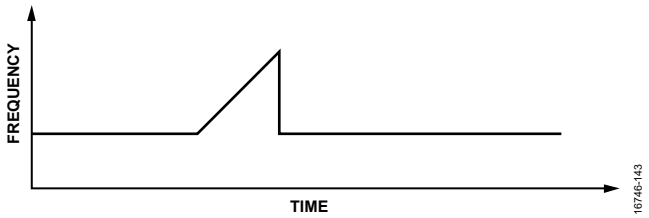

Figure 45. Single Sawtooth Burst

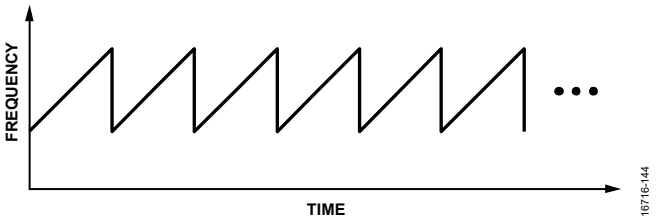

Figure 46. Continuous Sawtooth Ramp

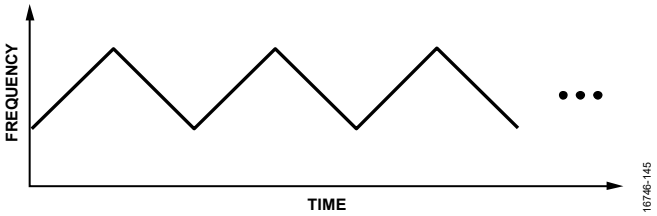

Figure 47. Continuous Triangular Ramp

WAVEFORM DEVIATIONS AND TIMING

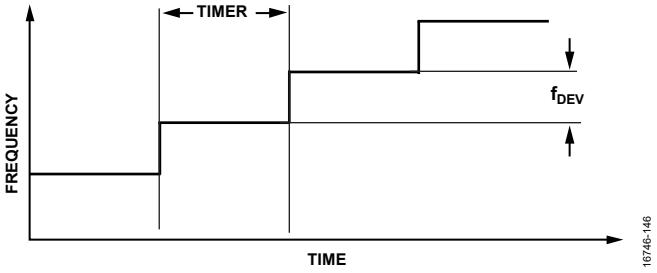

Figure 48. Waveform Timing

The key parameters that define a ramp are

- Frequency deviation
- Time per step
- Number of steps

Frequency Deviation

The frequency deviation for each frequency hop is set by

$$f_{DEV} = (f_{PFD}/2^{25}) \times (DEV \times 2^{DEV\_OFFSET}) \quad (7)$$

where:
f_{PFD} is the PFD frequency.
DEV is a 16-bit word (Bits[DB20:DB5] in Register R14).
DEV_OFFSET is a 4-bit word (Bits[DB24:DB21] in Register R14).

Time per step

The time between each frequency hop is set by

$$Timer = CLK_1 \times CLK_2 \times (1/f_{PFD}) \quad (8)$$

where:
CLK_1 and CLK_2 are the 12-bit clock values (12-bit CLK_1 divider in Register R7 and 12-bit CLK_2 divider in Register R13).

Bits[DB20:DB19] in Register R13 must be set to 11 for ramp divider.
f_{PFD} is the PFD frequency.

Either CLK_1 or CLK_2 must be greater than 1, that is, $CLK_1 = CLK_2 = 1$ is not allowed.

Number of Steps

A 20-bit step value (Bits[DB24:DB5] in Register R15) defines the number of frequency hops that take place. The INT value cannot be incremented by more than $2^8 = 256$ from its starting value.

RAMP AND MODULATION

All ramps are generated according to the scheme shown in Figure 49. The total ramp is separated into four sections. Each section consists of a delay section and a slope section. Each slope is made up of one or more steps. Each step has a programmed frequency deviation and step time.

There are numerous ramp shapes available (see the Waveform Generation section). Depending on the chosen shape, some or all of the ramp slopes must be programmed. Figure 49 shows what must be programmed for each shape. The slope being programmed is controlled by

- CLK DIV SEL (Register R13, Bits[DB6:DB5]).
- DEV SEL (Register R14, Bits[DB26:DB25]).
- Step SEL (Register R15, Bits[DB26:DB25]).

Typically, each register must be written multiple times, one time for each slope.

The frequency deviation for each step of a slope is set by

$$f_{DEV} = (f_{PFD}/2^{25}) \times (DEV \times 2^{DEV\_OFFSET})$$

where:
f_{DEV} is the frequency deviation of a step.
f_{PFD} is the PFD frequency.
DEV is the deviation value (Register R14, Bits[DB20:DB5]).
DEV_OFFSET is the deviation offset (Register R14, Bits[DB24:DB21]).

The time for each step of a slope is set by

$$Timer = CLK_1 \times CLK_2 \times (1/f_{PFD})$$

where:
Timer is the time per step.
CLK_1 is the CLK_1 value (Register R7, Bits[23:12]).
CLK_2 is the CLK_2 value (Register R13, Bits[18:7]).

CLK_1 is common to all slopes.

The number of steps per slope is programmed in Register R15, Bits[DB24:DB5].

When programming the registers for a ramp, write the registers in descending order. Then write to Register R5 to enable the ramp (Register R5, Bit DB29 = 1) must be last.

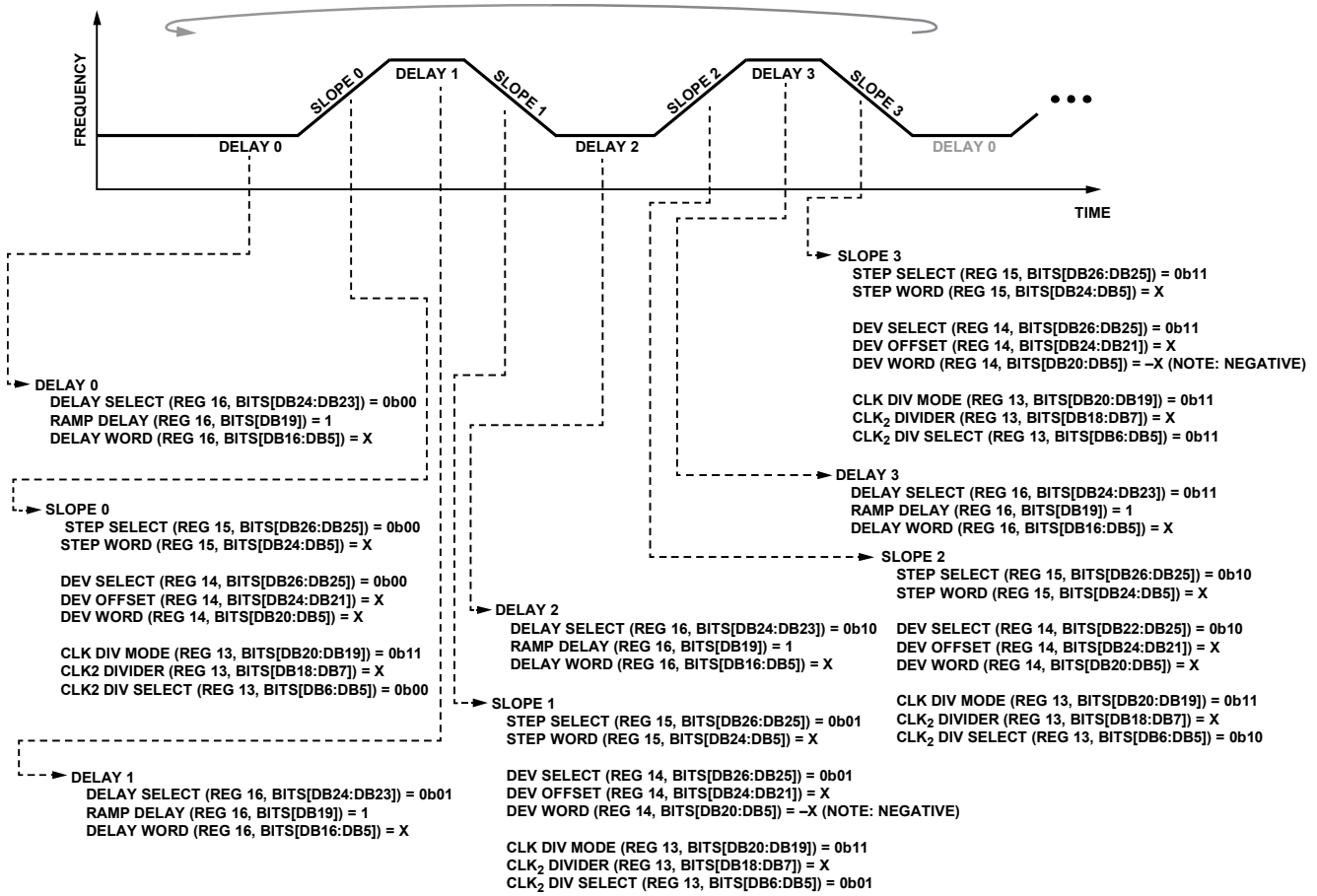

Figure 49. Ramp Sections

Ramp Complete and Ramp-Down Signals to MUXOUT

Figure 50 shows the ramp complete signal on MUXOUT.

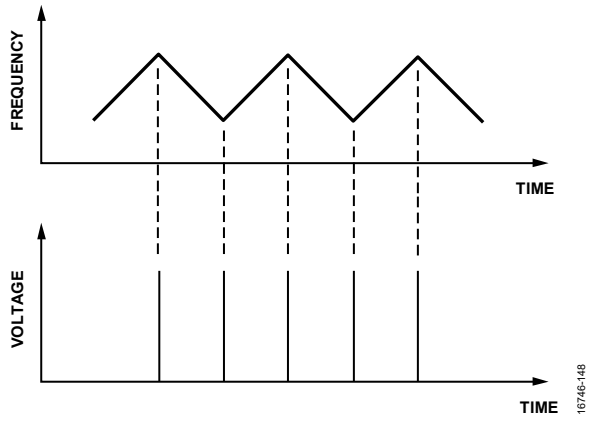

Figure 50. Ramp Complete Signal on MUXOUT

To activate this function, set Bits[DB15:DB12] in Register R3 to 1111, and set Bits[DB19:DB5] in Register R4 to 0x00C0.

Figure 51 shows the ramp-down signal on MUXOUT.

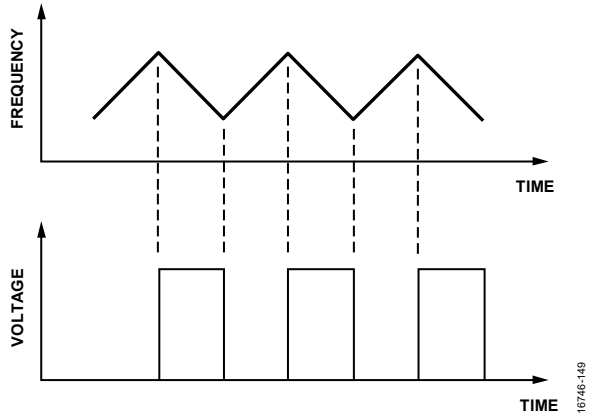

Figure 51. Ramp-Down Signal on MUXOUT

To activate this function, set Bits[DB15:DB12] in Register R3 to 1111, and set Bits[DB19:DB5] in Register R4 to 0x0100.

External Control of Ramp Steps

The internal ramp clock can be bypassed and each step can be triggered by a pulse on the TX_DATA pin. This process allows transparent control of each step. Enable this feature by setting Bit DB30 in Register R14 to 1.

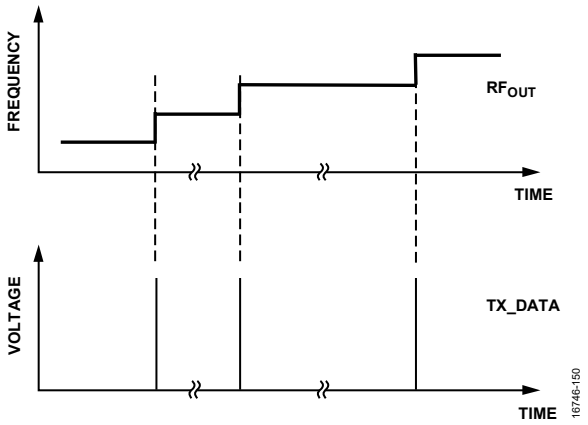

Figure 52. External Control of Ramp Steps

APPLICATION OF THE ADF5902 IN FMCW RADAR

Figure 53 shows the application of the ADF5902 in a frequency modulated continuous wave (FMCW) radar system.

In the FMCW radar system, the ADF5902 generates the sawtooth or triangle ramps necessary for this type of radar to operate.

The ADF5902 CP_{OUT} pin controls the V_{TUNE} pin on the ADF5902 transmitter MMIC and thus the frequency of the VCO and the transmitter output signal on $TX_{OUT}1$ or $TX_{OUT}2$. The LO signal from the ADF5902 is fed to the LO input on the ADF5904.

The ADF5904 downconverts the signal from the four receiver antennas to baseband with the LO signal from the transmitter MMIC.

The downconverted baseband signals from the four receiver channels on the ADF5904 are fed to the ADAR7251 4-channel, continuous time, Σ-Δ ADC.

A digital signal processor (DSP) follows the ADC to handle the target information processing.

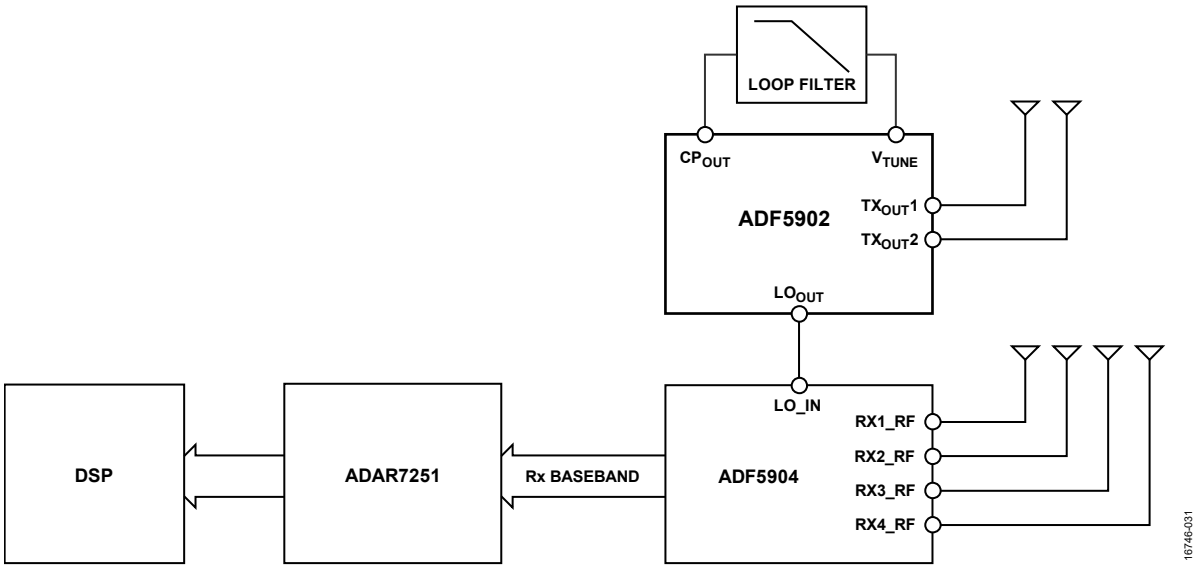

Figure 53. FMCW Radar with the ADF5902