EV14Y36A

EV14Y36A Evaluation Board User Guide

Introduction

The EV14Y36A evaluation board is developed based on Microchip's PD69210 and PD69208 (PD69208M/PD69208T4/PD69204T4) Power over Ethernet (PoE) chipset for use with Microchip's VSC56xx Ethernet switch development boards. The board operates on 24 4-pair PoE ports (two pairsets) based on the IEEE® 802.3bt specification.

Microchip's PD69208M/PD69208T4/PD69204T4 PoE manager IC integrates power, analog, and state-of-the-art logic into a single 56-pin, plastic QFN package. The device is used in Ethernet switches and midspans/injectors to allow network devices to share power and data over the same Ethernet cable.

The PD69208M/PD69208T4 device is an eight-port, and the PD69204T4 device is a four-port, mixed-signal and high-voltage PoE driver. With the PD69210 external MCU, it performs as a Power Sourcing Equipment (PSE) system. Microchip's PD69210 PoE controller is a cost-effective and pre-programmed MCU designed to implement the Enhanced Mode PoE system.

The PD69208M/PD69208T4/PD69204T4 and PD69210 chipset supports PoE Powered Device (PD) detection, power-up, and protection according to IEEE 802.3af/at/bt standards and a legacy/pre-standard PD detection. It provides real-time PD protection through the following mechanisms: overload, under-load, over-voltage, over-temperature, and short circuit, and enables operation in a Standalone mode. It also executes all real-time functions as specified in IEEE 802.3at and IEEE 802.3bt standards, including PD detection (AF and AT).

The PD69208M/PD69208T4/PD69204T4 device supports supply voltages between 32 V and 57 V without additional power sources. A system that powers over four pairs is implemented by combining two ports of PD69208M/T4 and PD69204T4, enabling an extra feature for simple and low-cost, high-power PD devices. Ongoing monitoring of system parameters for the host software is available through communication. For higher reliability, internal thermal protection is implemented in the chip. The PD69208M/PD69208T4/PD69204T4 is the most integrated PSE IC including internal MOSFET and sense resistor to achieve a low-power dissipation.

The PD69210 features an eSPI bus for each PD69208M/PD69208T4/PD69204T4. It is based on the Microchip D21 family. The PD69210 utilizes an I^2C or UART interface to the host CPU. It is designed to support the software that is field-upgradable through the communication interface. The evaluation system provides designers with the required environment to evaluate the performance.

The evaluation system has the following features.

- Interface to SparX VSC56xx switch development board
- Two connector gangs (each contains 12 4-pair ports)
- Switch domain isolated from PoE domain
- PoE controller manual Reset and serial communication settings
- LED status indication for all ports (LED–stream)
- Single power source
- 0 °C to 40 °C operating temperature
- RoHS compliant

Figure 1. EV14Y36A Evaluation Board and Dimensions

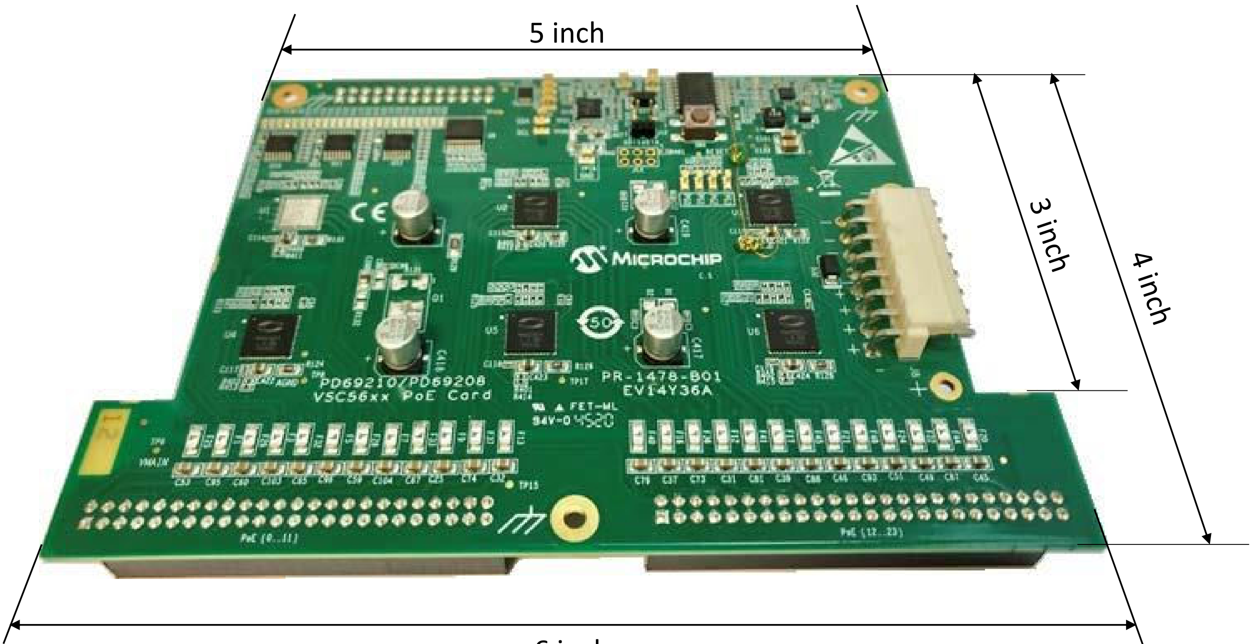
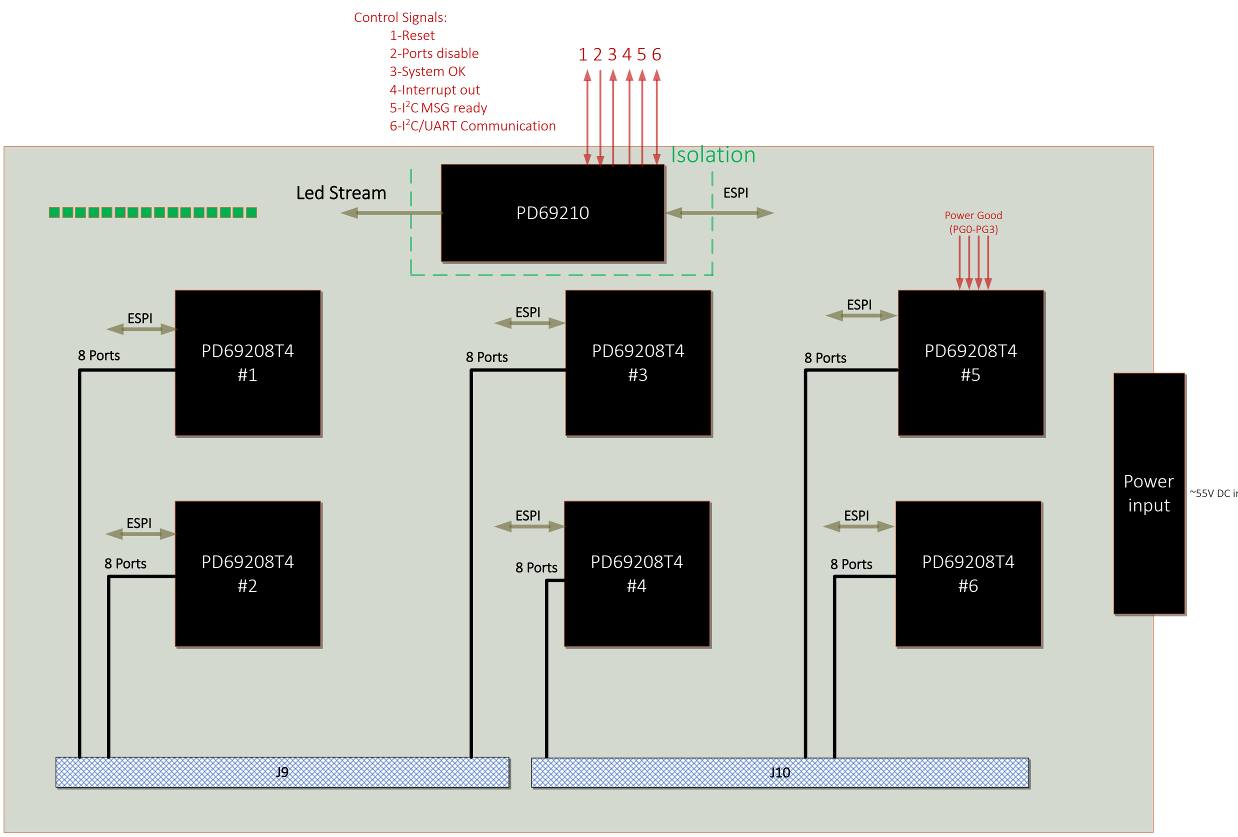


Figure 2. EV14Y36A Evaluation System Block Diagram



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1. Overview

This section provides the basic overview of the EV14Y36A evaluation board.

1.1 Power

The Evaluation Board (EVB) is powered by a single source via the DC connector J8. The input voltage level can be selected according to the IEEE 802.3 PoE standards.

- IEEE 802.3af: 44 V_{DC} to 57 V_{DC}
- IEEE 802.3at: 50 V_{DC} to 57 V_{DC}
- IEEE 802.3bt: 50 V_{DC} to 57 V_{DC} for type 3 and 52 V_{DC} to 57 V_{DC} for type 4.

The recommended voltage level is 55 V_{DC} that covers all PoE standards.

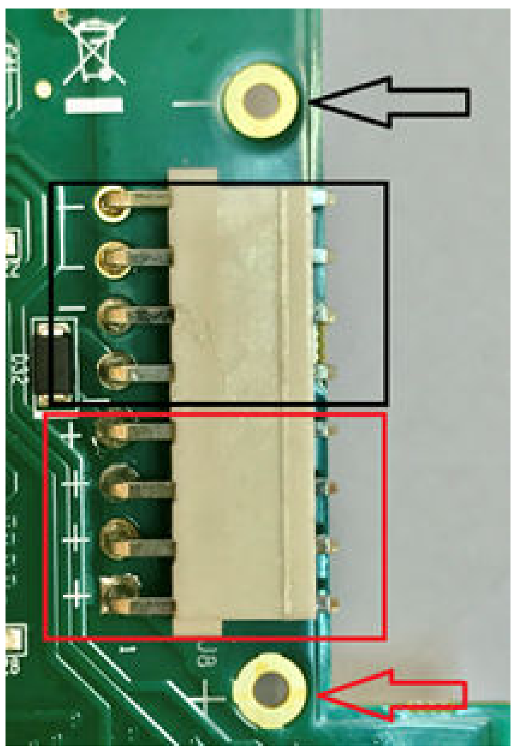
The EVB has two power domains:

- PoE domain, which is fed directly by the main supply, and it is the power domain provided by the J9 and J10 connectors.
- Isolated 3.3 V_{DC}, which feeds PD69210, LED-stream, and serial communication peripherals. The isolated 3.3 V_{DC} is generated by motherboard, provided by the J7 connector (a DC/DC module).

Note: The EVB DC is polarity sensitive. The correct polarity is shown in the following figure.

Important: The DC connector J8 is limited to current level up to 24 A (4 x 6 A per pin). If higher current is needed, the two via holes next to J8 can be used by soldering a cable to it. The two via holes support up to 40 A to feed the whole EVB.

Figure 1-1. Power via Holes



1.2 Interface and Control

This section describes the set-up procedures for serial communication, reset push-button, PoE ports disable, and power good input (PGD0–PGD3).

1.2.1 Serial Communication Settings

The EVB supports serial communication with the PD69210 by UART and I^2C, to allow a user-friendly experience using Microchip's dedicated GUI.

Two different I^2C address can be set by the host:

- When the host sets the address pin to 3.3 V ('1'), the PD69210 I^2C address is set to 0x3C.
- When the host sets the address pin to 0 V ('0'), the PD69210 I^2C address is set to 0x1C.

To change I^2C address, R439 should be installed according to the following table (while R411 is not installed). The EVB is set to I^2C address 0x3C (R439=7.5K, R441=20K).

When R439 and R441 are not installed, the PD69210 is set to UART.

The following figure shows I^2C address settings.

Figure 1-2. I^2C Address Settings Diagram

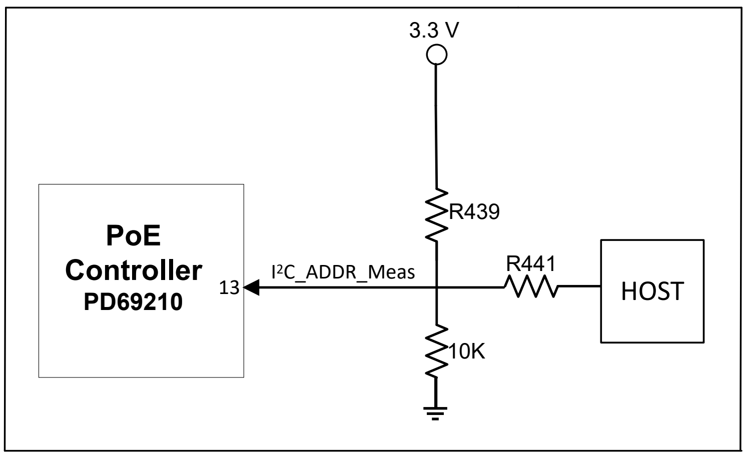


Table 1-1. I^2C Address Settings

I^2C Address	Address (Hex)	R439 (kΩ)
#0	UART	N.C
#1	0x4	147
#2	0x8	86.6
#3	0xC	57.6
#4	0x10	43.2
#5	0x14	34
#6	0x18	26.7
#7	0x1C	22.1
#8	0x20	18.2
#9	0x24	15.4
#10	0x28	13
#11	0x2C	11

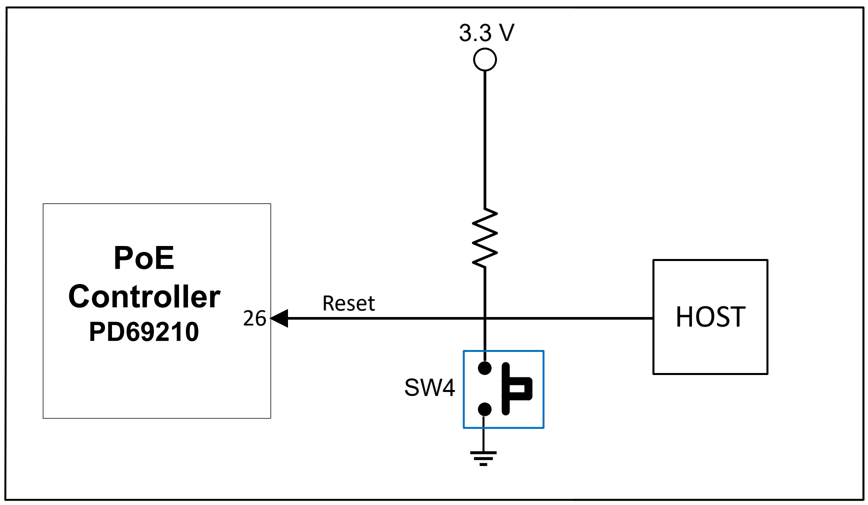
...........continued		
I²C Address	Address (Hex)	R439 (kΩ)
#12	0x30	9.31
#13	0x34	7.87
#14	0x38	6.49
#15	0x3C	5.49

1.2.2 Reset Push–button Settings

The push–button is connected to the Reset pin of the PD69210 (Pin 26). Pressing on switch SW4 connects the Reset pin to GND. The host can reset the board by setting this pin to ‘0’.

The following figure shows switch SW4.

Figure 1-3. Reset Control Diagram



1.2.3 PoE Ports Disable Settings

The jumper J12 is connected to the Disable pin of the PD69210 (Pin 4). When the jumper J12 is installed, the Disable pin is connected to GND. The host can disable all port by setting this pin to ‘0’.

The following figure shows the J12 jumper settings.

Figure 1-4. Ports Disable Control Jumper Diagram

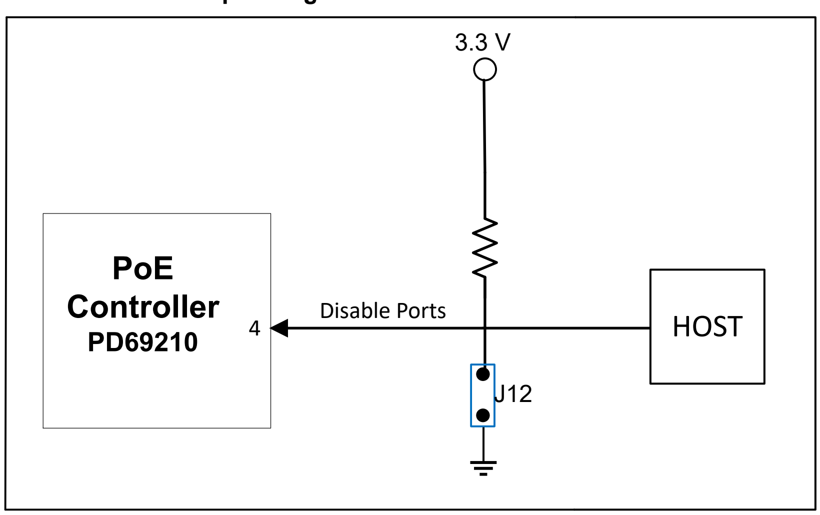
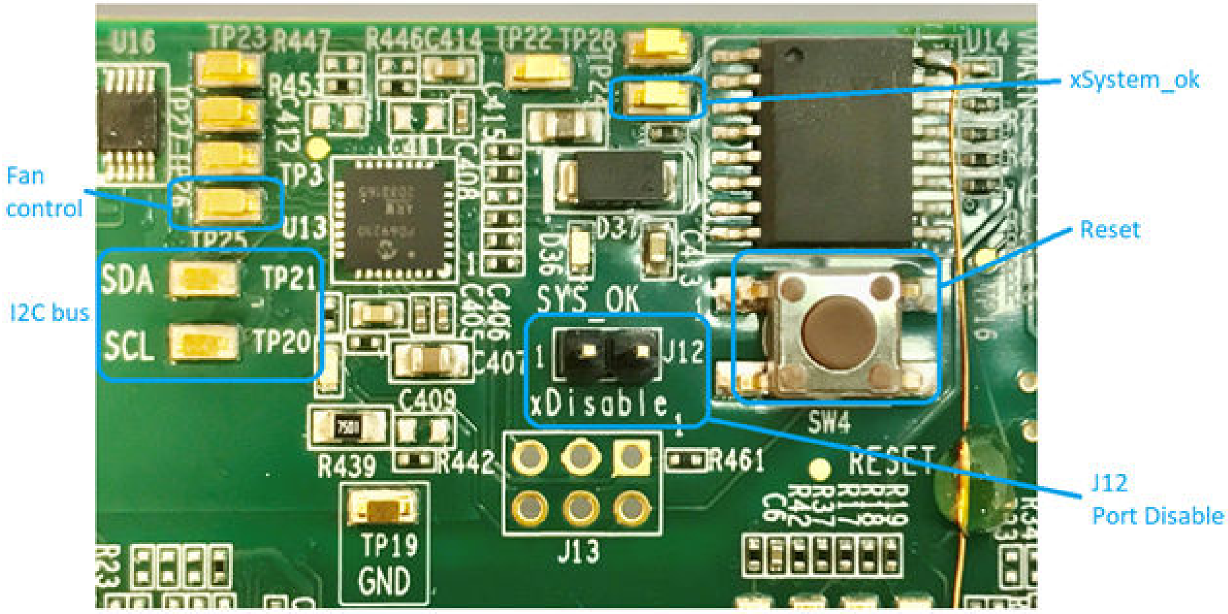


Figure 1-5. I2C Bus Test Point and Control Signals



1.2.4 Power Good Input (PGD0–PGD3) Settings

The EVB supports feeding from up to four power supplies, which includes 16 power banks (bank0 to bank15). Each power supply must generate a digital signal (3.3 V_{DC}), which indicates the power supply is active. The generated digital signal must be connected to one of the PGD pins of PD69208 (pins 41, 46, 47, and 56).

On the EVB, four PGD pins are pulled–down with a 10K resistor to DGND, which sets the default power bank to 0x00. To set a different bank than 0x00, the user can use the PG0-PG3 tests points, located next to U3.

Figure 1-6. PGD0-PGD3 Test Points Diagram

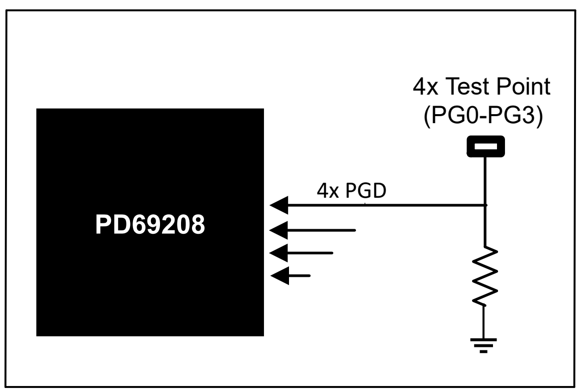
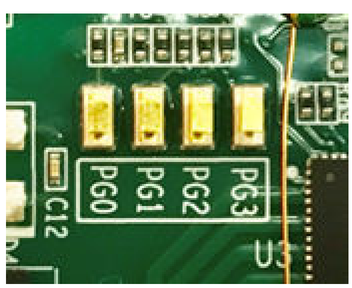


Figure 1-7. PGD0-PGD3 Test Points



1.3 LED Indication

The following table lists the evaluation board status indication LEDs.

Table 1-2. LED List

Designation	Function
D34	V_{main} ON
D35	Interrupt out (active–low)
D36	System OK (active–low)
Port (0-23)	Green LED per port: • LED OFF= Port is OFF • LED ON= Port is ON • LED blinking= Port is OFF due to error/under load/ power management

2. Installation and Settings

This section describes the installation and operation settings of the EV14Y36A evaluation board.

Take the following precautions before starting the installation.

- Ensure that the power supply of the board is turned off before plugging in the DC connecter.
- Ensure the correct polarity of the power supply cable. The polarity of the power supply cable is as shown in Figure 1-1.
- Install the EVB into the motherboard using both ports connectors (J9 and J10) and signal connector (J7).
- Turn the main supply ON after the DC connector is plugged in.
- After turning on the EVB DC power supply, turn on the motherboard power supply.

2.1 Ports Matrix

Ensure that the ports matrix is configured according to the following table.

Table 2-1. Ports Matrix

Logical Port	Physical Port A	Physical Port B
0	16	255
1	17	255
2	18	255
3	19	255
4	20	255
5	21	255
6	22	255
7	23	255
8	0	24
9	1	25
10	2	26
11	3	27
12	4	28
13	5	29
14	6	30
15	7	31
16	8	32
17	9	33
18	10	34
19	11	35
20	12	36
21	13	37
22	14	38
23	15	39

2.2 Fuses

On the main board, there are eight fuses for the PD69208, located on top and bottom side, close to the output port connectors J9 and J10. The fuse is connected on the Vport_Negpin of each port.

IEC62368-1 Ed2 (released in October 2018 and effective December 2020) requires per port fuses for a system power supply greater than 250 W.

Figure 2-1. Fuses—Top View

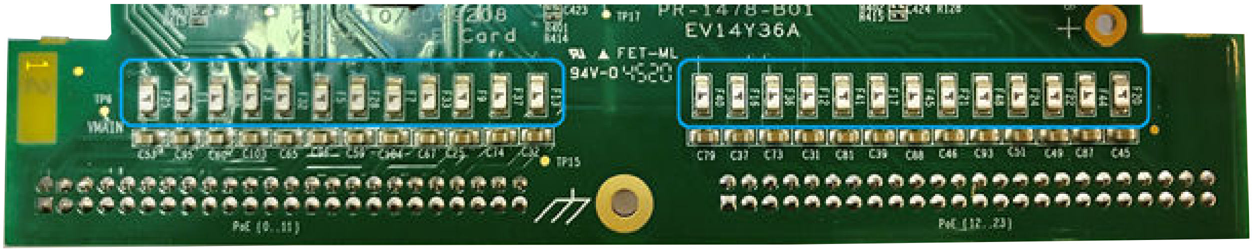
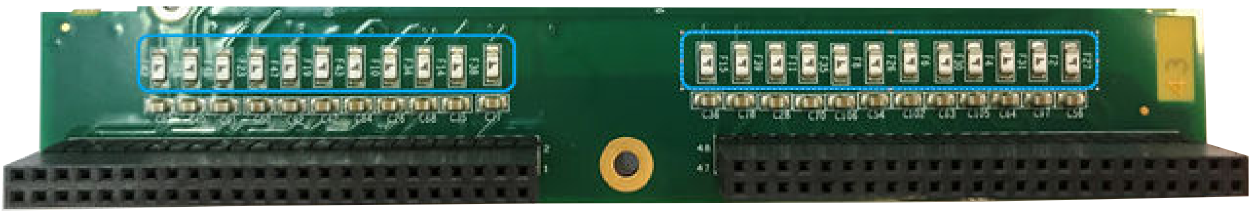


Figure 2-2. Fuses—Bottom View



Important: U1 (PD69208T4 #1) is not populated. Therefore, the EVB supports 8 2-pair ports and 16 4-pair ports. The following figure shows the unconnected pins 1, 7, 9, 15, 17, 23, 25, and 31 in J9.

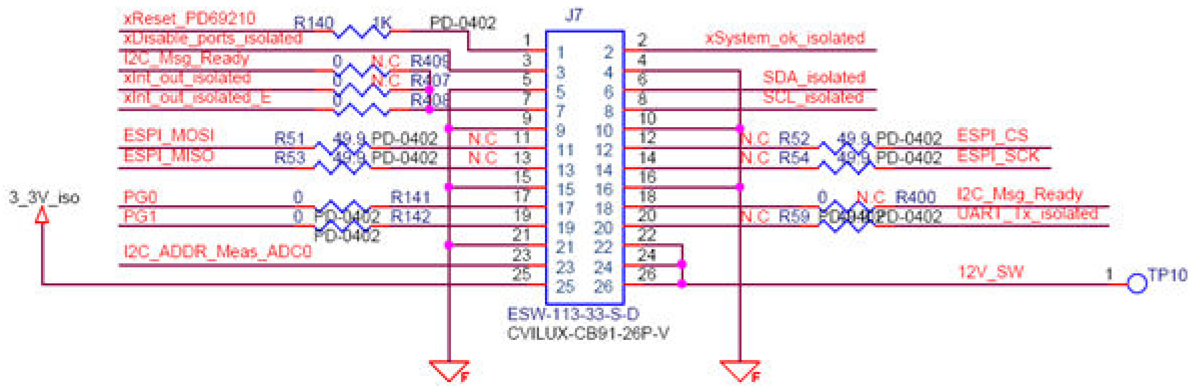
Figure 2-3. Unconnected Pins in J9

2.3 Connectors J7, J9, and J10

The EV14Y36A EVB contains three connectors that are connected to the host motherboard.

- The J7 carries isolated 3.3 V, control signals, communication signals, and the isolated ESPI signals.

Figure 2-4. Connector J7 Pinout Diagram



- The J9 and J10 carry the 24 PoE ports that have high PoE current.

Signals named VPORT_NEG_OUTn and VPORT_NEG_OUT_Un are connected to the physical ports of PD69208. The current can reach up to 1 A.

Figure 2-5. Connector J9 Pinout Diagram

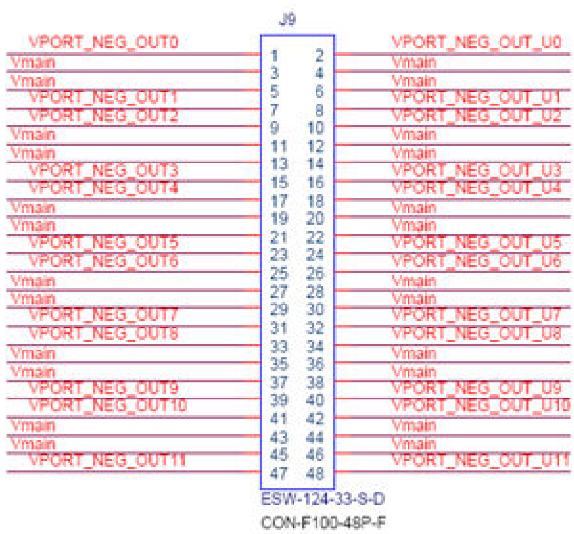
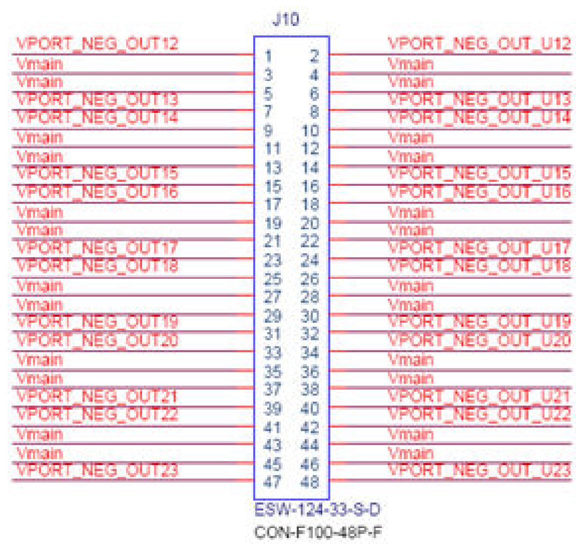


Figure 2-6. Connector J10 Pinout Diagram



2.4 Schematics

The full schematics of the EVB are available on the Microchip website.

3. Revision History

Revision	Date	Description
A	03/2021	Initial Revision

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