

DESCRIPTION

The EV1925-R-00A is an evaluation board for the MP1925, a high frequency Half-Bridge gate driver. Its high-side and low-side driver channels are independently controlled and matched with a time delay of less than 5ns.

The demo board is configured as a buck converter. INH and INL are independent signals of each other. Complementary PWMs with proper dead time should be implemented for INH and INL.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Driver Power Supply Voltage	V _{DD}	8 - 15	V
Input Power Supply Voltage	V _{IN}	0-100	V

FEATURES

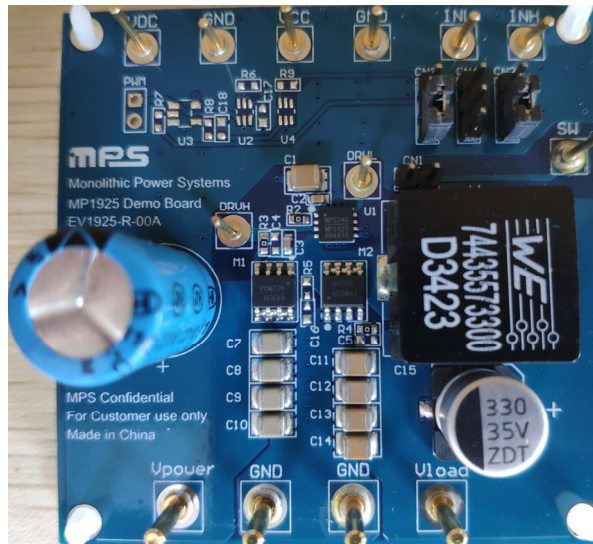
- 115V Bootstrap Voltage Range
- On-Chip Bootstrap Diode
- Quiescent Current of Less than 150uA
- Typical Propagation Delay of 20ns
- Gate Driver Matching of Less than 5ns
- UVLO for Both High-Side and Low-Side Gate Drivers
- TTL Compatible Input
- Available in a QFN-8 (4mmx4mm) Package

APPLICATIONS

- Motor Drivers
- Telecom Half-Bridge Power Supplies
- Avionics DC/DC converters

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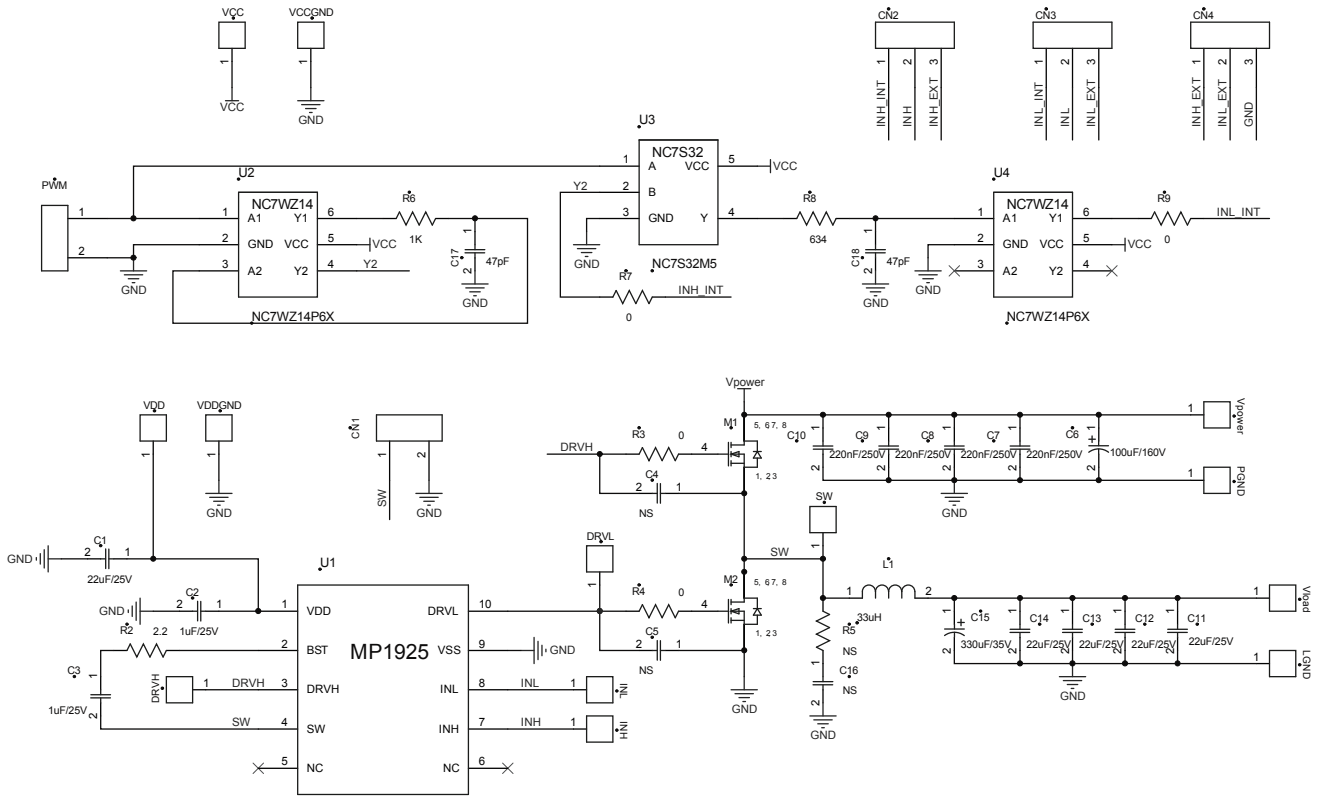
EV1925-R-00A EVALUATION BOARD



(L × W × H) 6.35cm x 6.35cm x 1cm

Board Number	MPS IC Number
EV1925-R-00A	MP1925GR

EVALUATION BOARD SCHEMATIC



EV1925-R-00A BILL OF MATERIALS

Qty	RefDes	Value	Description	Package	Manufacturer	Manufacturer P/N
5	C1, C11, C12, C13, C14	22µF/25V	Ceramic Cap., 25V, X5R	1210	Murata	GRM32ER71E226KE15L
2	C2, C3	1µF/25V	Ceramic Cap., 25V, X5R	0603	TDK	C1608X5R1E105K
3	C4, C5, C16	NS				
1	C6	100µF/160V	Electrolytic Cap., 160V	DIP	江海	CD110-160V100
4	C7, C8, C9, C10	220nF/250V	Ceramic Cap., 250V, X7R	1210	Murata	GRM32DR72E224KW01L
1	C15	330µF/35V	Electrolytic Cap., 35V	SMD	江海	VZ1-35V330
1	L1	33µH	Inductor, 33uH, 8.5A;	SMD	Würth	74435573300
1	R5	NS				
3	R2, R3, R4	0	Film Resistor, 5%,	0603	Yageo	RC0603JR-070RL
2	M1, M2	AM4490N	N-channel MOS	PowerPAK SO-8	Analog Power	AM4490N
1	U1	MP1925	Integrated Gate Driver	SOIC-8	MPS	MP1925GR
4	Vpower, Vload, GNDx2		2mm 金针			
9	VDD, GND, VCC, GND, INL, INH, DRVH, DRVL, SW		1mm 金针			

PRINTED CIRCUIT BOARD LAYOUT

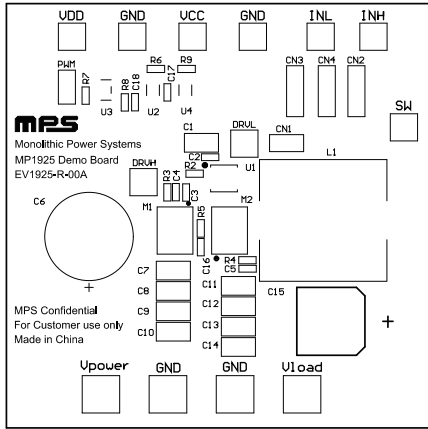


Figure 1: Top Silkscreen Layer

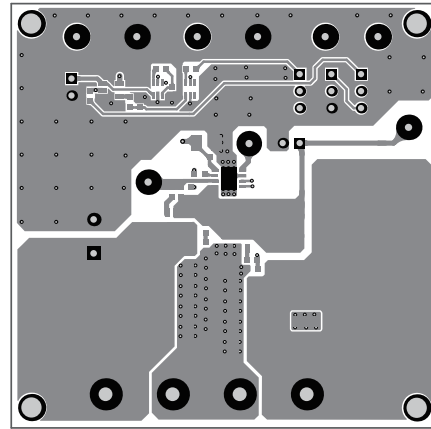


Figure 2: Top Layer

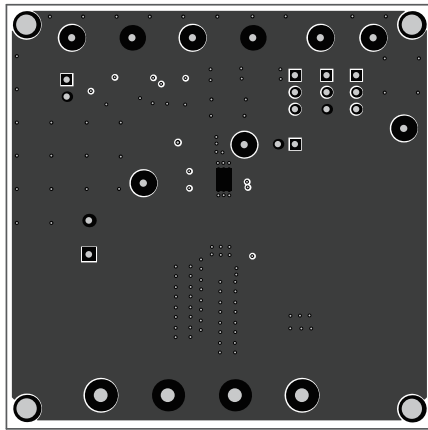


Figure 3: Mid-Layer 1

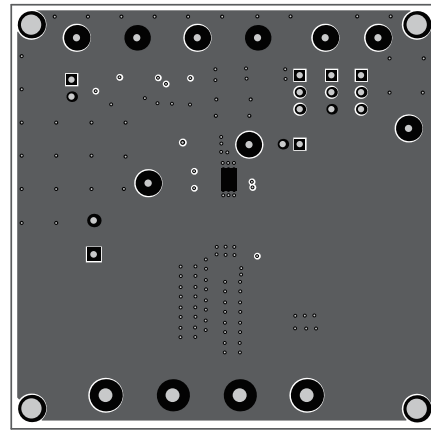


Figure 4: Mid-Layer 2

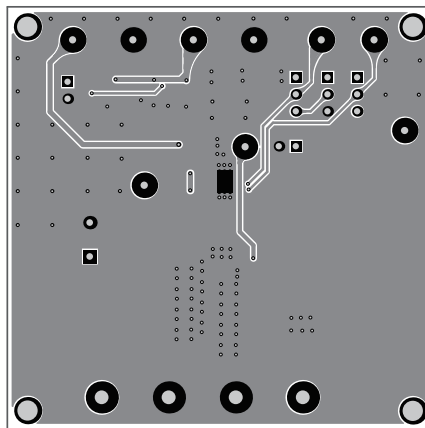


Figure 5: Bottom Layer