

v01.0316

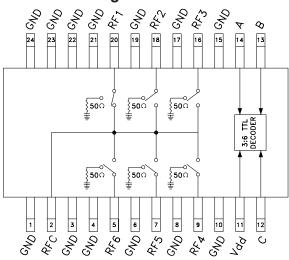
# GaAs MMIC SP6T NON-REFLECTIVE SWITCH, DC - 3 GHz

#### Typical Applications

The HMC252AQS24E is ideal for:

- Base Station
- CATV / DBS
- MMDS & WirelessLAN
- Test Equipment

### **Functional Diagram**



#### **Features**

Low Insertion Loss (2 GHz): 1.0 dB

Single Positive Supply:  $V_{DD} = +3V$  to +5V

Integrated 3:6 TTL Decoder

24 Lead QSOP Package

### General Description

The HMC252AQS24E is low-cost non-reflective SP6T switches in 24-lead QSOP packages featuring wideband operation from DC to 3.0 GHz. The switch offers a single positive bias and true TTL/CMOS compatibility. A 3:6 decoder is integrated on the switch requiring only 3 control lines and a positive bias to select each path. The HMC252AQS24E SP6T replaces multiple configurations of SP4T and SPDT MMIC switches and logic drivers.

## Electrical Specifications,

 $T_A = +25$ °C, For TTL Control and  $V_{DD} = +3.3V$ , 5V in a 50 Ohm System

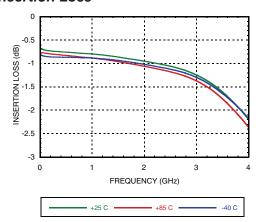
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Parameter	Fraguency	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Farameter	Frequency	\	Vdd = +3.3V		Vdd = +5V			
Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		0.8 1.0 1.2 1.4			0.8 1.0 1.2 1.4	1.2 1.3 1.5 1.8	dB
Isolation	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		45 40 38 32		38 32 29 26	45 40 38 32		dB
Return Loss "On State"	DC - 1 GHz DC - 2.5 GHz DC - 3.0 GHz		23 18 12		14 14 7	23 18 12		dB
Return Loss RF1-6 "Off State"	0.3 - 1 GHz 0.3 - 3.0 GHz 0.5 - 2.5 GHz		11 12 15		8 8 11	11 12 15		dB
Input Power for 1dB Compression	0.1 - 1.0 GHz 0.3 - 3.0 GHz		24 24		21	30 28		dBm
Input Third Order Intercept (Two-Tone Input Power = +10 dBm Each Tone)	0.3 - 3.0 GHz		47		42	47		dBm
Switching Characteristics								
tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	0.3 - 3.0 GHz		20 70			25 90		ns



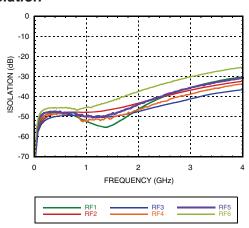
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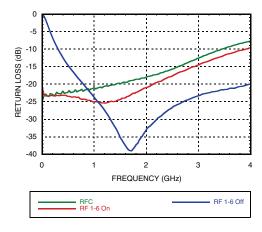
#### Insertion Loss [1]



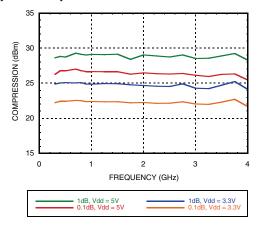
#### Isolation [1]



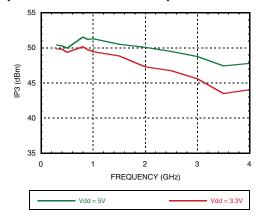
#### Return Loss [1]



#### **Input Compression**



#### **Input Third Order Intercept Point**



#### **Bias Voltages & Currents**

V <sub>DD</sub> (V)	ldd (Typ.) (mA)	Idd (Max.) (mA)
+3.3 (Vdc ± 5%)	3.3	7
+5.0 (Vdc ± 10%)	3.5	7

## TTL/CMOS Control Voltages

V <sub>DD</sub> (V)	State	Bias Condition	
+3.3	Low	0 to +0.8 Vdc @ 1μA Typ.	
	High	+2.0 to +3.3 Vdc @ 50 μA Typ.	
+5.0	Low	0 to +0.8 Vdc @ 2μA Typ.	
	High	+2.0 to +5 Vdc @ 60 μA Typ.	

 $[1] V_{DD} = 5V$ 

NOTE:

1. DC Blocking capacitors are required at ports RFC and RF1, 2, 3, 4, 5, 6.

2. Input is reflective when "ALL OFF" state is selected.

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## **Absolute Maximum Ratings**

Bias Voltage Range (Port Vdd)	+7 Vdc	
Control Voltage Range (A, B, C)	-0.5V to Vdd +1 Vdc	
Channel Temperature	150 °C	
Thermal Resistance Insertion Loss Path Terminated Path	130 °C/W 236 °C/W	
Storage Temperature	-65 to +150 °C	
Operating Temperature	-40 to +85 °C	
Maximum Input Power Vdd = +5 Vdc Insertion Loss Path Terminated Path	+29.8 dBm +24.4 dBm	
ESD Sensitivity (HBM)	Class 1A	

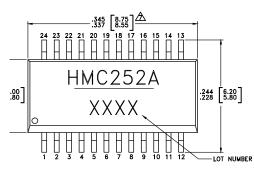
#### **Truth Table**

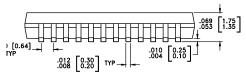
	Control Inpu	Signal Path State		
Α	В	С	RFCOM to:	
LOW	LOW	LOW	RF1	
HIGH	LOW	LOW	RF2	
LOW	HIGH	LOW	RF3	
HIGH	HIGH	LOW	RF4	
LOW	LOW	HIGH	RF5	
HIGH	LOW	HIGH	RF6	
LOW	HIGH	HIGH	ALL OFF	
HIGH	HIGH	HIGH	ALL OFF	

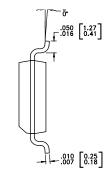


ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

## **Outline Drawing**







#### NOTES:

- 1. PACKAGE BODY MATERIAL:LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
- 2. LEAD MATERIAL: COPPER ALLOY.
- 3. LEAD PLATING: 100% MATTE TIN.
- 4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
- 5. CHARACTERS TO BE HELVETICA MEDIUM, .030 HIGH, LASER OR WHITE INK, LOCATED APPROXIMATELY AS SHOWN.
- A DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
- A DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
- 8. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

### Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC252AQS24E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	HMC252A XXXX

<sup>[1]</sup> Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX