HMC629ALP4E

v01.0716

3 dB LSB GaAs MMIC 4-BIT DIGITAL ATTENUATOR, DC - 10GHz

Typical Applications

The HMC629ALP4E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

3 dB LSB Steps to 45 dB

Power-Up State Selection

Low Insertion Loss: 2.25 dB

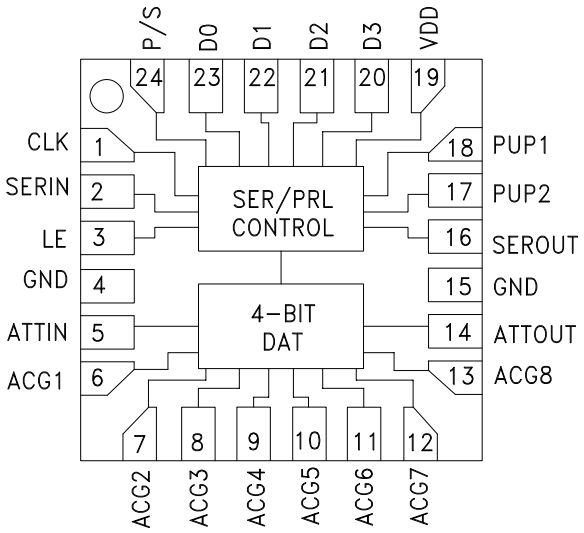
TTL/CMOS Compatible, Serial, Parallel or Latched Parallel Control

±0.25 dB Typical Step Error

Single +3V or +5V Supply

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

The HMC629ALP4E is a broadband 4-bit GaAs IC Digital Attenuator in a low cost leadless SMT package. This versatile digital attenuator incorporates off-chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 4-bit parallel word. The HMC629ALP4E is housed in a RoHS compliant 4x4 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25°C, 50 Ohm System, with Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 6 GHz 6 - 10 GHz		2.25 3.75		dB dB
Attenuation Range	DC - 10 GHz		45		dB
Return Loss (ATTIN, ATTOUT, All Atten. States)	DC - 6 GHz 6 - 10 GHz		17 15		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	DC - 6 GHz 6 - 10 GHz		± (0.4 + 4% of Atten. Setting) Max. ± (0.5 + 5% of Atten. Setting) Max.		dB dB
Input Power for 0.1 dB Compression	DC - 10 GHz		30 at Vdd=5V 25 at Vdd=3V		dBm
Input Third Order Intercept Point (Two-Tone Input Power = 20 dBm Each Tone)	DC - 10 GHz		55		dBm
Switching Speed tRise, tFall (10 / 90% RF) tON , tOFF (50% LE to 10 / 90% RF)	DC - 10 GHz		 100 120		 ns ns

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

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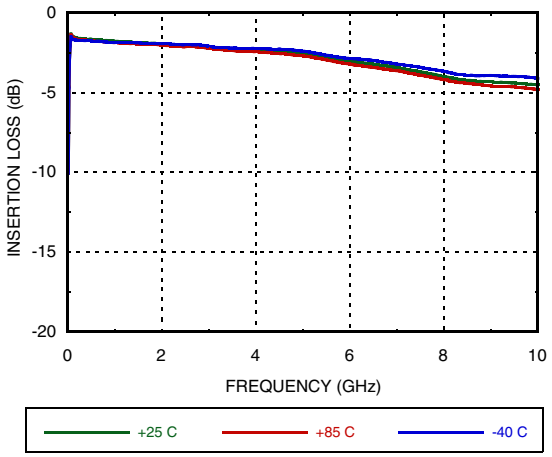
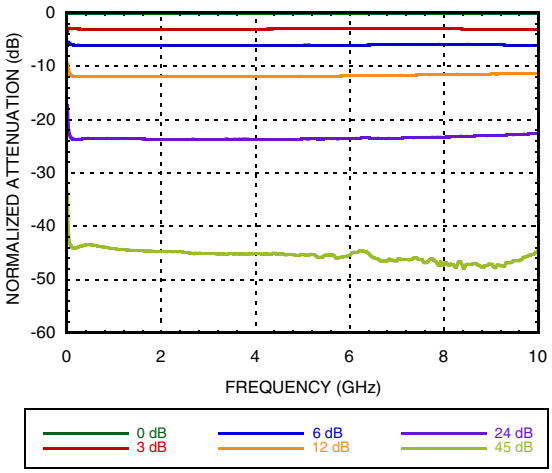
Insertion Loss vs. Temperature



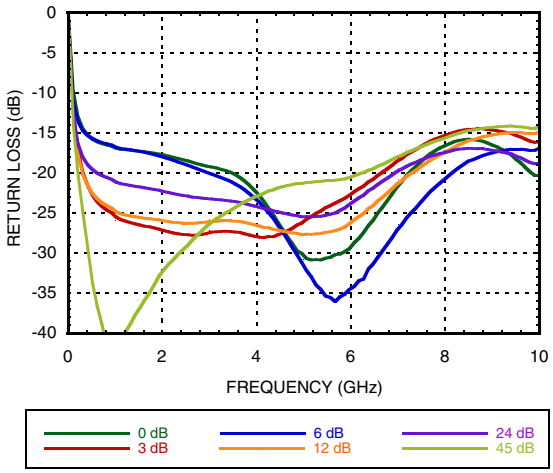
Normalized Attenuation

(Only Major States are Shown)



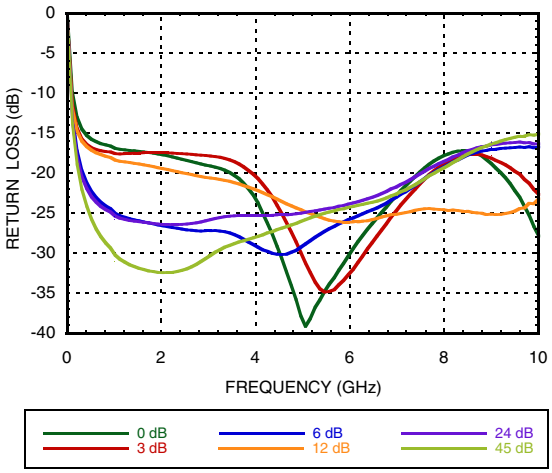
Input Return Loss

(Only Major States are Shown)

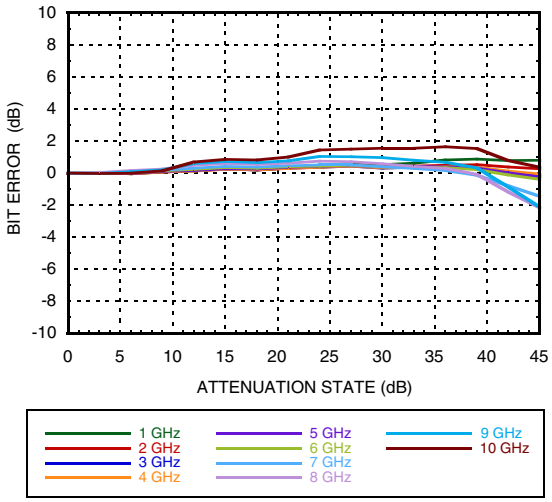


Output Return Loss

(Only Major States are Shown)

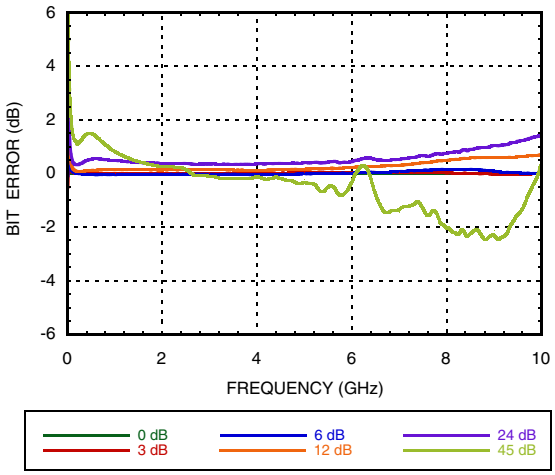


Bit Error vs. Attenuation State



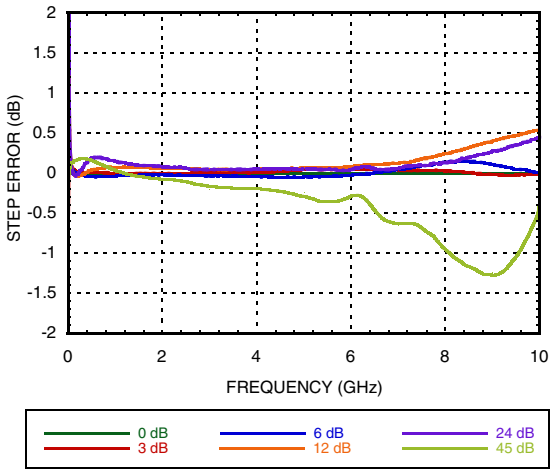
Bit Error vs. Frequency

(Only Major States are Shown)

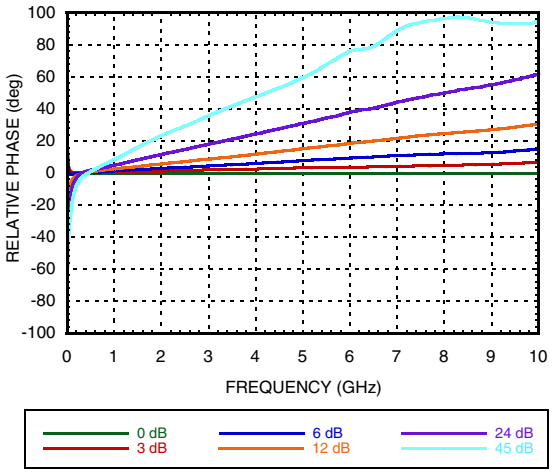


Step Error vs. Frequency

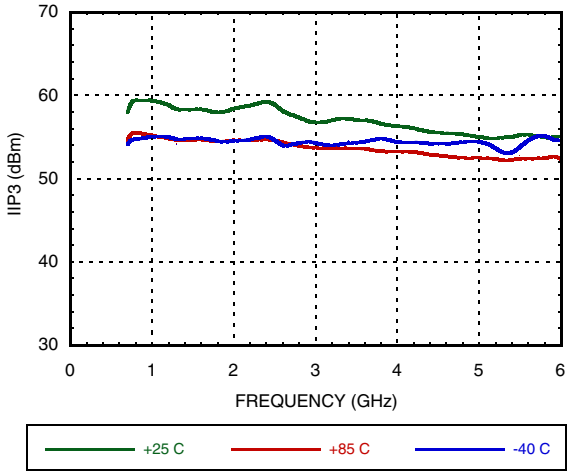
(Only Major States are Shown)



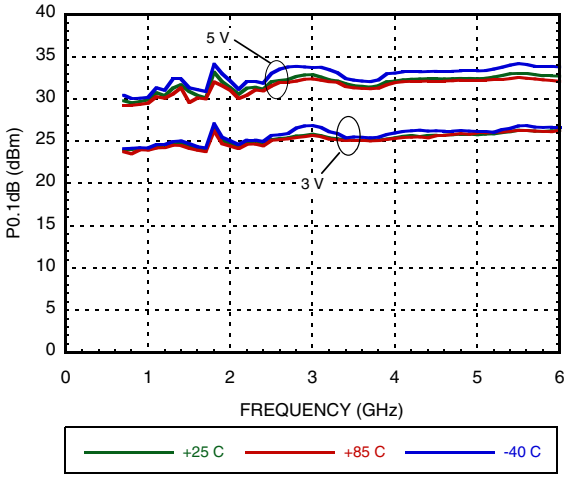
Normal Relative Phase vs. Frequency



IIP3 vs. Temperature, IL State



P0.1dB vs. Temperature, IL State

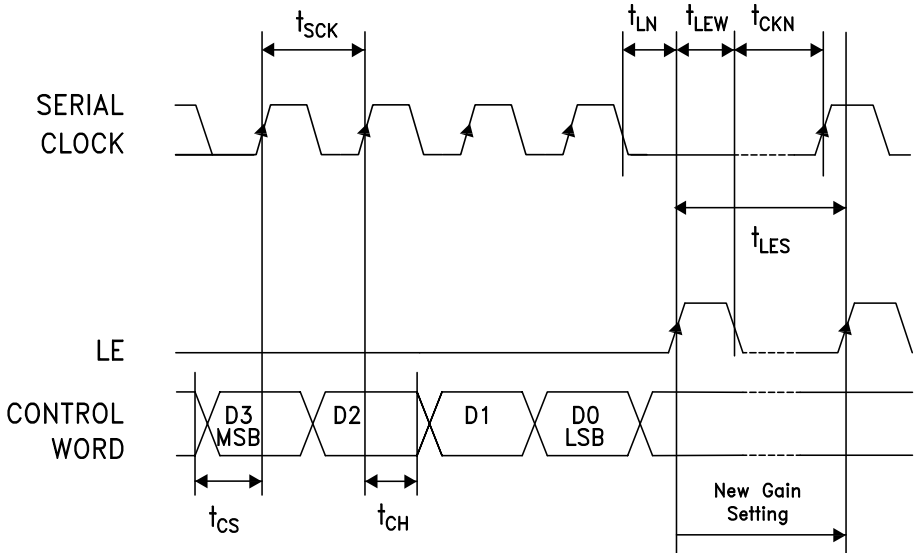


Serial Control Interface

The HMC629ALP4E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). The serial control interface is activated when P/S is kept high. The 4-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches are used, sufficient debouncing should be provided. When LE is high, 4-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and the input register is loaded with parallel digital inputs (D0-D3). When LE is high, 4-bit parallel data changes the state of the part per truth table.

For all modes of operations, the state will stay constant while LE is kept low.



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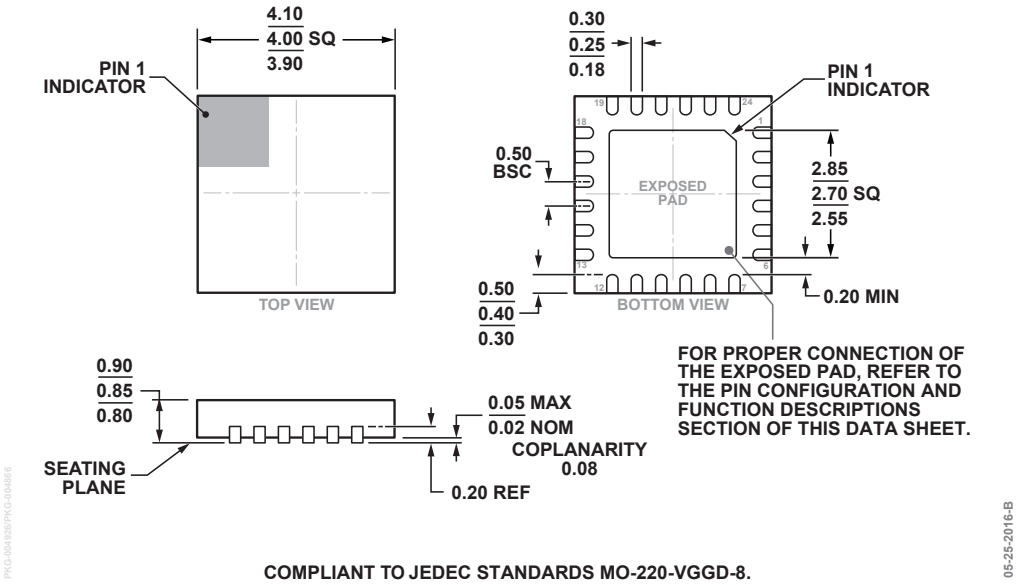
Absolute Maximum Ratings

RF Input Power (DC - 6 GHz)	28 dBm (T = +85 °C , Vdd= 5V)
Digital Inputs (Data, Shift Clock, Latch Enable & Serial Input)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.6V
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 14 mW/°C above 85 °C) [1]	0.88 W
Thermal Resistance	75 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

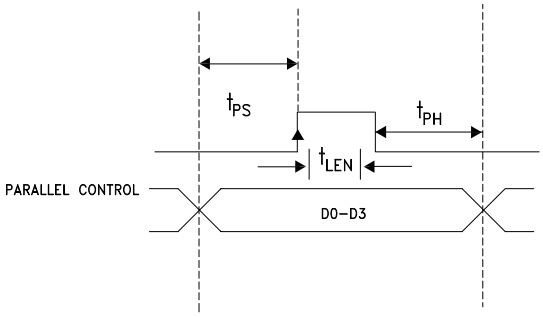
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC629ALP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 [1]	H629A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Parameter	Typ.(ns)
Min. serial period, t_{SCK}	100
Control set-up time, t_{CS}	20
Control hold-time, t_{CH}	20
LE setup-time, t_{LN}	10
Min. LE pulse width, t_{LEW}	10
Min LE pulse spacing, t_{LES}	630
Serial clock hold-time from LE, t_{CKN}	10
Hold Time, $t_{PH.}$	0
Latch Enable Minimum Width, t_{LEN}	10
Setup Time, t_{PS}	2

Timing Diagram *(Latched Parallel Mode)*



Parallel Mode *(Direct Parallel Mode & Latched Parallel Mode)*

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram below for reference.

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D3-D0 determines the power-up state of the part per truth table. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, VDD, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after VDD / GND

Bias Voltage

Vdd (Vdc)	Idd (Typ.) (mA)
5	1.5

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V at <1 µA	0 to 0.8V at <1 µA
High	2 to 3V at <1 µA	2 to 5V at <1 µA

PUP Truth Table

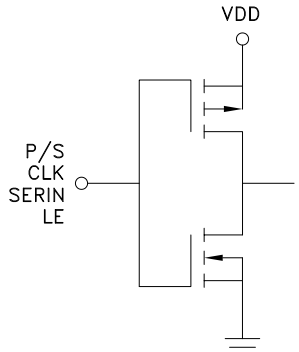
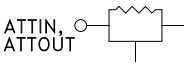
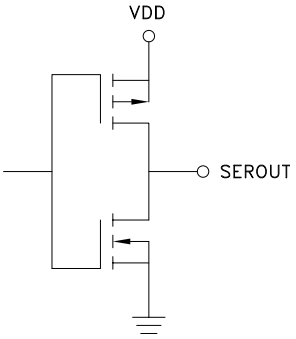
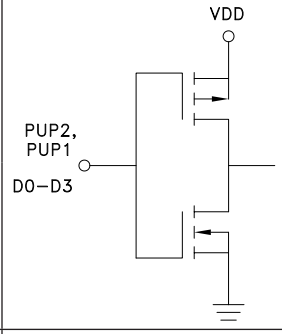
LE	PUP1	PUP2	Attenuation State
0	0	0	45 dB
0	1	0	45 dB
0	0	1	45 dB
0	1	1	Insertion Loss
1	X	X	0 to 45 dB

Note: This truth table is valid only when P/S = 0. Power-Up with LE= 1 provides direct parallel operation with D0 - D3.

Truth Table

Control Voltage Input				Attenuation State
D3	D2	D1	D0	
High	High	High	High	Reference I.L.
High	High	High	Low	3 dB
High	High	Low	High	6 dB
High	Low	High	High	12 dB
Low	High	High	High	24 dB
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.				

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
24	P/S	See truth table, control voltage table and timing diagram.	
1	CLK		
2	SERIN		
3	LE		
4, 15	GND	These pins and package bottom must be connected to RF/DC ground.	
5, 14	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
6 - 13	ACG1 - ACG6	External capacitors to ground are required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. See Application Circuit.	
16	SEROUT	Serial input data delayed by 4 clock cycles.	
17, 18	PUP2, PUP1	See truth table, control voltage table and timing diagram.	
20 - 23	D3, D2, D1, D0		
19	VDD	Supply voltage	

Application Circuit