Low Noise Amplifier, 0.01 GHz to 9 GHz

Data Sheet

HMC8413

FEATURES

- **Low noise figure: 1.9 dB typical at 0.01 GHz to 7 GHz**
- **Single positive supply (self biased)**
- **High gain: 19.5 dB typical at 0.01 GHz to 7 GHz**
- **High OIP3: 35 dBm typical at 0.01 GHz to 7 GHz**
- **RoHS-compliant, 2 mm × 2 mm, 6-lead LFCSP**

APPLICATIONS

- **Test instrumentation**
- **Military communications**
- **Military radar**
- **Telecommunications**

FUNCTIONAL BLOCK DIAGRAM

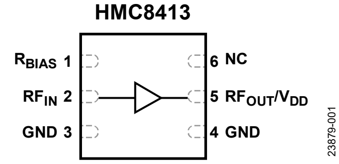

Figure 1.

GENERAL DESCRIPTION

The HMC8413 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 0.01 GHz to 9 GHz.

The HMC8413 provides a typical gain of 19.5 dB, a 1.9 dB typical noise figure, and a typical output third-order intercept (OIP3) of 35 dBm at 0.01 GHz to 7 GHz, requiring only 95 mA from a 5 V supply voltage. The saturated output power (P_{SAT}) of 22 dBm typical at 0.01 GHz to 7 GHz enables the low noise amplifier to function as a local oscillator (LO) driver for many of Analog Devices, Inc., balanced, in-phase/quadrature (I/Q) or image rejection mixers.

The HMC8413 also features inputs and outputs that are internally matched to 50 Ω, making the device ideal for surface-mounted technology (SMT)-based, high capacity microwave radio applications.

The HMC8413 is housed in an RoHS-compliant, 2 mm × 2 mm, 6-lead LFCSP.

Multifunction pin names may be referenced by their relevant function only.

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Technical Support
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REVISION HISTORY

10/2021—Revision 0: Initial Version

SPECIFICATIONS

0.01 GHz TO 7 GHz FREQUENCY RANGE

V_{DD} = 5 V, supply current (I_{DQ}) = 95 mA, R_{BIAS} = 787 Ω, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.01		7	GHz	
GAIN	17.5	19.5		dB	
Gain Variation over Temperature		0.013		dB/°C	
NOISE FIGURE		1.9		dB	
RETURN LOSS					
Input		15		dB	
Output		18		dB	
OUTPUT					
Output Power for 1 dB Compression (OP1dB)	19	21.5		dBm	
P_{SAT}		22		dBm	
OIP3		35		dBm	Measurement taken at output power (P_{OUT}) per tone = 5 dBm
Output Second-Order Intercept (OIP2)		39		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
POWER ADDED EFFICIENCY (PAE)		37		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		95		mA	
V_{DD}	2	5	6	V	

7 GHz TO 9 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 787 Ω, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	7		9	GHz	
GAIN	17	19		dB	
Gain Variation over Temperature		0.02		dB/°C	
NOISE FIGURE		2.8		dB	
RETURN LOSS					
Input		12		dB	
Output		15		dB	
OUTPUT					
OP1dB	16.5	19		dBm	
P_{SAT}		21		dBm	
OIP3		33		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
OIP2		45		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
PAE		22		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		95		mA	
V_{DD}	2	5	6	V	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD}	7 V
RF_{IN} Power	25 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 13.9 mW/°C Above 85°C)	1.25 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Peak Reflow (Moisture Sensitivity Level 1 (MSL1))	260°C
Junction to Maintain 1,000,000 Hours Mean Time to Failure (MTTF)	175°C
Nominal Junction (T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 95 mA)	119.2°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-6-12	72	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

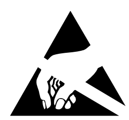
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for HMC8413

Table 5. HMC8413, 6-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

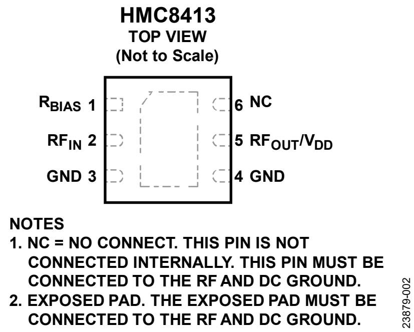


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{BIAS}	Current Mirror Bias Resistor. Use the R_{BIAS} pin via the external resistor (R2, see Figure 71) to set the current to the internal resistor. See Figure 3 for the interface schematic.
2	RF_{IN}	RF Input. The RF_{IN} pin is dc-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
3, 4	GND	Ground. This pin must be connected to the RF and dc ground. See Figure 6 for the interface schematic.
5	RF_{OUT}/V_{DD}	RF Output/Drain Bias for the Amplifier. The RF_{OUT}/V_{DD} pin is dc-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
6	NC	No Connect. This pin is not connected internally. This pin must be connected to the RF and dc ground.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground.

INTERFACE SCHEMATICS

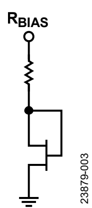


Figure 3. R_{BIAS} Interface Schematic

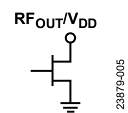


Figure 5. RF_{OUT}/V_{DD} Interface Schematic

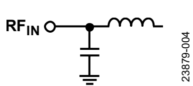


Figure 4. RF_{IN} Interface Schematic

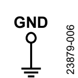


Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

I_{DQ} is the collector current without RF signal applied, and I_{DD} is the collector current with RF signal applied.

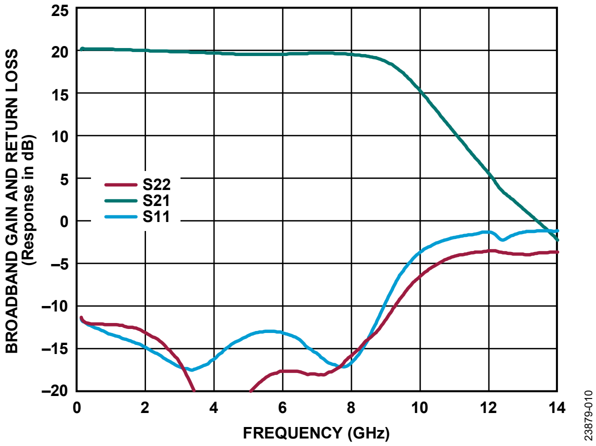


Figure 7. Broadband Gain and Return Loss vs. Frequency, 200 MHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA (S22 Is the Output Return Loss, S21 Is the Gain, and S11 Is the Input Return Loss)

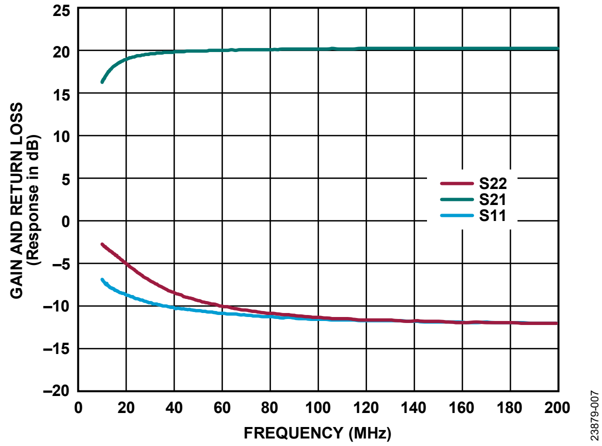


Figure 10. Gain and Return Loss vs. Frequency, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

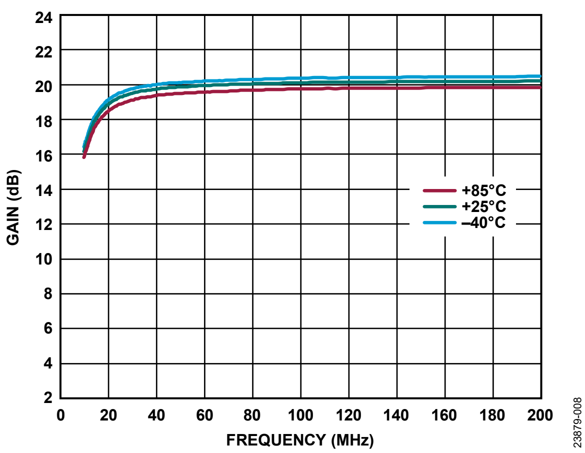


Figure 8. Gain vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

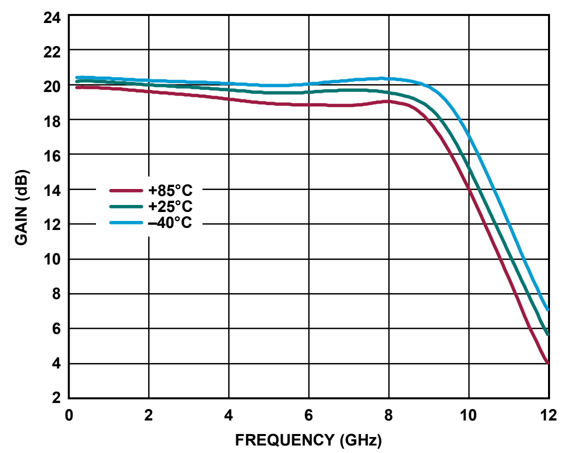


Figure 11. Gain vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

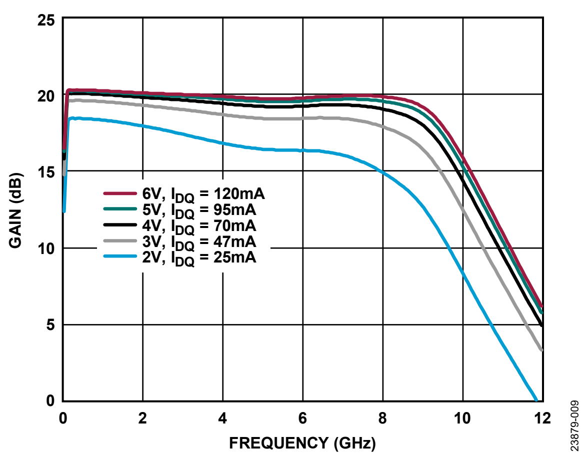


Figure 9. Gain vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 787 Ω

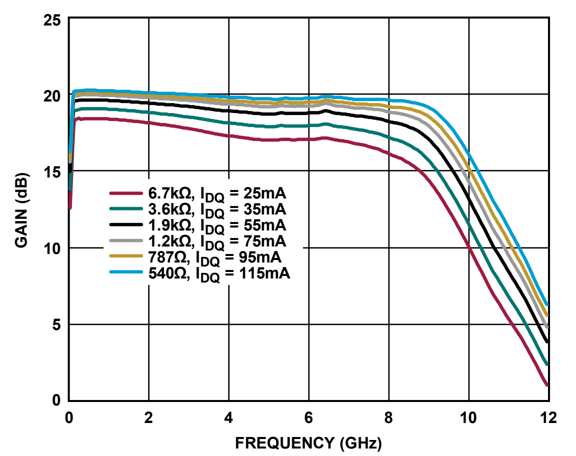


Figure 12. Gain vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

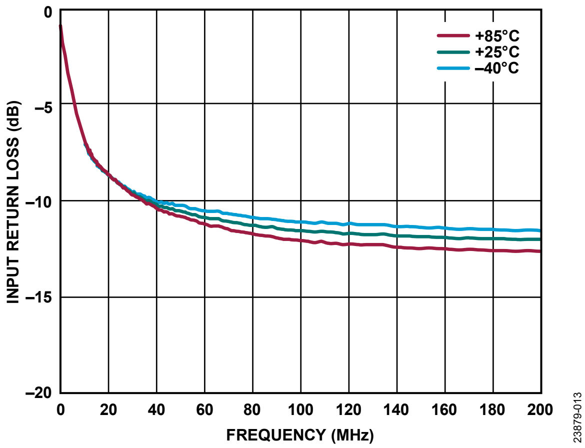


Figure 13. Input Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

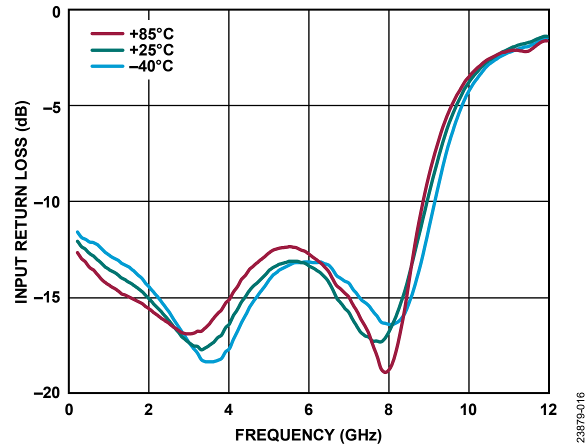


Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

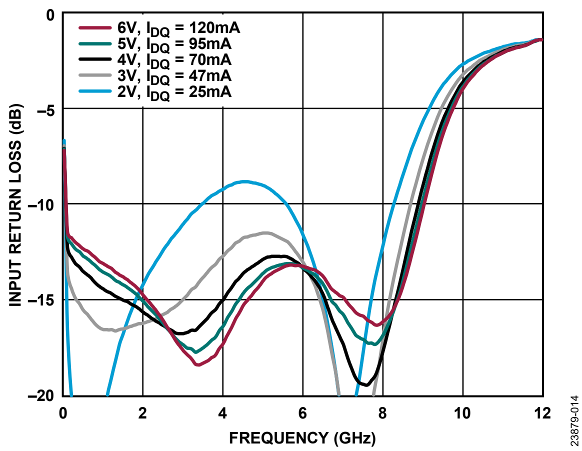


Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 787 Ω

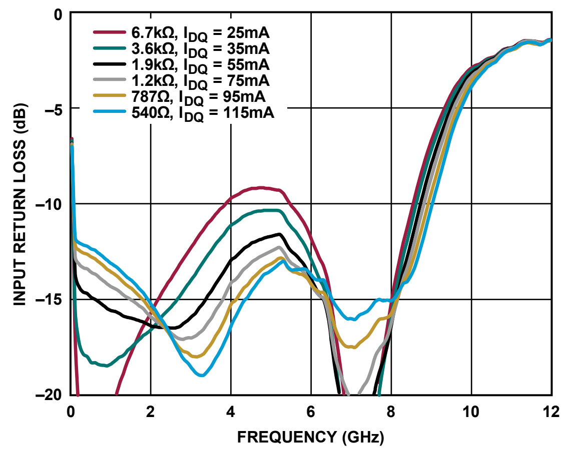


Figure 17. Input Return Loss vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

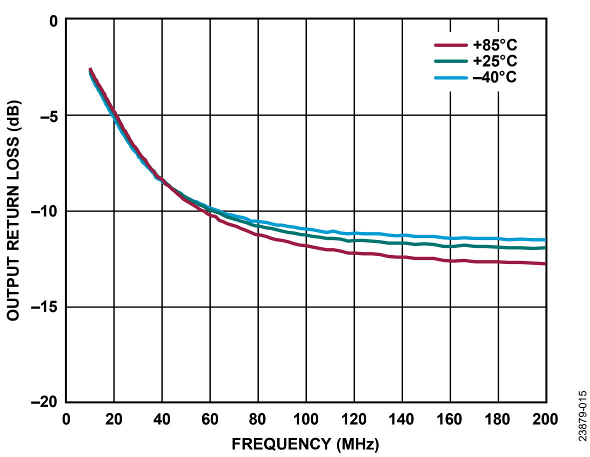


Figure 15. Output Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

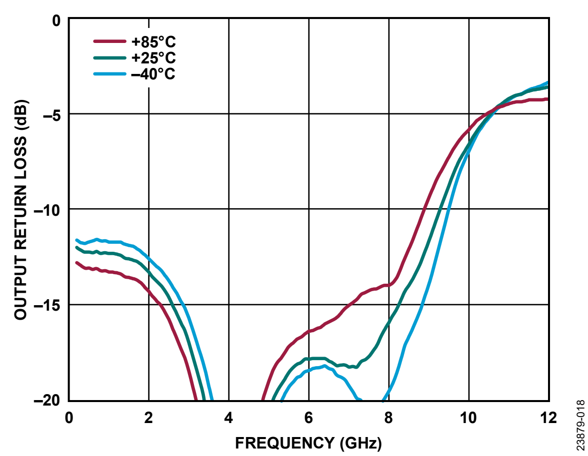


Figure 18. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

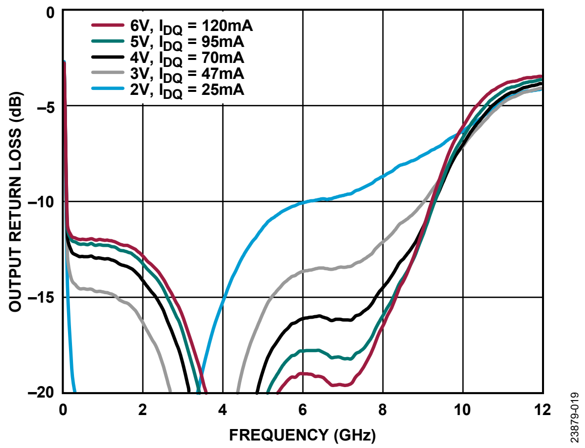


Figure 19. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 787 Ω

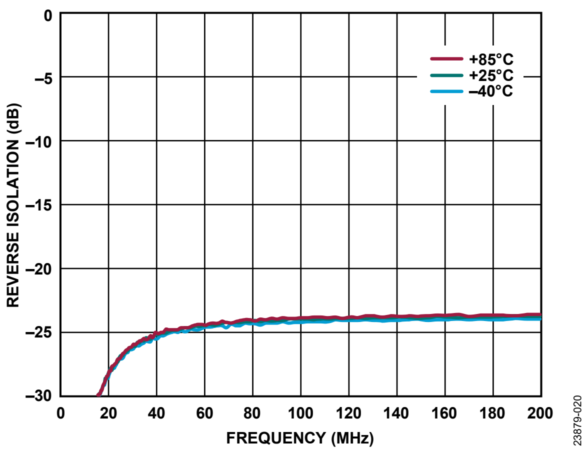


Figure 20. Reverse Isolation vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

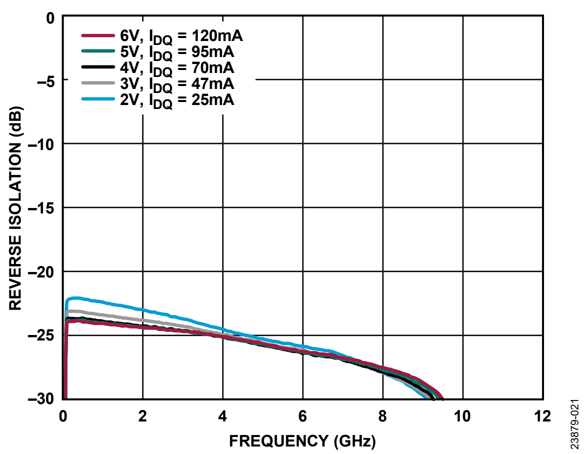


Figure 21. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 787 Ω

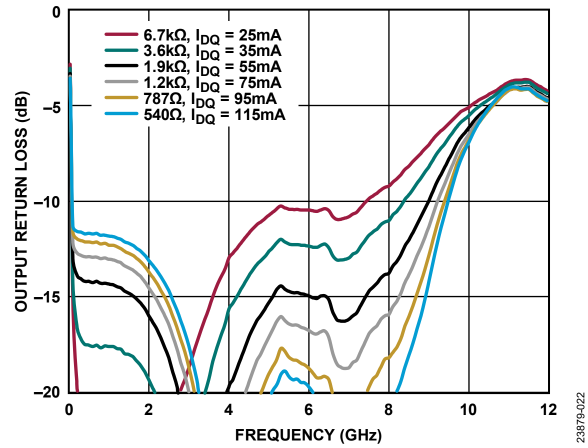


Figure 22. Output Return Loss vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

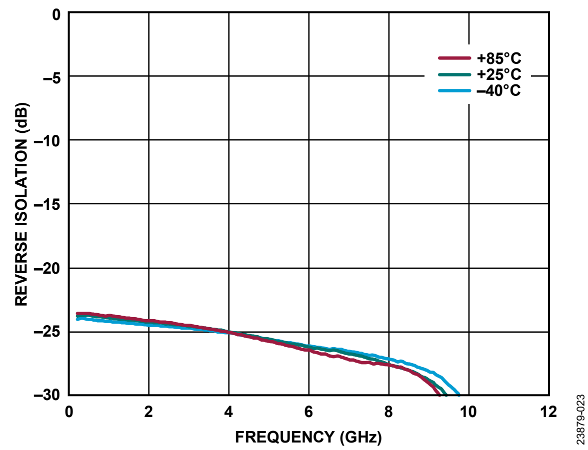


Figure 23. Reverse Isolation vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

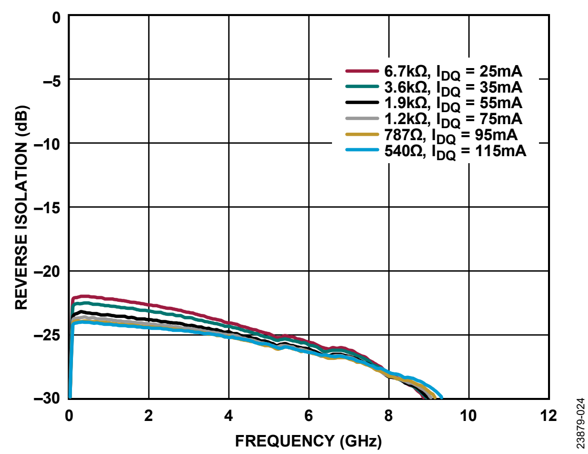


Figure 24. Reverse Isolation vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

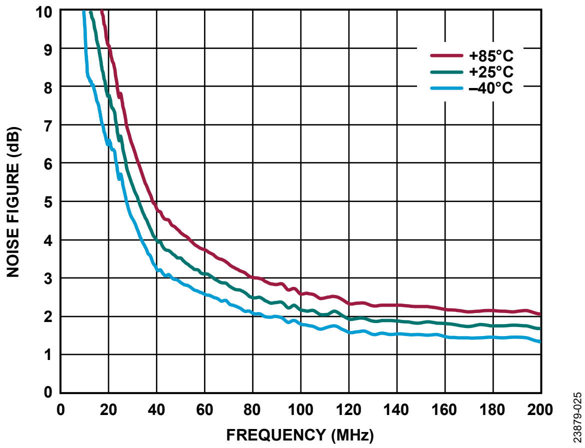


Figure 25. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

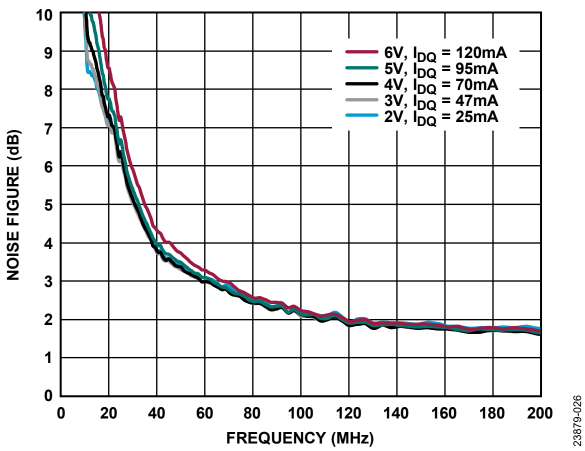


Figure 26. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ}, 10 MHz to 200 MHz, R_{BIAS} = 787 Ω

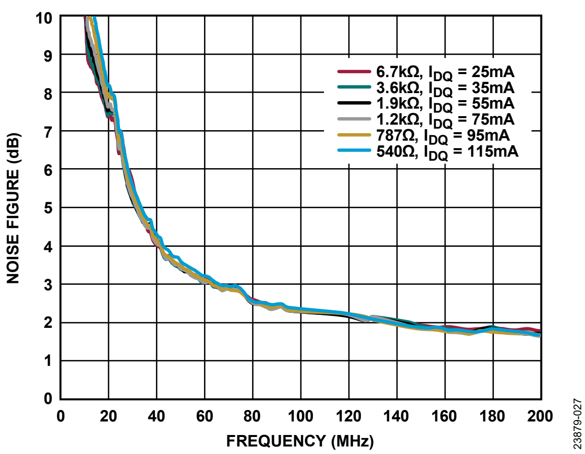


Figure 27. Noise Figure vs. Frequency for Various Bias Resistor Values and I_{DQ}, 10 MHz to 200 MHz, V_{DD} = 5 V

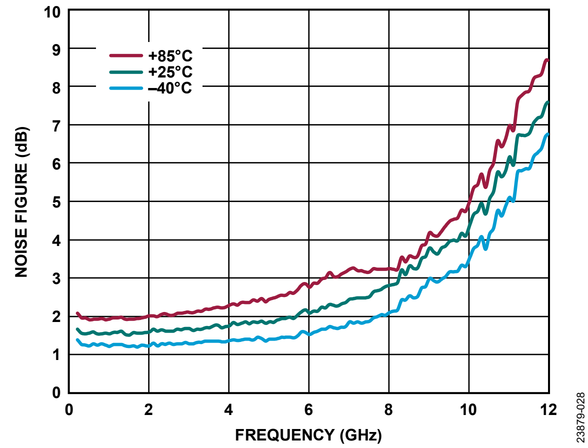


Figure 28. Noise Figure vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

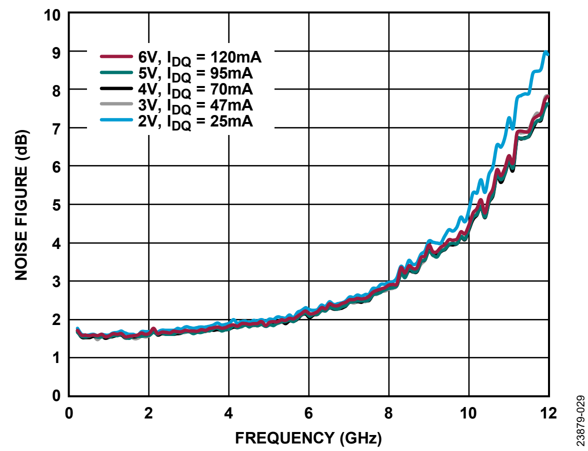


Figure 29. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ}, 200 MHz to 12 GHz, R_{BIAS} = 787 Ω

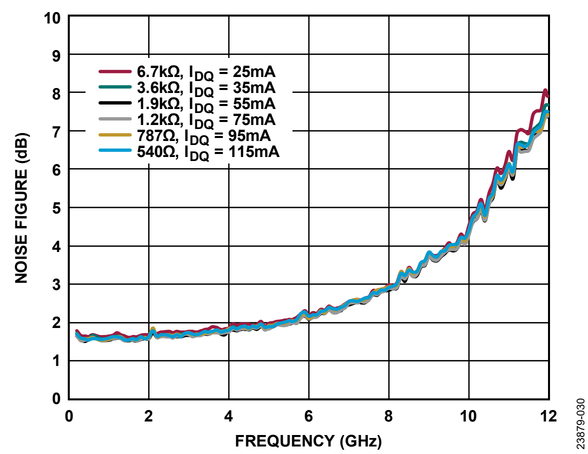


Figure 30. Noise Figure vs. Frequency for Various Bias Resistor Values and I_{DQ}, 200 MHz to 12 GHz, V_{DD} = 5 V

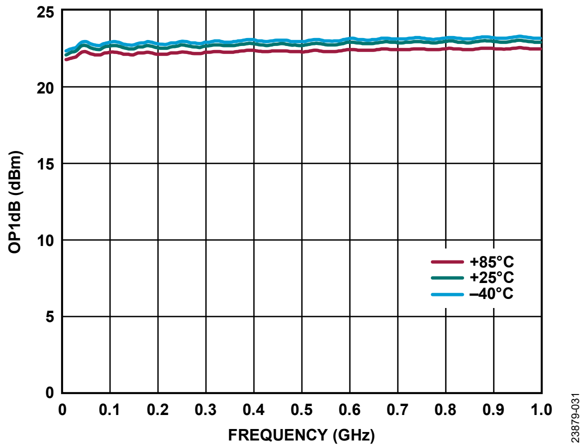


Figure 31. OP1dB vs. Frequency for Various Temperatures, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

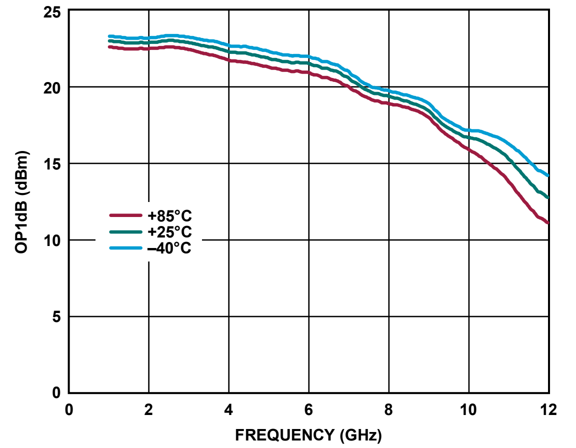


Figure 34. OP1dB vs. Frequency for Various Temperatures, 1 GHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

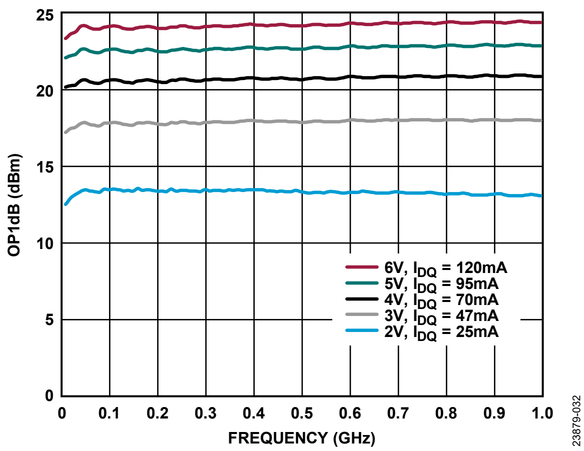


Figure 32. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ}, 0.01 GHz to 1.0 GHz, R_{BIAS} = 787 Ω

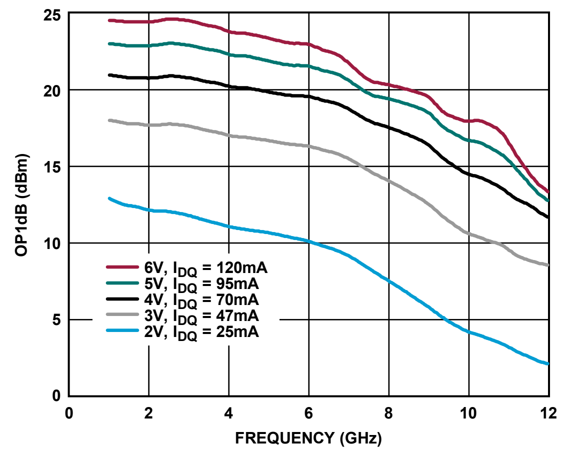


Figure 35. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ}, 1 GHz to 12 GHz, R_{BIAS} = 787 Ω

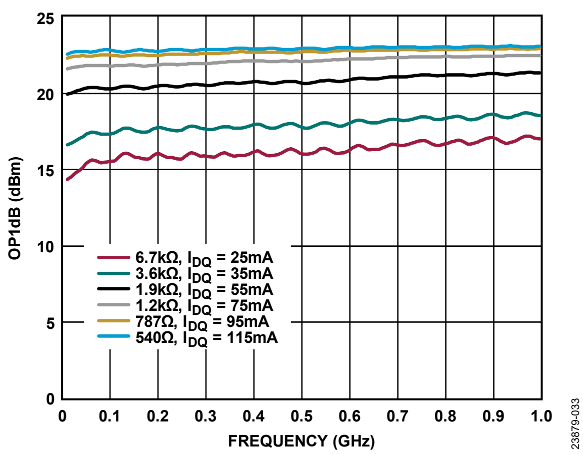


Figure 33. OP1dB vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V

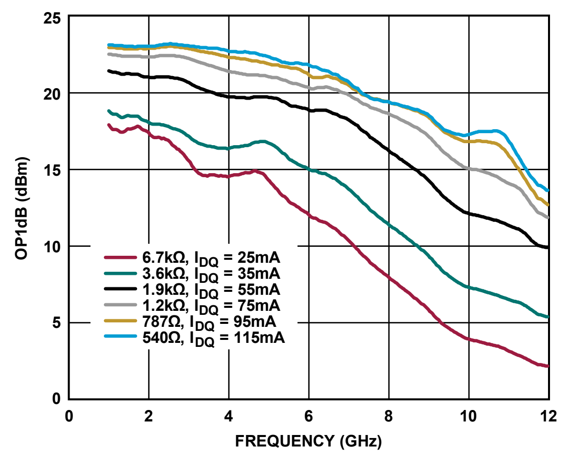


Figure 36. OP1dB vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 12 GHz, V_{DD} = 5 V

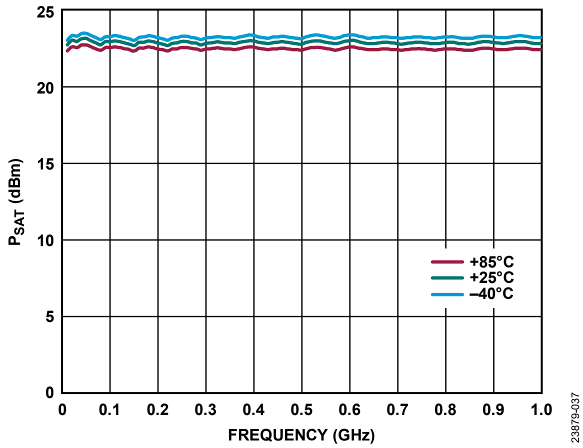


Figure 37. P_{SAT} vs. Frequency for Various Temperatures, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

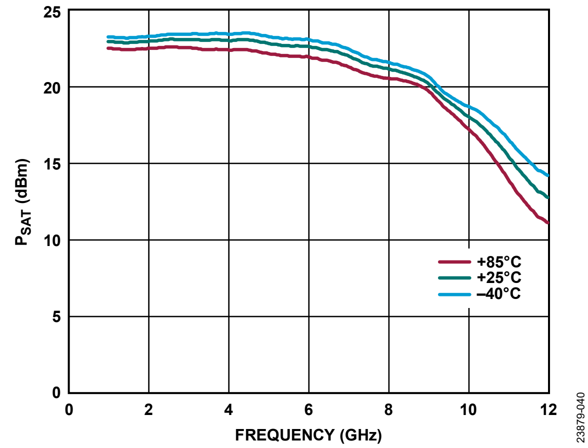


Figure 40. P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

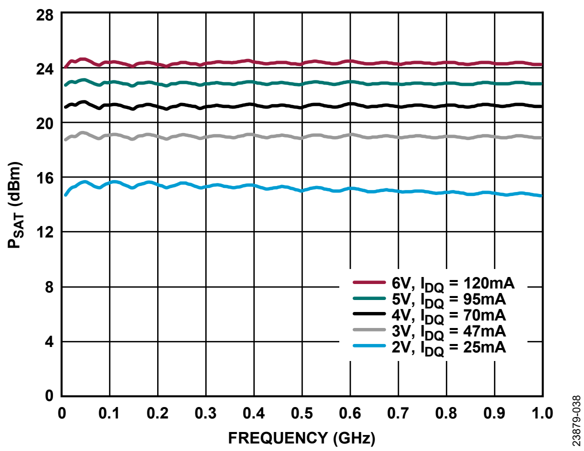


Figure 38. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ}, 0.01 GHz to 1.0 GHz, R_{BIAS} = 787 Ω

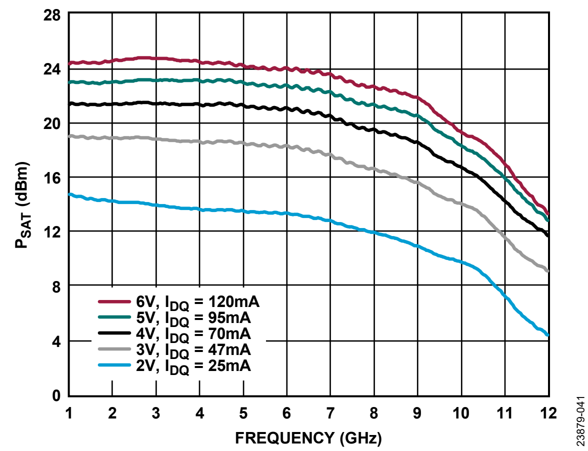


Figure 41. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ}, 1 GHz to 12 GHz, R_{BIAS} = 787 Ω

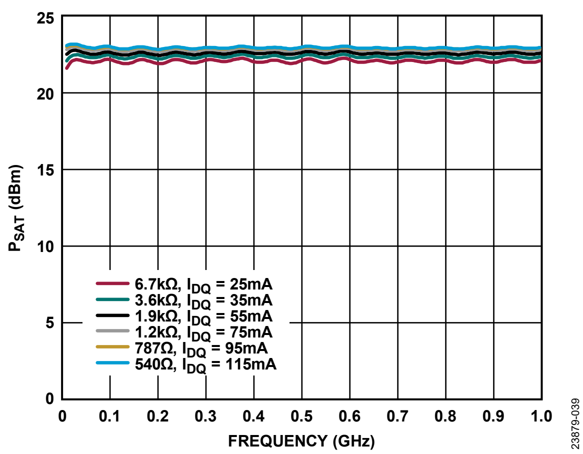


Figure 39. P_{SAT} vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V

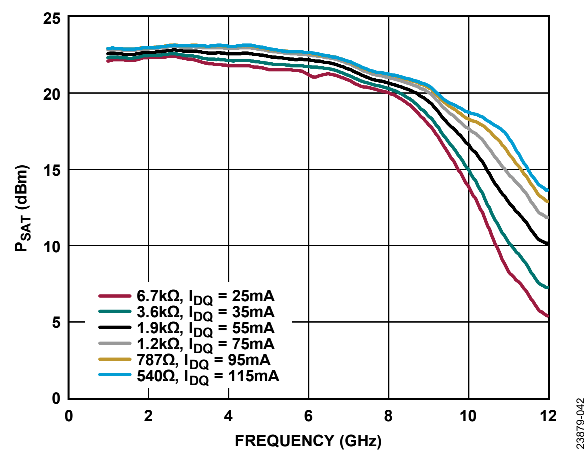


Figure 42. P_{SAT} vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 12 GHz, V_{DD} = 5 V

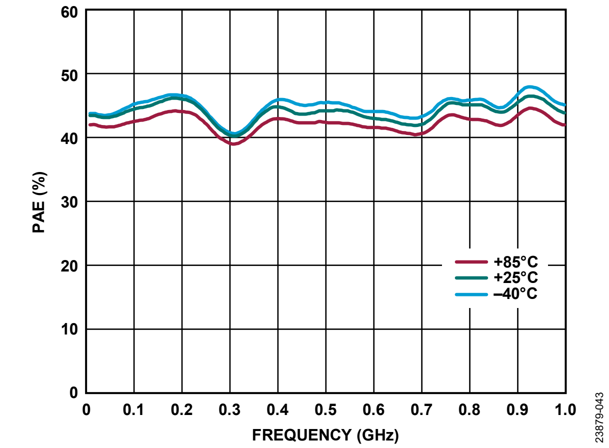


Figure 43. PAE vs. Frequency for Various Temperatures, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

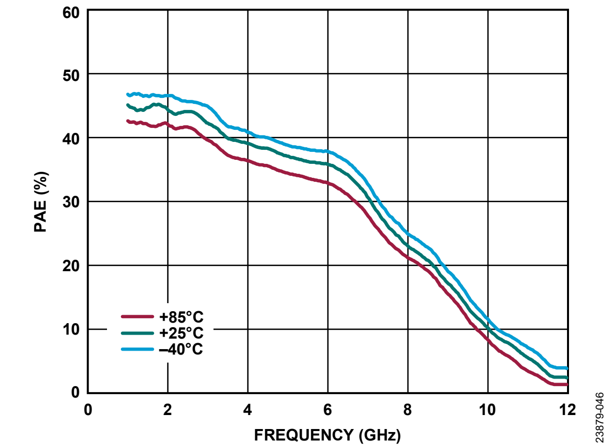


Figure 46. PAE vs. Frequency for Various Temperatures, 1 GHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

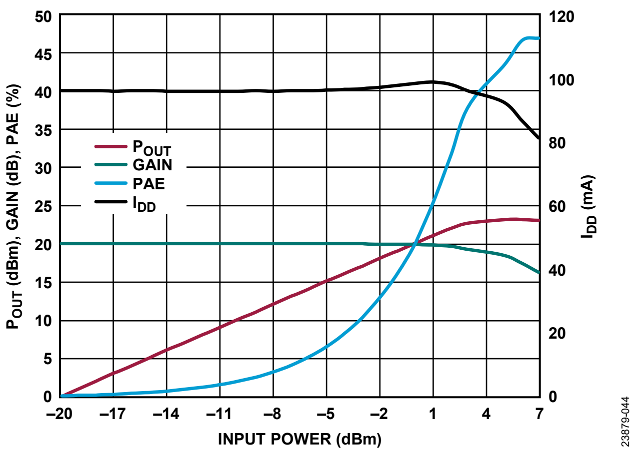


Figure 44. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 1 GHz, V_{DD} = 5 V, R_{BIAS} = 787 Ω

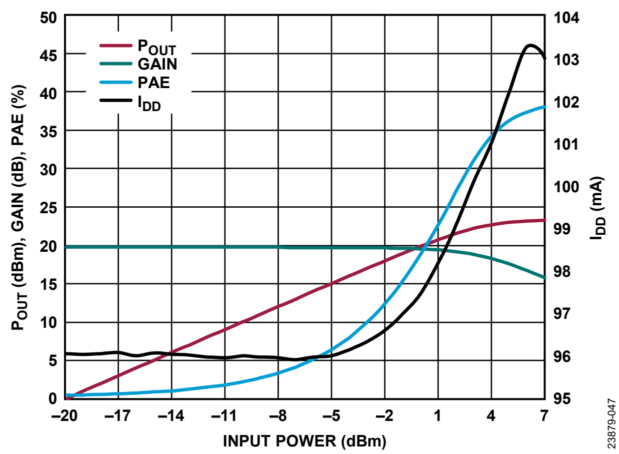


Figure 47. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 5 GHz, V_{DD} = 5 V, R_{BIAS} = 787 Ω

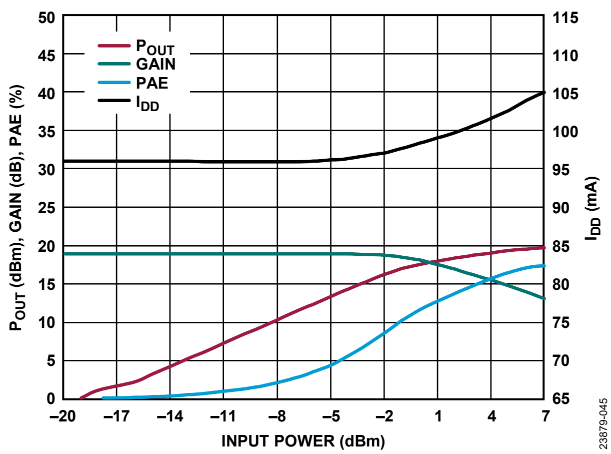


Figure 45. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 9 GHz, V_{DD} = 5 V, R_{BIAS} = 787 Ω

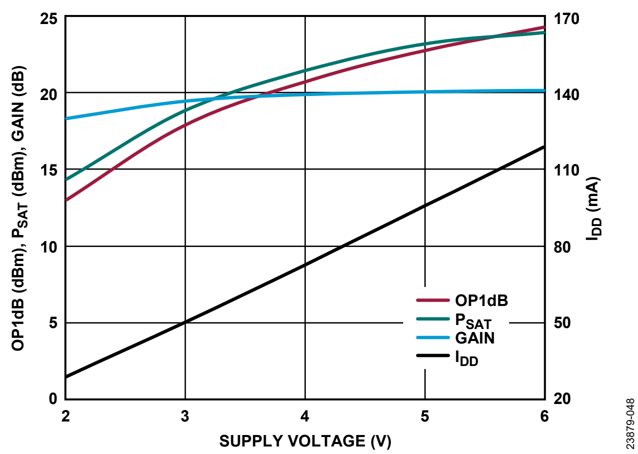


Figure 48. OP1dB, P_{SAT}, Gain, and I_{DD} vs. Supply Voltage, Power Compression at 1 GHz, R_{BIAS} = 787 Ω

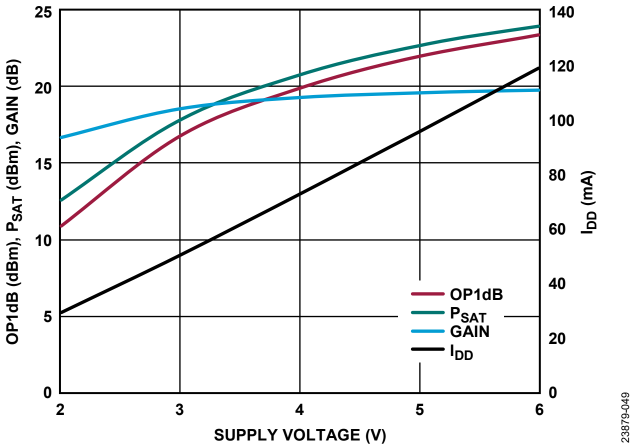


Figure 49. OP1dB, P_{SAT}, Gain, and I_{DD} vs. Supply Voltage, Power Compression at 5 GHz, R_{BIAS} = 787 Ω

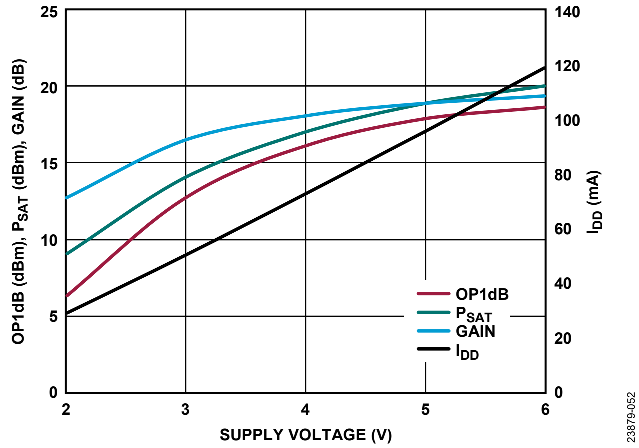


Figure 52. OP1dB, P_{SAT}, Gain, and I_{DD} vs. Supply Voltage, Power Compression at 9 GHz, R_{BIAS} = 787 Ω

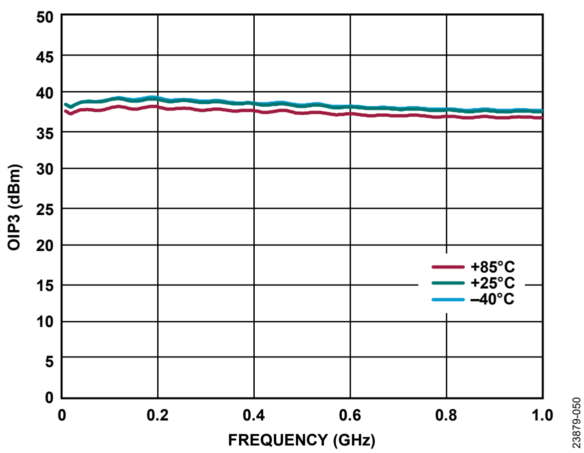


Figure 50. OIP3 vs. Frequency for Various Temperatures, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

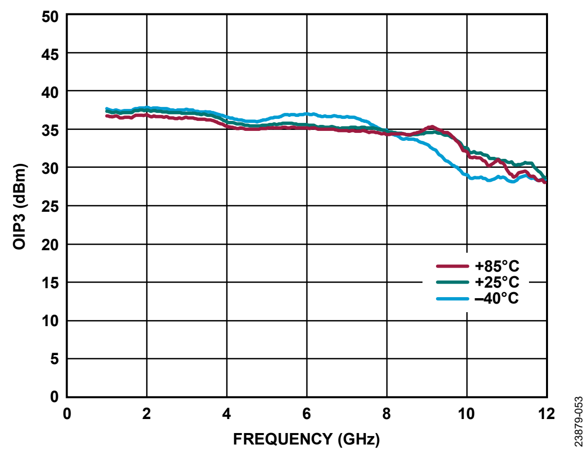


Figure 53. OIP3 vs. Frequency for Various Temperatures, 1 GHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

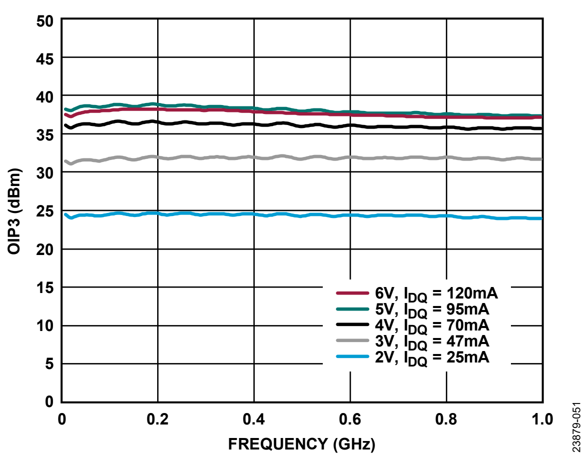


Figure 51. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ}, 0.01 GHz to 1.0 GHz, R_{BIAS} = 787 Ω

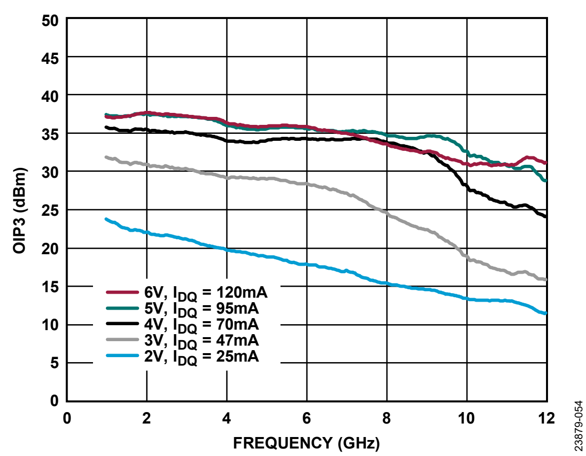


Figure 54. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ}, 1 GHz to 12 GHz, R_{BIAS} = 787 Ω

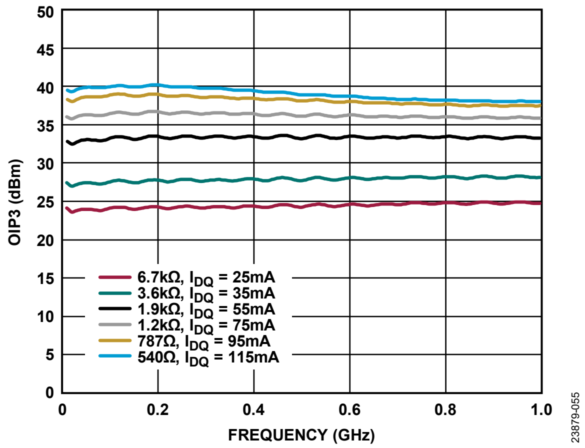


Figure 55. OIP3 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V

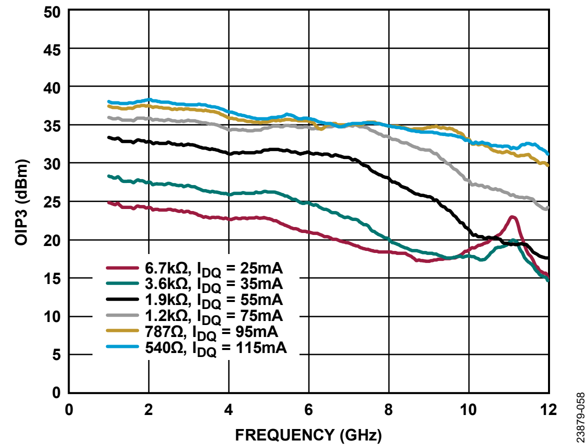


Figure 58. OIP3 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 12 GHz, V_{DD} = 5 V

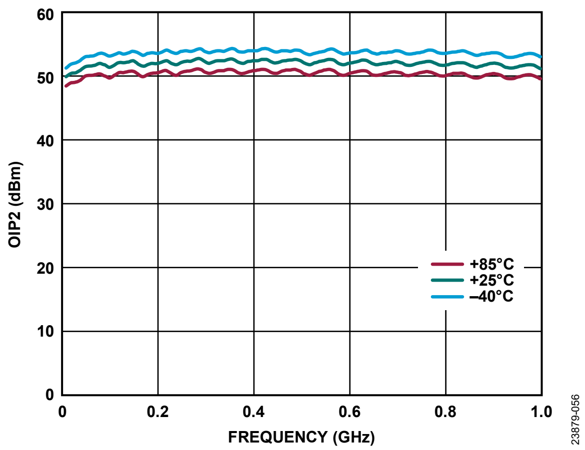


Figure 56. OIP2 vs. Frequency for Various Temperatures, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

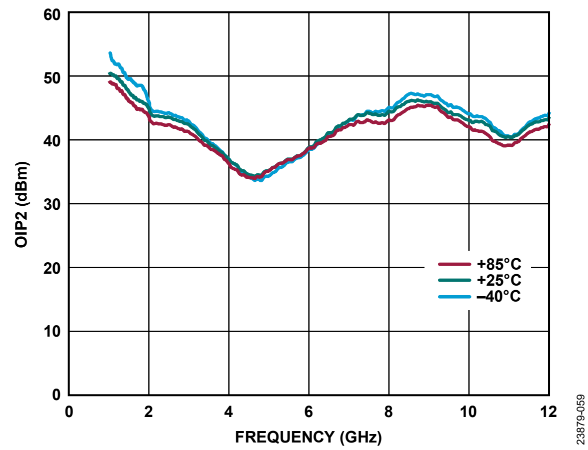


Figure 59. OIP2 vs. Frequency for Various Temperatures, 1 GHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

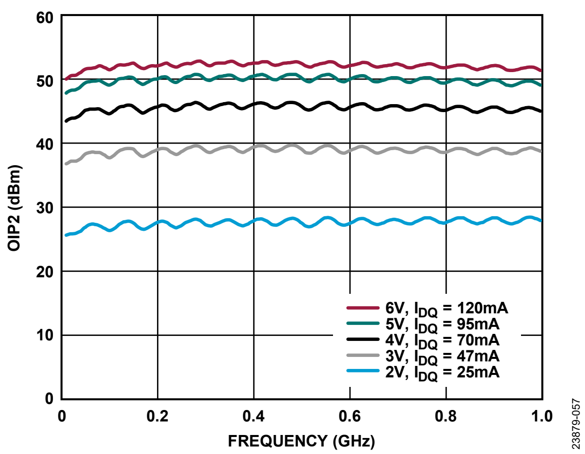


Figure 57. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ}, 0.01 GHz to 1.0 GHz, R_{BIAS} = 787 Ω

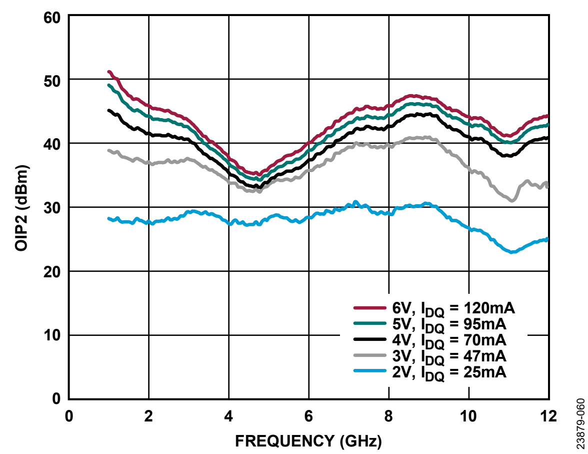


Figure 60. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ}, 1 GHz to 12 GHz, R_{BIAS} = 787 Ω

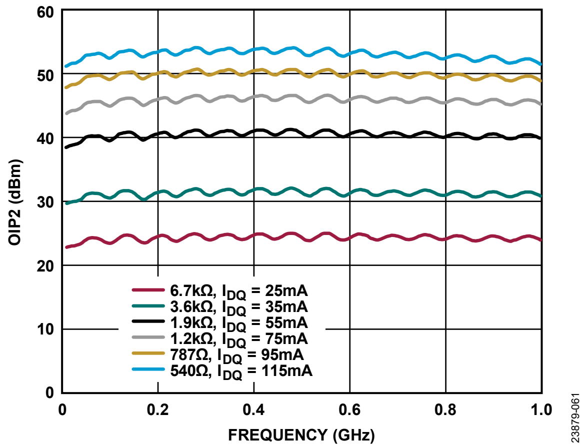


Figure 61. OIP2 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1.0 GHz, V_{DD} = 5 V

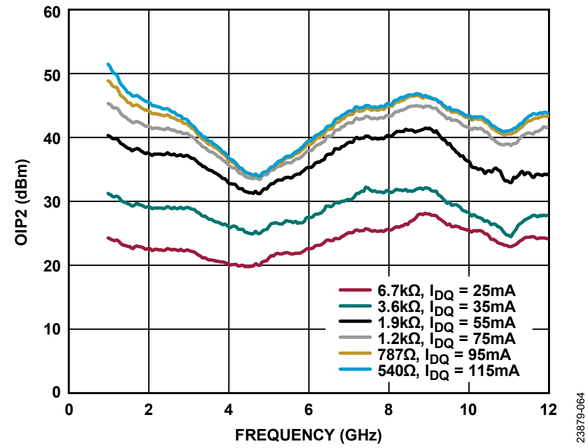


Figure 64. OIP2 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 12 GHz, V_{DD} = 5 V

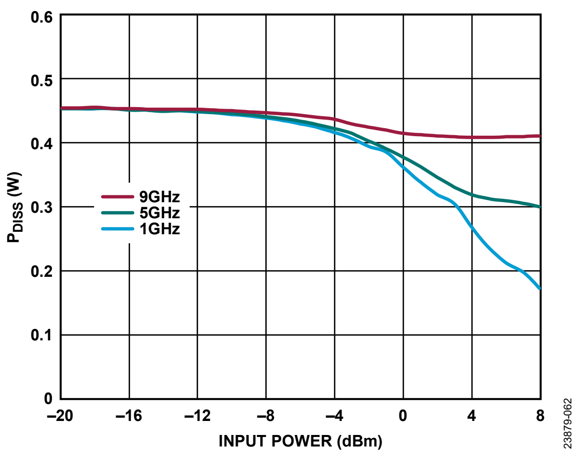


Figure 62. P_{DISS} vs. Input Power at T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 95 mA

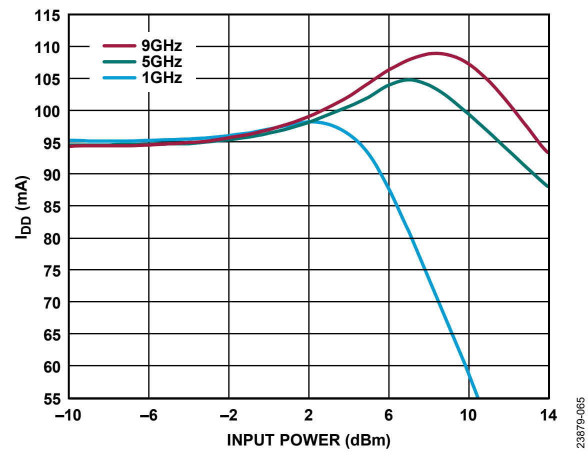


Figure 65. I_{DD} vs. Input Power for Various Frequencies, V_{DD} = 5 V

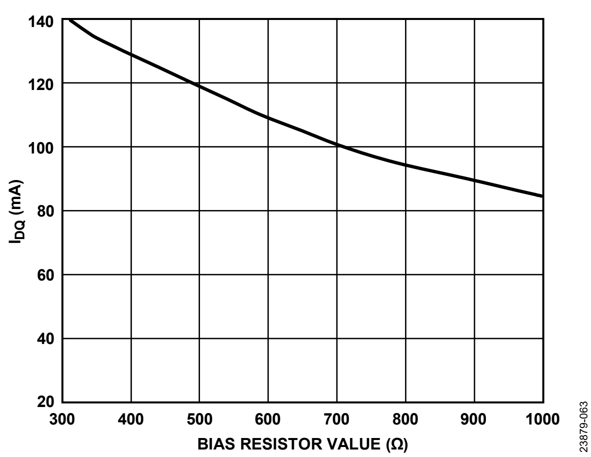


Figure 63. I_{DQ} vs. Bias Resistor Value, 300 Ω to 1 kΩ, V_{DD} = 5 V

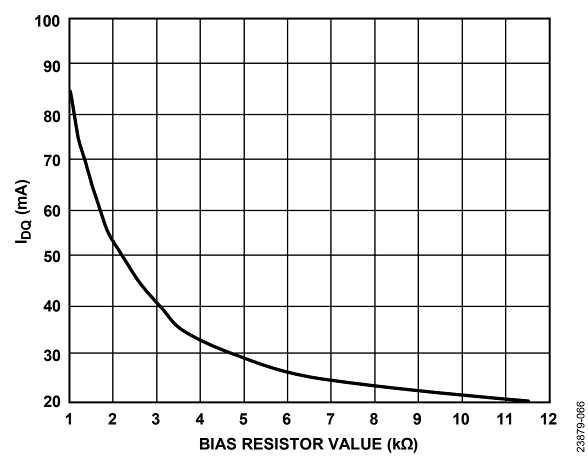


Figure 66. I_{DQ} vs. Bias Resistor Value, 1 kΩ to 12 kΩ, V_{DD} = 5 V

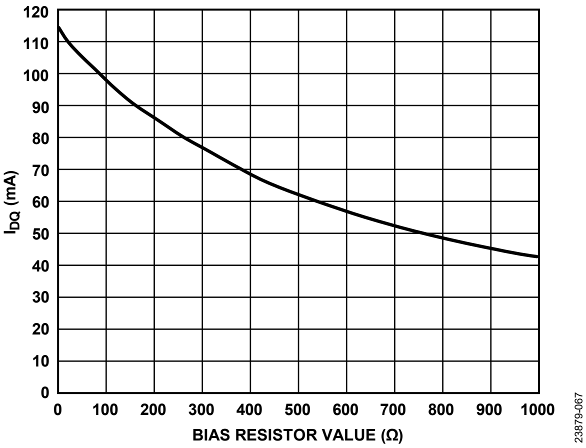


Figure 67. I_{DQ} vs. Bias Resistor Value, 1 Ω to 1 kΩ, V_{DD} = 3 V

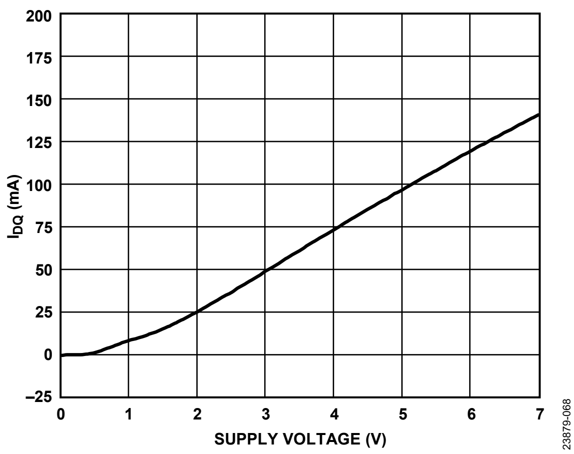


Figure 68. I_{DQ} vs. Supply Voltage, R_{BIAS} = 787 Ω

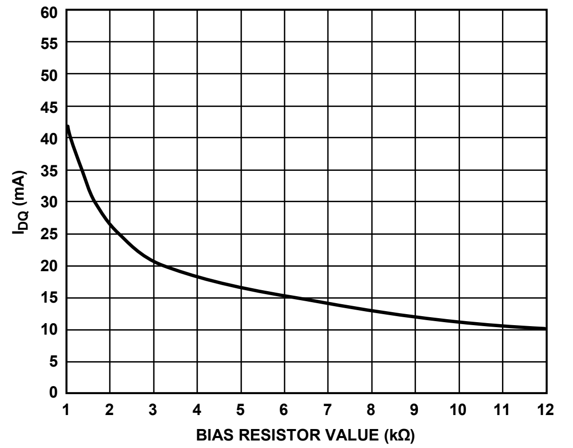


Figure 69. I_{DQ} vs. Bias Resistor Value, 1 kΩ to 12 kΩ, V_{DD} = 3 V

THEORY OF OPERATION

The HMC8413 is a GaAs, MMIC, pHEMT, low noise wideband amplifier. Figure 70 shows the simplified architecture of the HMC8413.

The HMC8413 has single-ended input and output ports with impedances that nominally equal 50 Ω over the 0.01 GHz to 9 GHz frequency range. Therefore, the HMC8413 can be directly inserted into a 50 Ω system with no required impedance matching circuitry, which also means that multiple HMC8413 amplifiers can be cascaded back to back without the need for external matching circuitry.

It is critical to supply very low inductance ground connections to the ground pins as well as to the backside exposed pad to ensure stable operation.

To achieve optimal performance from the HMC8413 and prevent damage to the device, do not exceed the absolute maximum ratings.

The R_{BIAS} pin is used to set the I_{DQ} with an external resistor, allowing single positive supply operation.

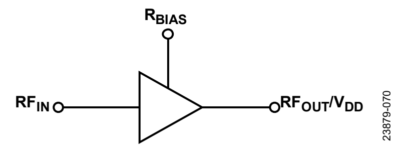


Figure 70. Simplified Architecture

APPLICATIONS INFORMATION

Figure 71 shows the basic connections for operating the HMC8413. AC couple the input and output of the HMC8413 with appropriately sized capacitors (American Technical Ceramics, 531Z104KTR16T). Use an appropriate bias tee on the RF_{OUT}/V_{DD} pin to provide both ac and dc coupling to the RF_{OUT}/V_{DD} pin. A 5 V dc bias is supplied to the amplifier through the choke inductor connected to the RF_{OUT}/V_{DD} pin. The recommended bias inductor is the Coilcraft® 0402DF-901XJRE, 0.9 µH.

The shunt resistor, inductor, capacitor (RLC) network on the input of the HMC8413 adds resistive loss to help stabilize the amplifier by reducing the gain at low frequencies. The shunt inductor makes the resistor frequency dependent. At low frequencies, the resistor becomes more active. The resistor has less influence at higher frequencies where the impedance of the choke is high. The capacitor blocks dc voltages and currents from flowing through the resistor and the inductor.

The bias condition, V_{DD} = 5 V and I_{DQ} = 95 mA, is the recommended operating point to achieve optimum performance. To set other bias conditions, adjust the value of R_{BIAS}. Table 7 shows the recommended bias resistor values and their associated quiescent current.

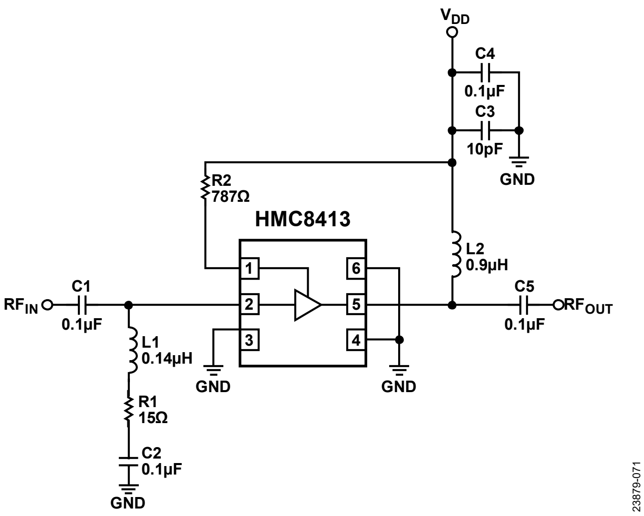


Figure 71. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

During Power-Up

The recommended bias sequence during power-up is as follows:

1. Set V_{DD} to 5 V.
2. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Set V_{DD} to 0 V.

Table 7. Recommended Bias Resistor Values

R_{BIAS} (Ω)	Total Current, I_{DQ} (mA)	Amplifier Current, I_{DQ_AMP} (mA)	R_{BIAS} Current, I_{RBIAS} (mA)
440	125	120.55	4.45
490	120	115.74	4.26
540	115	110.94	4.06
590	110	106.13	3.87
650	105	101.32	3.68
710	100	96.51	3.49
787	95	91.7	3.3
890	90	86.89	3.11
990	85	82.07	2.93
1100	80	77.26	2.74
1200	75	72.45	2.55
1360	70	67.63	2.37
1520	65	62.81	2.19
1700	60	57.99	2.01
1900	55	53.17	1.83
2240	50	48.36	1.64
2600	45	43.54	1.46
3080	40	38.72	1.28
3600	35	33.91	1.09
4780	30	29.12	0.88
6700	25	24.37	0.63
11900	20	19.62	0.38

EXTENDING OPERATION BELOW 10 MHz

The operation of the HMC8413 can be extended below 10 MHz by adding a 10 μH inductor (Coilcraft 0603AF-103XJE) and 1 kΩ shunt resistor. The 10 μH inductor and 1 kΩ shunt are placed in series with the 0.9 μH inductor (Coilcraft 0402DF-901XJRE) to form a multisection bias network. Figure 72 shows the broadband gain and return loss, and Figure 73 shows the narrowband gain and return loss. Figure 74 shows the application circuit for operation below 10 MHz.

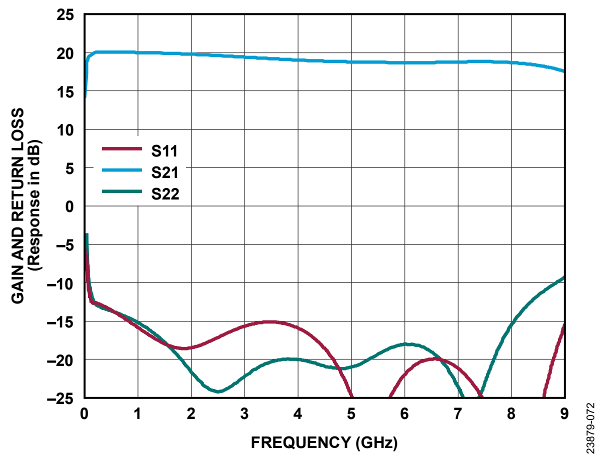


Figure 72. Gain and Return Loss vs. Frequency, 1 MHz to 9 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

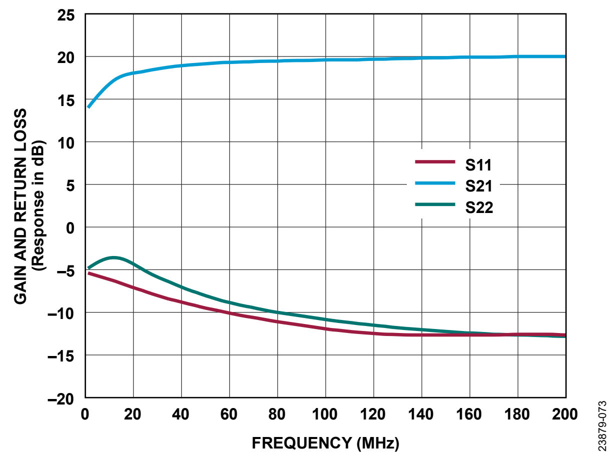


Figure 73. Gain and Return Loss vs. Frequency, 1 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

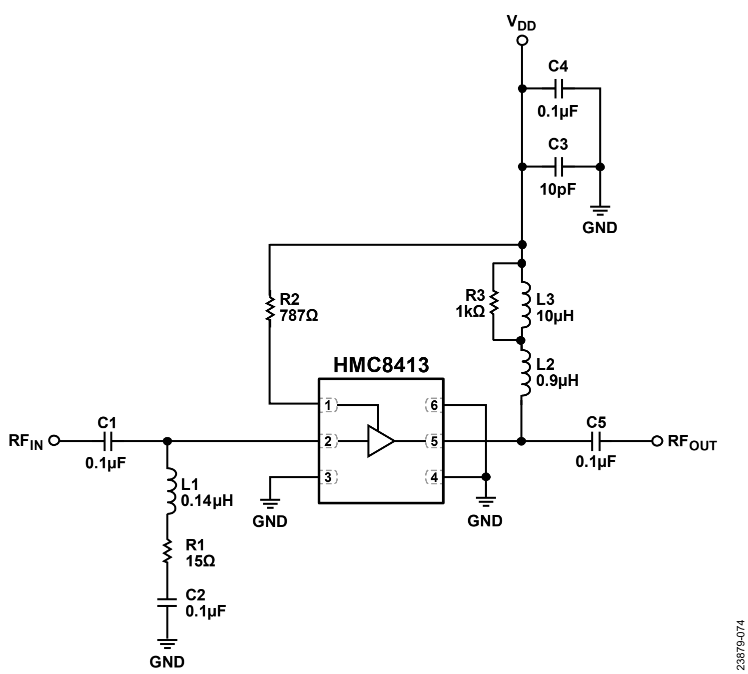


Figure 74. Application Circuit for Operation Below 10 MHz

BIASING THE HMC8413 USING THE LT3470A

The HMC8413 can be powered by using a well regulated power source. The LT3470A micropower, step-down, dc-to-dc converter is recommended to provide a 5 V supply to RF_{OUT}/V_{DD}. The regulator is designed for a wide input voltage range while maintaining a high efficiency and high power supply modulation ratio (PSMR). Using the LT3470A as a power supply for the HMC8413 results in high PSMR, and dynamic performance is achieved without degradation. Figure 75 shows the application circuit for the HMC8413 using the LT3470A regulator.

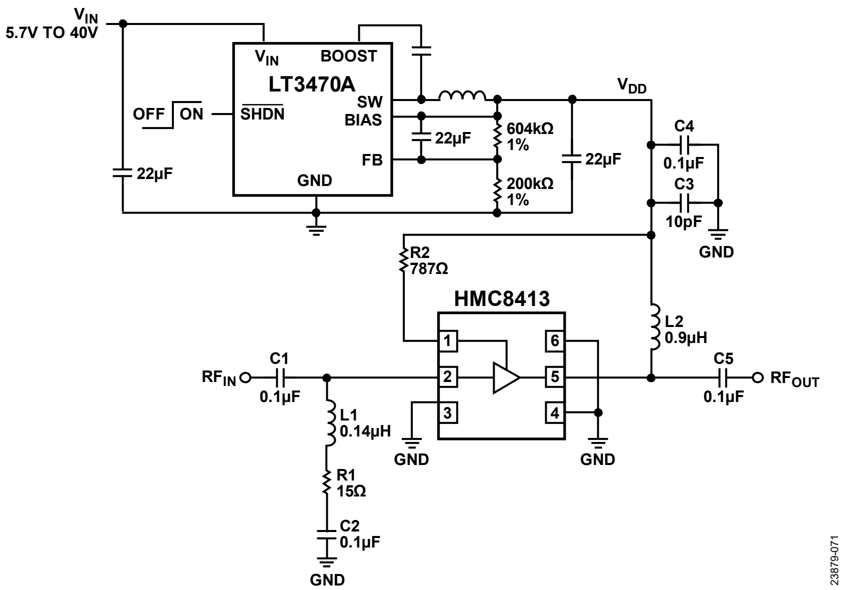


Figure 75. Application Circuit for the HMC8413 Using the LT3470A Regulator