



The Future of Analog IC Technology®

EV2016DJ-00A

42V Input Voltage, Low Power Adjustable Output Linear Regulator EV Board

DESCRIPTION

The MP2016 is a low power linear regulator that supplies power to systems with high voltage batteries. It includes a wide 4V to 42V input range, low dropout voltage and low quiescent supply current.

The MP2016 provides excellent line transient response time and 50dB power supply rejection ratio (PSRR). The MP2016 can be set externally from 1.2V to 24V through 2 resistors divider.

The MP2016 also includes thermal shutdown and current limiting fault protection, and is available in TSOT23-5 and QFN-8 packages.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Unites
Input Voltage	V_{IN}	7 to 42	V
Output Voltage	V_{OUT}	5	V
Operation Temp		-40 to +85	°C

FEATURES

- 4V to 45V Input Range
- 12 μ A Quiescent Supply Current
- <1.5 μ A Shutdown Current
- 1.2V to 24V Adjustable Output new bullet 30mA Output Current with 50mA Peak Current Limit
- \pm 2% Accuracy
- Thermal Shutdown
- Available in Tiny TSOT23-5 & QFN8 Packages

APPLICATIONS

- Notebook Computers
- Smart-Battery Packs
- PDAs
- Handheld Devices
- Battery-Powered Systems

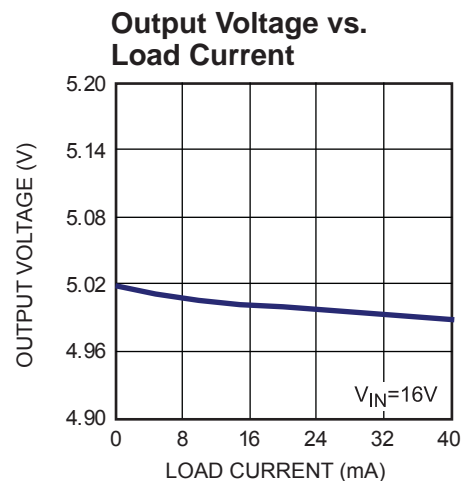
"MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

EV2016DJ-00A EVALUATION BOARD

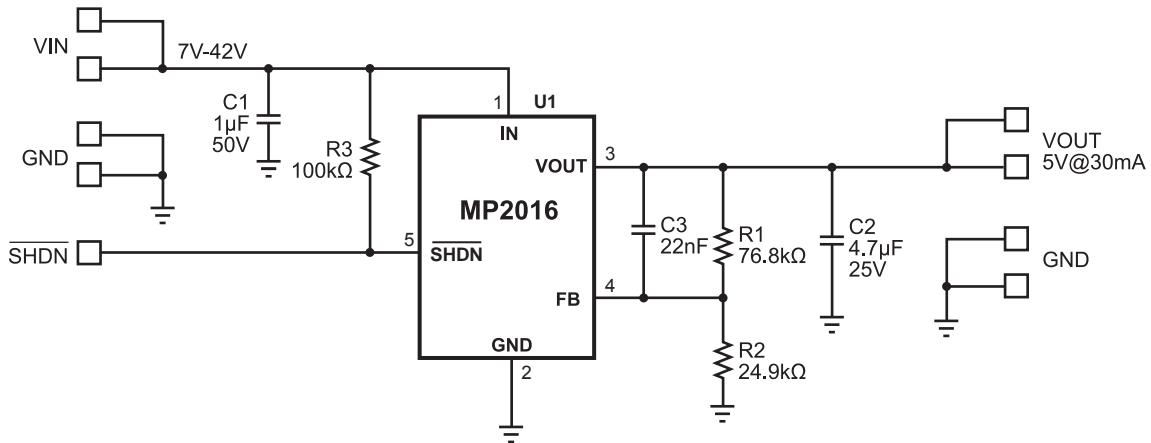


(L x W x H) 2.00" x 2.00" x 0.5"
(5.0cm x 5.0cm x 1.2cm)

Board Number	MPS IC Number
EV2016DJ-00A	MP2016DJ



EVALUATION BOARD SCHEMATIC



EV2016DJ-00A BILL OF MATERIAL

Qty	Ref.	Value	Description	Package	Manufacturer	Manufacturer P/N
1	C1	1µF	Ceramic Cap, X7R, 50V	1206	TDK	C3216X7R1H105K
1	C2	4.7µF	Ceramic Cap, X7R, 25V	1206	TDK	C3216X7R1C475K
1	C3	22nF	Ceramic Cap, X7R, 50V	603	TDK	C1608X7R1H223K
1	R1	76.8kΩ	Film Res., 1%	603	Panasonic	ERJ-3EKF7682V
1	R2	24.9kΩ	Film Res., 1%	603	Panasonic	ERJ-3EKF2492V
1	R3	100kΩ	Film Res., 5%	603	Panasonic	ERJ-6GEYJ104V
1	U1		MP2016DJ		MPS	MP2016DJ

PRINTED CIRCUIT BOARD LAYOUT

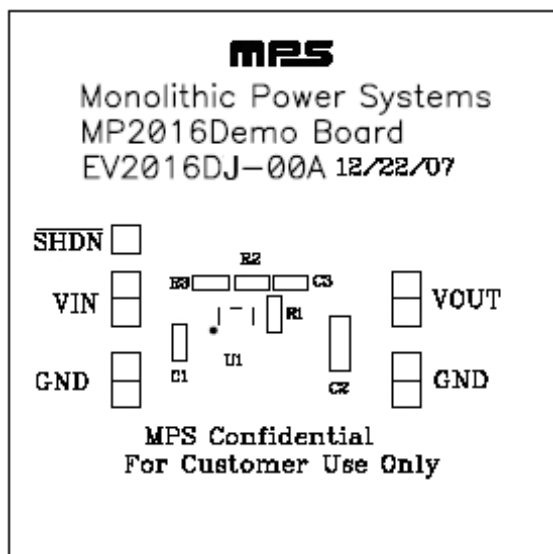


Figure 1—Top Silk Layer

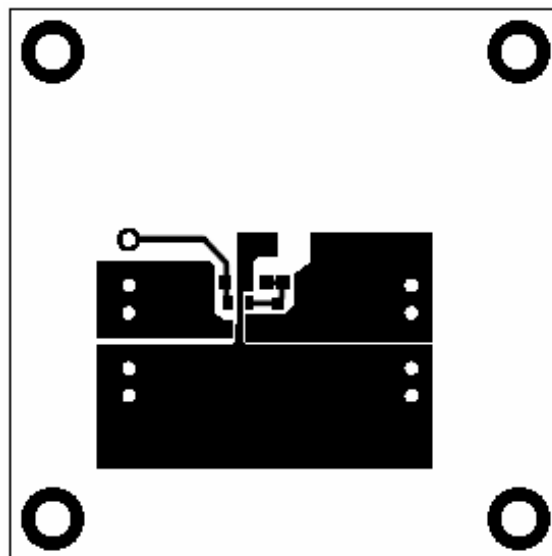


Figure 2—Top Layer

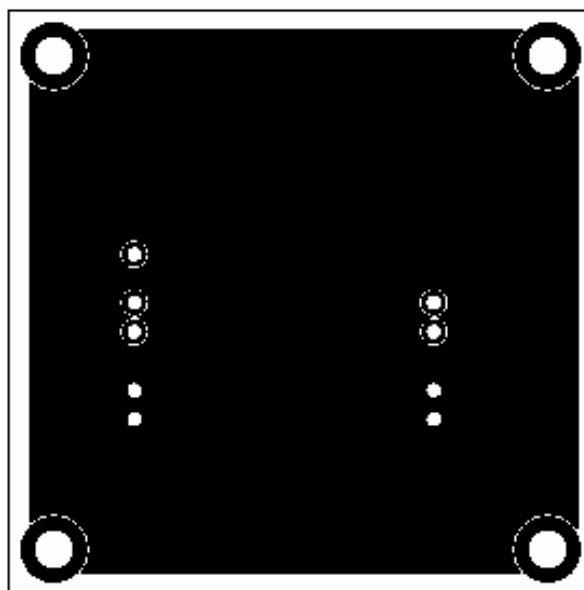


Figure 3—Bottom Layer