

DESCRIPTION

The MP2147 is a monolithic, step-down, switch-mode converter with internal power MOSFETs. It can achieve up to 4A continuous output current from a 2.8V-to-5.5V input voltage with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

Constant-on-time control provides a fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2147 is available in a small QFN2×3mm package and requires only a minimal number of readily-available, standard, external components.

The MP2147 is ideal for a wide range of applications, including storage (SSD, HDD), high-performance DSPs, FPGAs, and distributed power systems.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Input Voltage	V _{IN}	2.8–5.5	V
Output Voltage	V _{OUT}	1.2	V
Output Current	I _{OUT}	4	A

FEATURES

- Up to 4A Output Current
- Wide 2.8V-to-5.5V Operating Input Range
- 22mΩ and 14mΩ Internal Power MOSFETs
- 40µA Quiescent Current
- 1.2MHz Fixed Switching Frequency
- 1% Feedback Accuracy
- External Mode Control
- External VCON Control
- Adjustable Output from 0.6V
- 1.5ms Internal SS Time with Pre-Bias Startup
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection with Hiccup Mode
- Stable with Low-ESR Output Ceramic Capacitors
- Output Discharge Function
- Thermal Shutdown
- Available in a 2mm×3mm QFN Package

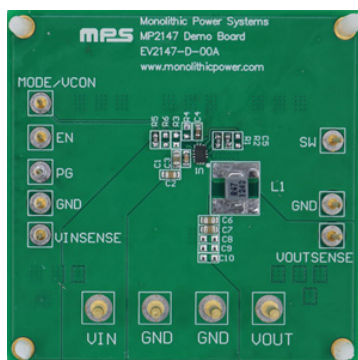
APPLICATIONS

- Storage (SSD, HDD)
- Portable Instruments
- Battery-Powered Devices

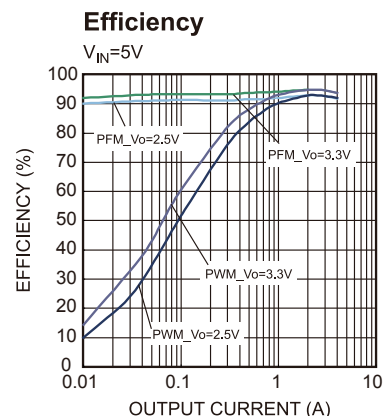
All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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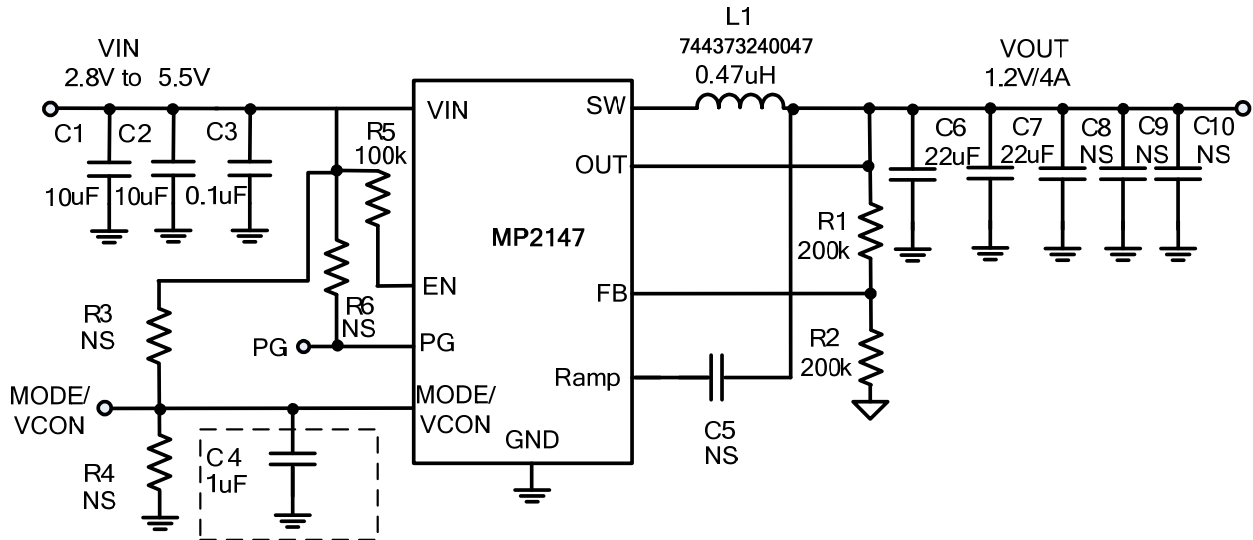
EV2147-D-00A EVALUATION BOARD



Board Number	MPS IC Number
EV2147-D-00A	MP2147GD



EVALUATION BOARD SCHEMATIC



Note: C4 is optional for "VCON" application.

EV2147-D-00A BILL OF MATERIALS

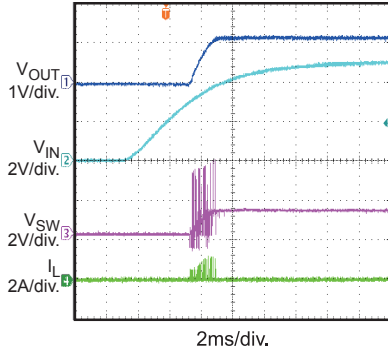
Qty	RefDes	Value	Description	Package	Manufacturer	Manufacturer P/N
2	C1, C2	10 μ F	Ceramic Cap,10V,X5R	0805	muRata	GRM21BR61A106KE19L
1	C3	0.1 μ F	Ceramic Cap,16V,X7R	0603	muRata	GRM188R71C104KA01D
1	C4	1 μ F	Ceramic Cap,6.3V,X7R	0603	muRata	GRM188R60J105KA01D
2	C6,C7	22 μ F	Ceramic Cap,10V,X5R	0805	muRata	GRM21BR61A226ME51L
1	L1	0.47 μ H	Inductor, 14.5A, 14m Ω	4x4mm	Würth	744 373 240 047
1	R1	200K	Film Res,1%	0603	ROYAL	RL0603FR-07200KL
1	R2	200K	Film Res,1%	0603	ROYAL	RL0603FR-07200KL
1	R5	100K	Film Res,5%	0603	ROYAL	RC0603JR-07100KL
1	U1	MP2147	Synchronous step-down switcher	QFN12 (2x3mm)	MPS	MP2147GD
0	C5,C8, C9,C10, R3,R4,R6	NS				

EVB TEST RESULTS

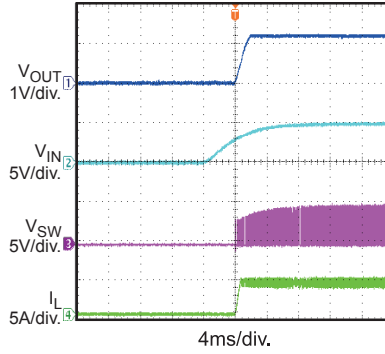
Performance waveforms are tested on the evaluation board.

$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $L = 0.47\mu H$, $C_{OUT} = 22\mu F \times 2$, $T_A = 25^\circ C$, unless otherwise noted.

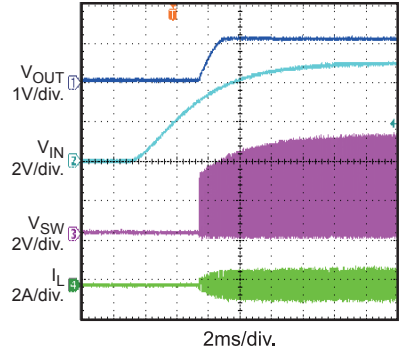
Power Up
 $I_{OUT} = 0A$, PFM



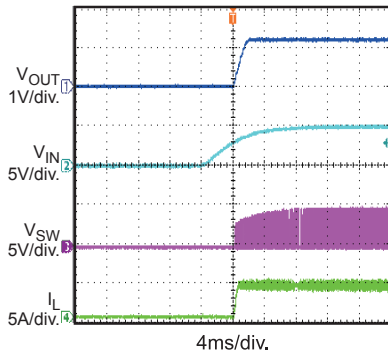
Power Up
 $I_{OUT} = 4A$, PFM



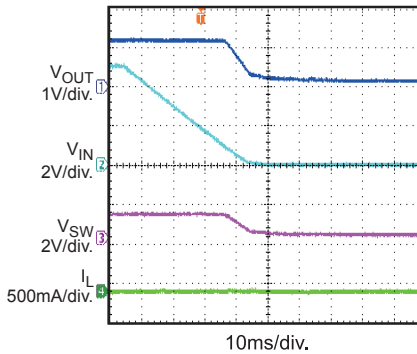
Power Up
 $I_{OUT} = 0A$, PWM



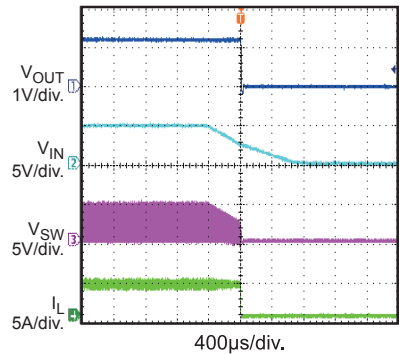
Power Up
 $I_{OUT} = 4A$, PWM



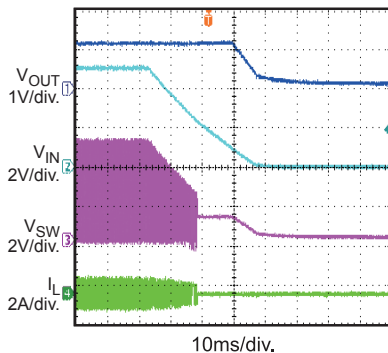
Power Off
 $I_{OUT} = 0A$, PFM



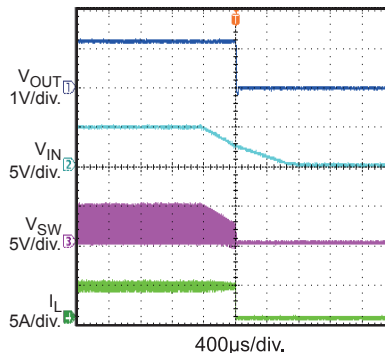
Power Off
 $I_{OUT} = 4A$, PFM



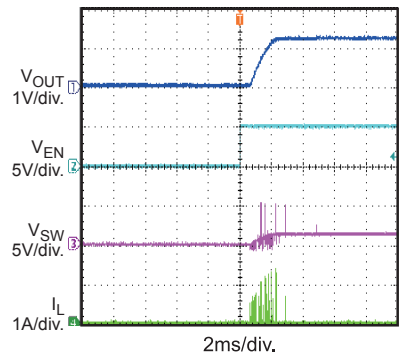
Power Off
 $I_{OUT} = 0A$, PWM



Power Off
 $I_{OUT} = 4A$, PWM



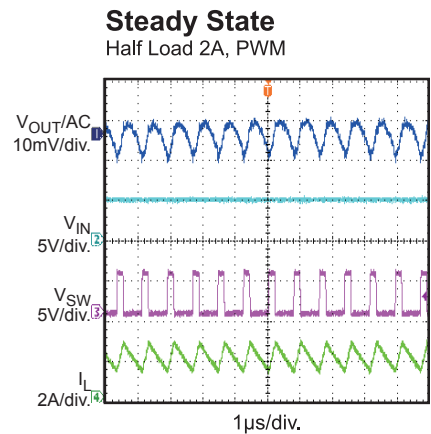
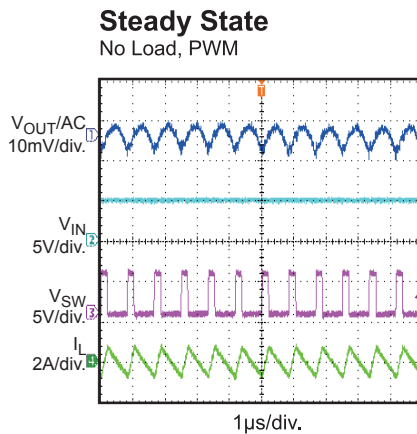
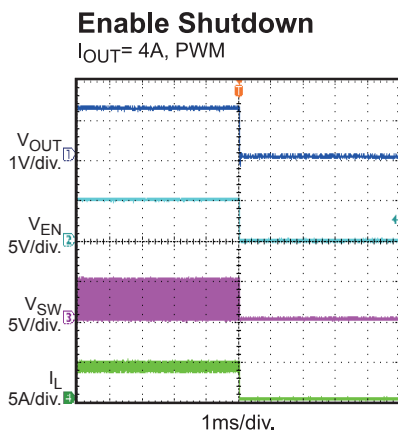
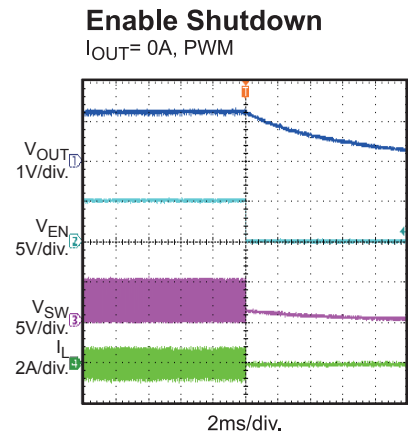
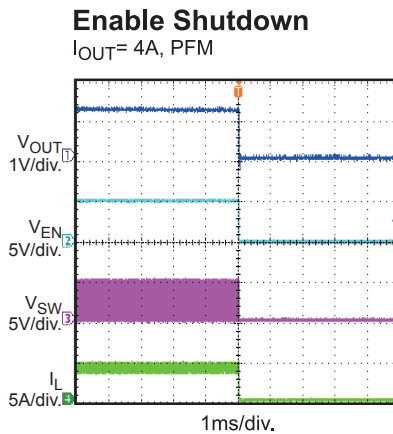
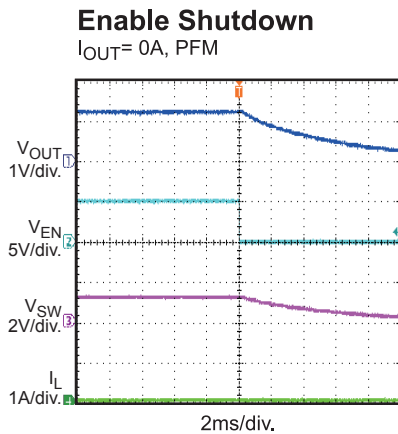
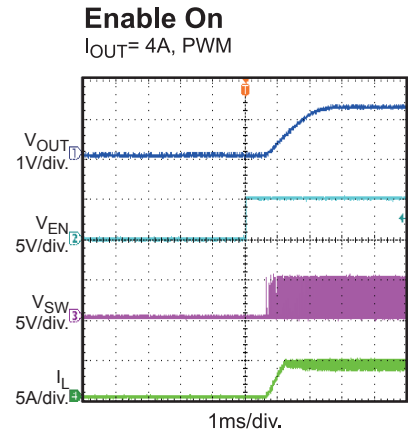
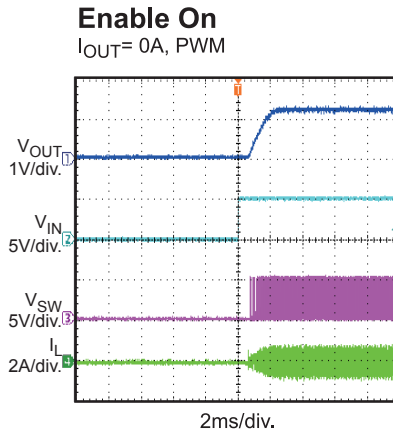
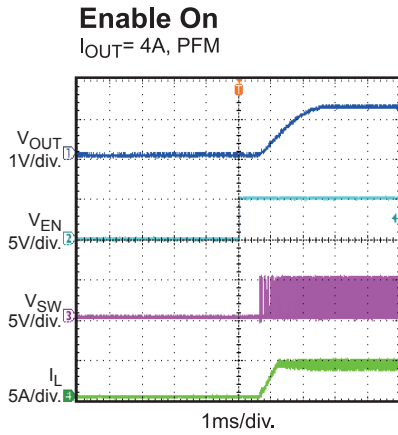
Enable On
 $I_{OUT} = 0A$, PFM



EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board.

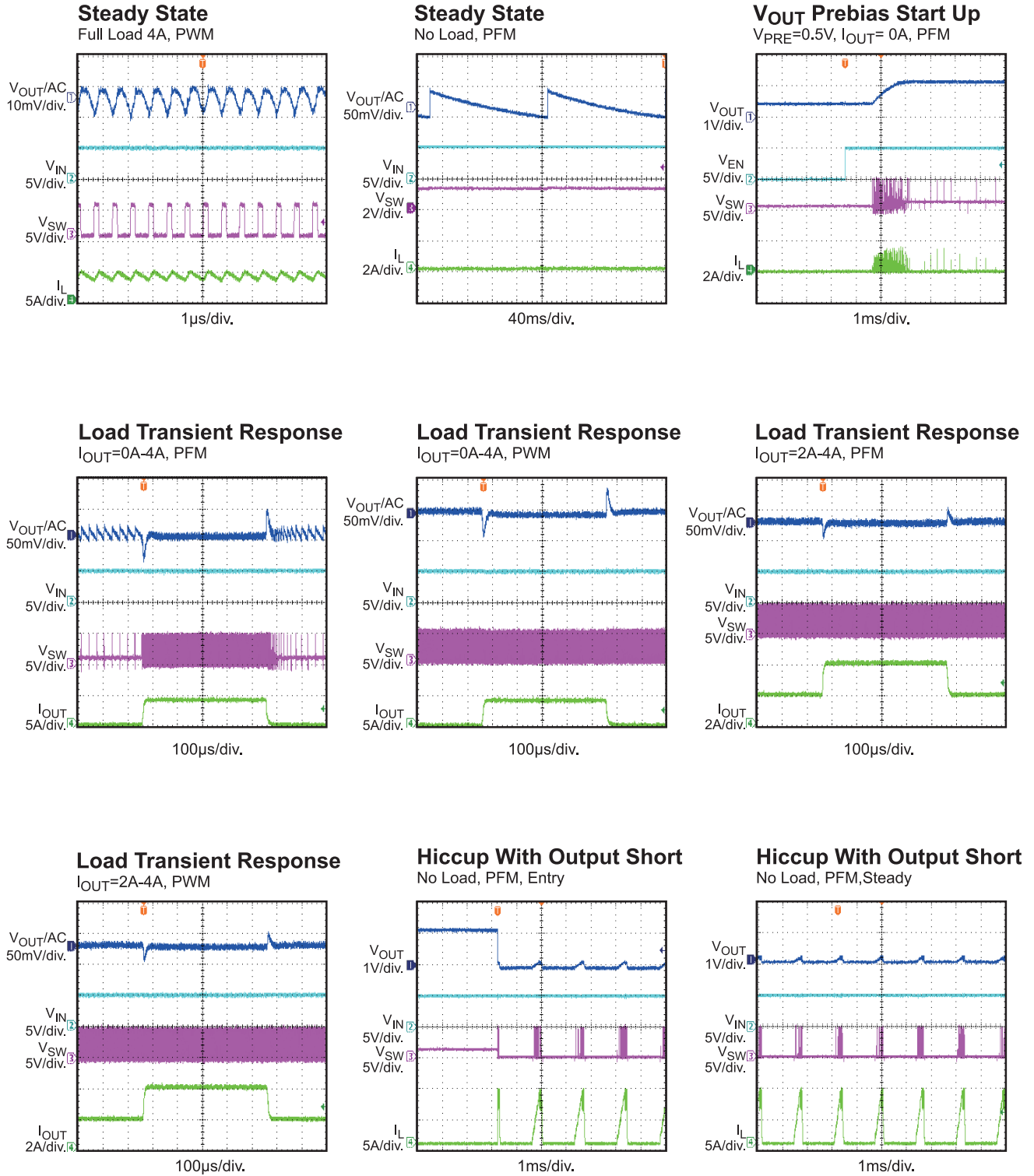
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EVB TEST RESULTS (continued)

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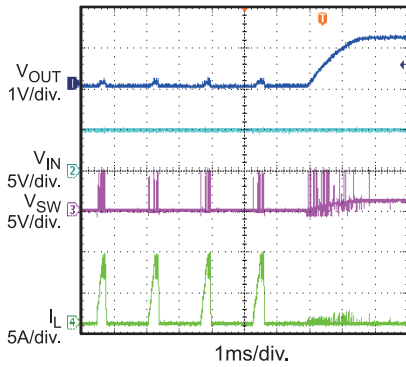


EVB TEST RESULTS (continued)

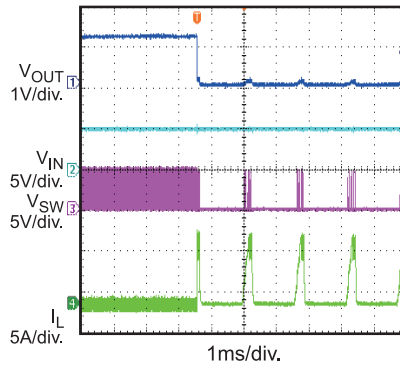
Performance waveforms are tested on the evaluation board.

$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $L = 0.47\mu H$, $C_{OUT} = 22\mu F \times 2$, $T_A = 25^\circ C$, unless otherwise noted.

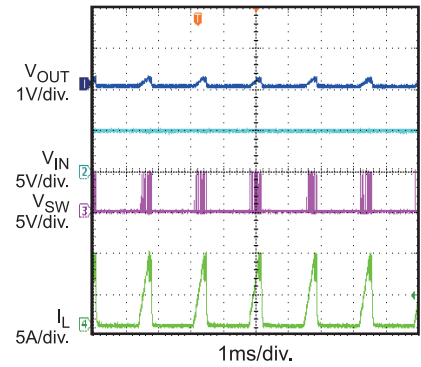
Hiccup With Output Short
No Load, PFM, Recovery



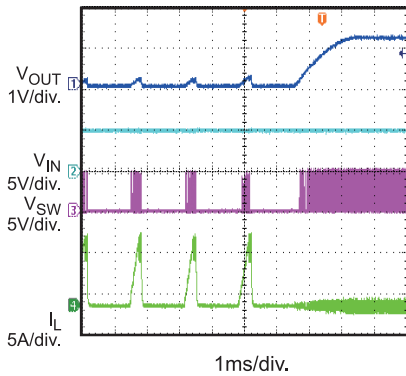
Hiccup With Output Short
No Load, PWM, Entry



Hiccup With Output Short
No Load, PWM, Steady



Hiccup With Output Short
No Load, PWM, Recovery



PRINTED CIRCUIT BOARD LAYOUT

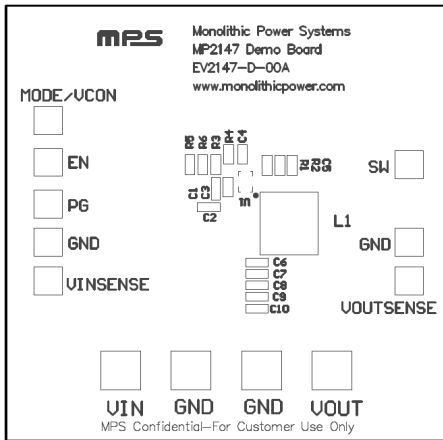


Figure 1—Top Silk Layer

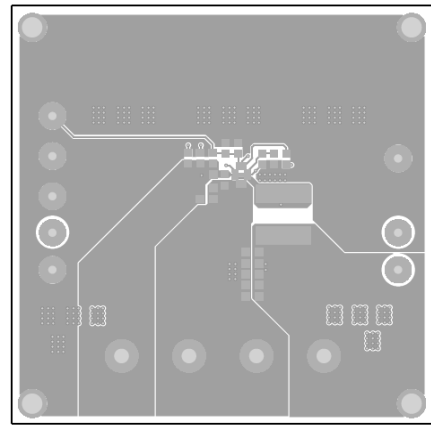


Figure 2—Top Layer

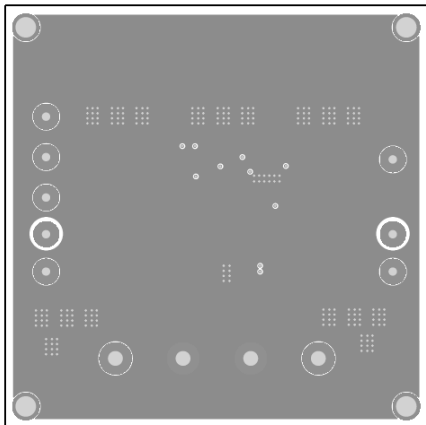


Figure 3—Inner 1 Layer

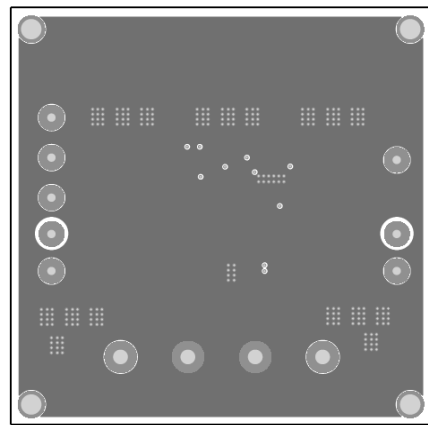


Figure 4—Inner 2 Layer

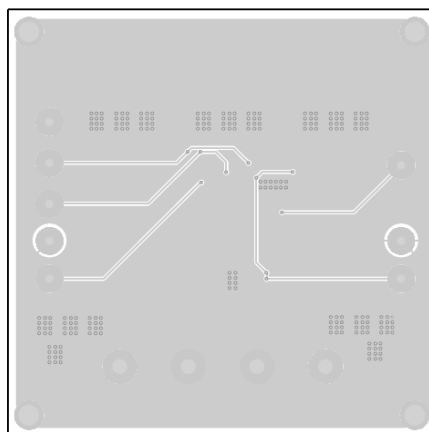


Figure 5—Bottom Layer