

# EV2313-J-00A

High Efficiency,24V,1A,2MHz,Synchronous **Step-Down Converter Evaluation Board** 

The Future of Analog IC Technology

# DESCRIPTION

The EV2313-J-00A is an evaluation board for MP2313, a high frequency, synchronous, rectified, step-down converter with built-in Power MOSFETs. The MP2313 offers a verv compact solution to achieve 1A continuous output current with excellent load and line regulation over a wide input supply range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection and thermal shutdown.

The MP2313 requires a minimum number of readily available standard external components and is available in a space saving TSOT23-8 package.

# ELECTRICAL SPECIFICATION (1)

Parameter	Symbol	Value	Units
Input Voltage	V <sub>IN</sub>	19	V
Output Voltage	V <sub>OUT</sub>	3.3	V
Output Current	Ι <sub>ουτ</sub>	1	Α

1). For different input, output spec, please refer to TYPICAL APPLICATION CIRCUIT section on datasheet to choose proper parameters.

### **FEATURES**

- 1A Continuous Load Current
- $110m\Omega/50m\Omega$  Low R<sub>DS(ON)</sub> Internal Power MOSFETs
- Fixed 2MHz Switching Frequency
- High Efficiency Synchronous Mode Operation
- External AAM pin for Power-Save Mode Programming
- Internal Soft-Start
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection with Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a TSOT23-8 Package

## APPLICATIONS

- Notebook System and I/O Power
- **Digital Set-Top Boxes**
- Flat-Panel Television and Monitors

Efficiency vs.

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

# **EV2313-J-00A EVALUATION BOARD**



MP2313GJ

		Output Current							
	١	$V_{OUT}$ =3.3V, L=1µH, I <sub>OUT</sub> =0.01A to 1A							
	F	R <sub>AAM</sub> =40.2k @ V <sub>IN</sub> =12V to 24V,							
	F	R <sub>AAM</sub> =80.6K @ V <sub>IN</sub> =5V							
ENCY (%)	95	Vin=5V							
	90								
	85								
	0.0	V <sub>IN</sub> =12V							
	80								
	75								
2	70	V <sub>IN</sub> =19V							
Ť	0.5								
	65	$V_{\rm IN}=24V$							
	60								
	55								
	0.	0.1 0.1 1							

EV2313-J-00A

www.MonolithicPower.com MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited. © 2015 MPS. All Rights Reserved.



## **EVALUATION BOARD SCHEMATIC**



# EV2313-J-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
1	C1	22µF	Ceramic Cap,25V,X5R	1206	muRata	GRM31CR61E226KE15L
1	C2	22µF	Ceramic Cap,10V,X7R	1206	muRata	GRM31CR71A226KE15L
1	C3	22pF	Ceramic Cap,50V,C0G	0603	muRata	GRM1885C1H220JA01D
2	C4,C5	0.1µF	Ceramic Cap,16V,X7R	0603	muRata	GRM188R71C104KA01D
1	C6	0.1µF	Ceramic Cap,25V,X7R	0603	muRata	GRM188R71E104KA01D
1	R1	20k	Thick Film Res,1%	0603	ROYAL	RL0603FR-0720KL
1	R2	6.34k	Thick Film Res,1%	0603	ROYAL	RL0603FR-076K34L
1	R3	40.2k	Thick Film Res,1%	0603	ROYAL	RL0603FR-0740K2L
1	R4	100k	Thick Film Res,1%	0603	ROYAL	RL0603FR-07100KL
1	R5	NS				
1	R6	20Ω	Thick Film Res,1%	0603	ROYAL	RL0603FR-0720RL
1	R7	10Ω	Thick Film Res,1%	0603	ROYAL	RL0603FR-0710RL
1	L1	1µH	Inductor, DCR=8.4mΩ, Isat=10.2A	SMD	Wurth	744777001
			Inductor,DCR=14mΩ Isat=5.26A	SMD	Sunlord	SWPA4030S1R0NT
1	U1	MP2313GJ	Synchronous Step- Down Convert	TSOT23-8	MPS	MP2313GJ



### **EVB TEST RESULTS**

Performance waveforms are tested on the evaluation board.  $V_{IN} = 19V$ ,  $V_{OUT} = 3.3V$ ,  $T_A=25$ °C, unless otherwise noted.



.0 www.MonolithicPower.com MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited. © 2015 MPS. All Rights Reserved.



#### EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board.  $V_{IN}$  = 19V,  $V_{OUT}$  = 3.3V,  $T_A$ =25°C, unless otherwise noted.





## PRINTED CIRCUIT BOARD LAYOUT



Figure 1—Top Silk Layer



Figure 2—Top Layer



Figure 3—Bottom Silk Layer

Figure 4—Bottom Layer